# TLV809
# 3 ピン電圧電源スーパーバイザ

## 1 特長

- 高精度電源電圧モニタ：2.5V/3V/3.3V/5V
- 200ms の固定遅延時間を持つパワー・オン・リセット・ジェネレータ
- 消費電流：9µA（標準値）
- 温度範囲：–40℃～+85℃
- 3 ピン SOT-23 パッケージ
- MAX809 とピン互換

## 2 アプリケーション

- ファクトリ・オートメーション
- 携帯型およびバッテリ駆動の機器
- セット・トップ・ボックス
- サーバー
- 家電製品
- 電気メーター
- ビル・オートメーション

## 3 説明

スーパーバイザ回路の TLV809 ファミリは、主に デジタル信号プロセッサ (DSP) およびプロセッサ・ベースのシステムの回路の初期化とタイミングの監視を行います。新しい TLV809E デバイスは、ピン互換の代替品です。

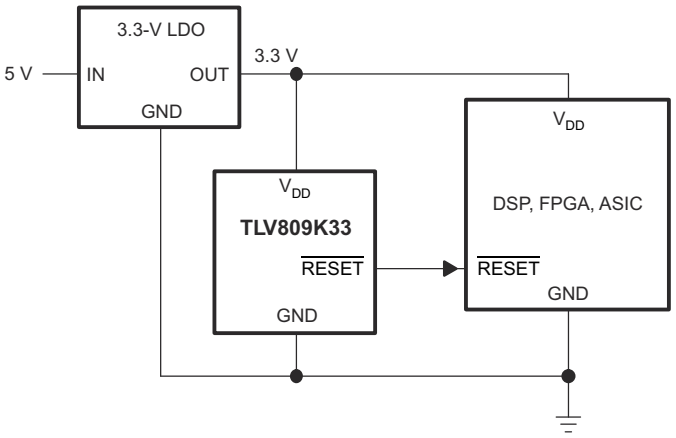
電源オン時に、電源電圧 ($V_{\overline{DD}}$) が 1.1V を超えると RESET がアサートされます。 その後、スーパーバイザ回路は $V_{DD}$ を監視し、 $V_{\overline{DD}}$ がスレッショルド電圧 $V_{\overline{IT}}$ を下回っている限り、 RESET をアクティブに維持します。内蔵されたタイマにより、出力が非アクティブ状態 (high) に戻るのを遅らせて、適切にシステムがリセットされるようにします。遅延時間 ($t_{d(typ)}$ = 200 ms) は、$V_{DD}$ がスレッショルド電圧 ($V_{IT}$) を上回ると開始します。電源電圧がスレッショルド電圧 ($V_{IT}$) を下回ると、出力は再びアクティブ (low) になります。外付け部品は不要です。このファミリの全デバイスは、内蔵分圧器で設定した固定検出スレッショルド電圧 ($V_{IT}$) を持っています。

この製品ファミリは、2.5V、3V、3.3V、5V の電源電圧用に設計されています。これらの回路は 3 ピンの SOT-23 パッケージで供給されます。このデバイスは、-40℃～+85℃ の温度範囲で動作が規定されています。

**製品情報**

| 型番 | パッケージ (1) | 本体サイズ (公称) |
|---|---|---|
| TLV809 | SOT-23 (3) (DBV) | 2.90mm × 1.60mm |
| | SOT-23 (3) (DBZ) | 2.92mm×1.30mm |

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**代表的なアプリケーション**

# Table of Contents



## 4 Revision History

**Changes from Revision E (November 2020) to Revision F (December 2020)** — **Page**

- Corrected missed change of VDD from 7 to 6.5 in *Absolute Maximum Ratings* for all other pins and in note2 ... 5

**Changes from Revision D (March 2016) to Revision E (November 2020)** — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「説明」セクションを更新 ... 1
- Updated *Device Comparison* ... 4
- Changed VDD from 7 to 6.5 in *Absolute Maximum Ratings* ... 5
- Changed $V_{OL}$ @ 500µA from 0.2 to 0.3 in *Electrical Characteristics* ... 6
- Changed $t_w$ pulse duration from 3 to 10µs in *Timing Requirements* ... 6
- Changed $t_{PHL}$ from 1 to 10µs in *Switching Characteristics* ... 6
- Deleted figure for Minimum Pulse Duration At $V_{DD}$ in Typical Characteristics ... 8
- Changed figure from Pulse Duration to $V_{OL}$, $I_{OL}$ in the Typical Application Section ... 11

**Changes from Revision C (February 2012) to Revision D (March 2016)** — **Page**

- 「*製品情報*」表、「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*概要*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 ... 1
- ページ 1 からピン配置図を削除 ... 1
- 「*説明*」セクションを変更： 3 番目の段落を追加し、セクションの表現を明確にするよう変更 ... 1
- Deleted soldering temperature parameter from *Absolute Maximum Ratings* table ... 5
- Changed $I_{DD}$ parameter test conditions in *Electrical Characteristics* table ... 6

**Changes from Revision B (September 2010) to Revision C (February 2012)** — **Page**

- Updated ordering information ... 4

**Changes from Revision A (July 2010) to Revision B (September 2010)** — **Page**

- 現行基準に合わせ文書形式を更新 ... 1

- ピン配置図に DBZ パッケージを追加
- Added *Thermal Information* table
- Changed 図 7-3

# 5 Device Comparison

**表 5-1. Device Threshold Options**

| PRODUCT | THRESHOLD VOLTAGE |
|---|---|
| TLV809J25 | 2.25 V |
| TLV809L30 | 2.64 V |
| TLV809K33 | 2.93 V |
| TLV809I50 | 4.55 V |

**表 5-2. Device Family Comparison**

| DEVICE | FUNCTION |
|---|---|
| TLV803 | Open-Drain, $\overline{\text{RESET}}$ Output |
| TLV809 | Push-Pull, $\overline{\text{RESET}}$ Output |
| TLV810 | Push-Pull, RESET Output |

# 6 Pin Configuration and Functions

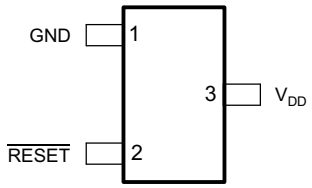



**図 6-1. DBV, DBZ Packages**
**3-Pin SOT-23**
**Top View**

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | GND | — | Ground pin. This pin must be connected to ground with a low-impedance connection. |
| 2 | $\overline{\text{RESET}}$ | O | $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ is an active low signal, asserting when $V_{DD}$ is below the threshold voltage. When $V_{DD}$ rises above $V_{IT}$, there is a delay time ($t_d$) until $\overline{\text{RESET}}$ deasserts. $\overline{\text{RESET}}$ is a push-pull output stage. |
| 3 | $V_{DD}$ | I | Supply voltage pin. A 0.1-µF ceramic capacitor from this pin to ground is recommended to improve stability of the threshold voltage. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage(2) | | 6.5 | V |
| | All other pins(2) | –0.3 | 6.5 | |
| $I_{OL}$ | Maximum low output current | | 5 | mA |
| $I_{OH}$ | Maximum high output current | | –5 | mA |
| $I_{IK}$ | Input clamp current ($V_I$ < 0 or $V_I$ > $V_{DD}$) | | ±20 | mA |
| $I_{OK}$ | Output clamp current ($V_O$ < 0 or $V_O$ > $V_{DD}$) | | ±20 | mA |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, do not operate the device at 6.5 V for more than t = 1000h continuously.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

at specified temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2 | | 6 | V |
| $C_{IN}$ | $V_{DD}$ bypass capacitor | | 0.1 | | µF |
| $T_A$ | Operating free-air temperature range | –40 | | 85 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TLV809 | | UNIT |
|---|---|---|---|---|
| | | DBV (SOT-23) | DBZ (SOT-23) | |
| | | 3 PINS | 3 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 242.1 | 286.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 213.0 | 105.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 123.4 | 124.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 45.7 | 25.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 130.9 | 107.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

at $T_A$ = –40°C to +85°C (unless otherwise noted); typical values are at $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $V_{DD}$ = 2.5 V to 6 V, $I_{OH}$ = –500 µA | $V_{DD}$ – 0.2 | | | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OH}$ = –2 mA | $V_{DD}$ – 0.4 | | | |
| | | | $V_{DD}$ = 6 V, $I_{OH}$ = –4 mA | $V_{DD}$ – 0.4 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{DD}$ = 2 V to 6 V, $I_{OH}$ = 500 µA | | | 0.3 | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OH}$ = 2 mA | | | 0.4 | |
| | | | $V_{DD}$ = 6 V, $I_{OH}$ = 4 mA | | | 0.4 | |
| | Power-up reset voltage[1] | | $V_{DD}$ ≥ 1.1 V, $I_{OL}$ = 50 µA | | | 0.2 | V |
| $V_{IT–}$ | Negative-going input threshold voltage[2] | TLV809J25 | $T_A$ = –40°C to +85°C | 2.20 | 2.25 | 2.30 | V |
| | | TLV809L30 | | 2.58 | 2.64 | 2.70 | |
| | | TLV809K33 | | 2.87 | 2.93 | 2.99 | |
| | | TLV809I50 | | 4.45 | 4.55 | 4.65 | |
| $V_{hys}$ | Hysteresis | TLV809J25 | | | 30 | | mV |
| | | TLV809L30 | | | 35 | | |
| | | TLV809K33 | | | 40 | | |
| | | TLV809I50 | | | 60 | | |
| $I_{DD}$ | Supply current | | $V_{DD}$ = 2 V, RESET is unconnected | | 9 | 12 | µA |
| | | | $V_{DD}$ = 6 V, RESET is unconnected | | 20 | 25 | |
| $C_I$ | Input capacitance | | $V_I$ = 0 V to $V_{DD}$ | | 5 | | pF |

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,\ VDD}$ ≥ 15 ms/V.
(2) To ensure best stability of the threshold voltage, place a bypass capacitor ( 0.1-µF ceramic) near the supply pins.

## 7.6 Timing Requirements

at $T_A$ = 25°C, $R_L$ = 1 MΩ, and $C_L$ = 50 pF

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_w$ | Pulse duration at $V_{DD}$ | $V_{DD}$ = $V_{IT–}$ + 0.2 V, $V_{DD}$ = $V_{IT–}$ – 0.2 V | 10 | | | µs |

## 7.7 Switching Characteristics

at $T_A$ = 25°C, $R_L$ = 1 MΩ, and $C_L$ = 50 pF

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time | | $V_{DD}$ ≥ $V_{IT–}$ + 0.2 V; see 図 7-1 | 120 | 200 | 280 | ms |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $V_{DD}$ to $\overline{\text{RESET}}$ delay | $V_{IL}$ = $V_{IT–}$ – 0.2 V, $V_{IH}$ = $V_{IT–}$ + 0.2 V | | 10 | | µs |

## 7.8 Timing Diagrams

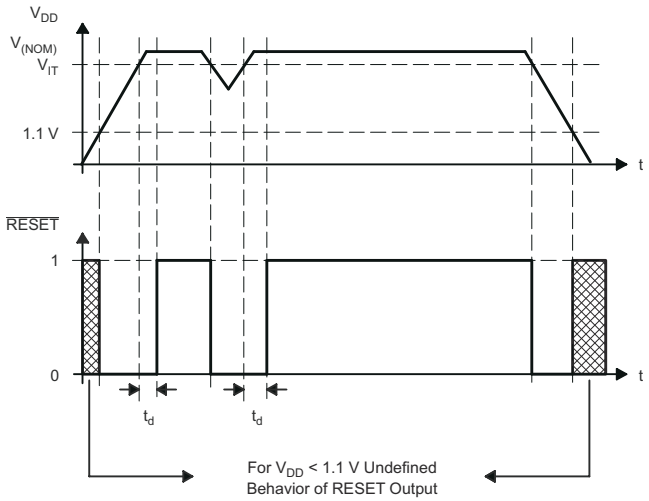



**図 7-1. Timing Diagram**

## 7.9 Typical Characteristics

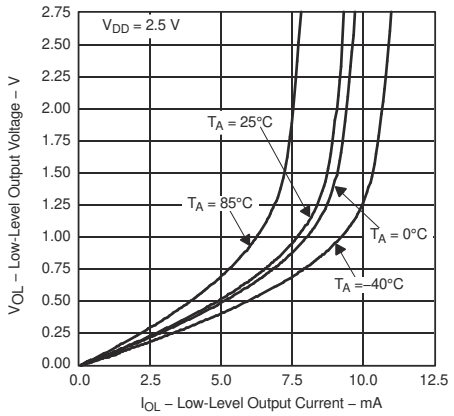



**図 7-2. Low-Level Output Voltage vs Low-Level Output Current**

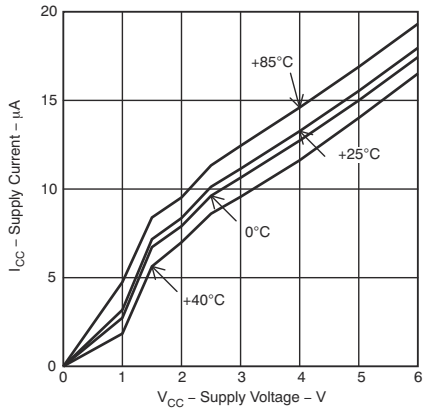



**図 7-3. Supply Current vs Supply Voltage**

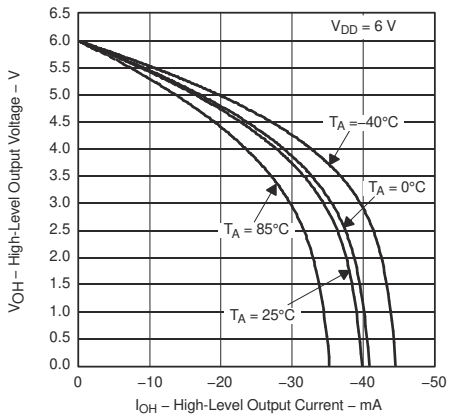



**図 7-4. High-Level Output Voltage vs High-Level Output Current**

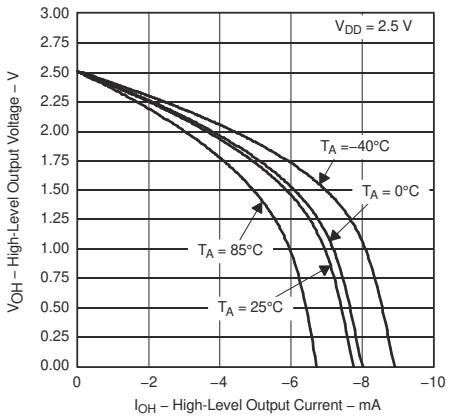



**図 7-5. High-Level Output Voltage vs High-Level Output Current**

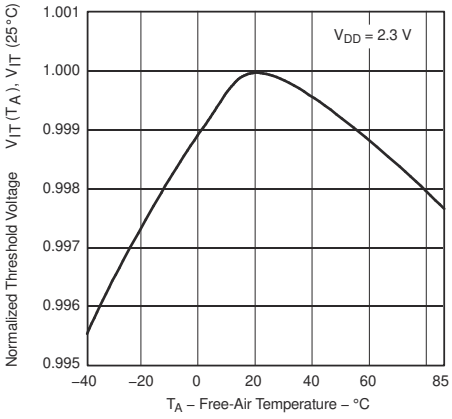


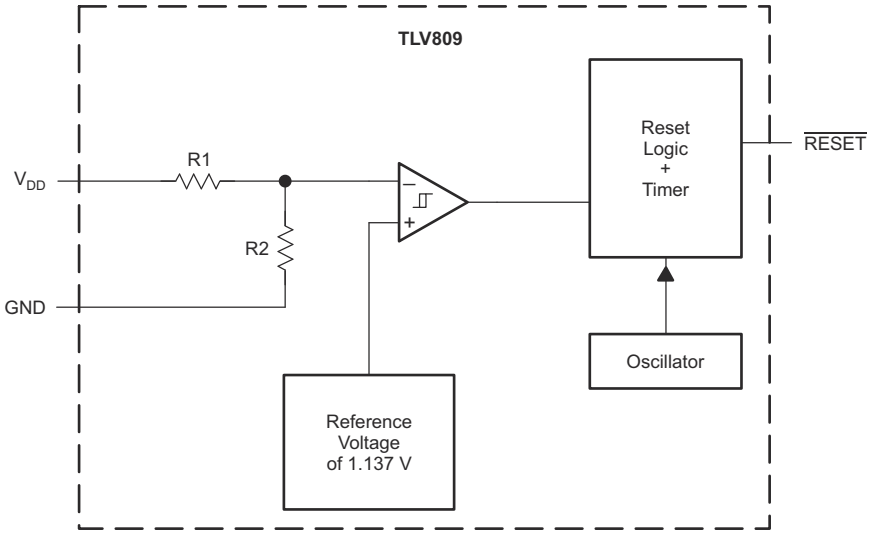

**図 7-6. Normalized Input Threshold Voltage vs Free-Air Temperature at $V_{DD}$**

# 8 Detailed Description

## 8.1 Overview

The TLV809 is a 3-pin voltage detector with fixed detection thresholds, an active-low push-pull $\overline{\text{RESET}}$ output, and an internal timer to delay the $\overline{\text{RESET}}$ signal when $V_{DD}$ rises above the threshold voltage.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Supply Voltage Monitoring

The device actively monitors its supply voltage to ensure that the power supply is above a certain voltage threshold.

The device offers various fixed threshold options that are approximately 10% below several standard supply voltages (2.5 V, 3.0 V, 3.3 V, 5.0 V).

### 8.3.2 $\overline{\text{RESET}}$ Output

The device has a $\overline{\text{RESET}}$ output to indicate the status of the input power supply.

$\overline{\text{RESET}}$ is an active low signal, asserting when $V_{DD}$ is below the threshold voltage. When $V_{DD}$ rises above $V_{IT}$, there is a delay time ($t_d$) until $\overline{\text{RESET}}$ deasserts.

$\overline{\text{RESET}}$ is a push-pull output stage.

## 8.4 Device Functional Modes

When the input supply voltage is in its recommended operating range (2 V to 6 V), the device is in a normal operational mode. In normal operational mode the device monitors $V_{DD}$ for undervoltage detection.

When the input supply is below its recommended operating range, the device is in shutdown mode and therefore tries to assert $\overline{\text{RESET}}$.

# 9 Application and Implementation

**注**

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

### 9.1.1 $V_{DD}$ Transient Rejection

The device has built-in rejection of fast transients on the $V_{DD}$ pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the device, as shown in 図 9-1.

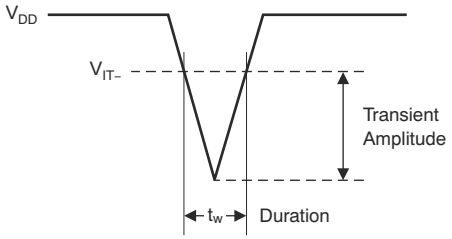



**図 9-1. Voltage Transient Measurement**

The device does not respond to transients that are fast duration and low amplitude or long duration and small amplitude. Transients meeting or longer than the $t_w$ specified in the セクション 7.6 section triggers a reset.

### 9.1.2 Reset During Power-Up and Power-Down

The device output is valid when $V_{DD}$ is greater than 1.1 V. When $V_{DD}$ is less than 1.1 V, the output transistor turns off and becomes high impedance. The voltage on the $\overline{\text{RESET}}$ pin rises to the voltage level connected to the pullup resistor. 図 9-2 shows a typical waveform for power-up.

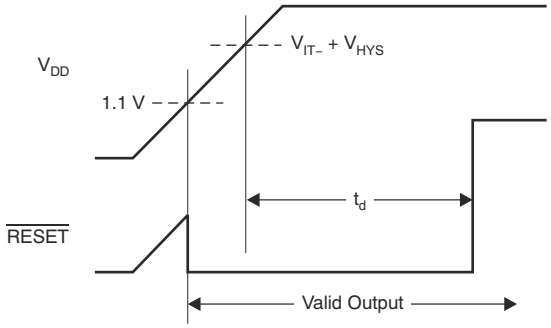



**図 9-2. Power-Up Response**

## 9.2 Typical Application

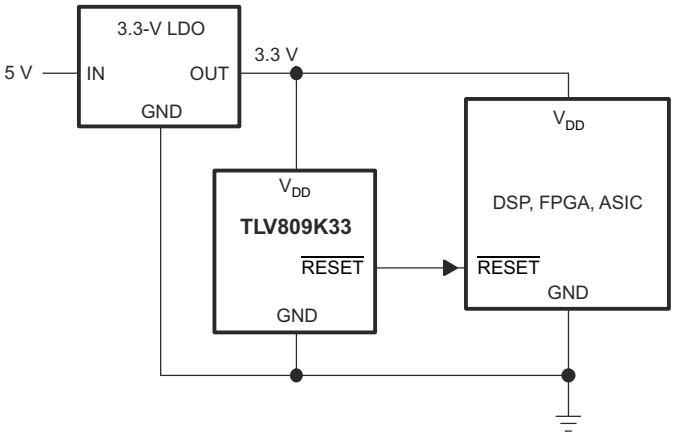



**図 9-3. Monitoring a 3.3-V Supply**

### 9.2.1 Design Requirements

The device must ensure that the supply voltage does not drop more than 15% below 3.3 V. If the supply voltage falls below 3.3 V – 15%, then the load must be disabled.

### 9.2.2 Detailed Design Procedure

The TLV809K33 is selected to ensure that $V_{DD}$ is greater than 2.87 V when the load is enabled.

### 9.2.3 Application Curve

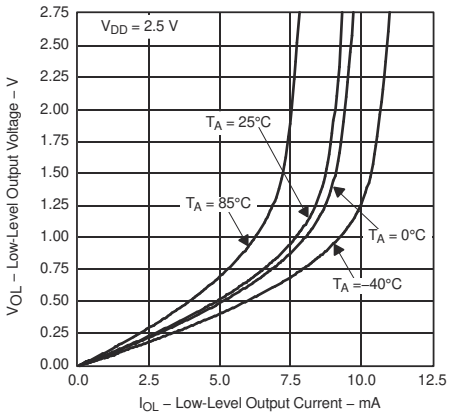



**図 9-4. Low-Level Output Voltage vs Low-Level Output Current**

# 10 Power Supply Recommendations

Power the device with a low-impedance supply. A 0.1-µF bypass capacitor from $V_{DD}$ to ground is recommended.

# 11 Layout

## 11.1 Layout Guidelines

Place the device near the load for the input power supply, with a low-impedance connection to the power supply pins of the load to sense the supply voltage.

## 11.2 Layout Example

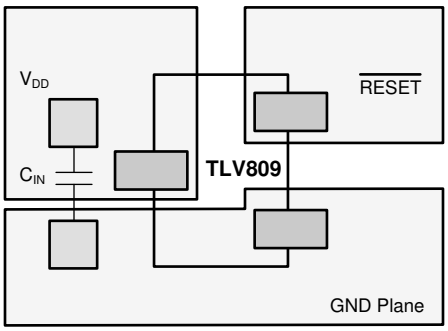



**図 11-1. Example Layout**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

TLV803 Data Sheet, SBVS157

TLV810 Data Sheet, SBVS158

## 12.2 サポート・リソース

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## 12.3 Trademarks

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## 12.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 12.5 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV809I50DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTBI | Samples |
| TLV809I50DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTBI | Samples |
| TLV809I50DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMV | Samples |
| TLV809I50DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMV | Samples |
| TLV809J25DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTCI | Samples |
| TLV809J25DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTCI | Samples |
| TLV809J25DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMT | Samples |
| TLV809J25DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | RoHS & Green | NIPDAUAG \| SN | Level-1-260C-UNLIM | -40 to 85 | BCMT | Samples |
| TLV809K33DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTRI | Samples |
| TLV809K33DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTRI | Samples |
| TLV809K33DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMX | Samples |
| TLV809K33DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMX | Samples |
| TLV809L30DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTXI | Samples |
| TLV809L30DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTXI | Samples |
| TLV809L30DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMZ | Samples |
| TLV809L30DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | BCMZ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

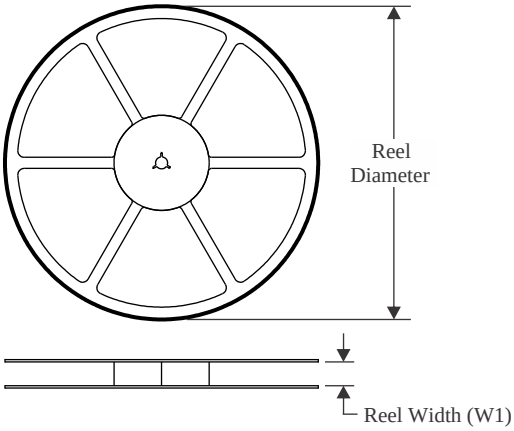
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

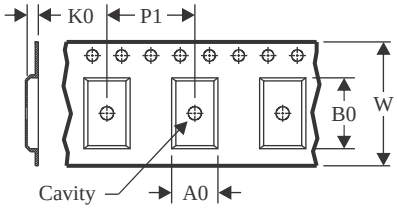
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

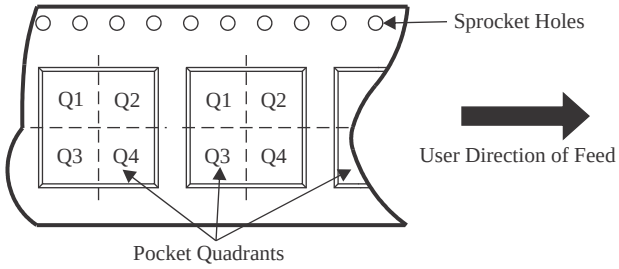



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

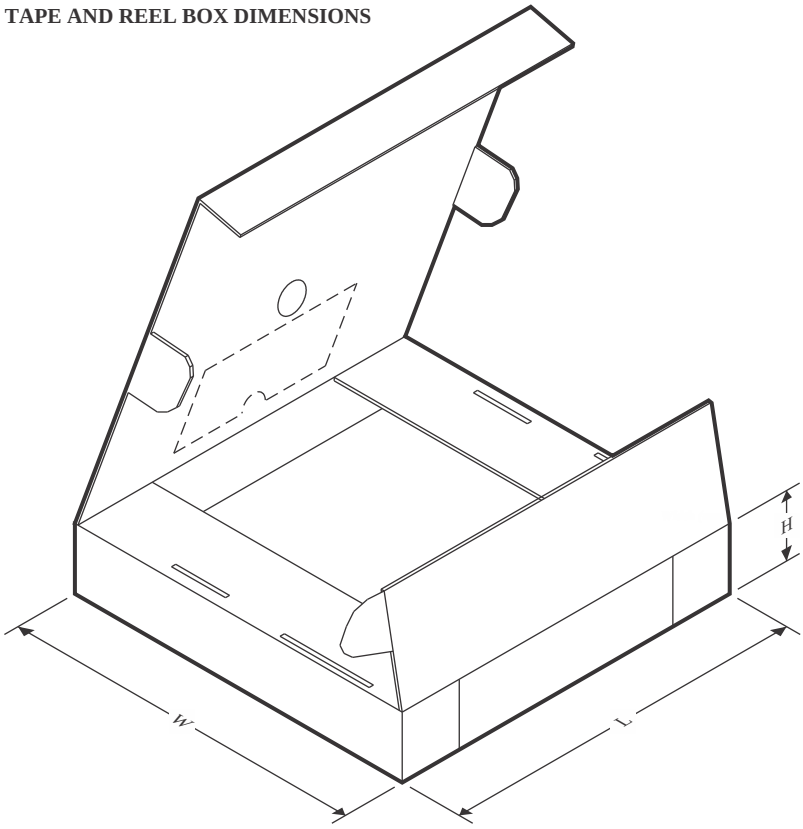
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV809I50DBVR | SOT-23 | DBV | 3 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809I50DBVT | SOT-23 | DBV | 3 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809I50DBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809I50DBZT | SOT-23 | DBZ | 3 | 250 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809J25DBVR | SOT-23 | DBV | 3 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809J25DBVT | SOT-23 | DBV | 3 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809J25DBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809J25DBZT | SOT-23 | DBZ | 3 | 250 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809K33DBVR | SOT-23 | DBV | 3 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809K33DBVT | SOT-23 | DBV | 3 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809K33DBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809K33DBZT | SOT-23 | DBZ | 3 | 250 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809L30DBVR | SOT-23 | DBV | 3 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809L30DBVT | SOT-23 | DBV | 3 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV809L30DBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809L30DBZT | SOT-23 | DBZ | 3 | 250 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

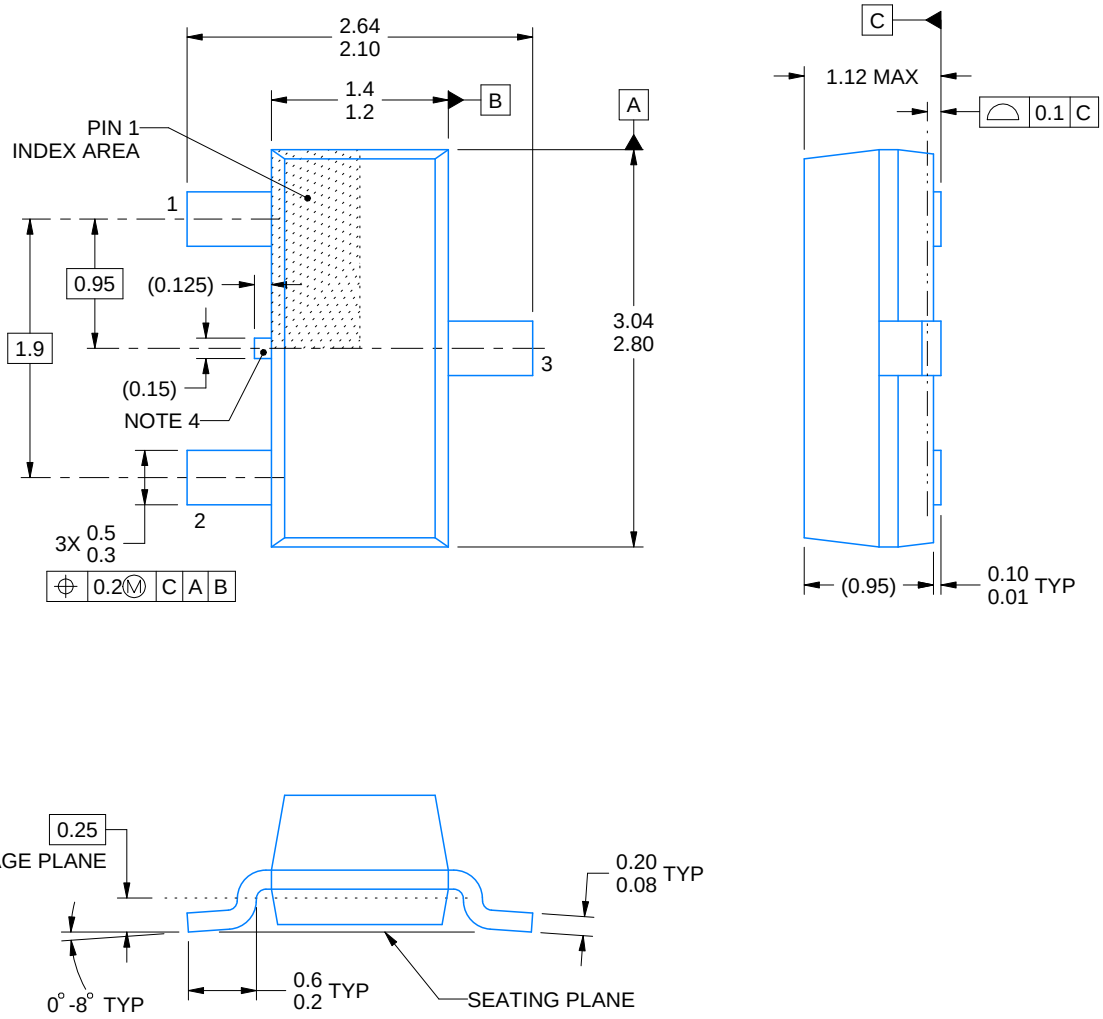
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV809I50DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809I50DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809I50DBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809I50DBZT | SOT-23 | DBZ | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809J25DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809J25DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809J25DBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809J25DBZT | SOT-23 | DBZ | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809K33DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809K33DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809K33DBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809K33DBZT | SOT-23 | DBZ | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809L30DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809L30DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809L30DBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809L30DBZT | SOT-23 | DBZ | 3 | 250 | 180.0 | 180.0 | 18.0 |

# PACKAGE OUTLINE

## DBZ0003A

## SOT-23 - 1.12 mm max height

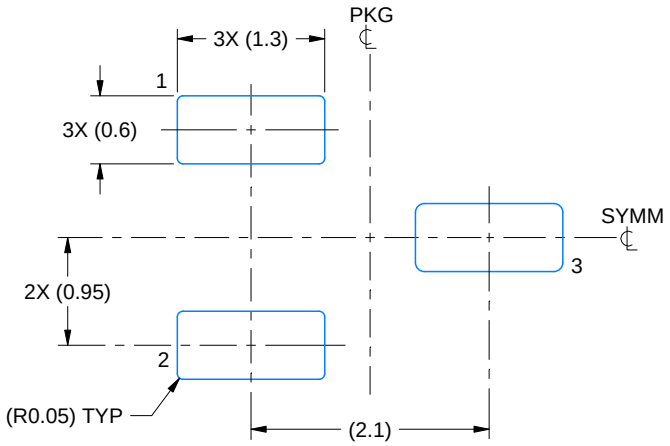
SMALL OUTLINE TRANSISTOR



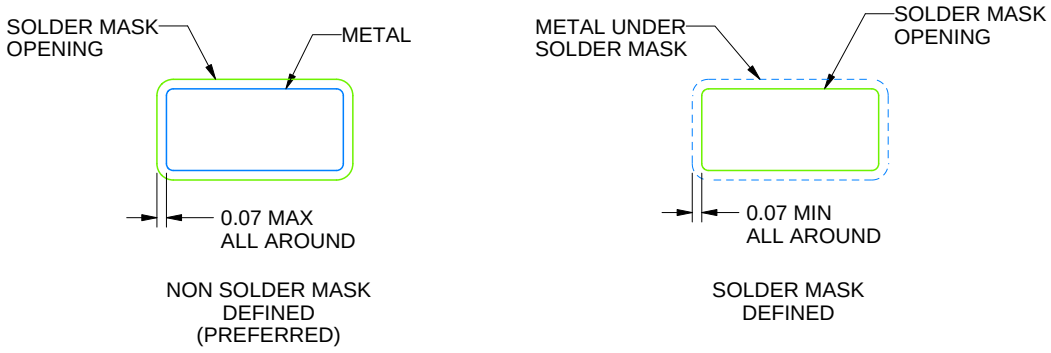

4214838/D 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE:15X

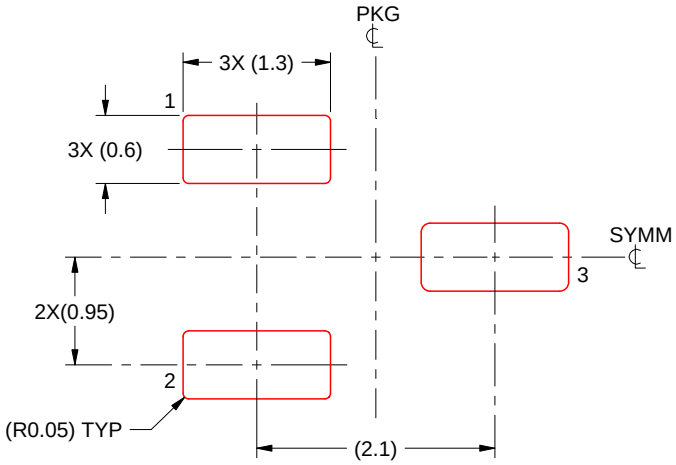



SOLDER MASK DETAILS

4214838/D 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/D 03/2023

NOTES: (continued)

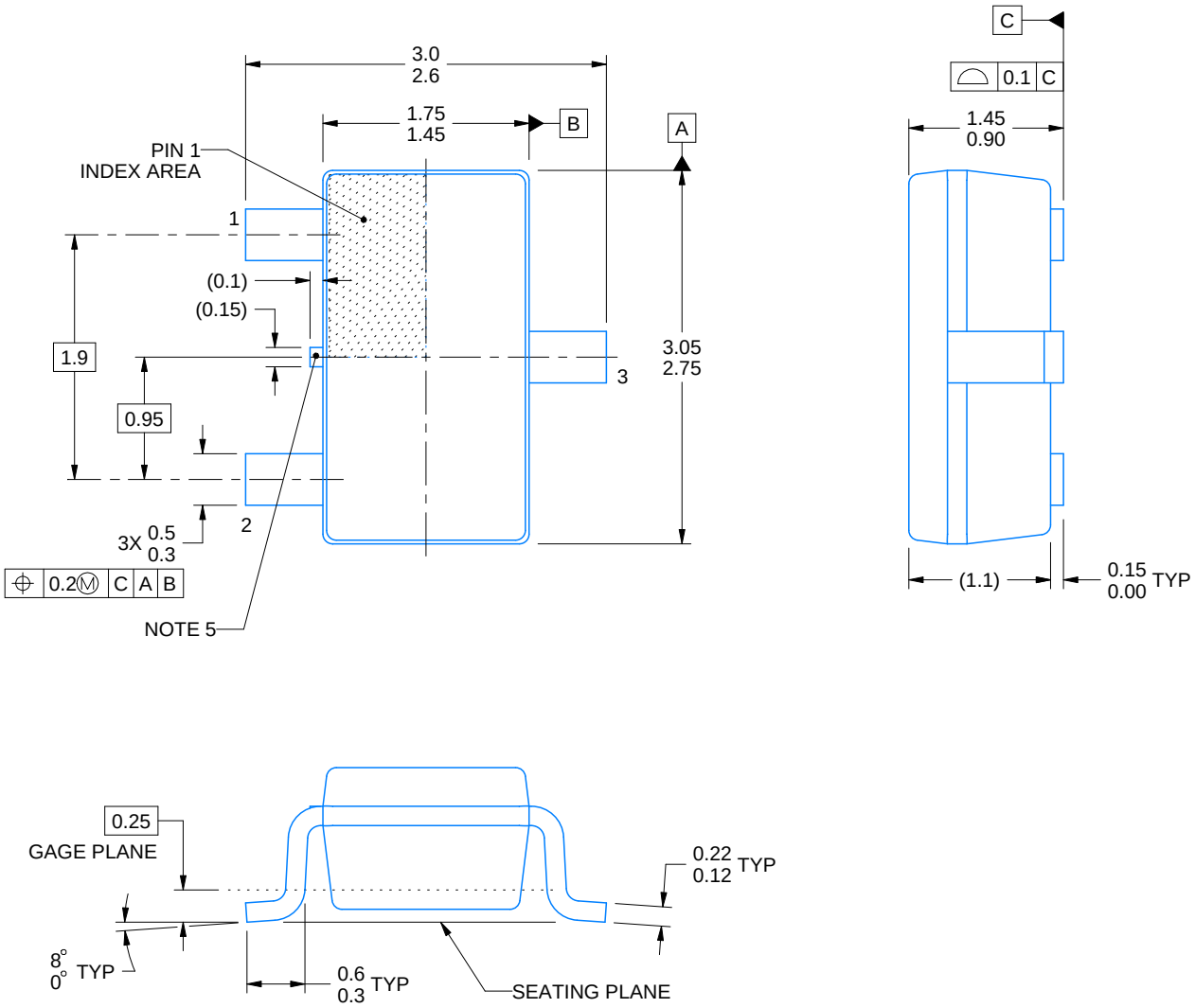
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0003A

## SOT-23 - 1.45 mm max height

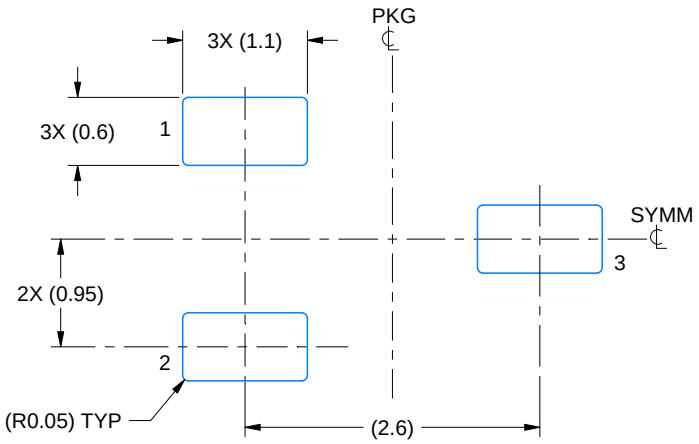
SMALL OUTLINE TRANSISTOR



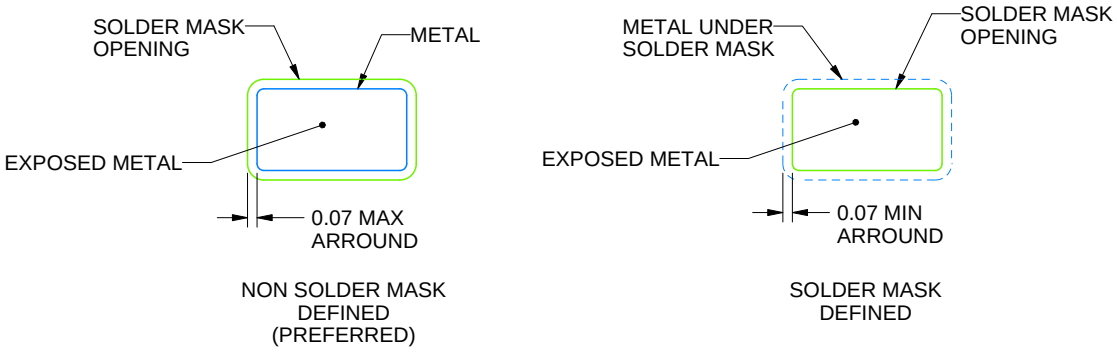

4220743/B 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

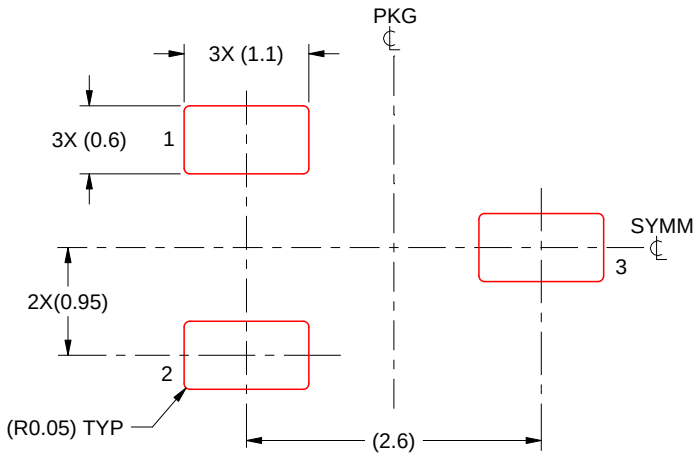



SOLDER MASK DETAILS

4220743/B 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220743/B 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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