

TLV905x-Q1 車載、5MHz、15V/μs、高スルーレート、RRIO、CMOS オペアンプ

1 特長

- 高いスルーレート: 15V/μs
- 低い静止電流: 330μA
- レール ツー レール入出力
- 低い入力オフセット電圧: ±0.33mV
- ユニティゲイン帯域幅: 5MHz
- 低い広帯域ノイズ: 15nV/√Hz
- 低い入力バイアス電流: 2pA
- ユニティゲイン安定
- 内部 RFI および EMI フィルタ
- 低コストのアプリケーション向けのスケラブルな CMOS オペアンプ ファミリ
- 最低 1.8V の電源電圧で動作
- 拡張温度範囲: -40°C ~ 125°C

2 アプリケーション

- AEC-Q100 グレード 1 アプリケーションに最適化
- HEV/EV のトラクション インバータおよびモータ制御
- HEV/EV の DC/DC コンバータ
- HEV/EV のバッテリー管理システム (BMS)
- オンボード チャージャ (OBC) およびワイヤレス チャージャ
- 車載各種ボディ モーター
- 車載のエアコン (冷暖房)

3 概要

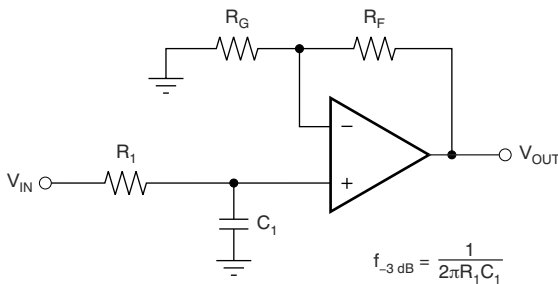
TLV9051-Q1、TLV9052-Q1、TLV9054-Q1 デバイスは、それぞれシングル、デュアル、クワッドのオペアンプです。これらのデバイスは 1.8V~6.0V の低電圧で動作するように設計されています。入力と出力は、非常に高いスルーレートでレール ツー レール動作が可能です。これらのデバイスは、コストが制限され、低電圧動作、高いスルーレート、小さい静止電流が要求されるアプリケーションに理想的です。TLV905x-Q1 ファミリの容量性負荷の駆動能力は 150pF であり、オープン ループ出力インピーダンスが抵抗性なので、はるかに大きな容量性負荷についても容易に安定化できます。

TLV905x-Q1 ファミリのデバイスはユニティゲイン安定で、RFI および EMI フィルタが内蔵され、オーバードライブ状況でも位相反転が発生しないため、簡単に使用できます。

製品情報

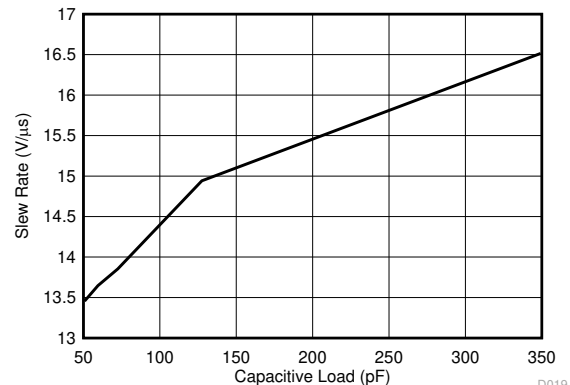
部品番号 ⁽¹⁾	チャネル数	パッケージ	パッケージサイズ ⁽³⁾
TLV9051-Q1	シングル	DBV (SOT-23, 5) ⁽²⁾	2.90mm × 2.80mm
		DCK (SC70, 5) ⁽²⁾	2.00mm × 2.10mm
TLV9052-Q1	デュアル	D (SOIC, 8) ⁽²⁾	4.90mm × 6.00mm
		PW (TSSOP, 8) ⁽²⁾	3.00mm × 6.40mm
		DGK (VSSOP, 8) ⁽²⁾	3.00mm × 4.90mm
TLV9054-Q1	クワッド	D (SOIC, 14) ⁽²⁾	8.65mm × 6.00mm
		PW (TSSOP, 14) ⁽²⁾	5.00mm × 6.40mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) このパッケージはプレビュー専用です。
- (3) パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

シングル ポールのローパス フィルタ



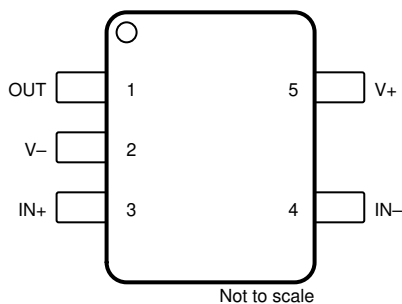
スルー レートと負荷容量との関係



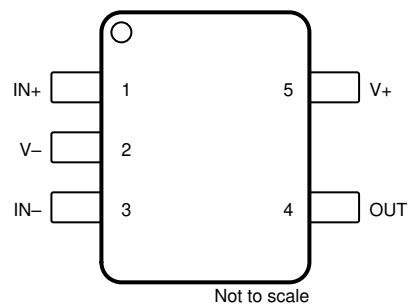
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4 Pin Configuration and Functions



**図 4-1. TLV9051-Q1 DBV Package,
5-Pin SOT-23
(Top View)**



**図 4-2. TLV9051-Q1 DCK Package,
5-Pin SC70
(Top View)**

表 4-1. Pin Functions: TLV9051-Q1

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	SOT-23	SC-70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	—	Negative (low) supply or ground (for single-supply operation)
V+	5	5	—	Positive (high) supply

(1) I = input, O = output

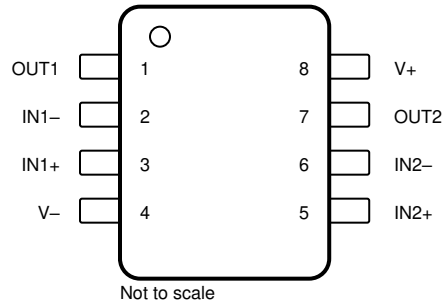
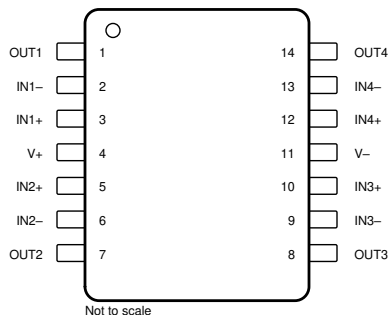


図 4-3. TLV9052-Q1 D, DGK, PW Packages,
8-Pin SOIC, VSSOP, TSSOP
(Top View)

表 4-2. Pin Functions: TLV9052-Q1

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply

(1) I = input, O = output



**図 4-4. TLV9054-Q1 D, PW Packages,
14-Pin SOIC, TSSOP
(Top View)**

表 4-3. Pin Functions: TLV9054-Q1

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	—	Negative (low) supply or ground (for single-supply operation)
V+	4	—	Positive (high) supply

(1) I = input, O = output

5 Specifications

5.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り)⁽¹⁾

			最小値	最大値	単位
電源電圧				7	V
信号入力ピン	電圧 ⁽²⁾	同相	(V-) - 0.5	(V+) + 0.5	V
		差動		(V+) - (V-) + 0.2	
	電流 ⁽²⁾		-10	10	mA
出力短絡 ⁽³⁾			連続		mA
温度	規定、T _A		-40	125	°C
	接合部、T _J			150	
	保存、T _{stg}		-65	150	

- (1) 「絶対最大定格」の範囲を超える動作は、デバイスの永続的な損傷の原因となる可能性があります。「絶対最大定格」は、これらの条件において、または「推奨動作条件」に示された値を超える他のいかなる条件でも、本製品が正しく動作することを暗に示すものではありません。「絶対最大定格」の範囲内であっても「推奨動作条件」の範囲外で使用した場合、本デバイスは完全に機能するとは限らず、このことが本デバイスの信頼性、機能、性能に影響を及ぼし、本デバイスの寿命を縮める可能性があります。
- (2) 入力ピンは、電源レールに対してダイオード クランプされています。電源レールを超えて 0.5V 以上スイングする入力信号は、電流を 10mA 以下に抑える必要があります。
- (3) グランドへの短絡、パッケージあたり 1 台のアンプ。

5.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V _(ESD) - Other Packages	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage	1.8	6	V
V _I	Common mode voltage range	(V-) - 0.1	(V+) + 0.1	V
T _A	Specified temperature	-40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC ⁽¹⁾		TLV9051-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	TBD	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Thermal Information for Dual Channel

THERMAL METRIC ⁽¹⁾		TLV9052-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	TBD	TBD	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.6 Thermal Information for Quad Channel

THERMAL METRIC ⁽¹⁾		TLV9054-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	TBD	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.7 Electrical Characteristics: V_S (Total Supply Voltage) = $(V^+) - (V^-) = 1.8V$ to $5.5V$

at $T_A = 25^\circ C$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted);

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5V		±0.33	±1.6	mV
		V _S = 5V, T _A = −40°C to +125°C			±2	
dV _{OS} /dT	Drift	V _S = 5V, T _A = −40°C to +125°C		±0.5		μV/°C
PSRR	Power-supply rejection ratio	V _S = 1.8V – 5.5V, V _{CM} = (V−)		±13	±80	μV/V
	Channel separation, dc	At dc		115		dB
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage	V _S = 1.8V to 5.5V	(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V _S = 5.5V, (V−) − 0.1V < V _{CM} < (V+) − 1.4V, T _A = −40°C to +125°C	80	96		dB
		V _S = 5.5V, V _{CM} = −0.1V to 5.6V, T _A = −40°C to +125°C	62	79		
		V _S = 1.8V, (V−) − 0.1V < V _{CM} < (V+) − 1.4V, T _A = −40°C to +125°C		88		
		V _S = 1.8V, V _{CM} = −0.1V to 1.9V, T _A = −40°C to +125°C		72		
INPUT BIAS CURRENT						
I _B	Input bias current			±2	±18 ⁽²⁾	pA
		T _A = −40°C to +125°C			±525 ⁽²⁾	pA
I _{OS}	Input offset current			±1	±15 ⁽²⁾	pA
		T _A = −40°C to +125°C			±440 ⁽²⁾	pA
NOISE						
E _n	Input voltage noise (peak-to-peak)	V _S = 5V, f = 0.1Hz to 10Hz		6		μV _{PP}
e _n	Input voltage noise density	V _S = 5V, f = 10kHz		15		nV/√Hz
		V _S = 5V, f = 1kHz		20		nV/√Hz
i _n	Input current noise density	f = 1kHz		18		fA/√Hz
INPUT CAPACITANCE						
C _{ID}	Differential			2		pF
C _{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 1.8V, (V−) + 0.04V < V _O < (V+) − 0.04V, R _L = 10kΩ		106		dB
		V _S = 5.5V, (V−) + 0.05V < V _O < (V+) − 0.05V, R _L = 10kΩ	104	128		
		V _S = 1.8V, (V−) + 0.06V < V _O < (V+) − 0.06V, R _L = 2kΩ		108		
		V _S = 5.5V, (V−) + 0.15V < V _O < (V+) − 0.15V, R _L = 2kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V _S = 5.5V, G = +1		5		MHz
φ _m	Phase margin	V _S = 5.5V, G = +1		60		Degrees
SR	Slew rate	V _S = 5.5V, G = +1, C _L = 130pF		15		V/μs
t _S	Settling time	To 0.1%, V _S = 5.5V, 2-V step , G = +1, C _L = 100pF		0.75		μs
		To 0.01%, V _S = 5.5V, 2-V step , G = +1, C _L = 100pF		1		
t _{OR}	Overload recovery time	V _S = 5.5V, V _{IN} × gain > V _S		0.3		μs
THD + N	Total harmonic distortion + noise ⁽¹⁾	V _S = 5.5V, V _{CM} = 2.5V, V _O = 1V _{RMS} , G = +1, f = 1kHz		0.0006%		

5.7 Electrical Characteristics: V_S (Total Supply Voltage) = $(V_+) - (V_-) = 1.8V$ to $5.5V$ (続き)

at $T_A = 25^\circ C$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted);

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V _O	Voltage output swing from supply rails	V _S = 5.5V, R _L = 10kΩ,			16	mV
		V _S = 5.5V, R _L = 2kΩ,			40	
I _{SC}	Short-circuit current	V _S = 5V		±50		mA
Z _O	Open-loop output impedance	V _S = 5V, f = 5MHz		250		Ω
POWER SUPPLY						
I _Q	Quiescent current per amplifier	V _S = 5.5V, I _O = 0mA,		330	450	μA
		V _S = 5.5V, I _O = 0mA, T _A = −40°C to +125°C			475	

- (1) Third-order filter; bandwidth = 80kHz at $-3dB$.
- (2) Specified by design and characterization; not production tested.

5.8 Typical Characteristics

at $T_A = 25^\circ C$, $V_S = 5.5V$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

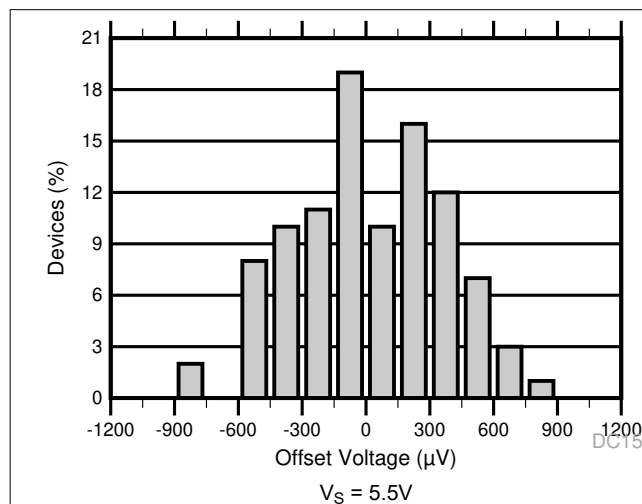


図 5-1. Offset Voltage Production Distribution

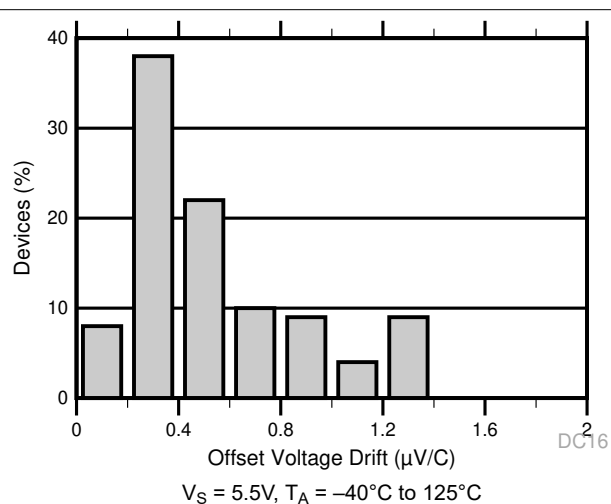


図 5-2. Offset Voltage Drift Distribution

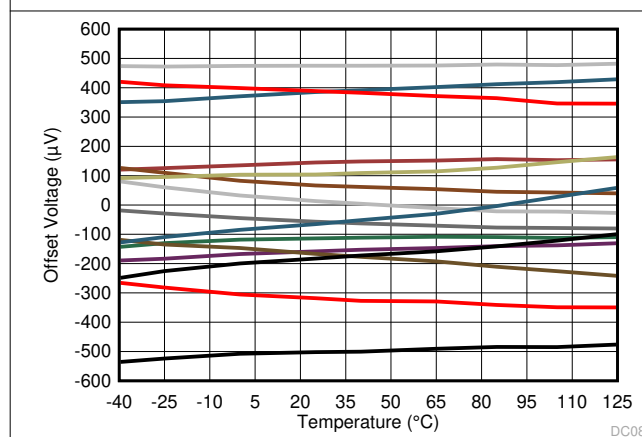


図 5-3. Offset Voltage vs Temperature

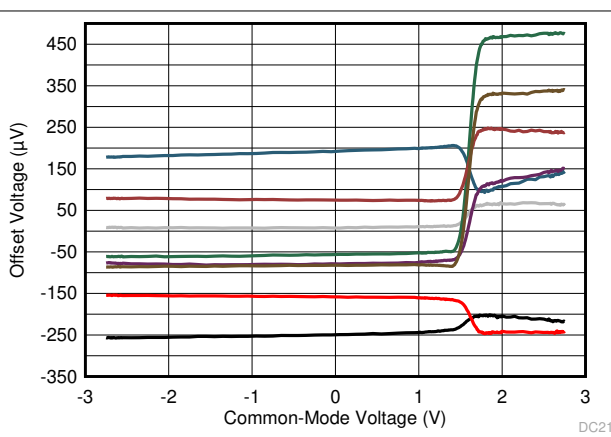


図 5-4. Offset Voltage vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

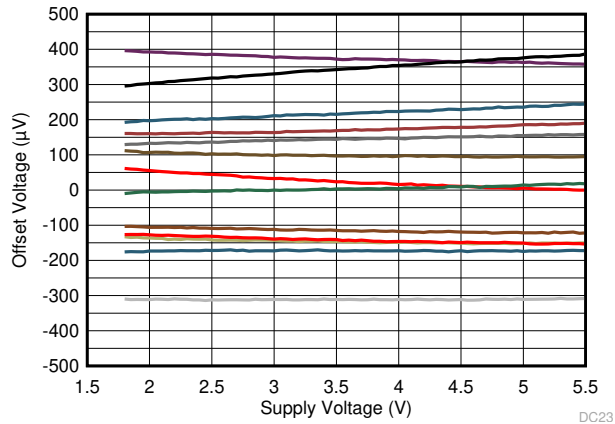


図 5-5. Offset Voltage vs Power Supply

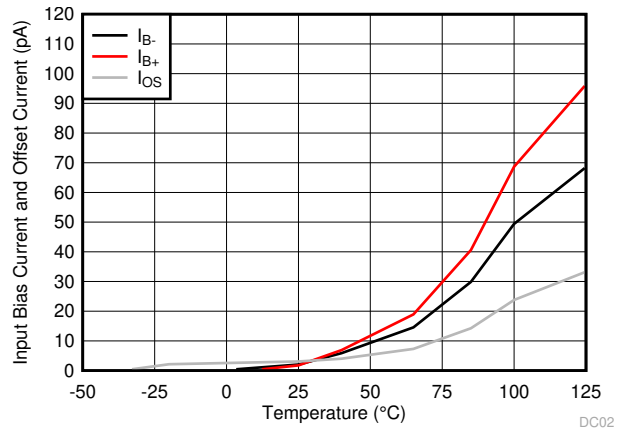


図 5-6. Input Bias Current vs Temperature

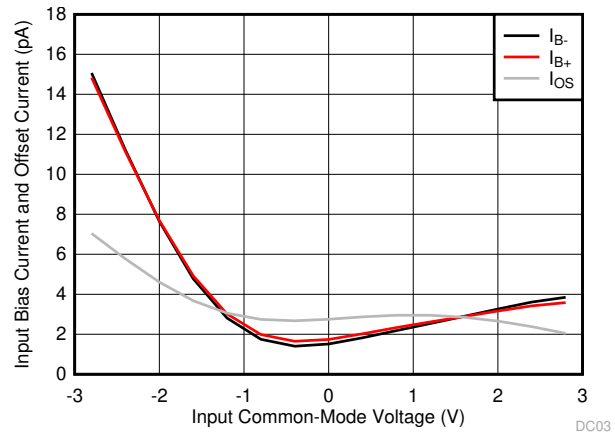


図 5-7. Input Bias Current and Offset Current vs Common-Mode Voltage

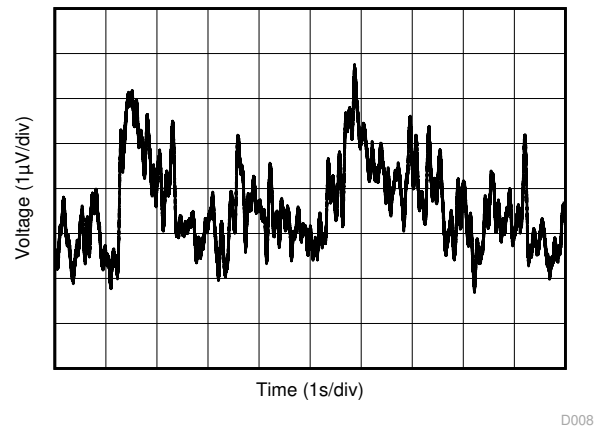


図 5-8. 0.1-Hz to 10-Hz Input Voltage Noise

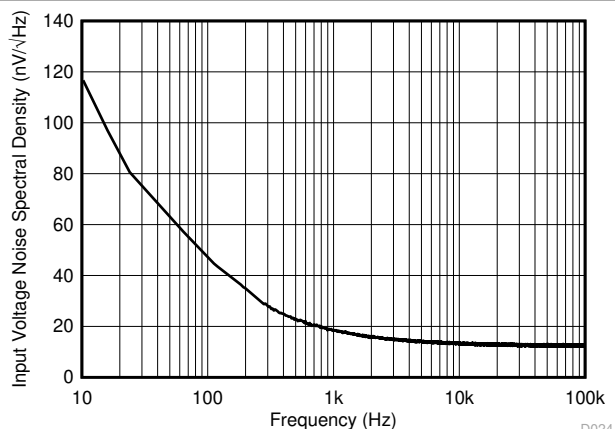


図 5-9. Input Voltage Noise Spectral Density vs Frequency

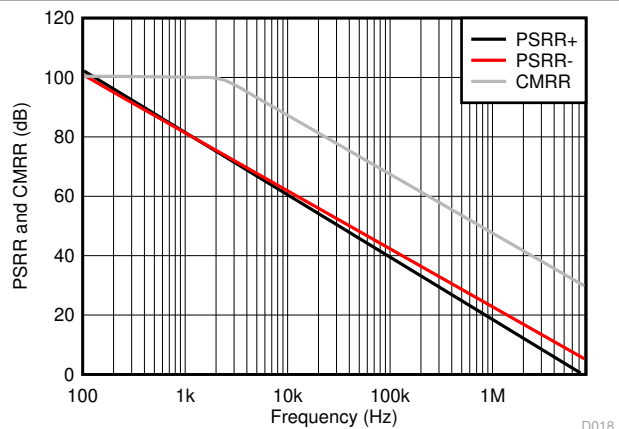
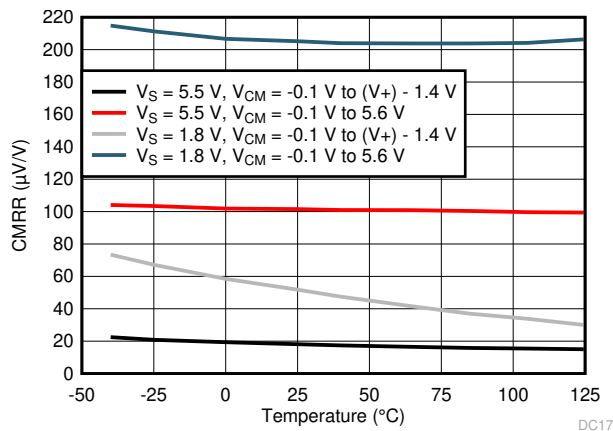


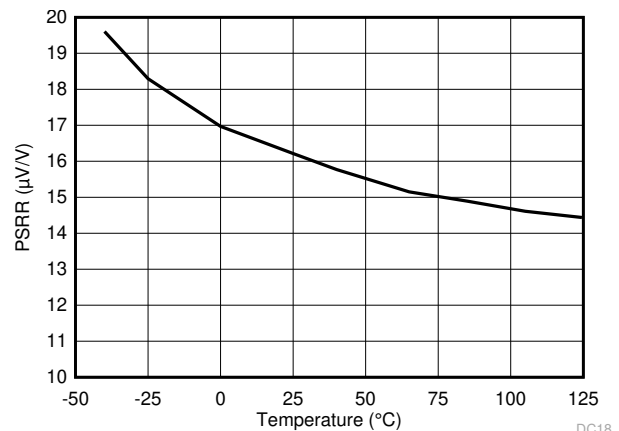
図 5-10. CMRR and PSRR vs Frequency (Referred to Input)

5.8 Typical Characteristics (continued)

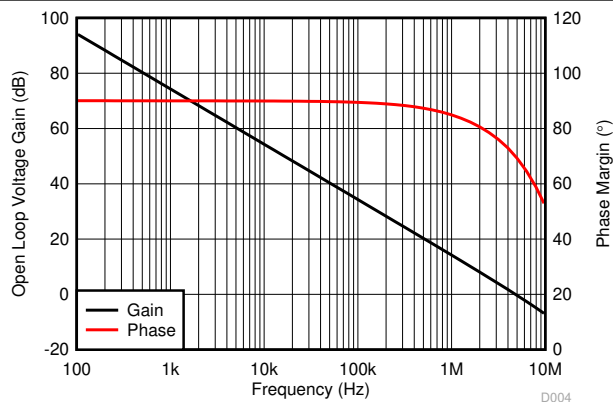
at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



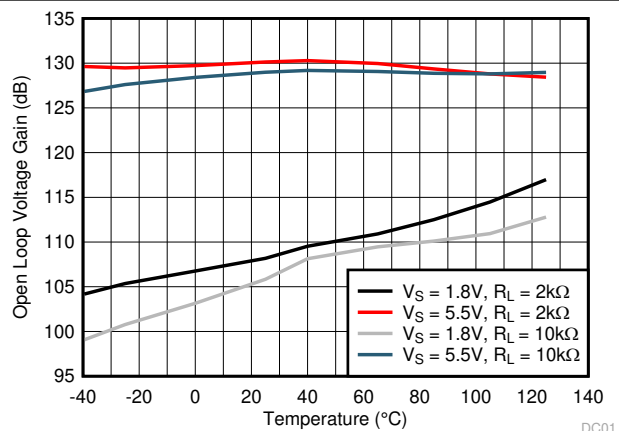
5-11. CMRR vs Temperature



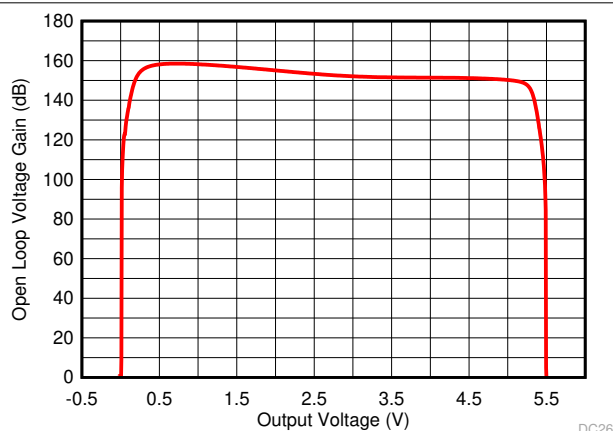
5-12. PSRR vs Temperature



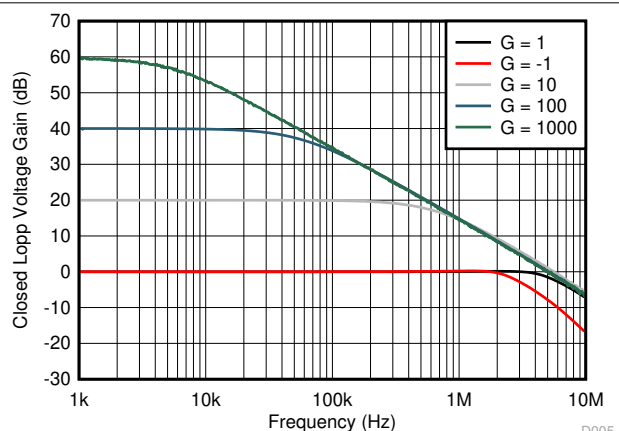
5-13. Open Loop Voltage Gain and Phase vs Frequency



5-14. Open Loop Voltage Gain vs Temperature



5-15. Open Loop Voltage Gain vs Output Voltage



5-16. Closed Loop Voltage Gain vs Frequency

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

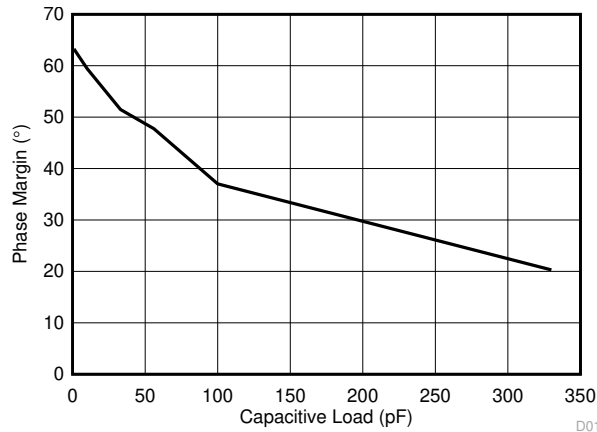


Figure 5-17. Phase Margin vs Capacitive Load

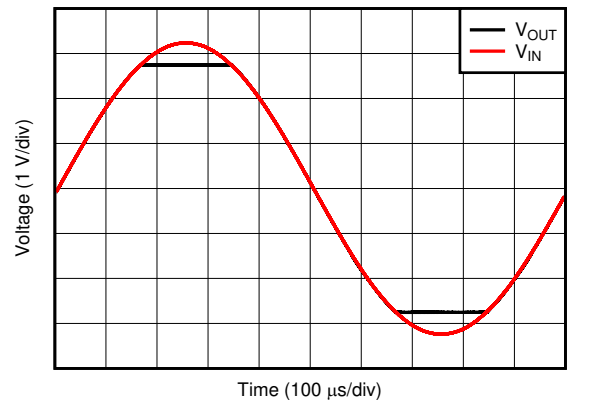


Figure 5-18. No Phase Reversal

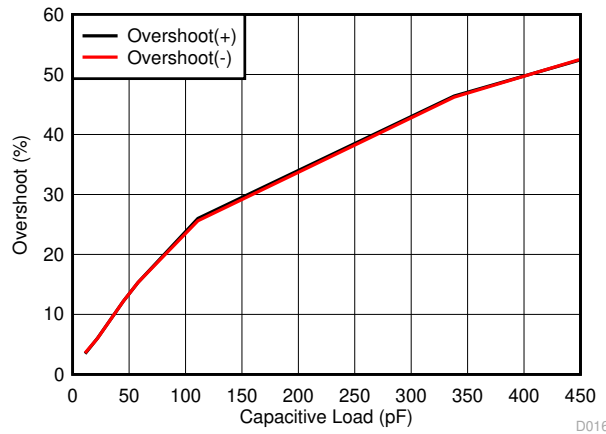


Figure 5-19. Small-Signal Overshoot vs Load Capacitance

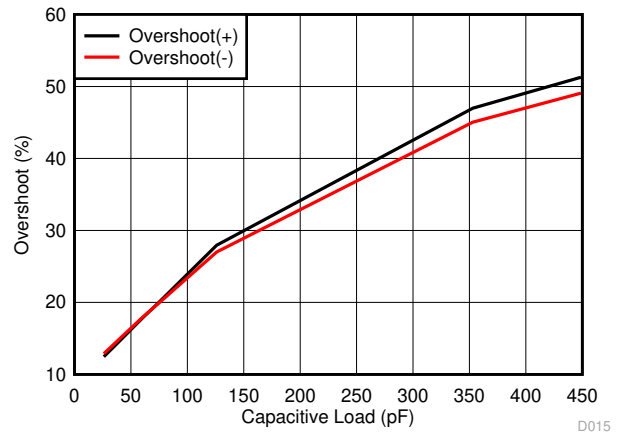


Figure 5-20. Small-Signal Overshoot vs Load Capacitance

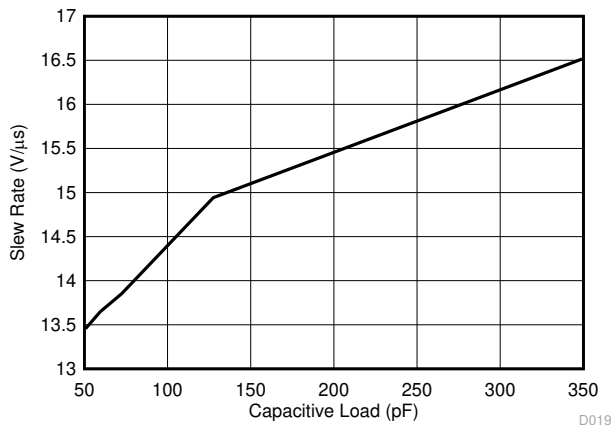


Figure 5-21. Slew Rate vs Capacitive Load

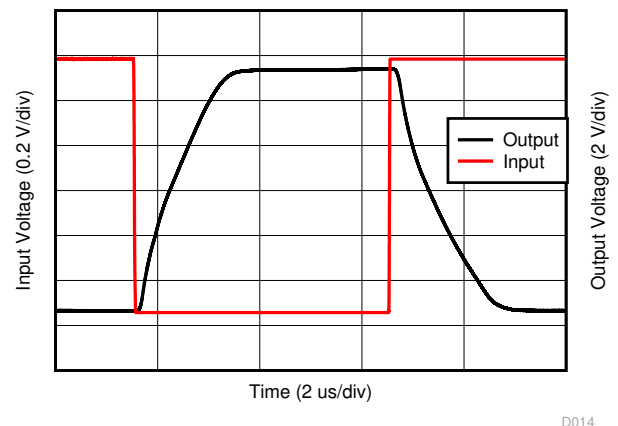
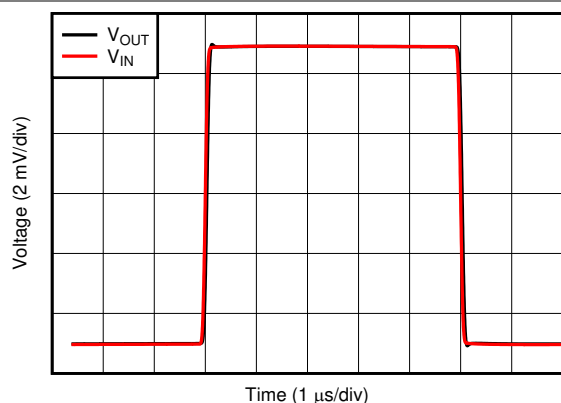


Figure 5-22. Overload Recovery

5.8 Typical Characteristics (continued)

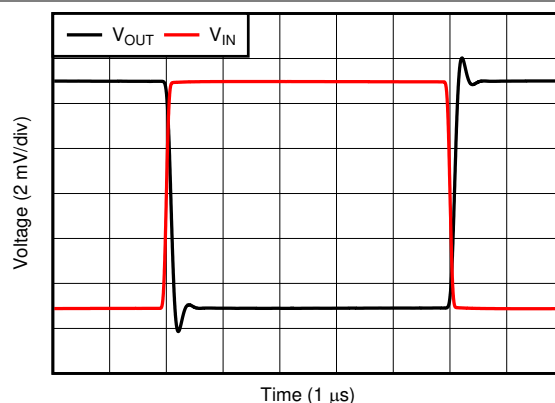
at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



D021

$G = +1\text{V/V}$
 V_{OUT} step = 10
mV_{p-p}

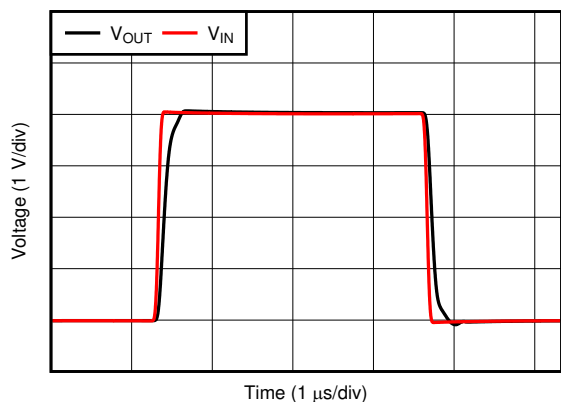
5-23. Small-Signal Step Response



D020

$G = -1\text{V/V}$
 V_{OUT} step = 10
mV_{p-p}

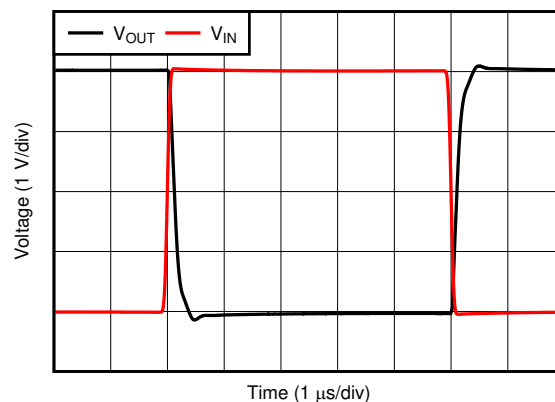
5-24. Small-Signal Step Response



D012

$G = +1\text{V/V}$
 V_{OUT} step = 4V_{p-p}

5-25. Large-Signal Step Response



D011

$G = -1\text{V/V}$
 V_{OUT} step = 4V_{p-p}

5-26. Large-Signal Step Response

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

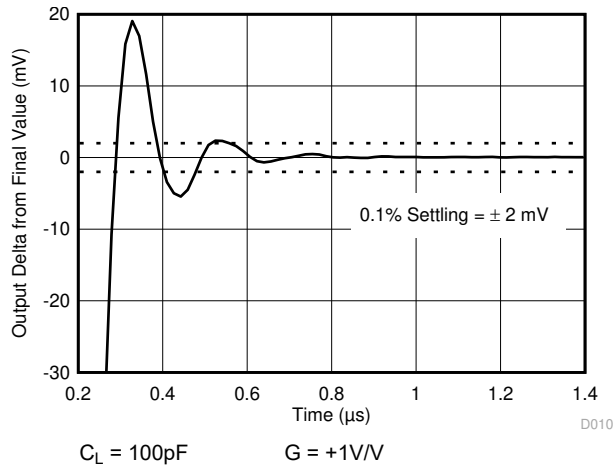


Figure 5-27. Positive Large-Signal Settling Time

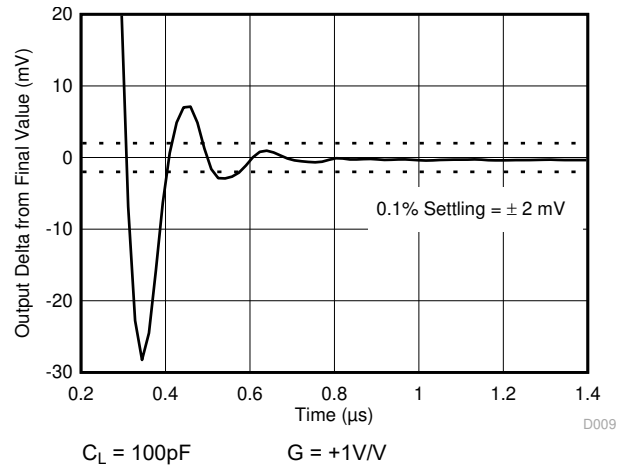


Figure 5-28. Negative Large-Signal Settling Time

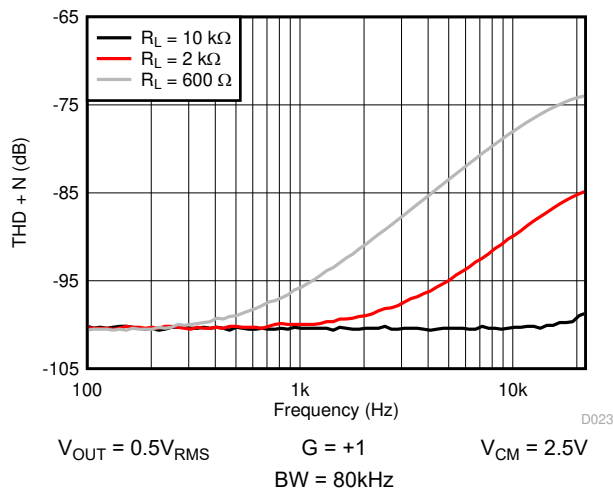


Figure 5-29. THD + N vs Frequency

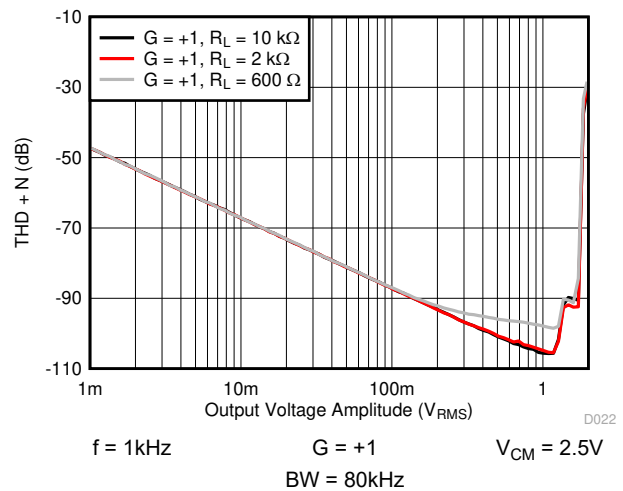


Figure 5-30. THD + N vs Amplitude

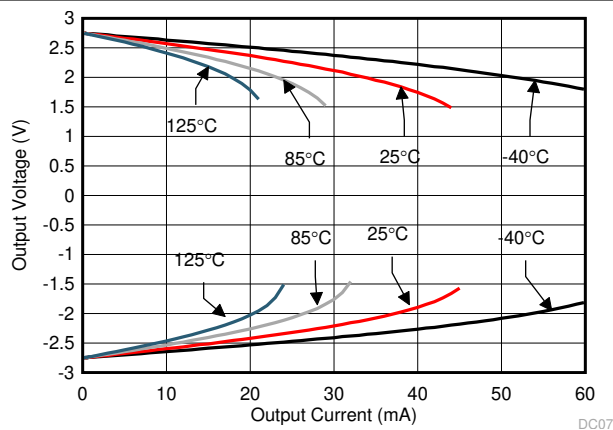


Figure 5-31. Output Voltage Swing vs Output Current

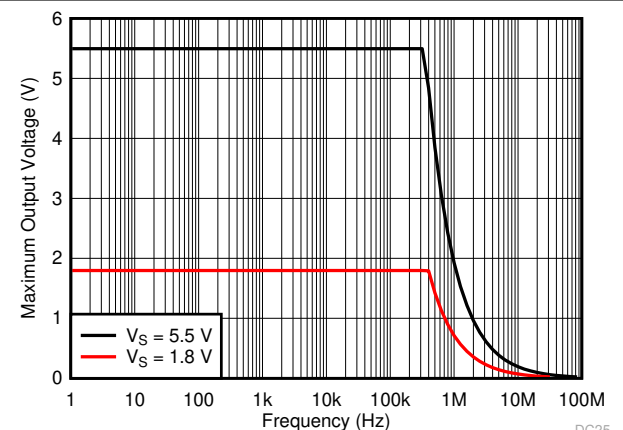


Figure 5-32. Maximum Output Voltage vs Frequency and Supply Voltage

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

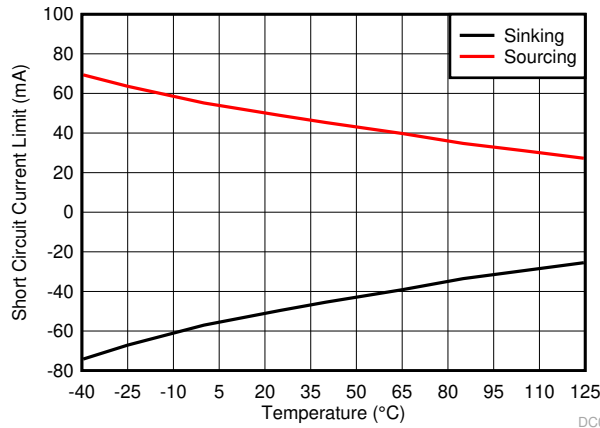


FIG 5-33. Short-Circuit Current vs Temperature

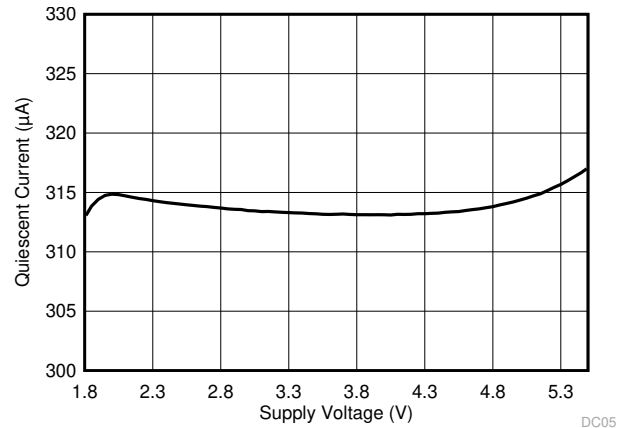


FIG 5-34. Quiescent Current vs Supply Voltage

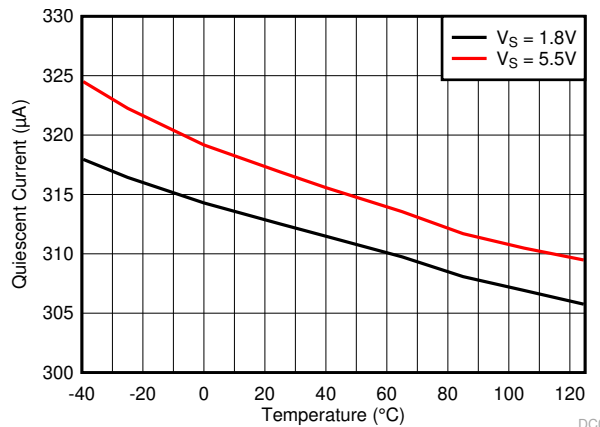


FIG 5-35. Quiescent Current vs Temperature

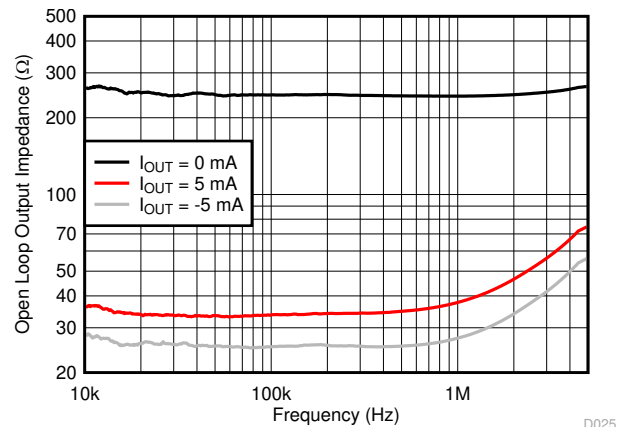


FIG 5-36. Open-Loop Output Impedance vs Frequency

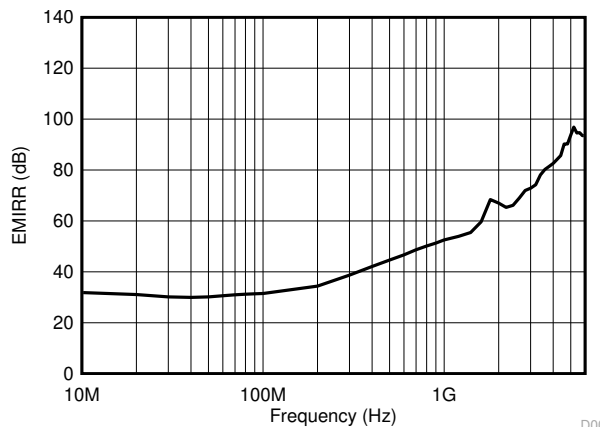


FIG 5-37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

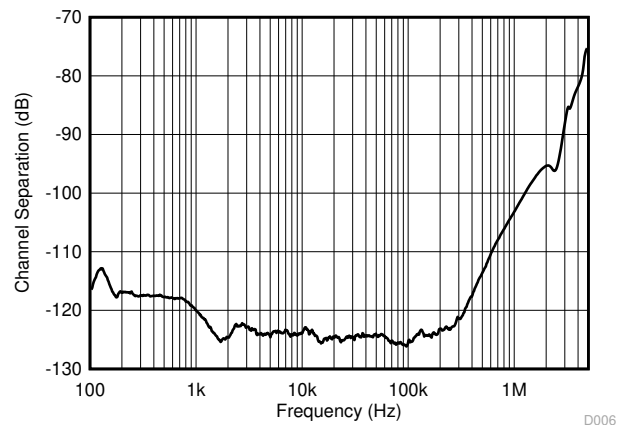


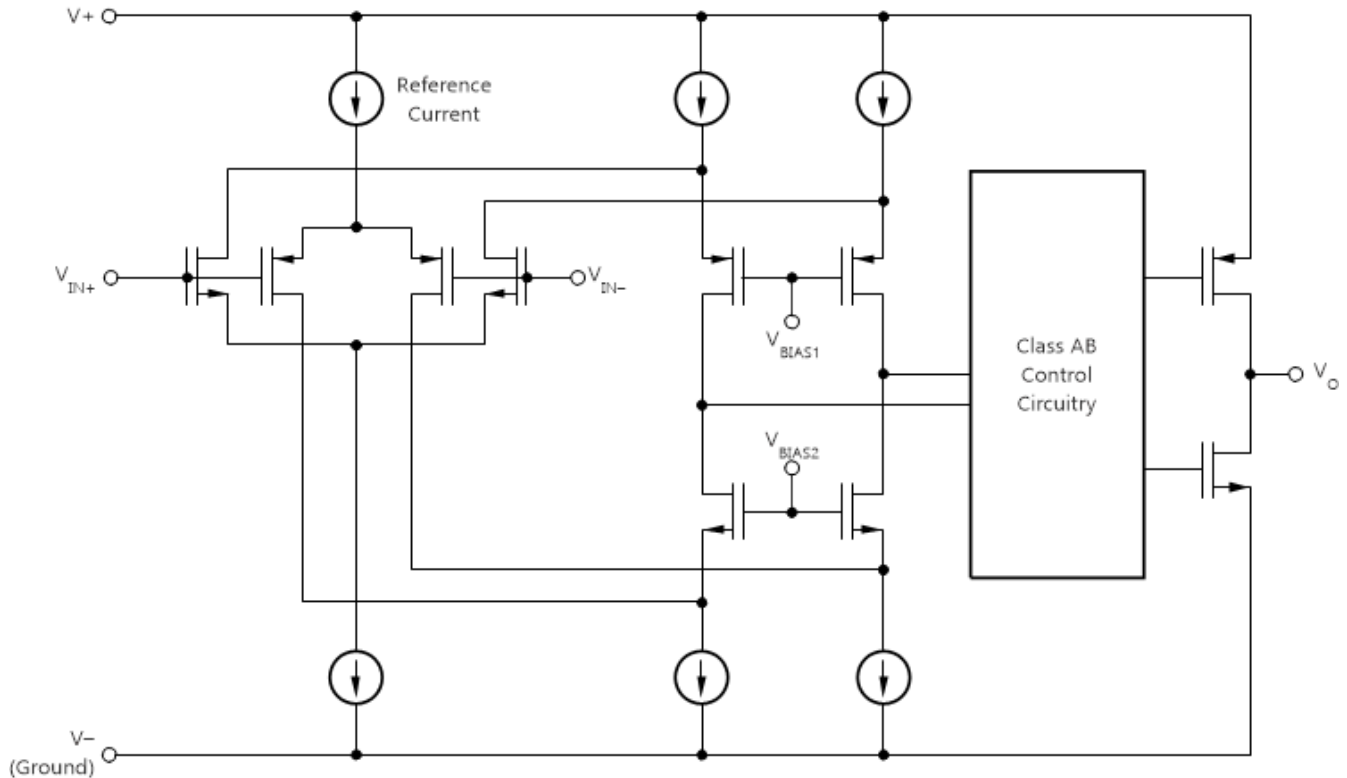
FIG 5-38. Channel Separation vs Frequency

6 Detailed Description

6.1 Overview

The TLV905x-Q1 devices are a 5MHz family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 6V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV905x-Q1 family to be used in virtually any single-supply application. The unique combination of a high slew rate and low quiescent current makes this family a potential choice for battery-powered motor-drive applications. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Voltage

The TLV905x-Q1 family of op amps is specified for operation from 1.8V to 6.0V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are illustrated in the [Typical Characteristics](#).

6.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV905x-Q1 family extends 100mV beyond the supply rails for the full supply voltage range of 1.8V to 6.0V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4\text{V}$ to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately $(V+) - 1.4\text{V}$. There is a small transition region, typically $(V+) - 1.2\text{V}$ to $(V+) - 1\text{V}$, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (with both stages on) can range from $(V+) - 1.4\text{V}$ to $(V+) - 1.2\text{V}$ on the low end, and up to $(V+) - 1\text{V}$ to $(V+) - 0.8\text{V}$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

6.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage operational amplifiers, the TLV905x-Q1 family delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10k Ω , the output swings to within 16mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

6.3.4 EMI Rejection

The TLV905x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV905x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. [図 6-1](#) shows the results of this testing on the TLV905x-Q1. [表 6-1](#) lists the EMIRR IN+ values for the TLV905x-Q1 at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

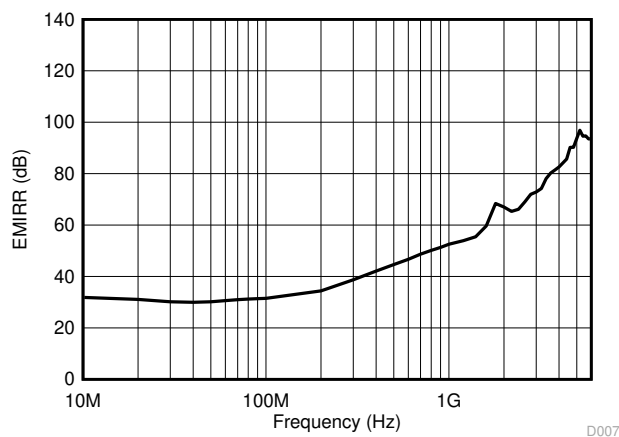


図 6-1. EMIRR Testing

表 6-1. TLV905x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	41.8dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	53.1dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	71.8dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	81.2dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	92.5dB

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After the device enters the saturation region, the output devices require time to return to the linear operating state. After the output devices return to a linear operating state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV905x-Q1 family is approximately 300ns.

6.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance ESD circuitry has to an electrical overstress event is helpful. [図 6-2](#) shows the ESD circuits contained in the TLV905x-Q1 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the diode routes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

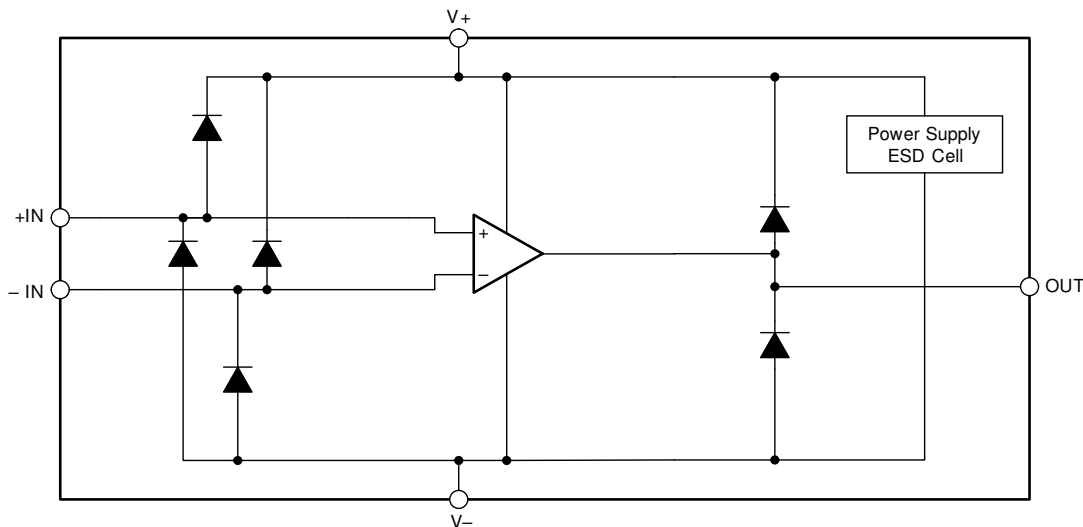


図 6-2. Equivalent Internal ESD Circuitry

6.3.7 Input Protection

The TLV905x-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA (for more information, see [Absolute Maximum Ratings](#)). 図 6-3 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

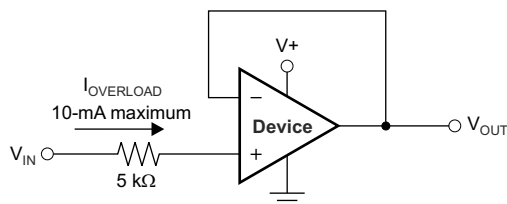


図 6-3. Input Current Protection

6.4 Device Functional Modes

The TLV905x-Q1 family is operational when the power-supply voltage is between 1.8V (± 0.9 V) and 6.0V (± 3.0 V).

7 Application and Implementation

注

以下のアプリケーションに関するセクションの情報は、TI の部品仕様の一部ではなく、TI はこれらの情報の正確性や完全性を保証しません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TLV905x-Q1 family features 5MHz bandwidth and very high slew rate of 15V/μs with only 330μA of supply current per channel, providing excellent AC performance at very low-power consumption. DC applications are well served with a very low input noise voltage of 15nV/√Hz at 10kHz, low input bias current, and a typical input offset voltage of 0.33mV.

7.2 Typical Low-Side Current Sense Application

図 7-1 shows the TLV905x-Q1 configured in a low-side current sensing application.

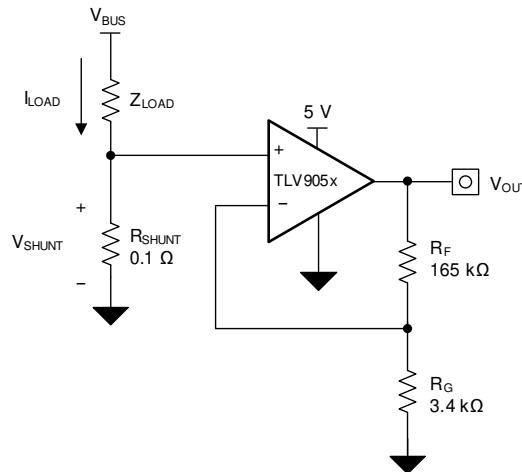


図 7-1. TLV905x-Q1 in a Low-Side, Current-Sensing Application

7.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.95V
- Maximum shunt voltage: 100mV

7.2.2 Detailed Design Procedure

The transfer function of the circuit in 図 7-1 is given in 式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using 式 2.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

Using 式 2, R_{SHUNT} equals 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV905x-Q1 device to produce an output voltage of approximately 0V to 4.95V. 式 3 calculates the gain required for the TLV905x-Q1 device to produce the required output voltage.

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using 式 3, the required gain equals 49.5V/V, which is set with the R_F and R_G resistors. 式 4 sizes the R_F and R_G resistors to set the gain of the TLV905x-Q1 device to 49.5V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F to equal 165kΩ and R_G to equal 3.4kΩ provides a combination that equals approximately 49.5V/V. 図 7-2 shows the measured transfer function of the circuit shown in 図 7-1.

7.2.3 Application Curve

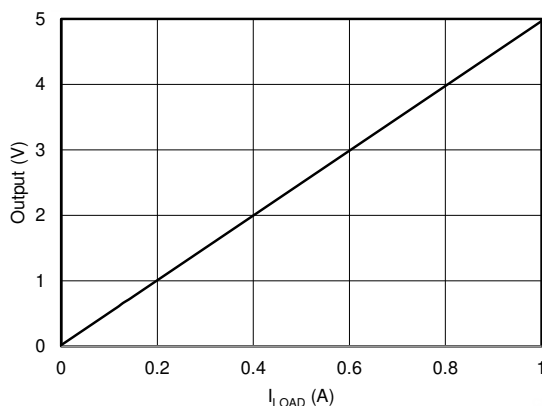


図 7-2. Low-Side, Current-Sense Transfer Function

7.3 Power Supply Recommendations

The TLV905x-Q1 family is specified for operation from 1.8V to 6.0V ($\pm 0.9V$ to $\pm 3.0V$); many specifications apply from -40°C to 125°C . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages larger than 7V can permanently damage the device; for more information, see the [Absolute Maximum Ratings](#) table.

Place 0.1 μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more-detailed information on bypass capacitor placement, see [Figure 7-3](#).

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 7-3](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

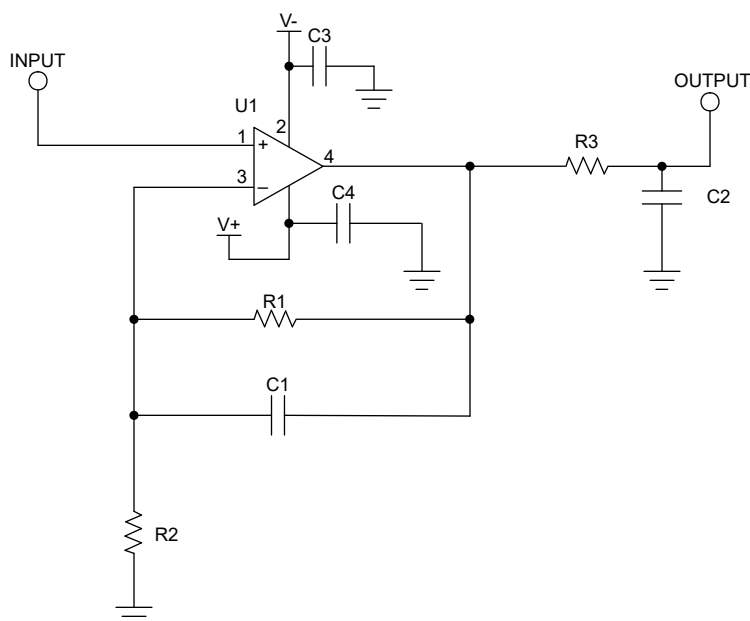


図 7-3. Schematic for Noninverting Configuration Layout Example

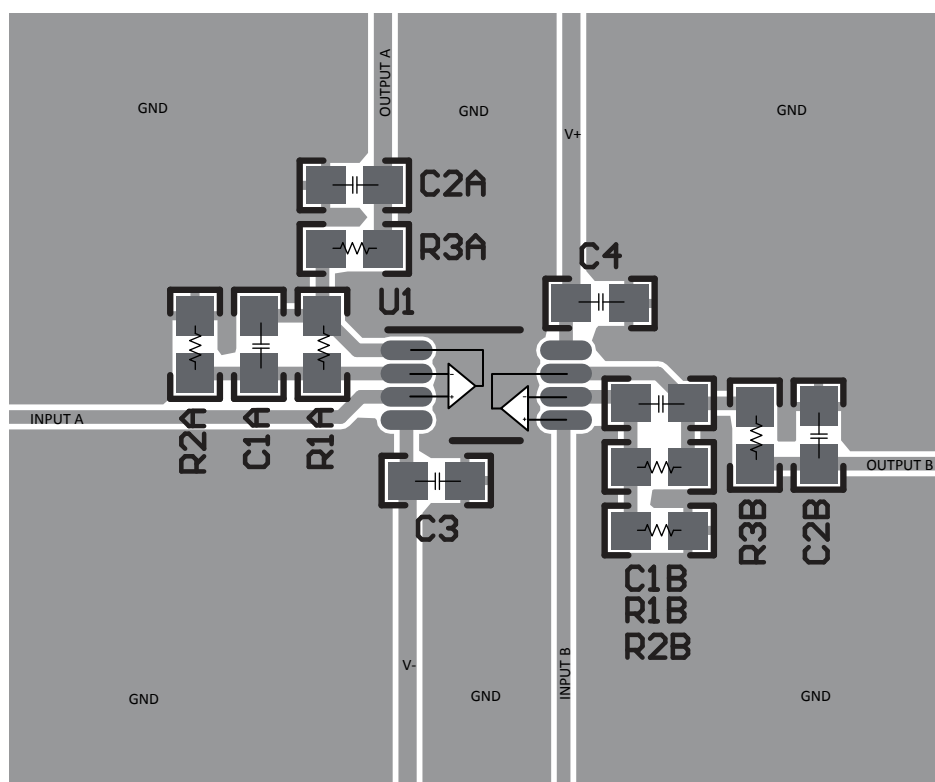


図 7-4. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers application report](#)
- Texas Instruments, [Low Voltage, High Slew Rate Op-amps for Motor Drive Circuits application report](#)
- Texas Instruments, [TI Analog Circuit Cookbook Analog Engineer's Circuit](#)
- Texas Instruments, [TI Precision Labs - Amplifiers training video](#)

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

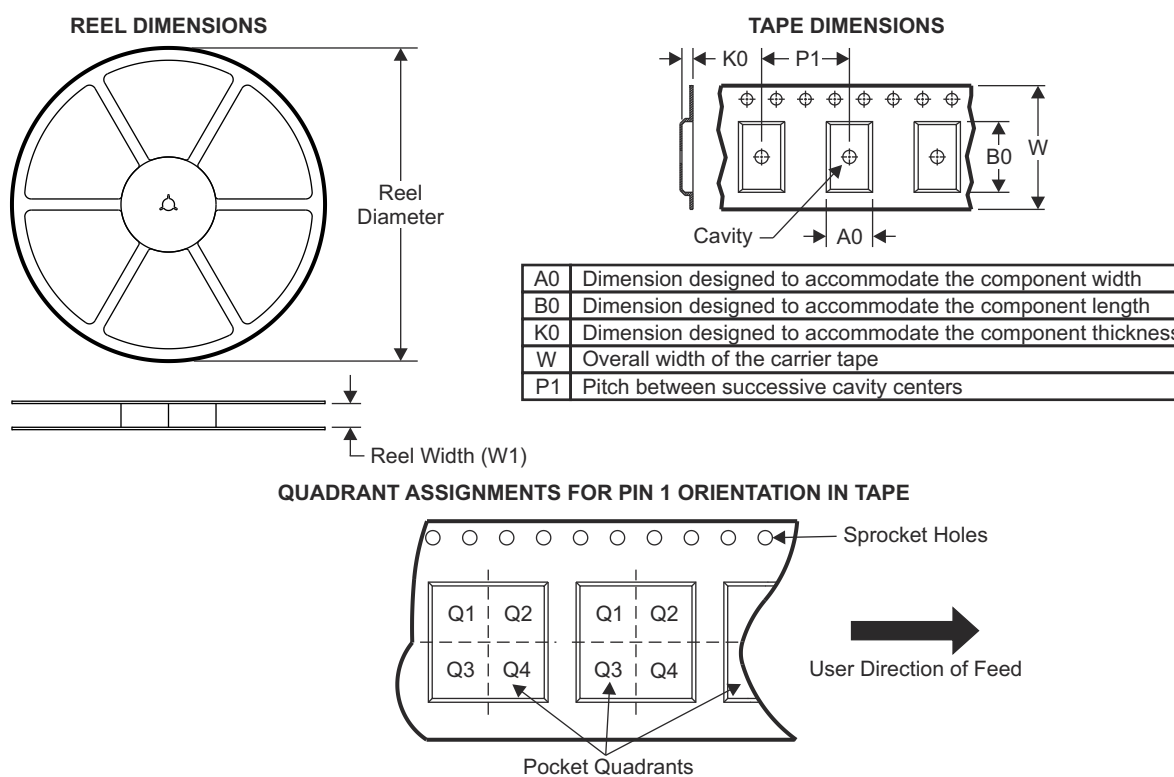
9 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

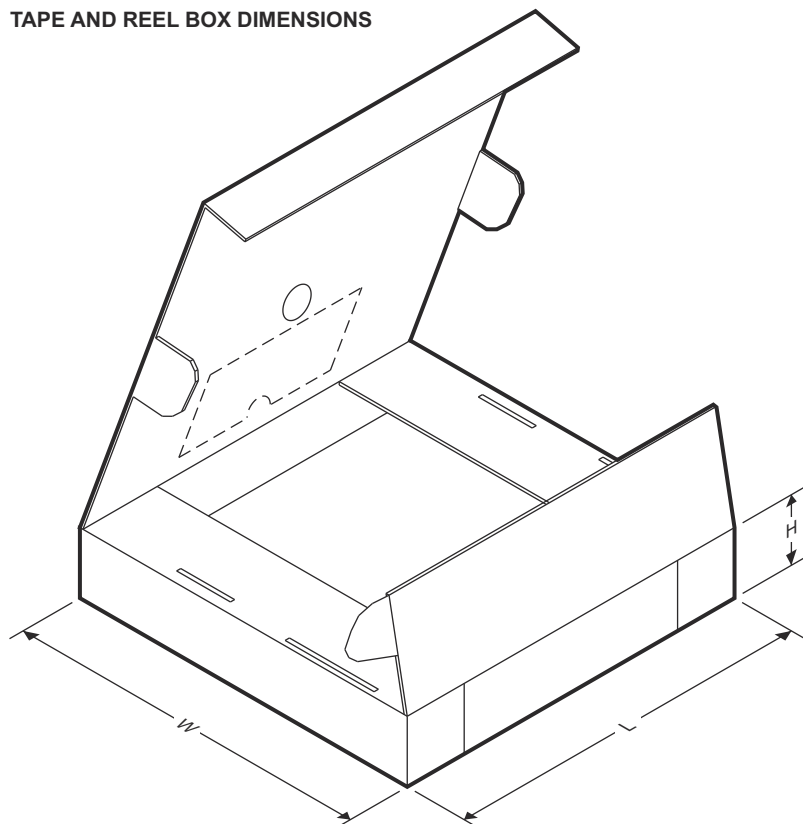
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

10.1 Tape and Reel Information



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9051QDBVRQ1	SOT-23	DBV	5	3000	180	8	3.2	3.2	1.4	4	5.3	Q3
TLV9052QPWRQ1	TSSOP	PW	8	3000	330	12	7	3.6	1.6	8	12	Q3

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9051QDBVRQ1	SOT-23	DBV	5	3000	210	185	35
TLV9052QPWRQ1	TSSOP	PW	8	3000	470	380	18

10.2 Mechanical Data

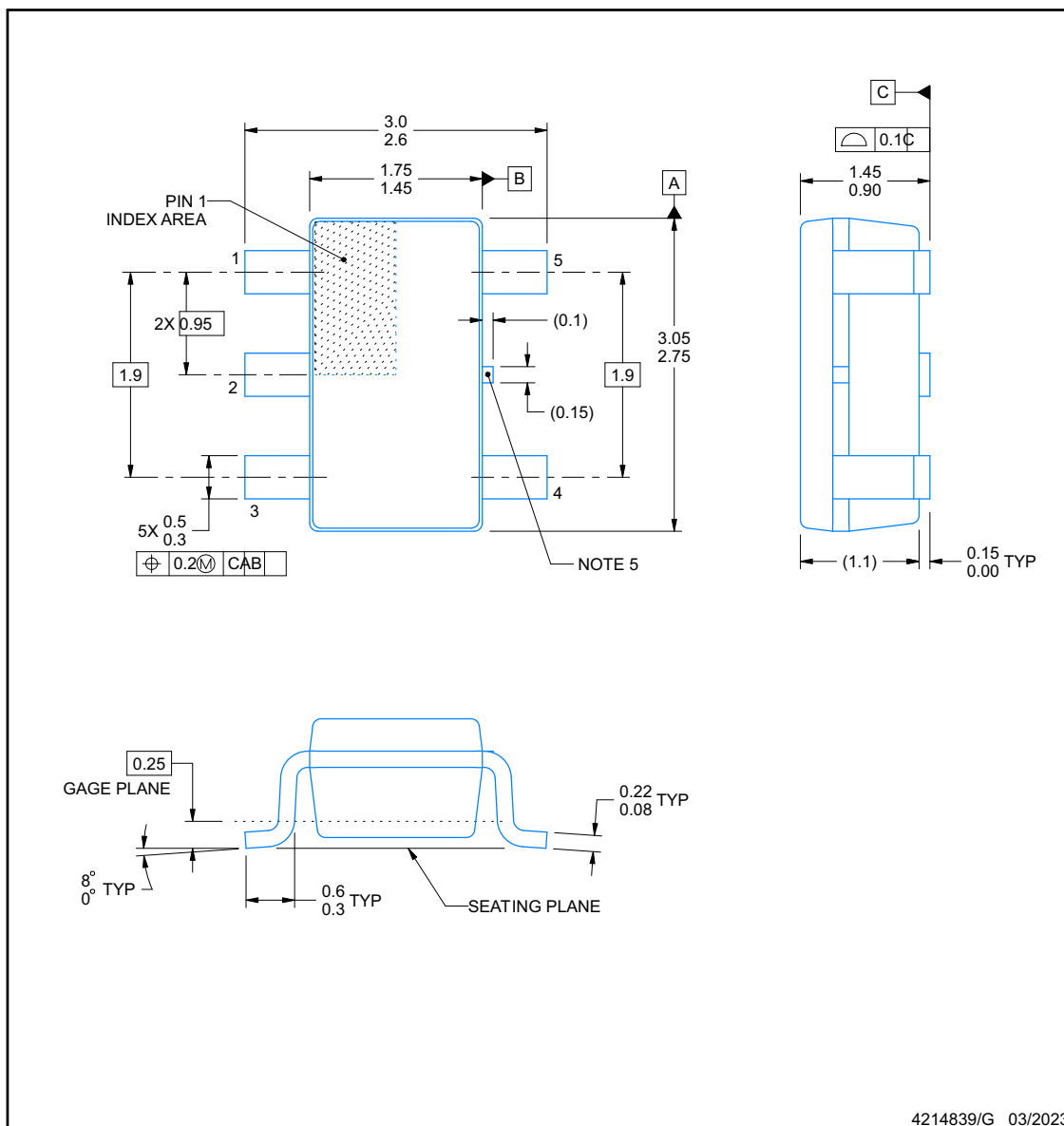
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

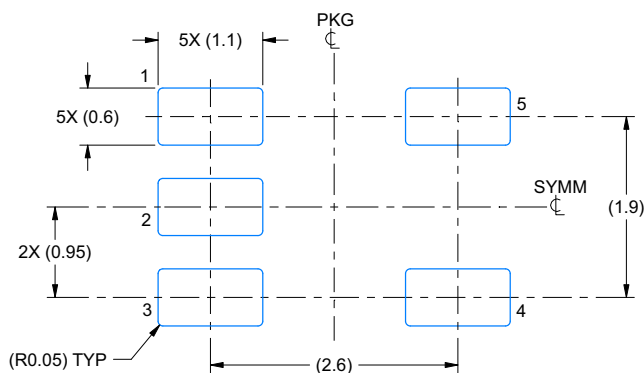
EXAMPLE BOARD LAYOUT

DBV0005A

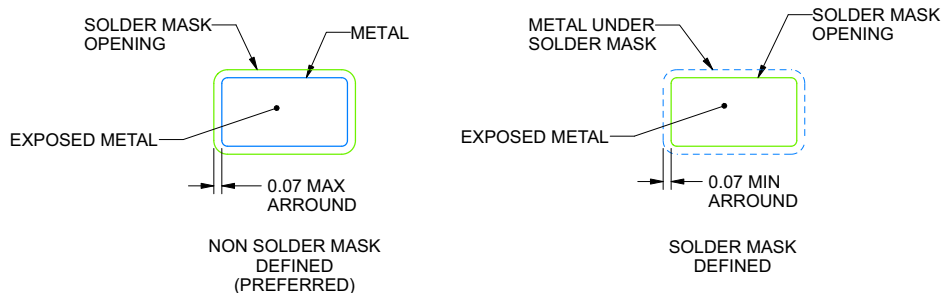
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

ADVANCE INFORMATION



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

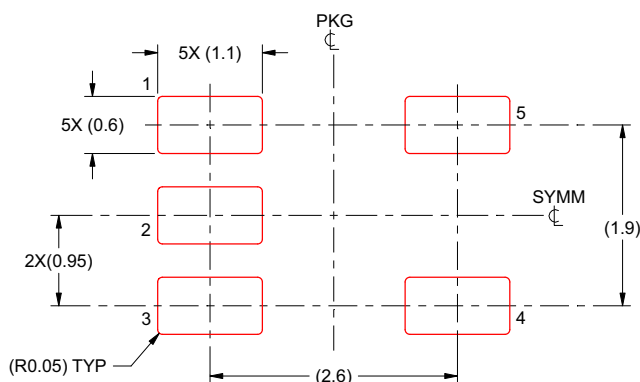
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

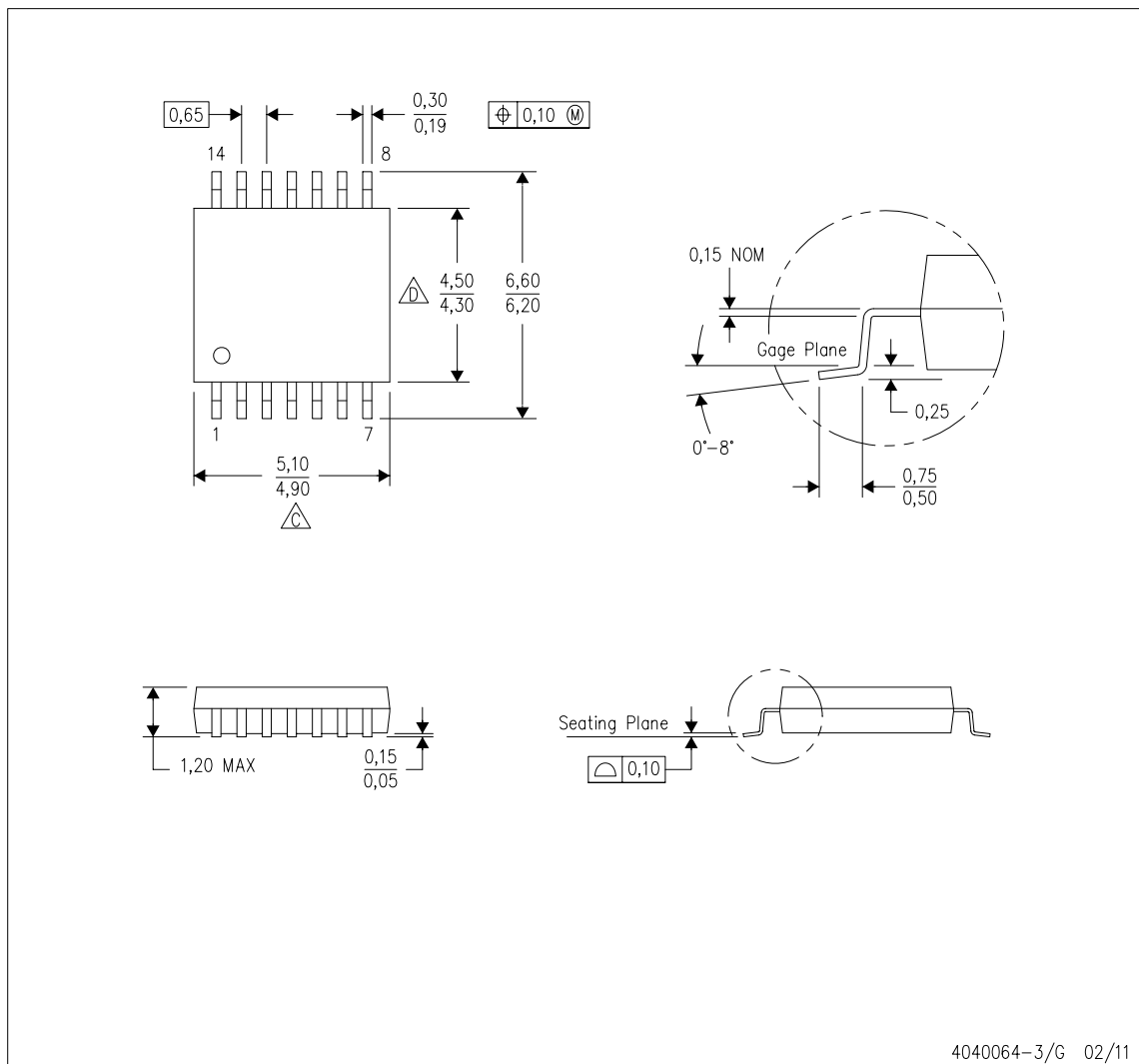
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

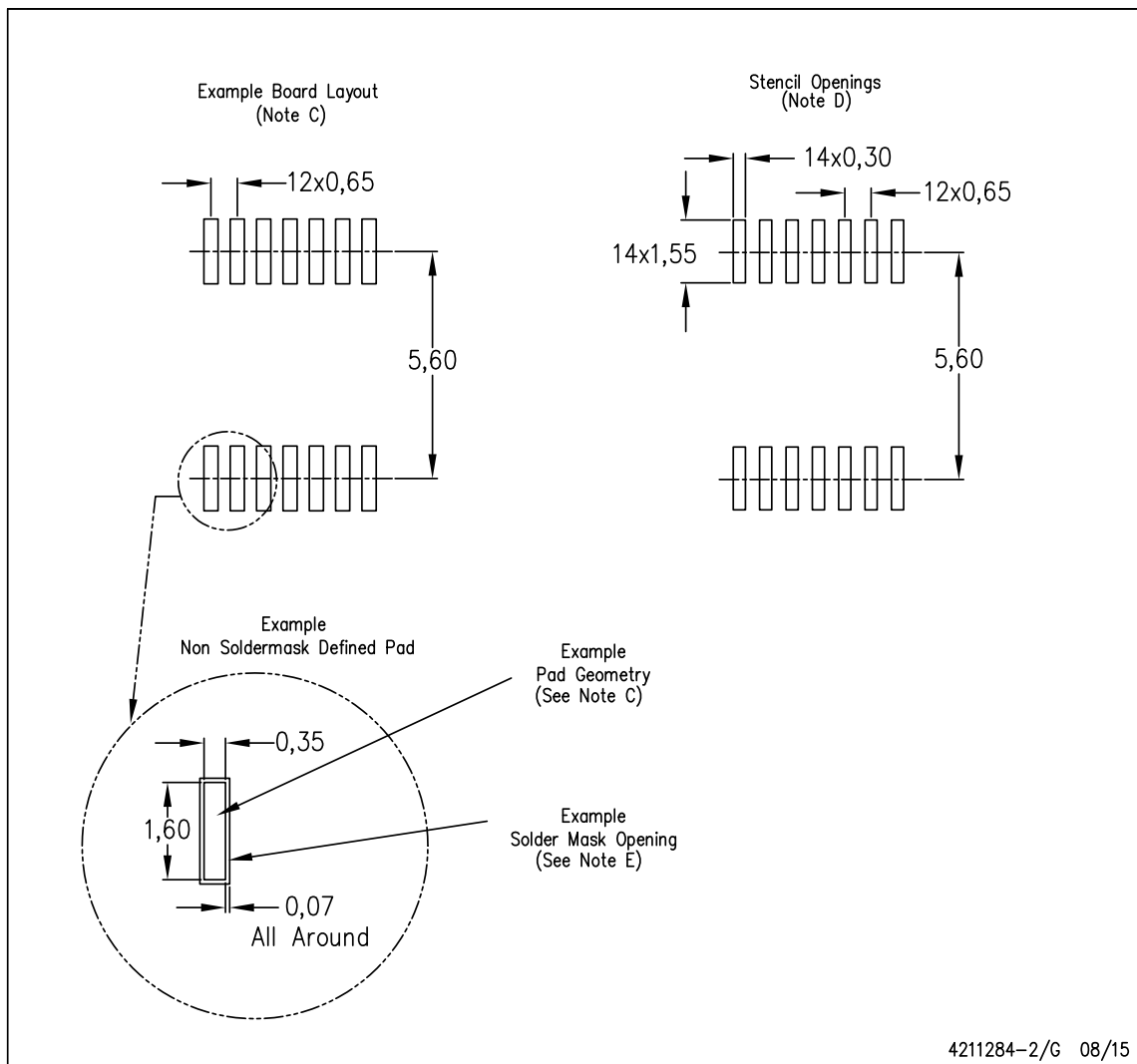


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9051QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV9052QPWRQ1	ACTIVE	TSSOP	PW	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV9052-Q1 :

- Catalog : [TLV9052](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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