TEXAS INSTRUMENTS
TMUXHS4446
JAJST97 – FEBRUARY 2024

TMUXHS4446 USB-C 10Gbps 代替モード クロスバー マルチプレクサ

1 特長

- パッシブ双方向 USB-C 代替モード マルチプレクサにより USB と DisplayPort 信号を切り替え
- レーンあたり最大 10Gbps の USB 3.2 (Gen 2.0) および最大 10Gbps の DisplayPort 2.1 (UHBR10) をサポート
- ソース/ホストおよびシンク/デバイス アプリケーションと互換
- -3dB 差動 BW :9.5GHz
- 動的特性
  - 挿入損失:-1.6dB (5GHz)
  - 反射損失:–18dB (5GHz)
- 0V～1.8V の同相電圧 (CMV) をサポート
- 適応型 CMV トラッキング
- 6V 許容の SBU ピンにより VBUS への短絡イベントに耐性
- GPIO ピンまたは I^2C により設定可能
- 1.8V と 3.3V の両方の I^2C をサポート
- 電源電圧、V_{CC}:3.3V
- 動作時消費電力:340µA
- 低いスタンバイ消費電力:0.5µA (ピン モード)
- 拡張産業用温度範囲:-40℃～105℃
- 3mm × 6mm の QFN パッケージで供給

2 アプリケーション

- PC およびノートパソコン
- テレビ
- ゲーム
- ドッキング ステーション
- ホーム シアターおよびエンターテインメント
- ファクトリ オートメーション / 制御
- 電子 POS (EPOS)
- スマートフォン
- タブレット

3 概要

TMUXHS4446 は、高速の双方向パッシブ クロスポイント スイッチ、すなわちクロスバー (XBAR) です。このデバイスは、USB-C インターフェイスとも呼ばれる USB Type-C 経由の信号を、3.2 Gen2 SuperSpeed と DisplayPort1.4/2.1 (最大 10Gbps UHBR10) の間で切り替えるために使用されます。このデバイスは、DisplayPort 補助チャネルに使用される低速 SBU 信号の切り替えも行います。TMUXHS4446 は、同相電圧 (CMV) 範囲が 0V～1.8V、差動振幅が 0V～1800mVpp の差動信号をサポートしています。適応型 CMV トラッキングにより、デバイスを通るチャネルが同相電圧範囲全体にわたって変化しないようにしています。

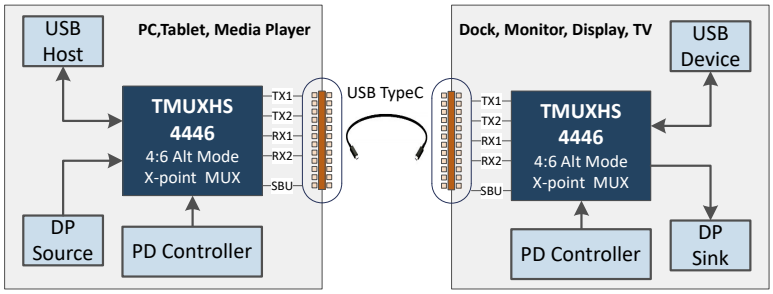
TMUXHS4446 の動的特性が可能にした高速スイッチングでは、信号アイ ダイアグラムの減衰は最小化され、発生するジッタは非常に低いレベルに抑えられます。このデバイスのシリコン設計は、高い周波数の信号帯域でも優れた周波数応答が得られるように最適化されています。TMUXHS4446 のシリコン信号トレースとスイッチ ネットワークは、最良のペア内スキュー性能が得られるように整合されています。

TMUXHS4446 は、産業用および高信頼性用途などの多数の堅牢なアプリケーションに適した拡張産業用温度範囲 (−40°C から 105°C) で動作します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TMUXHS4446	RET (WQFN、40)	6mm × 3mm

(1) 供給されているすべてのパッケージについては、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション使用事例

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4 Pin Configuration and Functions

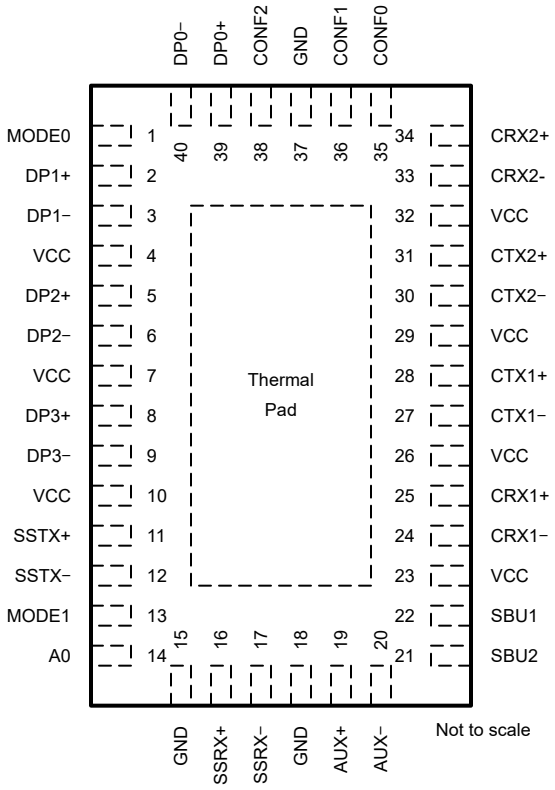

図 4-1. RET Package With Thermal Pad (40 Pin QFN - Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DP0+	39	HS I/O	System-side, high-speed differential positive signal for DisplayPort DP0
DP0–	40	HS I/O	System-side, high-speed differential negative signal for DisplayPort DP0
DP1+	2	HS I/O	System-side, high-speed differential positive signal for DisplayPort DP1
DP1–	3	HS I/O	System-side, high-speed differential negative signal for DisplayPort DP1
DP2+	5	HS I/O	System-side, high-speed differential positive signal for DisplayPort DP2
DP2–	6	HS I/O	System-side, high-speed differential negative signal for DisplayPort DP2
DP3+	8	HS I/O	System-side, high-speed differential positive signal for DisplayPort DP3
DP3–	9	HS I/O	System-side, high-speed differential negative signal for DisplayPort DP3
SSTX+	11	HS I/O	System-side, high-speed differential positive signal for USB TX pins
SSTX–	12	HS I/O	System-side, high-speed differential negative signal for USB TX pins
SSRX+	16	HS I/O	System-side, high-speed differential positive signal for USB RX pins
SSRX–	17	HS I/O	System-side, high-speed differential negative signal for USB RX pins
CRX1–	24	HS I/O	Connector-side, high-speed differential negative signal for USB-C RX pins
CRX1+	25	HS I/O	Connector-side, high-speed differential positive signal for USB-C RX pins
CTX1–	27	HS I/O	Connector-side, high-speed differential negative signal for USB-C TX pins
CTX1+	28	HS I/O	Connector-side, high-speed differential positive signal for USB-C TX pins

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CTX2–	30	HS I/O	Connector-side, high-speed differential negative signal for USB-C TX pins
CTX2+	31	HS I/O	Connector-side, high-speed differential positive signal for USB-C TX pins
CRX2-	33	HS I/O	Connector-side, high-speed differential negative signal for USB-C RX pins
CRX2+	34	HS I/O	Connector-side, high-speed differential positive signal for USB-C RX pins
AUX+	19	LS I/O	System-side, low-speed SBU signal for USB-C SBU pin
AUX–	20	LS I/O	System-side, low-speed SBU signal for USB-C SBU pin
SBU1	22	LS I/O	Connector-side, low-speed SBU signal for USB-C SBU1 pin
SBU2	21	LS I/O	Connector-side, low-speed SBU signal for USB-C SBU2 pin
MODE0	1	CTRL	Control mode selection MODE0 = 1, I^2C control MODE0 = 0, GPIO or pin control through CONF[2:0]
MODE1	13	CTRL	I^2C logic level control (MODE0 = 1) MODE1 = 0, 1.8V I^2C logic level MODE1 = 1, 3.3V I^2C logic level
CONF0	35	CTRL	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to the *Device Functional Modes* section for details.
A1		CTRL	I^2C control (MODE0 = 1) Configurable I^2C target address bit
CONF1	36	CTRL	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to the *Device Functional Modes* section for details.
SCL		CTRL	I^2C control (MODE0 = 1) I^2C clock input
CONF2	38	CTRL	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to the *Device Functional Modes* section for details.
SDA		CTRL	I^2C control (MODE0 = 1) I^2C data input
A0	14	CTRL	I^2C control (MODE0 = 1) Configurable I^2C target address bit
VCC	4, 7, 10, 23, 26, 29, 32	P	Power
GND	15, 18, 37, Thermal Pad	G	Ground

(1) HS I/O = High-Speed Input/Output, LS I/O = Low-Speed Input/Output, CTRL = Control Inputs, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{CC-ABSMAX}$	Supply voltage	–0.5	4	V
$V_{HS-ABSMAX}$	High Speed Differential I/O pin voltage ([SS/C]TXx[+/-], [SS/C]RXx[+/-], DPx[+/-])	–0.5	2.4	V
$V_{L\ S-ABSMAX}$	Low Speed I/O pin voltage (AUX[+/-], SBUx)	–0.5	6.0	V
$V_{CTR-ABSMAX}$	Control pin voltage (MODE[1:0], CONF[2:0], A[1:0], SDA, SCL)	–0.5	V_{CC}+0.4	V
$T_{J-ABSMAX}$	Junction temperature	–65	125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3.0	3.3	3.6	V
$V_{CC-RAMP}$	Supply voltage ramp time		0.1		100	ms
(1)DR_{HS}	Data rate, high speed datapaths (Cx to DPx/SSx)	Differential AC coupled interfaces			10	Gbps
(1)DR_{SBU}	Data rate, SBU/AUX paths	Differential or single ended signals			1	Gbps
$V_{IH-GPIO}$	Input high voltage on GPIO pins	A[1:0], MODE[1:0], CONF[2:0] pins	0.75 * V_{CC}			V
$V_{IL-GPIO}$	Input low voltage on GPIO pins	A[1:0], MODE[1:0], CONF[2:0] pins			0.4	V
V_{IH-I2C}	Input high voltage on I^2C pins	SDA, SCL pins; 3.3V I^2C mode	0.75 * V_{CC}			V
		SDA, SCL pins; 1.8V I^2C mode	1.3			V
V_{IL-I2C}	Input low voltage on I^2C pins	SDA, SCL pins; 3.3V I^2C mode			0.25 * V_{CC}	V
		SDA, SCL pins; 1.8V I^2C mode			0.5	V
$V_{IO\ -LS}$	I/O voltage on low speed pins	SBUx and AUX[+/-] pins	–0.45		V_{CC}	V
I_{HS-SW}	Current through high speed switch	Cx[p or n] to DPx/SSx[p or n]			12	mA
$V_{DIFF-HS}$	High-speed signal pins differential voltage		0		1.8	V_{pp}
VCM	High speed signal pins common mode voltage		0		1.8	V
T_A	Operating free-air/ambient temperature		–40		105	°C

(1) Actual data rates can be more or less depending on link budget, margin and performance of other link elements

5.4 Thermal Information

THERMAL METRIC(1)		TMUXHS4446 RET (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	33.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	°C/W

THERMAL METRIC(1)		TMUXHS4446 RET (WQFN) 40 PINS	UNIT
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Pin (VCC)						
I_{CC}	Device active current	0V ≤ V_{CM} ≤ 1.8V		380	530	µA
I_{STDN}	Device shutdown current	All switches open; CONF[2:0] = 000, I^2C mode		5	10	µA
		All switches open; CONF[2:0] = 000, GPIO Mode		0.5	2.5	µA
High Speed Pins ([SS/C]TXx[+/-], [SS/C]RXx[+/-], DPx[+/-])						
C_{ON}	Output ON capacitance to GND	f = 5GHz		0.3		pF
C_{OFF}	Output OFF capacitance to GND	CONF[2:1] = 00		0.3		pF
$I_{IH,HS,SEL}$	Input high current, selected high-speed pins	V_{IN} = 1.8V for selected port p and n pins			6	µA
$I_{IH,HS,NSEL}$	Input high current, non-selected high-speed pins	V_{IN} = 1.8V for non-selected port			110	µA
$I_{IL,HS}$	Input low current, high-speed pins	V_{IN} = 0V			1	µA
$I_{FS,HS}$	Failsafe leakage current for HS data pins	Data pins = 1.8V V_{CC} = 0V			10	µA
$R_{A,p2n}$	DC Impedance between C[Tx/Rx]x+ and C[Tx/Rx]x- pins			20		KΩ
SBU Pins (SBUx, AUX[+/-])						
$I_{IH,SBU}$	Input high current, SBU, AUX pins	V_{IN} = V_{CC} for selected port			0.16	µA
$I_{IL,SBU}$	Input low current, SBU, AUX pins	V_{IN} = 0V			0.1	µA
$I_{FS,SBU}$	Failsafe leakage current for SBU pins	SBU pins = 3.6V, VCC = 0V			10	µA
$C_{ON,SBU}$	Output ON capacitance to GND	f = 1MHz		6	8	pF
$C_{OFF,SBU}$	Output OFF capacitance to GND	f = 1MHz		6	8	pF
$R_{ON,SBU}$	Output ON resistance	0 ≤ V_{IN} ≤ 3.3V; I_O = –8mA		7		Ω
Control Pins (MODE[1:0], CONF[2:0], A[1:0], SDA, SCL)						
$I_{IH,CTRL}$	Input high current, control pins	V_{IN} = V_{CC}			1	µA
$I_{IL,CTRL}$	Input low current, control pins	V_{IN} = 0V			1	µA
C_{IN}	Input capacitance			20		pF

5.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BW_{HS}	–3dB bandwidth for high-speed paths - DP and USB	-3dB loss compared to DC frequency point at 10Mhz		9.5		GHz
I_L	Differential insertion loss, V_{CM-HS} = 0.6V	f = 10MHz		–0.9		dB
		f = 2.7GHz		–1.2		
		f = 4GHz		–1.4		
		f = 5GHz		–1.6		
R_L	Differential return loss V_{CM-HS} = 0.6V	f = 10MHz		–22		dB
		f = 2.7GHz		–20		dB
		f = 4GHz		–16		dB
		f = 5GHz		–18		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
O_{IRR}	Differential OFF isolation	f = 10MHz		–60		dB
		f = 2.7GHz		–26		
		f = 4GHz		–22		
		f = 5GHz		–21		
X_{TALK}	Differential crosstalk	f = 10MHz		–50		dB
		f = 2.7GHz for DP2-DP1 or CTX1-CTX2		–28		dB
		f = 2.7GHz for all other channel combinations		–40		dB
		f = 5.0GHz for DP2-DP1 or CTX1-CTX2		–22		dB
		f = 5.0GHz for all other channel combinations		–38		dB
BW_{SBU}	–3dB bandwidth for SBU pins	-3dB loss compared to DC frequency point at 10Mhz		1000		MHz

5.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
Device Switching Time						
$t_{SW\_POWER\_ON}$	Device power ON time			80		µs
$t_{SW\_POWER\_OFF}$	Device power OFF time			160		ns
High Speed Pins						
t_{PD}	Switch propagation delay	f = 1GHz		70		ps
$t_{SW\_CM\_SHIFT}$	Switching time to change from one switching mode to another	Biased from CTXx/ CRXx side with CMV difference <1.8V		1.2		us
t_{SW}	Switching time to change from one switching mode to another	Biased from CTXx/ CRXx side with CMV difference <100mV		120		ns
t_{SK_INTRA}	Intra-pair output skew between + and - pins for same channel	f = 1GHz		2.5		ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1GHz		16		ps
SBU Pins						
$t_{PD\text{-}SBU}$	Switch propagation delay			220		ps
$t_{SW\text{-}SBU}$	Switching time to change from one switching mode to another	Biased from SBUx side with VIN = 3.3V		450		ns
$t_{SK\text{-}SBU}$	Output skew between SBU1 and SBU2 pins	f = 1MHz		2.5		ps

5.8 I²C Timing Characteristics

For pins SDA, SCL and A[1:0] when the device is in I²C control mode (MODE0 = H)

PARAMETER			MIN	TYP	MAX	UNIT
f_{SCL}	Clock frequency on SCL pin				400	kHz
t_{CH}	Clock HIGH time on SCL pin		0.6			µs
t_{CL}	Clock LOW time on SCL pin		1.3			µs
t_{SETSTA}	Start or repeated start condition setup time		0.6			µs
t_{HSTA}	Start or repeated start condition hold time		0.6			µs
t_{SETDAT}	Data setup time		100			ns
t_{HDAT}	Data hold time		0		0.9	µs
t_r	Input rise time		20 + 0.1 C_b (1)		300	ns
t_f	Input fall time		20 + 0.1 C_b (1)		300	ns
t_{SETSTO}	Stop condition setup time		0.6			us
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns

For pins SDA, SCL and A[1:0] when the device is in I²C control mode (MODE0 = H)

PARAMETER			MIN	TYP	MAX	UNIT
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs

(1) C_b = total bus capacitance of one bus line in pF

5.9 Typical Characteristics

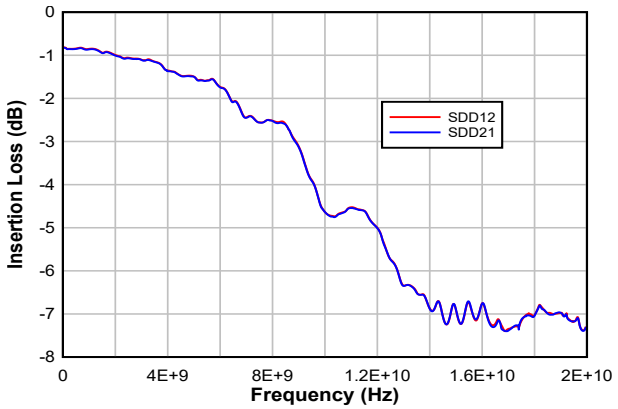

図 5-1. Insertion Loss for a Typical Channel at Nominal PVT

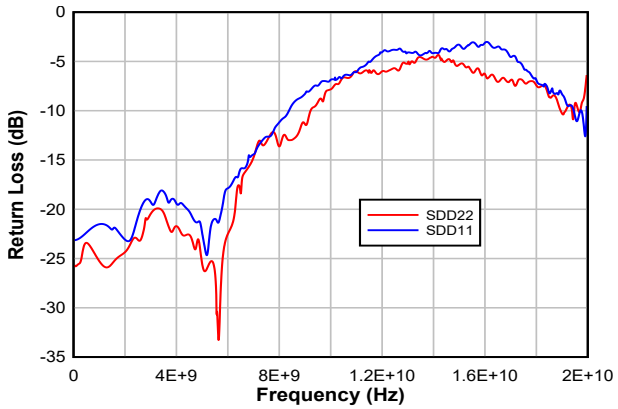

図 5-2. Return Loss for a Typical Channel at Nominal PVT

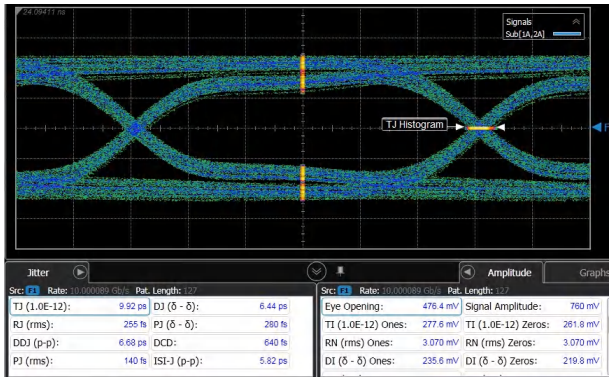

図 5-3. Eye Diagram at 10Gbps Through Baseline Setup (Cal-Trace, no DUT)

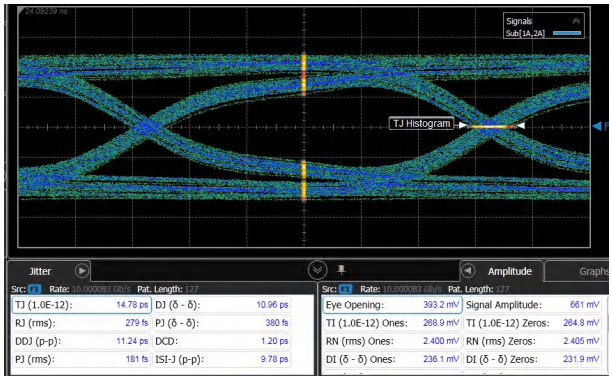

図 5-4. Eye Diagram at 10Gbps Through TMUXHS4446 (Cal-Trace + DUT)

6 Detailed Description

6.1 Overview

The TMUXHS4446 is a high-speed bidirectional passive crosspoint (Xbar) switch in mux or demux configurations. This device is used to switch between USB 3.2 Gen2 SuperSpeed and DisplayPort 1.4/2.1 (up to 10Gbps UHBR10) signals over a USB Type-C interface. The device also provides switching for the low-speed SBU signals typically used for DisplayPort auxiliary channels. The SBU pins are 6V tolerant to survive a short-to-VBUS event. The TMUXHS4446 supports differential signaling with common mode voltage range (CMV) from 0V to 1.8V and with differential amplitude from 0V to 1800mVpp. Adaptive CMV tracking enables the channel through the device to remain unchanged for the entire common-mode voltage range.

The dynamic characteristics of the TMUXHS4446 allows high-speed switching, minimum attenuation to the signal eye diagram, and with very little added jitter. The silicon design is optimized for excellent frequency response at higher frequency spectrum of the signals, and the silicon signal traces and switch network are matched for best intra-pair skew performance.

The TMUXHS4446 provides two forms of control modes: GPIO and I^2C. In the GPIO mode the control pins are set high or low. In the I^2C mode, an external I^2C controller (such as USB PD controller) sets the mux configurations and device control. The control configuration flexibility allows compatibility with a wide variety of USB PD controllers.

6.2 Functional Block Diagram

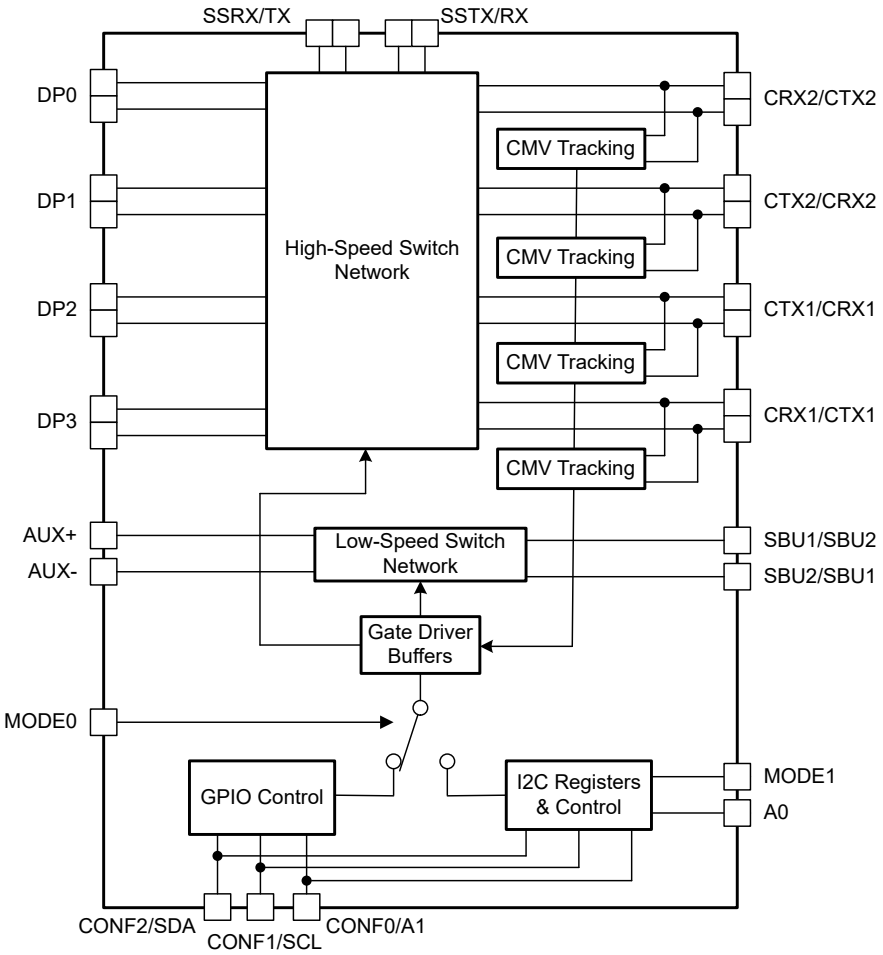

図 6-1. TMUXHS4446 Functional Block Diagram

6.3 Feature Description

6.3.1 High-Speed Differential Signal Switching

Based on the data sent to the control pins, TMUXHS4446 provides the following muxing options:

- USB SS only: connects only one group of TX & RX signals on the USB-C connector to a USB source/sink.
- USB SS only (flipped): enables the *USB SS only* mode when the USB-C connector is flipped around.
- 4 Ln DP: connects both groups of TX/RX signals on the USB-C connector to a DisplayPort source/sink.
- 4 Ln DP (flipped): enables the *4 Ln DP* mode when the USB-C connector is flipped around.
- 2 Ln DP + USB SS: connects one group of TX/RX signals to a DisplayPort source/sink and connects the other group to a USB source/sink.
- 2 Ln DP + USB SS (flipped): enables the *2 Ln DP + USB SS* mode when the USB-C connector is flipped around.
- Open (powered down): opens all switch and cuts of power to the device.
- Open (powered on): opens all switches but keeps power to the device.

6.3.2 Low-Speed SBU Signal Switching

The TMUXHS4446 provides switching for the low-speed sideband signals for DisplayPort that are transmitted over the SBU lines on the USB-C connector. These signals are connected to the AUX+ and AUX– pins. The switch is required to route the signals to the right locations if the USB-C connector is flipped. The SBU pins are 6V tolerant.

6.3.3 GPIO and I²C Control Modes

The TMUXHS4446 can toggle between GPIO and I²C control modes through the MODE0 pin being driven high or low. When set to GPIO mode (MODE0 = low), the CONF[2:0] pins are driven either high or low to set the switch configurations. When set to I²C mode (MODE0 = high), an external I²C controller (for example, a PD controller) writes into the TMUXHS4446 register bits through the SDA and SCL pins to set mux configurations and device control.

The MODE1 pin is used to control the logic level of the I²C data. If MODE1 is high, then the logic level is 3.3V and 1.8V if MODE1 is low.

6.4 Device Functional Modes

This section describes how to configure the TMUXHS4446 control pins to configure device modes and mux configurations.

表 6-1 shows how MODE0 and MODE1 pins are used to set device control configuration modes.

表 6-1. Control Mode Configuration

Control Mode	MODE0	MODE1
GPIO/Pin Control Mode	0	X
I²C (1.8V logic)	1	0
I²C (3.3V logic)	1	1

表 6-2 shows I2C Register sets. A1 and A0 (Byte 1, bits 2 and 1) are set by pins 35 and 14. CONF[2-0] (Byte 3, bits 2-0) sets the device configurations in I²C mode.

表 6-2. I²C Control

Byte # & Description	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte 1, I²C Secondary Target address	1	0	1	0	1	A1	A0	0/1 (W/R)
Byte 2, Device ID (read only)	0	0	0	0	0	0	0	0
Byte 3, Selection control (read/write)	0	0	0	0	0	CONF[2]	CONF[1]	CONF[0]

表 6-3 shows how CONF[2:0] pins in GPIO mode and registers Byte 3, bits 2-0 (CONF[2-0]) as shown in 表 6-2 sets mux configurations in source applications.

表 6-3. High-Speed and Low-Speed Channel Mapping for Source Applications

System-Side Channel	Connector-Side Channel Connected To System-Side Channel							
	Open (powered down)	Open (powered on)	USB-C USB 3.x		DP Alt Mode Receptacle DFP Pin Assignment (Source)			
			USB SS only	USB SS only Flip	C, E 4 Ln DP	C, E Flip 4 Ln DP	D 2 Ln DP + USB SS	D Flip 2 Ln DP + USB SS
	CONF[2:0] = 000	CONF[2:0] = 001	CONF[2:0] = 100	CONF[2:0] = 101	CONF[2:0] = 010	CONF[2:0] = 011	CONF[2:0] = 110	CONF[2:0] = 111
SSTX	X	X	CTX1	CTX2	X	X	CTX1	CTX2
SSRX	X	X	CRX1	CRX2	X	X	CRX1	CRX2
DP0	X	X	X	X	CRX2	CRX1	CRX2	CRX1
DP1	X	X	X	X	CTX2	CTX1	CTX2	CTX1
DP2	X	X	X	X	CTX1	CTX2	X	X
DP3	X	X	X	X	CRX1	CRX2	X	X
AUX+	X	X	X	X	SBU1	SBU2	SBU1	SBU2
AUX-	X	X	X	X	SBU2	SBU1	SBU2	SBU1

図 6-2 illustrates pictorial view of the TMUXHS4446 mux configurations for a source application based on 表 6-3. In this illustration all signals are differential with both positive and negative pins, but shown as single for brevity.

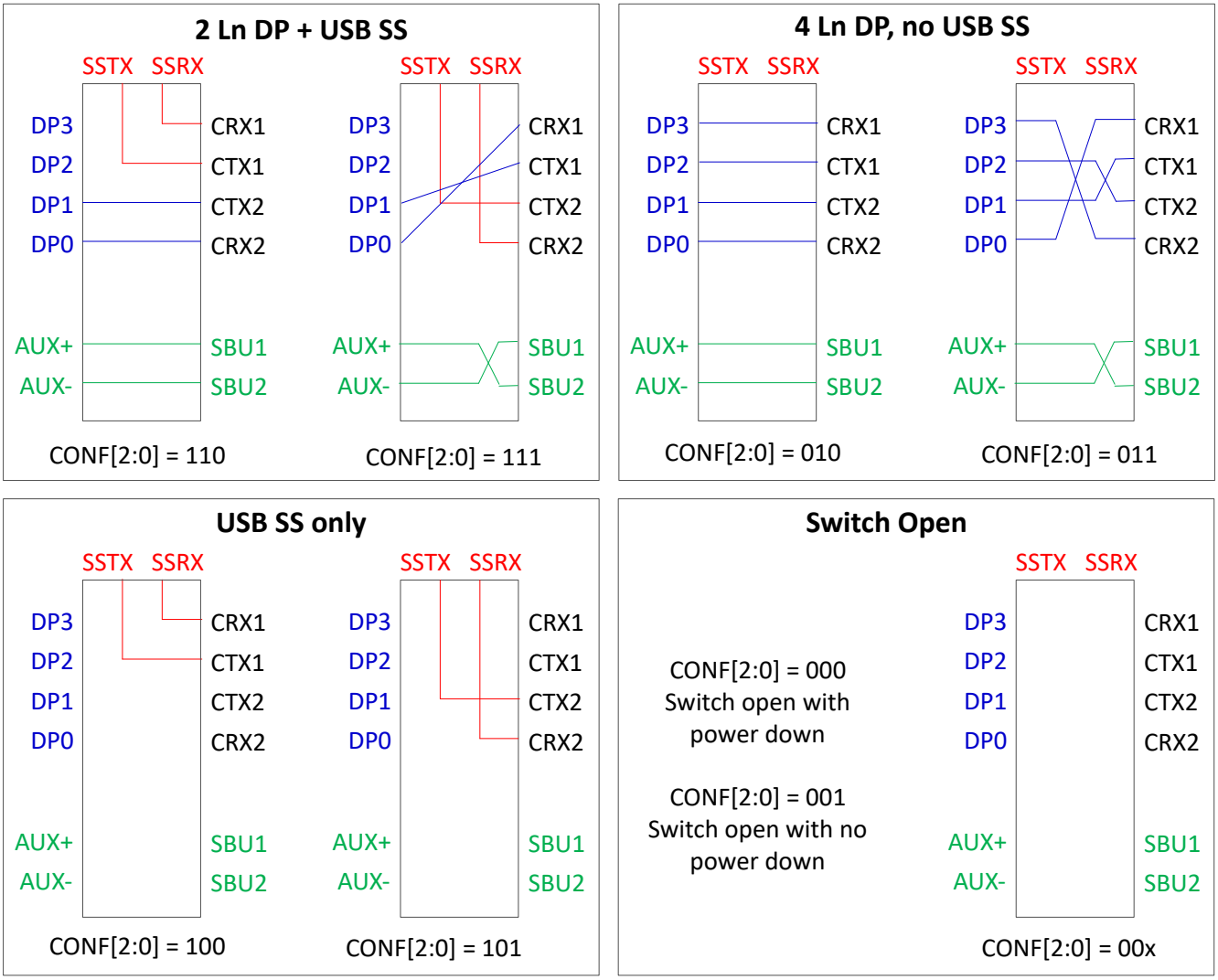

図 6-2. TMUXHS4446 Signal Flow Diagrams in Different Configurations for Source Applications

The sink side signal flow can also be constructed based on 表 6-4.

表 6-4. High-Speed and Low-Speed Channel Mapping for Sink Applications

System-Side Channel	Connector-Side Channel Connected To System-Side Channel							
	Open (powered down)	Open (powered on)	USB-C USB 3.x		DP Alt Mode Receptacle UFP Pin Assignment (Sink)			
			USB SS only	USB SS only Flip	C 4 Ln DP	C Flip 4 Ln DP	D 2 Ln DP + USB SS	D Flip 2 Ln DP + USB SS
	CONF[2:0] = 000	CONF[2:0] = 001	CONF[2:0] = 100	CONF[2:0] = 101	CONF[2:0] = 010	CONF[2:0] = 011	CONF[2:0] = 110	CONF[2:0] = 111
SSTX	X	X	CTX1	CTX2	X	X	CTX1	CTX2
SSRX	X	X	CRX1	CRX2	X	X	CRX1	CRX2
DP0	X	X	X	X	CTX2	CTX1	CTX2	CTX1
DP1	X	X	X	X	CRX2	CRX1	CRX2	CRX1
DP2	X	X	X	X	CRX1	CRX2	X	X
DP3	X	X	X	X	CTX1	CTX2	X	X
AUX+	X	X	X	X	SBU2	SBU1	SBU2	SBU1

表 6-4. High-Speed and Low-Speed Channel Mapping for Sink Applications (続き)

System-Side Channel	Connector-Side Channel Connected To System-Side Channel							
	Open (powered down)	Open (powered on)	USB-C USB 3.x		DP Alt Mode Receptacle UFP Pin Assignment (Sink)			
			USB SS only	USB SS only Flip	C 4 Ln DP	C Flip 4 Ln DP	D 2 Ln DP + USB SS	D Flip 2 Ln DP + USB SS
	CONF[2:0] = 000	CONF[2:0] = 001	CONF[2:0] = 100	CONF[2:0] = 101	CONF[2:0] = 010	CONF[2:0] = 011	CONF[2:0] = 110	CONF[2:0] = 111
AUX-	X	X	X	X	SBU1	SBU2	SBU1	SBU2

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TMUXHS4446 is an analog crosspoint or crossbar mux/demux or switch specially designed for USB Type-C or USB-C alternate mode applications. The device supports USB SS signaling up to 10Gbps and alternate mode signaling such as DisplayPort up to 10Gbps.

The crosspoint selection of the device is typically configured by a USB power delivery (PD) controller by an I^2C interface. The TMUXHS4446 is an analog mux which can be used in USB Type-C ecosystem with DP as alternate mode in two distinct application configurations: one is for DP Source/USB Host, the other one for the DP Sink/USB Device/Dock. 図 7-1 shows a typical application block diagrams for these two cases: left source and right sink.

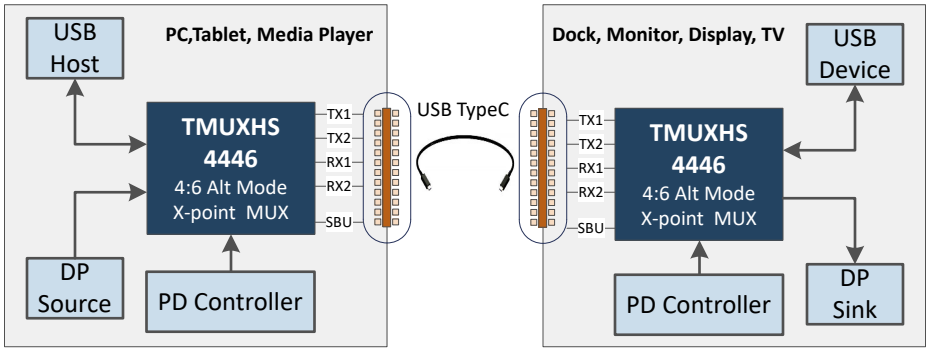

図 7-1. TMUXHS4446 in USB Type-C Source and Sink Applications

7.2 Typical Application: USB-C with DP Alternate Mode - Source

図 7-2 shows a simplified schematic diagram for a typical USB Type-C source application. Implementation for a sink use case is similar.

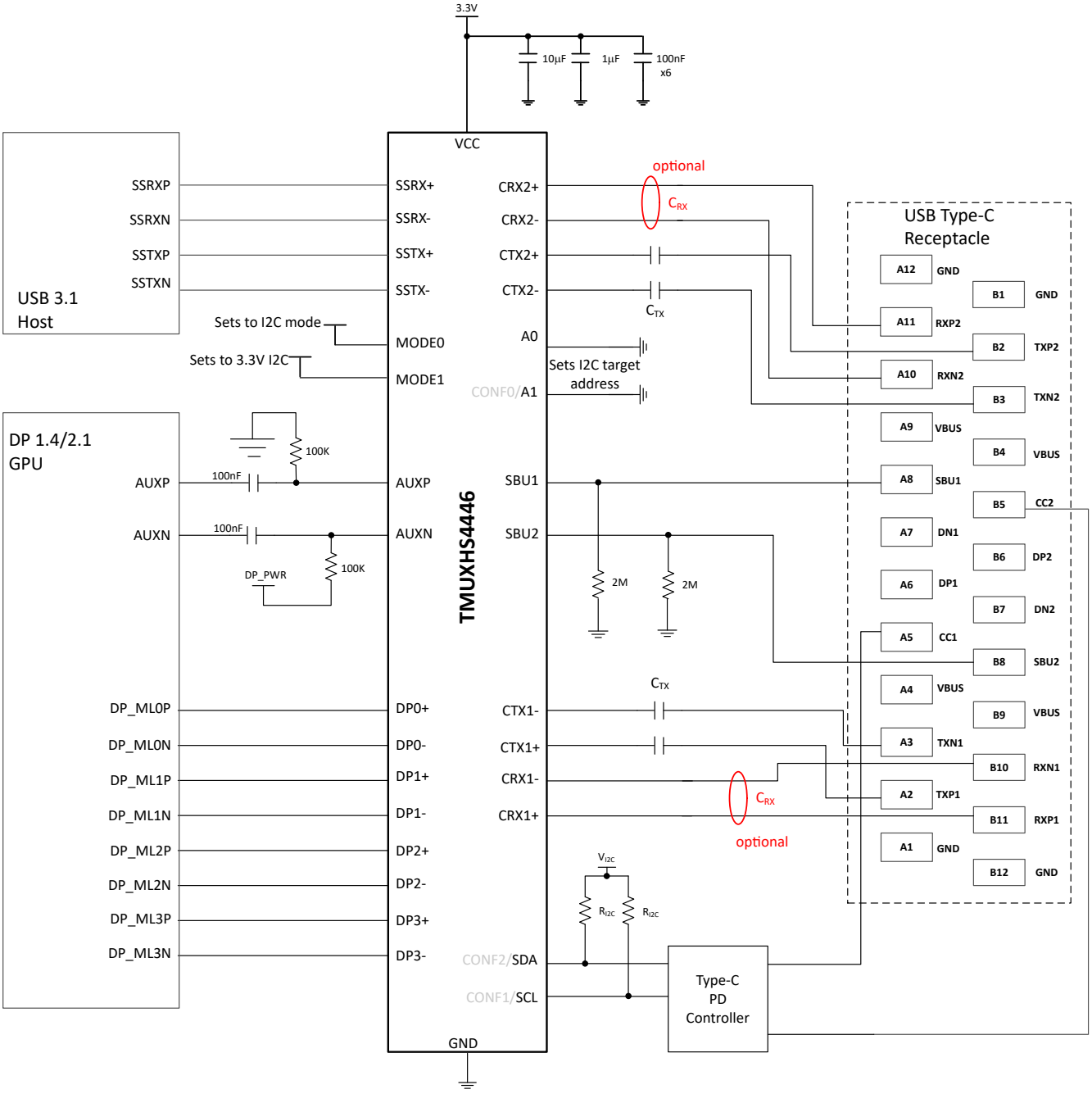

図 7-2. Application Schematic for TMUXHS446 in a Typical USB Type-C Source Use Case

7.2.1 Design Requirements

For this design example, use the parameters shown in 表 7-1.

表 7-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC}	3.3V
AC coupling capacitors for TX pins on USB-C connector side, C_{TX}	220nF
I^2C pullup resistor, R_{I2C}	2kΩ
I^2C pullup voltage, V_{I2C}	3.3V

表 7-1. Design Parameters (続き)

PARAMETER	VALUE
DP Auxiliary channel pullup voltage, DP_PWR	3.3V
DP Auxiliary channel coupling capacitor, C_{AUX}	100nF

7.2.2 Detailed Design Procedure

During implementation of a USB Type-C with DP alternate mode, the AC coupling capacitors must be placed carefully. 図 7-3 depicts the AC coupling capacitor placement for typical applications. Note TMUXHS4446 supports a Vcm range, not exceeding the typical range of 0 – 1.8V. Note the AC caps are used only on TX pins on both source and sink ends. However, if there is an application where such Vcm range is not assured, TI recommends to make changes on AC coupling capacitor placements. 図 7-4 illustrates such implementation. Additional optional AC coupling capacitors are used for RX pins. In detailed source schematic shown in 図 7-2 such capacitors are marked as C_{RX} and TI recommends them to be 0.5µF.

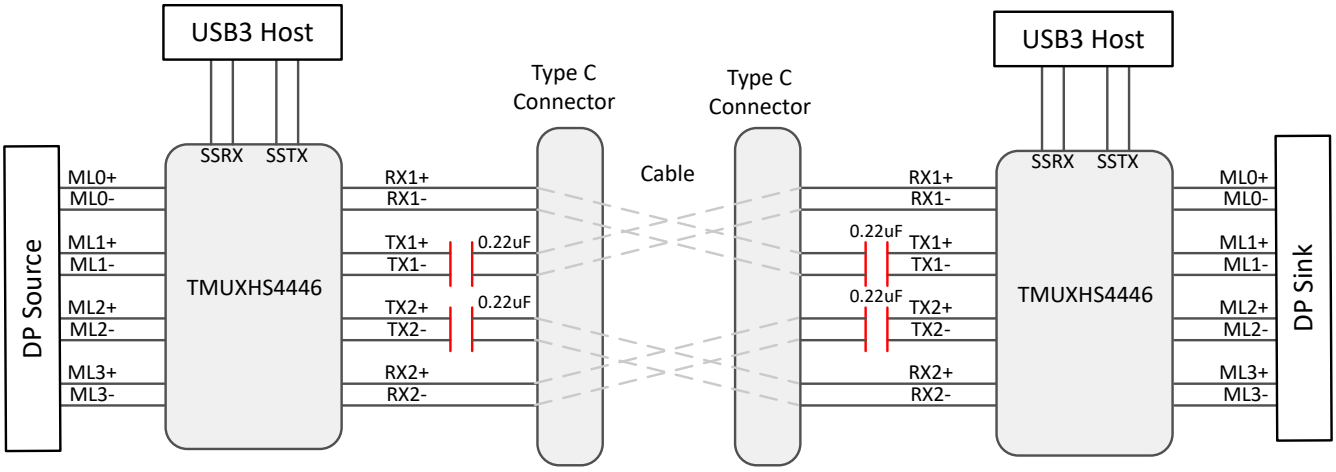

図 7-3. Typical Placement of AC Coupling Capacitors with Vcm ≤ 1.8V

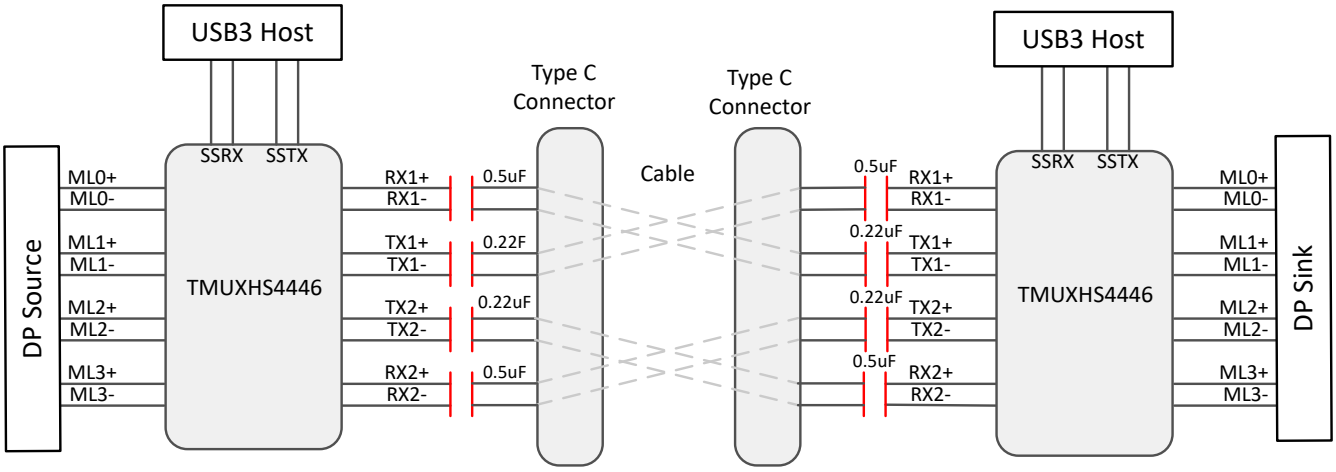

図 7-4. Placement of AC coupling Capacitors with Vcm > 1.8V

7.2.3 Application Curves

図 7-5 through 図 7-8 illustrate DisplayPort 1.4 Tx compliance results at HBR3 8.1Gbps. Eye diagrams (in scope, no cable model) are compared from the baseline setup and from the same setup plus TMUXHS4446 board. The

diagrams are for lane 0. Other lanes also result in to similar eye diagrams. Jitter degradation through TMUXHS4446 is minimal.

図 7-5. 8.1Gbps DP Compliance Setup - Baseline (no DUT)

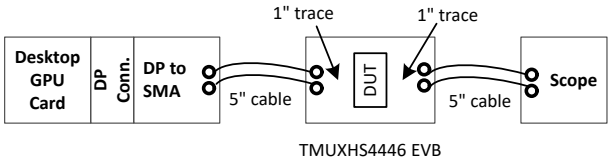

図 7-6. 8.1Gbps DP Compliance Setup - with TMUXHS4446

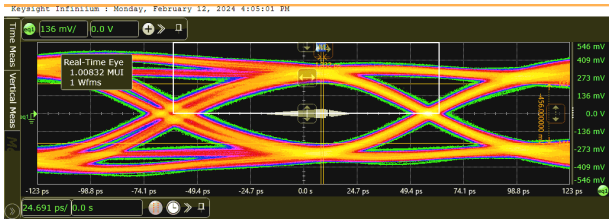

図 7-7. 8.1Gbps DP Compliance Eye Diagram - Baseline Setup (no DUT)

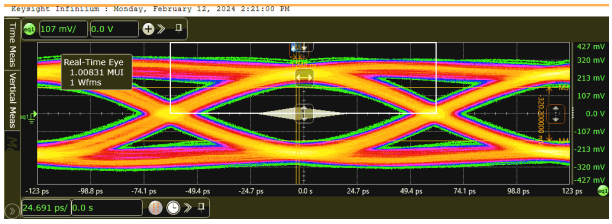

図 7-8. 8.1Gbps DP Compliance Eye Diagram - with TMUXHS4446

図 7-9 through 図 7-12 illustrate USB 3.x Gen2 Tx compliance results at 10Gbps. Eye diagrams (in scope, near end) are compared from the baseline setup and from the same setup plus TMUXHS4446 board. The diagrams are for lane 0. Other lanes also result in to similar eye diagrams. Jitter degradation through TMUXHS4446 is minimal.

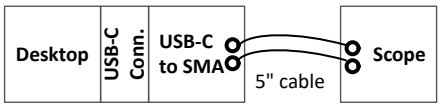

図 7-9. 10Gbps USB Compliance Setup - Baseline (no DUT)

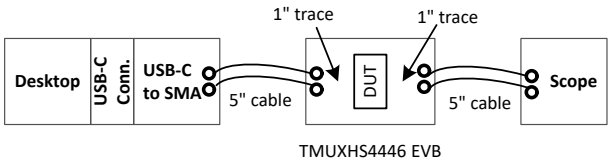

図 7-10. 10Gbps USB Compliance Setup - with TMUXHS4446

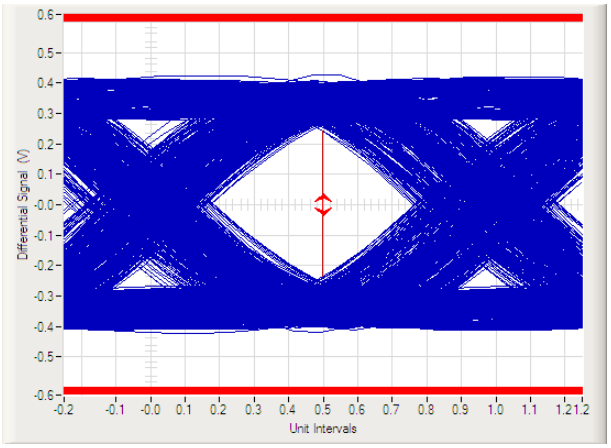

図 7-11. 10Gbps USB Compliance Eye Diagram - Baseline Setup (no DUT)

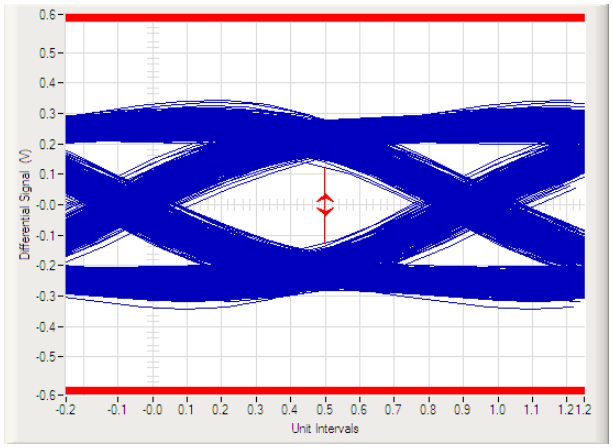

図 7-12. 10Gbps USB Compliance Eye Diagram - with TMUXHS4446

7.3 Power Supply Recommendations

The TMUXHS4446 does not require a power supply sequence. However, TI recommends that the device is powered on after device supply V_{CC} is stable and in specification. TI also recommends to place ample decoupling capacitors at the device VCC near the pins.

7.4 Layout

7.4.1 Layout Guidelines

On a high-K board, TI always recommends to solder the PowerPAD™ integrated circuit package onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the Power-pad package. On a high-K board, the TMUXHS4446 can operate over the full temperature range by soldering the Power-pad onto the thermal land without vias.

For high speed layout guidelines refer to the *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* application note.

On a low-K board, use a 1-oz Cu trace to connect the GND pins to the thermal land for the device to operate across the temperature range. A general PCB design guide for Power-pad packages is provided in the *Power-pad Thermally-Enhanced Package* application note.

7.4.2 Layout Example

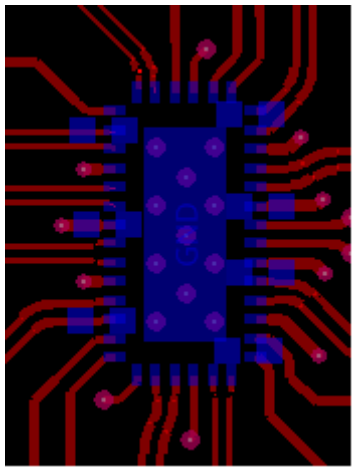

図 7-13. TMUXHS4446 Layout Example

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* application note
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application note

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUXHS4446IRETR	ACTIVE	WQFN	RET	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TMX4446	Samples
TMUXHS4446IRETT	ACTIVE	WQFN	RET	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TMX4446	Samples
TMUXHS4446RETR	ACTIVE	WQFN	RET	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TMX4446	Samples
TMUXHS4446RETT	ACTIVE	WQFN	RET	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TMX4446	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

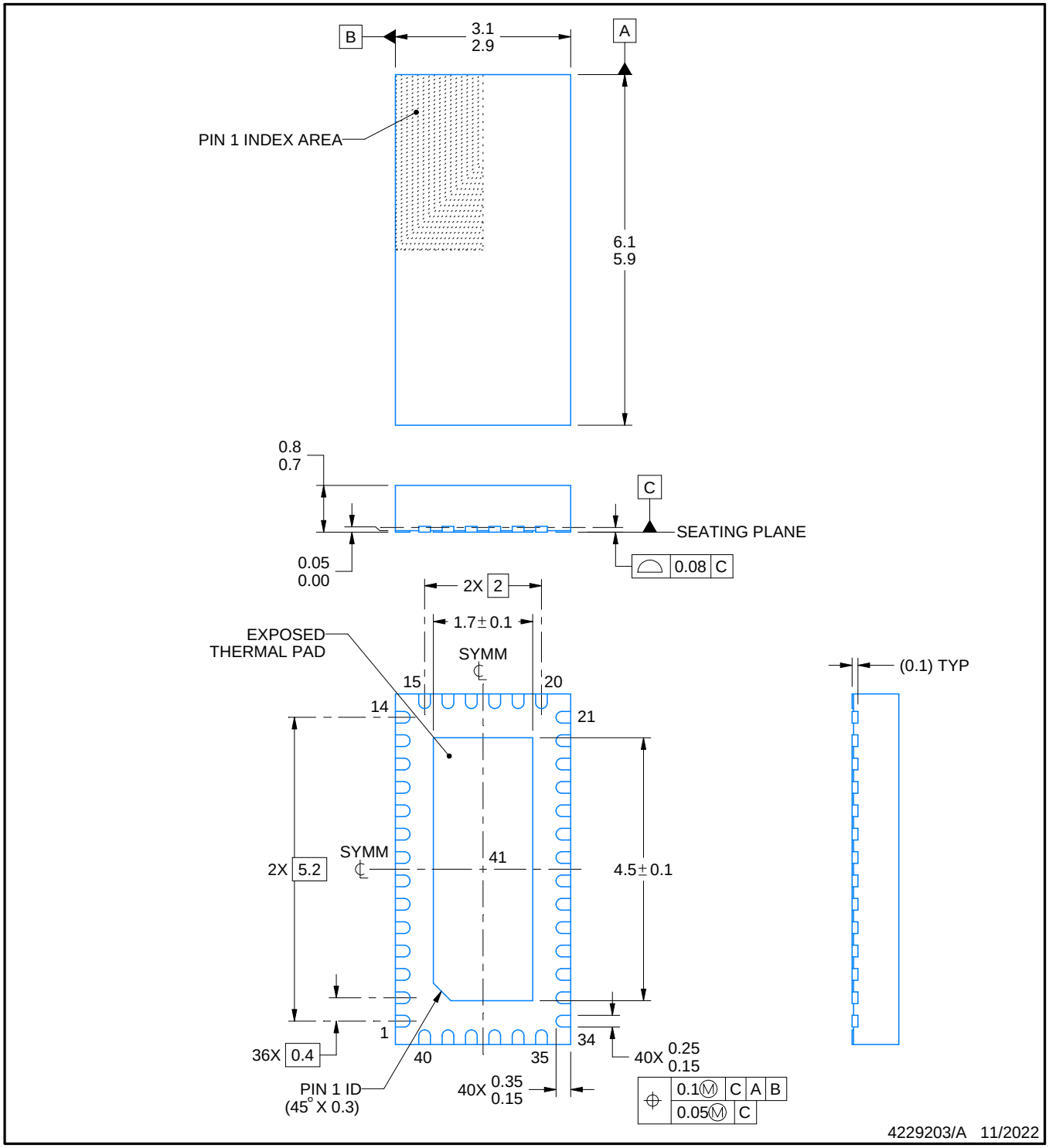
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RET0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

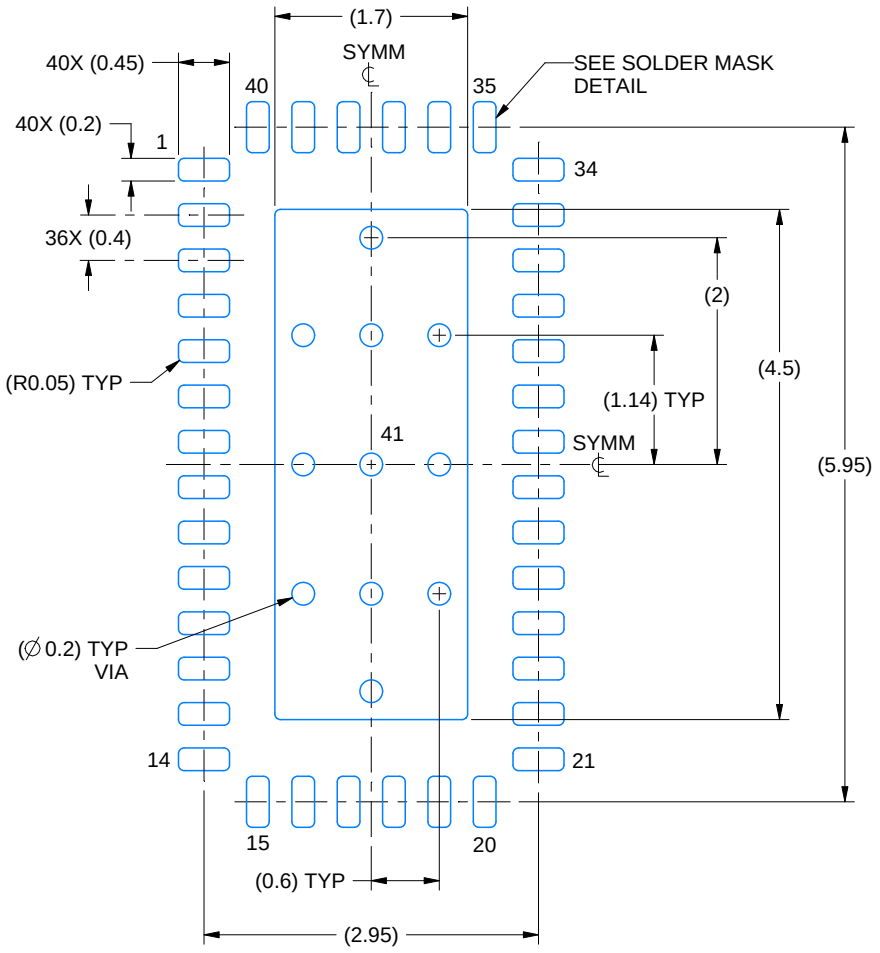
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

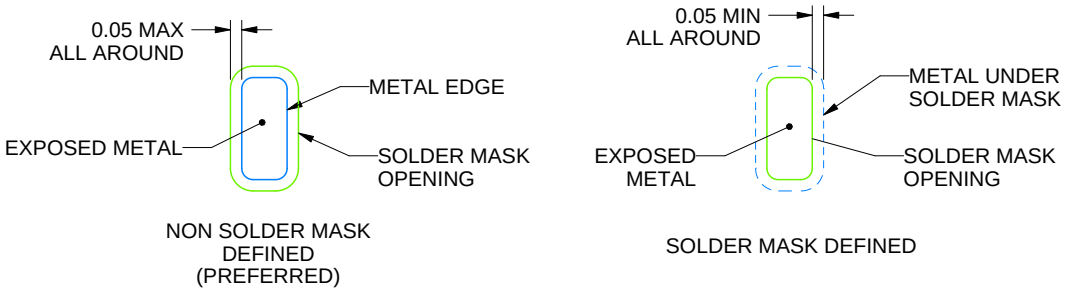
RET0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

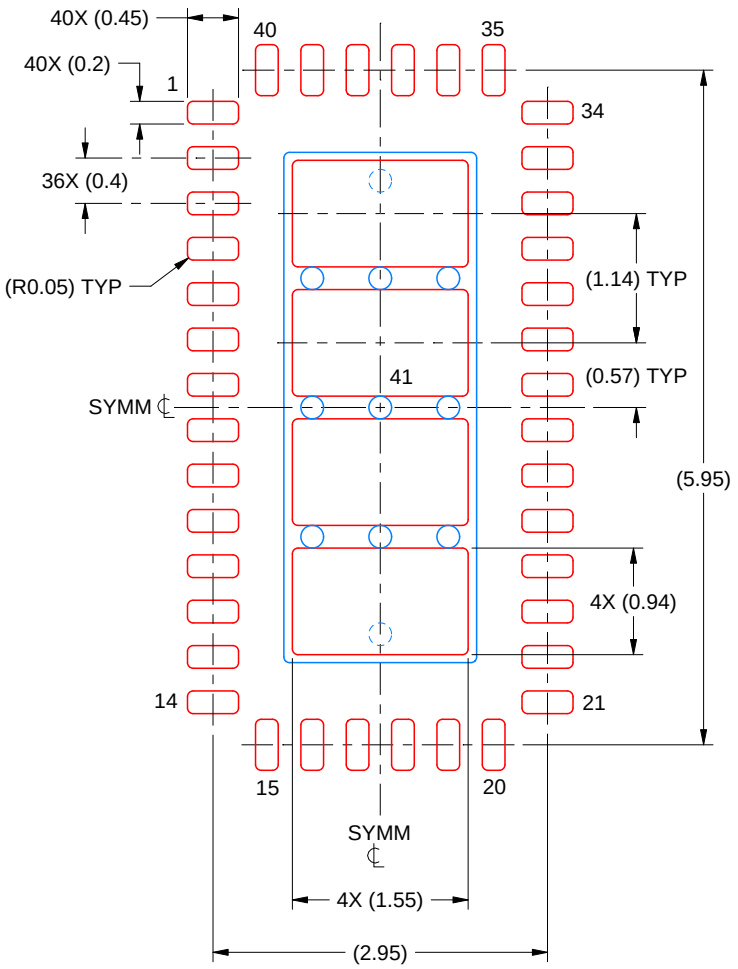


SOLDER MASK DETAILS

4229203/A 11/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229203/A 11/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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