TPS3840-Q1 $\overline{MR}$ およびプログラマブル遅延機能搭載、車載用、ナノ I_Q 電圧スーパーバイザ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度 -40°C～+125°C
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C7B
- 広い動作電圧範囲：1.5V～10V
  - 外付け抵抗を使用して Vin 範囲を拡大
- ナノアンペア単位の消費電流：標準値 350nA、最大値 700nA
- 固定スレッショルド電圧 (V_{IT-})
  - 1.6V から 4.9V まで 0.1V 刻みのスレッショルド
  - 高精度:標準値 1%、最大値 1.5%
  - ヒステリシス内蔵 (V_{IT+})
    - $1.6V < V_{IT-} \leq 3.0V$:100mV (標準値)
    - $3.1V \leq V_{IT-} < 4.9V$:200mV (標準値)
- スタートアップ遅延 (t_{STRT})：350µs (最大値)
- コンデンサでプログラム可能なリセット遅延時間
  - t_D:50µs (コンデンサなし) から 6.2s (10µF) まで
- アクティブ LOW のマニュアル・リセット ($\overline{MR}$)
- 3 つの出力トポロジ
  - TPS3840DL-Q1:オープン・ドレイン、アクティブ LOW ($\overline{RESET}$)
  - TPS3840PL-Q1:プッシュプル、アクティブ LOW ($\overline{RESET}$)
  - TPS3840PH-Q1:プッシュプル、アクティブ HIGH (RESET)
- パッケージ：5 ピン SOT-23 (DBV)

2 アプリケーション

- 車載用ヘッド・ユニットおよびクラスタ
- 車載用ディスプレイ、統合型コックピットおよびドライバー監視
- テレマティクス制御ユニット、緊急通話

3 概要

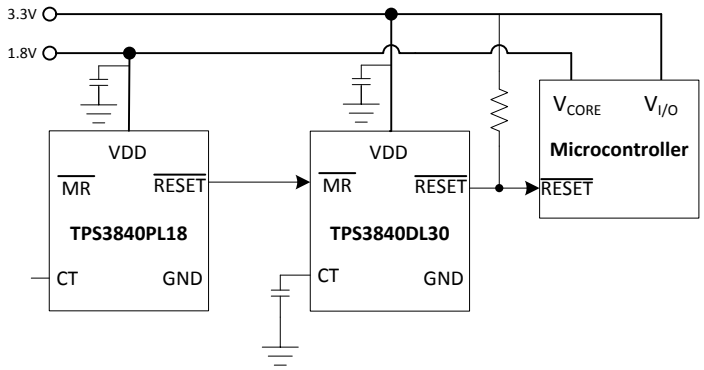
TPS3840-Q1 ファミリの電圧スーパーバイザまたはリセット IC は、V_{DD} と温度範囲の全体にわたって非常に小さな静止電流を維持しながら、高い電圧レベルで動作できます。TPS3840-Q1 は低消費電力、高精度、短い伝搬遅延時間 (t_{p_HL}= 30µs、標準値) の最良の組み合わせを実現しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS3840-Q1	SOT-23 (5) (DBV)	2.90mm×1.60mm

(1) パッケージの詳細については、このデータシートの末尾の外形図を参照してください。

代表的なアプリケーション回路



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年4月発行のものから更新 **Page**

- 事前情報を量産データのリリースに ... 1

5 概要（続き）

リセット出力信号は、VDD の電圧が負の電圧スレッショルド (V_{IT-}) を下回ったとき、またはマニュアル・リセットが LOW に設定されたとき ($V_{\overline{MR}\_L}$) にアサートされます。リセット信号は、V_{DD} が V_{IT-} にヒステリシスを加えた値 (V_{IT+}) を上回ったとき、またはマニュアル・リセット ($\overline{MR}$) がフローティングまたは $V_{\overline{MR}\_H}$ を上回った状態でリセット遅延時間 (t_D) が経過したとき、クリアされます。CT ピンとグランドの間にコンデンサを接続することで、リセット遅延時間をプログラムできます。高速にリセットする場合、CT ピンをフローティングのままにできます。

追加機能：低いパワー・オン・リセット電圧 (V_{POR})、$\overline{MR}$ および VDD のグリッチ耐性保護機能の内蔵、ヒステリシスの内蔵、小さいオープン・ドレイン出力リーク電流 ($I_{LKG(OD)}$)。TPS3840-Q1 は、車載用アプリケーションやバッテリ駆動/低消費電力アプリケーション用の電圧監視ソリューションに理想的です。

6 Device Comparison Table

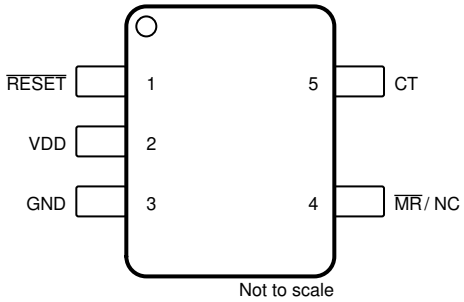
Device Comparison Table shows the variants planned to release at RTM, however other voltages from 表 3 at the end of datasheet can be sample upon request, please contact TI sales representative for details.

PART NUMBER	OUTPUT TOPOLOGY	THRESHOLD (V_{it-}) (V)	HYSTERESIS (mV)
TPS3840DL16DBVRQ1 (1)	Open-Drain, Active-Low	1.6	100
TPS3840DL25DBVRQ1 (1)	Open-Drain, Active-Low	2.5	100
TPS3840DL28DBVRQ1 (1)	Open-Drain, Active-Low	2.8	100
TPS3840DL29DBVRQ1 (1)	Open-Drain, Active-Low	2.9	100
TPS3840DL30DBVRQ1 (1)	Open-Drain, Active-Low	3.0	100
TPS3840DL31DBVRQ1 (1)	Open-Drain, Active-Low	3.1	200
TPS3840DL41DBVRQ1 (1)	Open-Drain, Active-Low	4.1	200
TPS3840DL42DBVRQ1 (1)	Open-Drain, Active-Low	4.2	200
TPS3840DL44DBVRQ1 (1)	Open-Drain, Active-Low	4.4	200
TPS3840DL45DBVRQ1 (1)	Open-Drain, Active-Low	4.5	200
TPS3840PL25DBVRQ1 (2)	Push-Pull, Active-Low	2.5	100
TPS3840PH27DBVRQ1 (3)	Push-Pull, Active-High	2.7	100
TPS3840PH30DBVRQ1 (3)	Push-Pull, Active-High	3.0	100

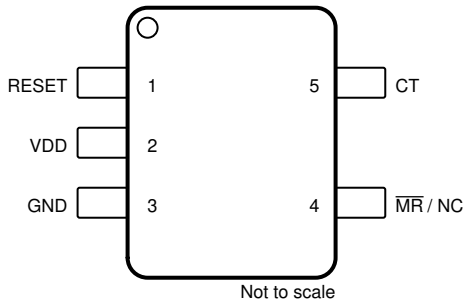
(1) TPS3840DL-Q1: Open-Drain, Active-Low ($\overline{\text{RESET}}$)
(2) TPS3840PL-Q1: Push-Pull, Active-Low ($\overline{\text{RESET}}$)
(3) TPS3840PH-Q1: Push-Pull, Active-High (RESET)

7 Pin Configuration and Functions

DBV Package
5-Pin
TPS3840PL-Q1, TPS3840DL-Q1 Top View



DBV Package
5-Pin
TPS3840PH-Q1 Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS3840PL-Q1, TPS3840DL-Q1	TPS3840PH-Q1		
RESET	N/A	1	O	**Active-High Output Reset Signal:** This pin is driven high when either the $\overline{MR}$ pin is driven to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after both $\overline{MR}$ is floating or above $V_{\overline{MR}\_L}$ and VDD voltage rise above V_{IT+}.
$\overline{RESET}$	1	N/A	O	**Active-Low Output Reset Signal:** This pin is driven logic when either the $\overline{MR}$ pin is driven to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{RESET}$ remains low (asserted) for the delay time period (t_D) after both $\overline{MR}$ is floating or above $V_{\overline{MR}\_L}$ and VDD voltage rise above V_{IT+}.
VDD	2	2	I	**Input Supply Voltage.** TPS3840-Q1 monitors VDD voltage
GND	3	3	_	**Ground**
$\overline{MR}$ / NC	4	4	I	**Manual Reset**. Pull this pin to a logic low ($V_{\overline{MR}\_L}$) to assert a reset signal in the output pin. After the $\overline{MR}$ pin is left floating or pull to V_{MR_H} the output goes to the nominal state after the reset delay time(t_D) expires. **$\overline{MR}$ can be left floating when not in use. NC stands for "No Connection" or floating.**
CT	5	5	-	**Capacitor Time Delay Pin**. The CT pin offers a user-programmable delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	12	V
	$\overline{\text{RESET}}$ (TPS3840PL)	–0.3	V_{DD} + 0.3	
	RESET (TPS3840PH)	–0.3	V_{DD} + 0.3	
	$\overline{\text{RESET}}$ (TPS3840DL)	–0.3	12	
	$\overline{\text{MR}}$(2)	–0.3	12	
	CT	–0.3	5.5	
Current	$\overline{\text{RESET}}$ pin and RESET pin		±70	mA
Temperature(3)	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If the logic signal driving MR is less than V_{DD}, then additional current flows into V_{DD} and out of MR. V_{MR} should not be higher than V_{DD}.
(3) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	1.5		10	V
$V_{\overline{\text{RESET}}}$, V_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin voltage	0		10	V
$I_{\overline{\text{RESET}}}$, I_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin current	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C
$V_{\overline{\text{MR}}}$(1)	Manual reset pin voltage	0		V_{DD}	V

(1) If the logic signal driving MR is less than V_{DD}, then additional current flows into V_{DD} and out of MR. V_{MR} should not be higher than V_{DD}.

8.4 Thermal Information

THERMAL METRIC(1)		TPS3840 DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

At 1.5 V ≤ V_{DD} ≤ 10 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage		1.5		10	V
V_{IT-}	Negative-going input threshold accuracy(1)	-40°C to 125°C	–1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 3.1 V to 4.9 V	175	200	225	mV
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 1.6 V to 3.0 V	75	100	125	mV
I_{DD}	Supply current into VDD pin	VDD = 1.5 V < V_{DD} < 10 V VDD > V_{IT+}(2) T_A = -40°C to 125°C		300	700	nA
$V_{\overline{MR}\_L}$	Manual reset logic low input(3)				600	mV
$V_{\overline{MR}\_H}$	Manual reset logic high input(3)		0.7V_{DD}			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
R_{CT}	CT pin internal resistance		350	500	650	kΩ
TPS3840PL (Push-Pull Active-Low)						
V_{POR}	Power on Reset Voltage(4)	$V_{OL(max)}$ = 200 mV $I_{OUT(Sink)}$ = 200 nA			300	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
V_{OH}	High level output voltage	1.5 V < V_{DD} < 5 V V_{DD} > V_{IT+}(2) $I_{OUT(Source)}$) = 2 mA	0.8V_{DD}			V
		5 V < V_{DD} < 10 V V_{DD} > V_{IT+}(2) $I_{OUT(Source)}$ = 5 mA	0.8V_{DD}			V
TPS3840PH (Push-Pull Active-High)						
V_{POR}	Power on Reset Voltage(4)	V_{OH}, $I_{OUT(Source)}$ = 500 nA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} > V_{IT+}(2) $I_{OUT(Sink)}$ = 2 mA			200	mV
		1.5 V < V_{DD} < 5 V V_{DD} > V_{IT+}(2) $I_{OUT(Sink)}$ = 5 mA			200	mV
V_{OH}	High level output voltage	1.5 V < V_{DD} < 5 V, V_{DD} < V_{IT-}, $I_{OUT(Source)}$ = 2 mA	0.8V_{DD}			V
TPS3840DL(Open-Drain)						
V_{POR}	Power on Reset Voltage(4)	$V_{OL(max)}$ = 0.2 V $I_{OUT\ (Sink)}$ = 5.6 uA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	$\overline{RESET}$ pin in High Impedance, V_{DD} = V_{RESET} = 5.5 V V_{IT+} < V_{DD}			90	nA

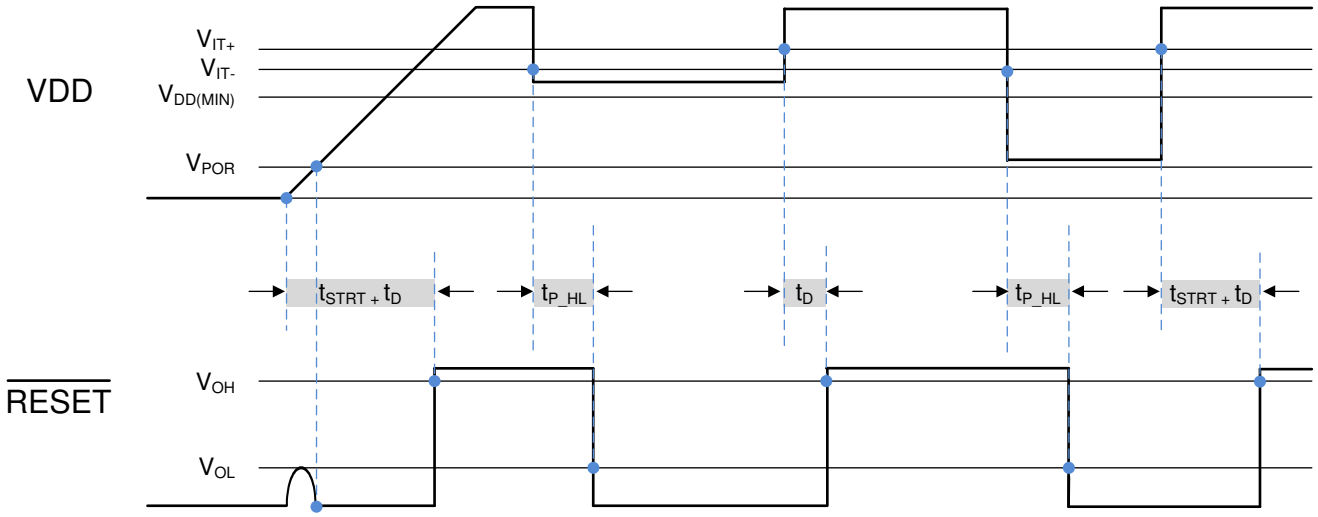
(1) V_{IT-} threshold voltage range from 1.6 V to 4.9 V in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) V_{IT+} = V_{HYS} + V_{IT-}
(3) If the logic signal driving $\overline{MR}$ is less than VDD, then additional current flows into VDD and out of $\overline{MR}$
(4) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate ≤ 100mV/µs

8.6 Timing Requirements

At 1.5 V ≤ V_{DD} ≤ 10 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, VDD slew rate < 100mV / us, unless otherwise noted. Typical values are at T_J = 25°C.

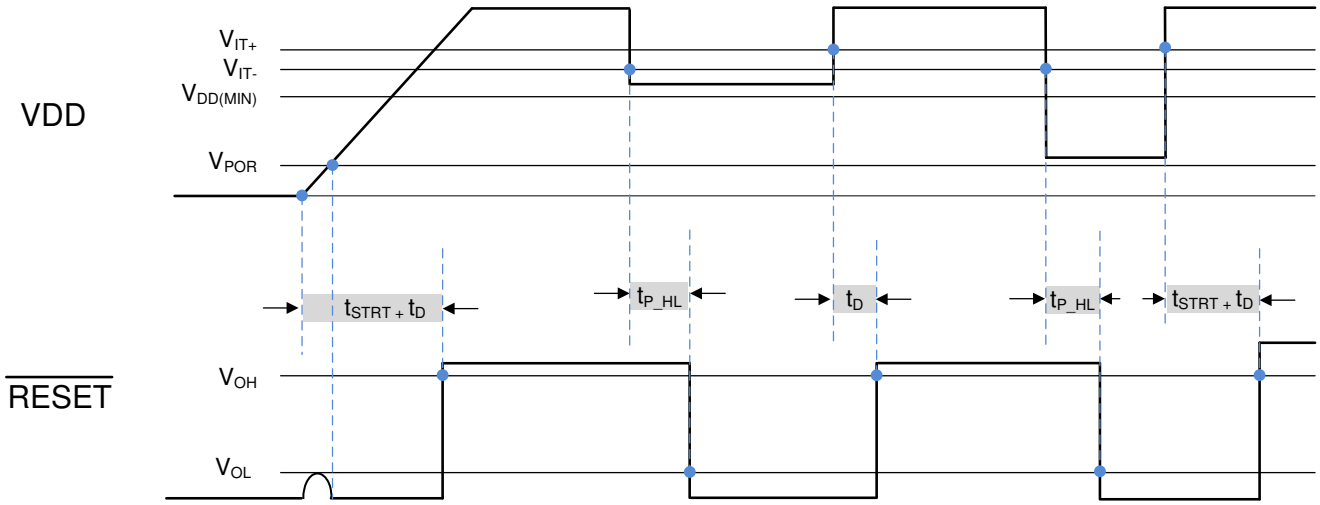
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay(1)	CT pin open	100	220	350	µs
t_{P_HL}	Propagation detect delay for VDD falling below V_{IT-}	V_{DD} = V_{IT+} to (V_{IT-}) - 10%(2)		15	30	µs
t_D	Reset time delay	CT pin = open			50	µs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 µF		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(3)		10		µs
t_{MR_PW}	$\overline{MR}$ pin pulse duration to initiate reset			300		ns
t_{MR_RES}	Propagation delay from $\overline{MR}$ low to reset	V_{DD} = 4.5 V, $\overline{MR}$ < $V_{\overline{MR}\_L}$		700		ns
t_{MR_tD}	Delay from release $\overline{MR}$ to deasert reset	V_{DD} = 4.5 V, $\overline{MR}$ = $V_{\overline{MR}\_L}$ to $V_{\overline{MR}\_H}$		t_D		ms

(1) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT+}, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add t_D delay to t_{STRT} time
(2) t_{P_HL} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Overdrive % = [(V_{DD}/ V_{IT-}) - 1] × 100%



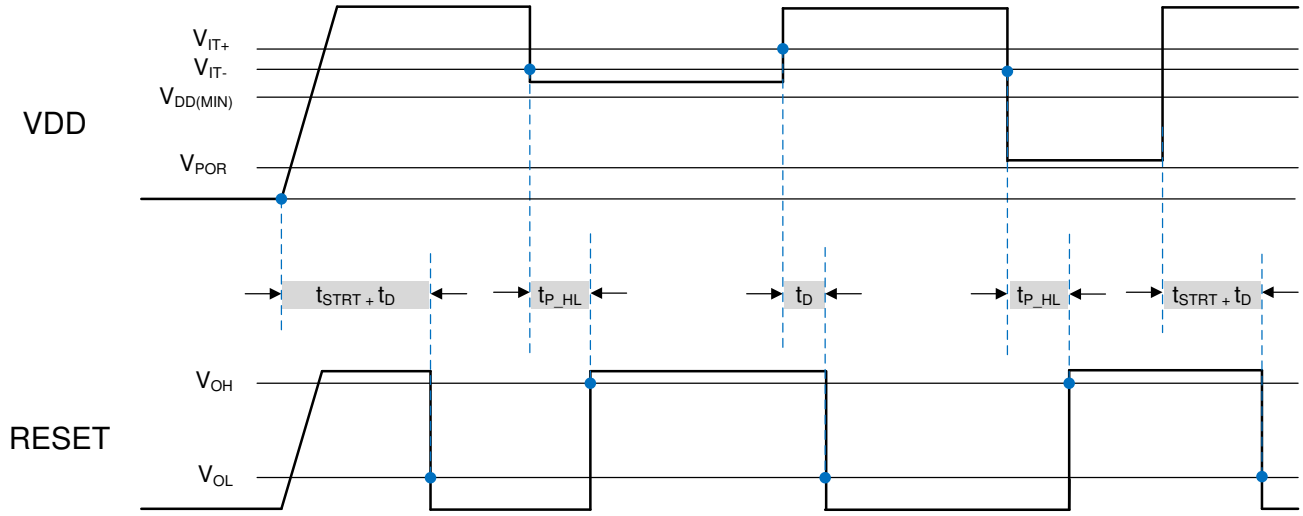
(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / µs.
(2) Open-Drain timing diagram assumes pull-up resistor is connected to $\overline{RESET}$

図 3. Timing Diagram TPS3840DL-Q1 (Open-Drain Active-Low)



(3) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time will be added to the startup time. VDD slew rate = 100 mV / µs.

図 4. Timing Diagram TPS3840PL-Q1 (Push-Pull Active-Low)



(4) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time will be added to the total startup time. VDD slew rate = 100 mV / µs.

図 5. Timing Diagram TPS3840PH-Q1 (Push-Pull Active-High)

8.7 Typical Characteristics

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

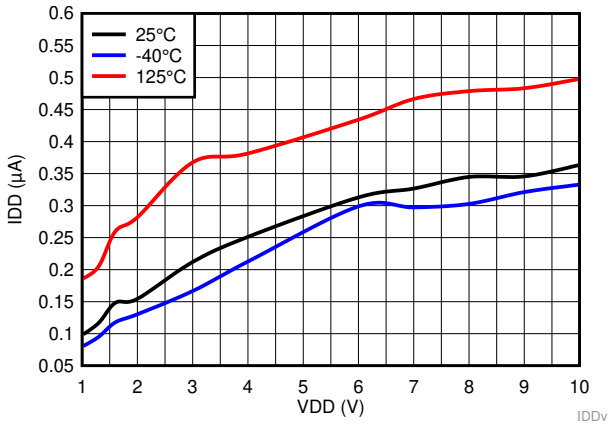


図 6. Supply Current vs Supply Voltage for TPS3840DL49-Q1

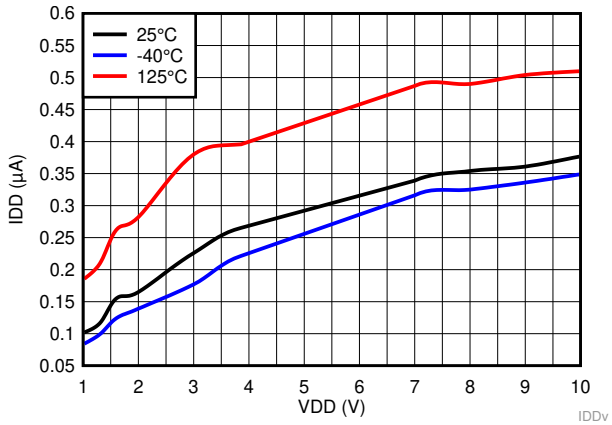


図 7. Supply Current vs Supply Voltage for TPS3840PL49-Q1

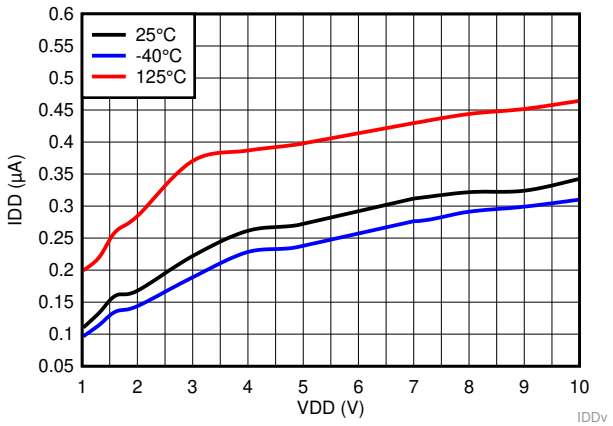


図 8. Supply Current vs Supply Voltage for TPS3840PH49-Q1

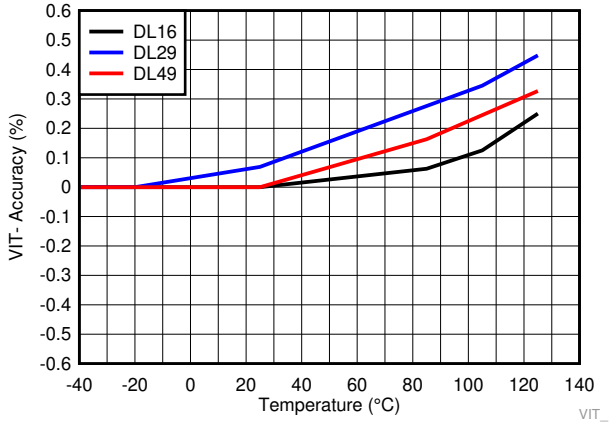


図 9. Negative-going Input Threshold Accuracy over Temperature for TPS3840DL-Q1

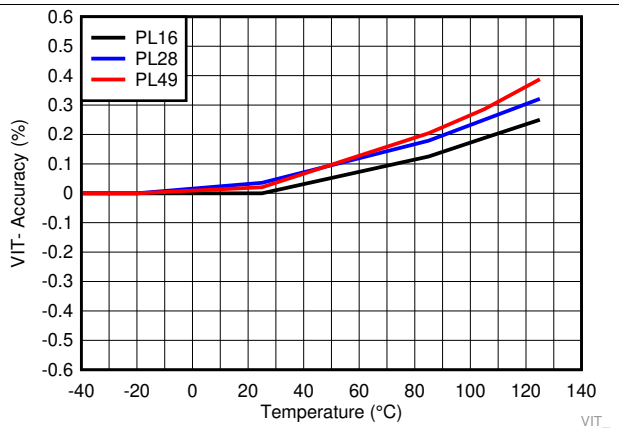


図 10. Negative-going Input Threshold Accuracy over Temperature for TPS3840PL-Q1

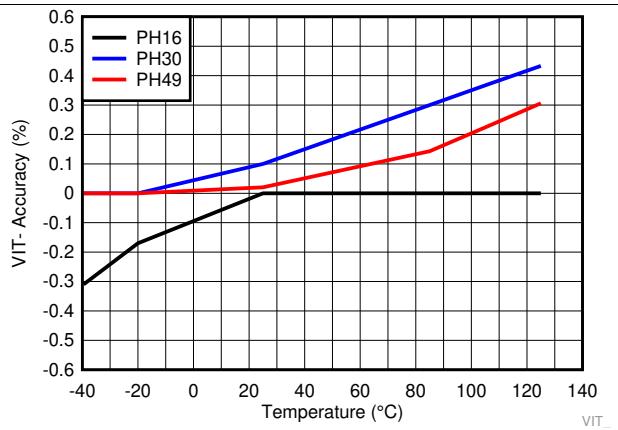


図 11. Negative-going Input Threshold Accuracy over Temperature for TPS3840PH-Q1

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

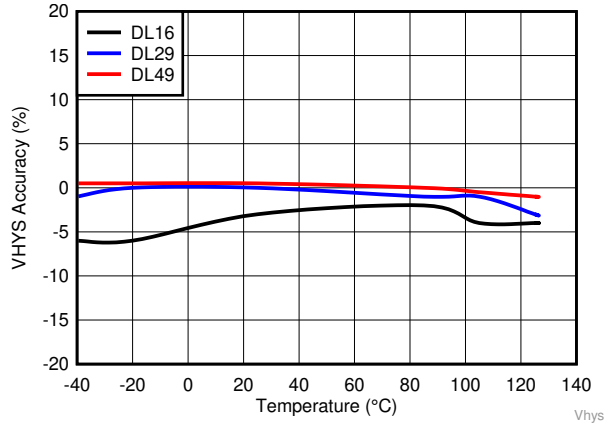


図 12. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840DL-Q1

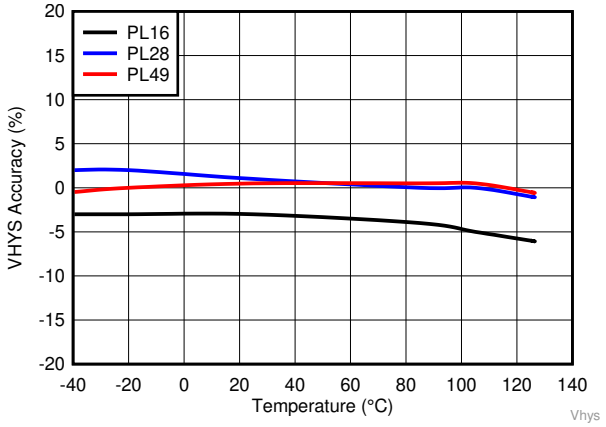


図 13. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840PL-Q1

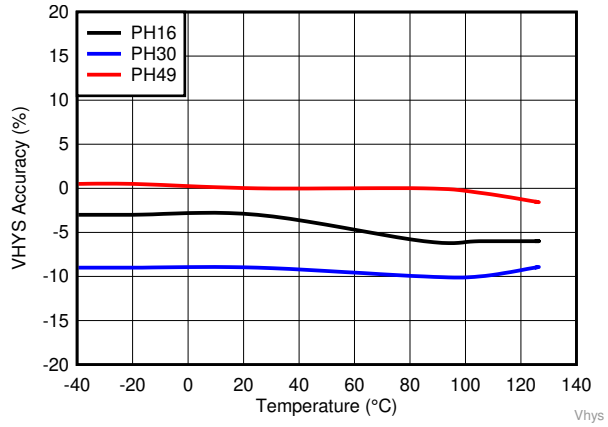


図 14. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840PH-Q1

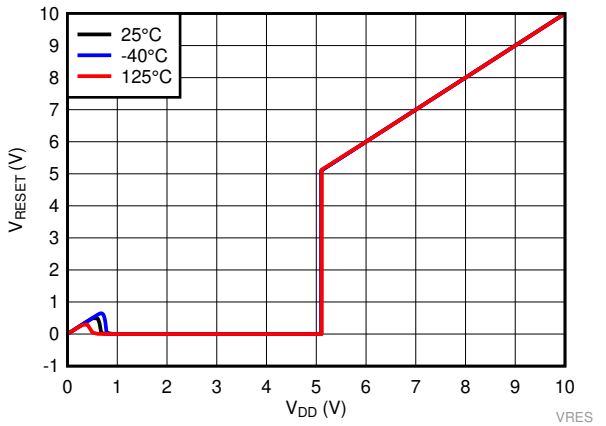


図 15. Output Voltage vs Input Voltage for TPS3840DL49-Q1

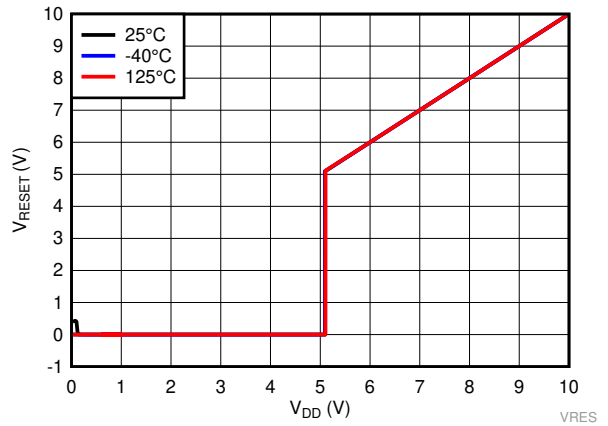


図 16. Output Voltage vs Input Voltage for TPS3840PL49-Q1

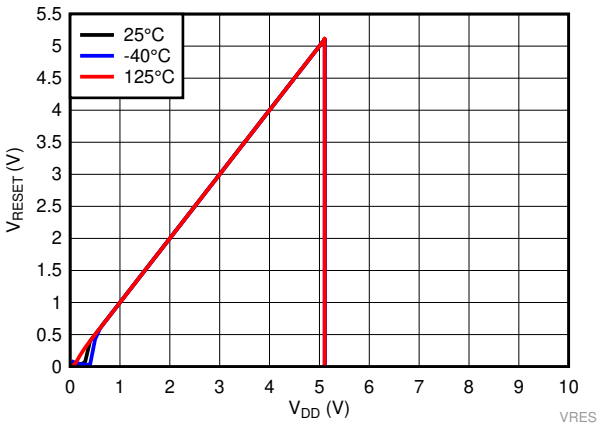


図 17. Output Voltage vs Input Voltage for TPS3840PH49-Q1

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

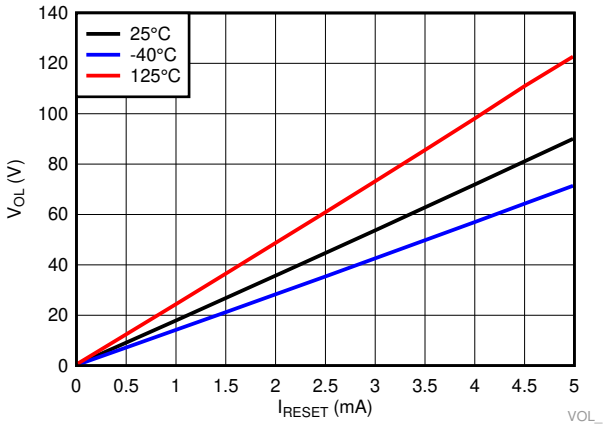


図 18. Low Level Output Voltage vs I_{RESET} for TPS3840DL49-Q1

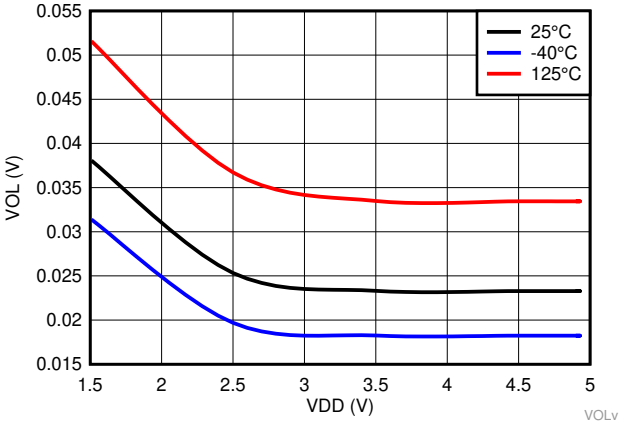


図 19. Low Level Output Voltage vs V_{DD} for TPS3840DL49-Q1

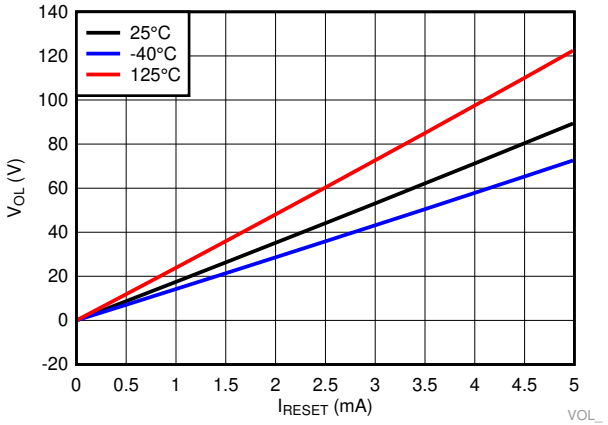


図 20. Low Level Output Voltage vs I_{RESET} for TPS3840PL49-Q1

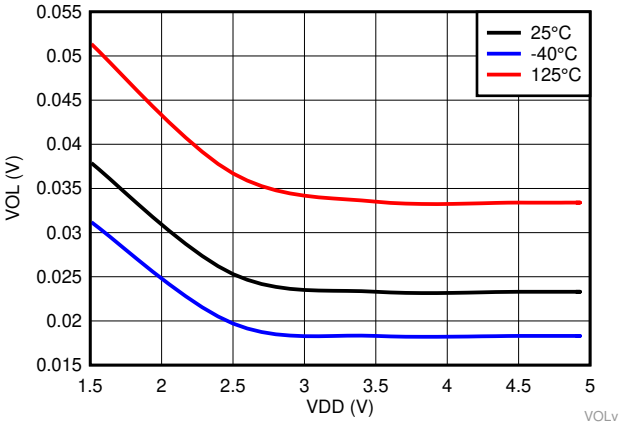


図 21. Low Level Output Voltage vs VDD for TPS3840PL49-Q1

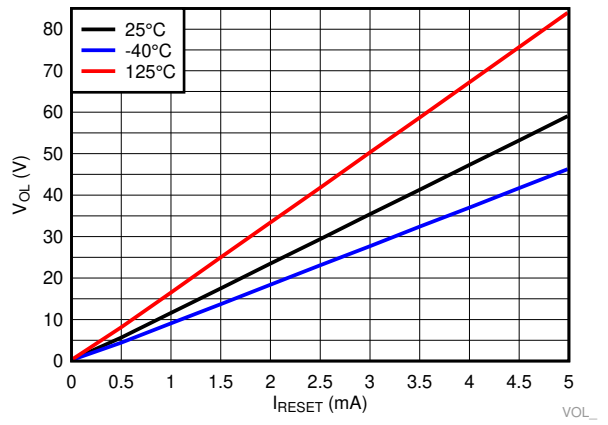


図 22. Low Level Output Voltage vs I_{RESET} for TPS3840PH49-Q1

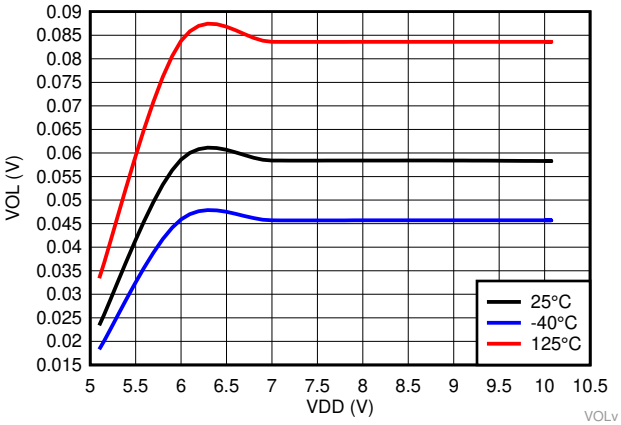


図 23. Low Level Output Voltage vs VDD for TPS3840PH49-Q1

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

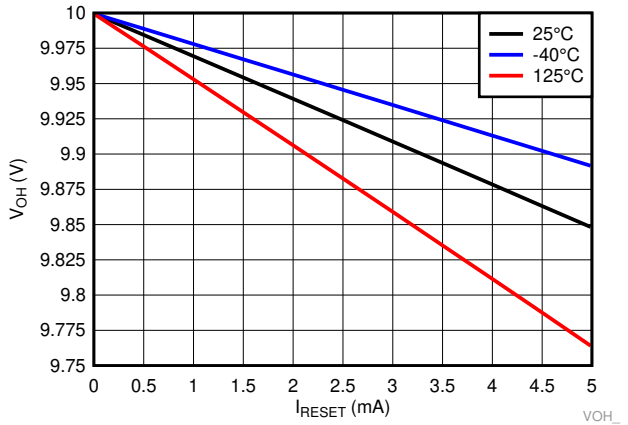


図 24. High Level Output Voltage vs I_{RESET} for TPS3840PL49-Q1

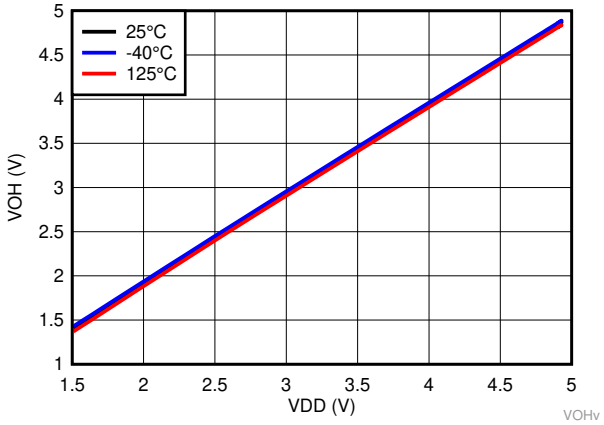


図 25. High Level Output Voltage over Temperature for TPS3840PL49-Q1

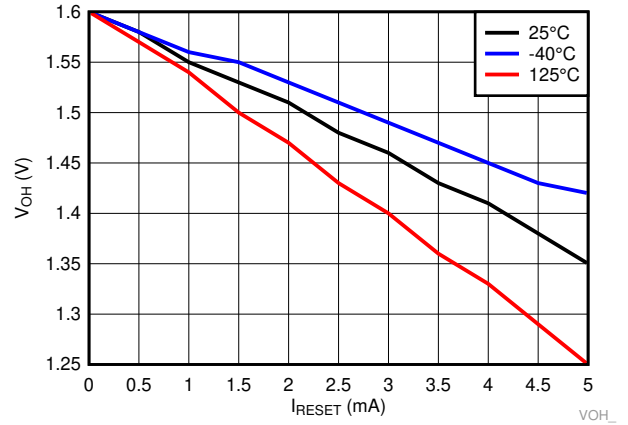


図 26. High Level Output Voltage vs I_{RESET} for TPS3840PH49-Q1

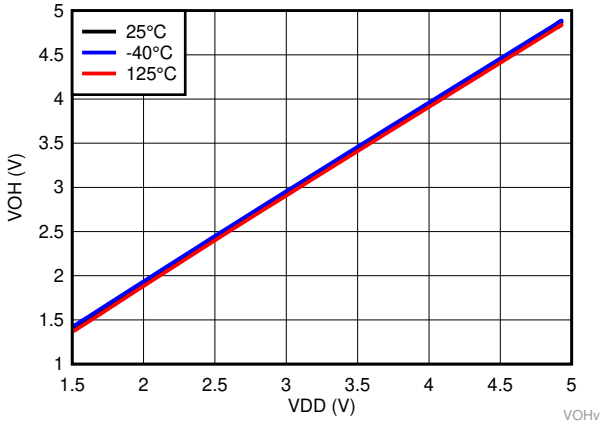


図 27. High Level Output Voltage Over Temperature for TPS3840PH49-Q1

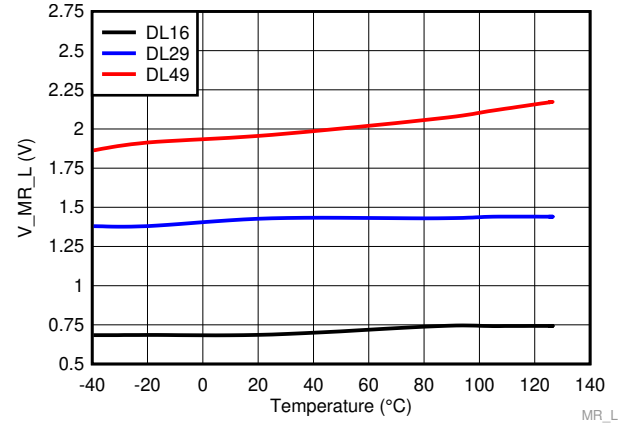


図 28. Manual Reset Logic Low Voltage Threshold Over Temperature for TPS3840DL-Q1

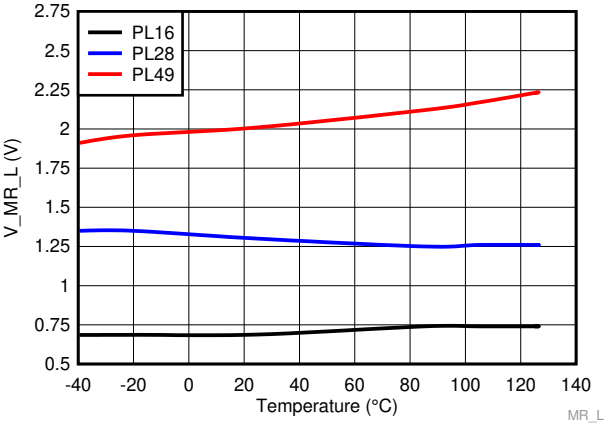


図 29. Manual Reset Logic Low Voltage Threshold Over Temperature for TPS3840PL-Q1

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

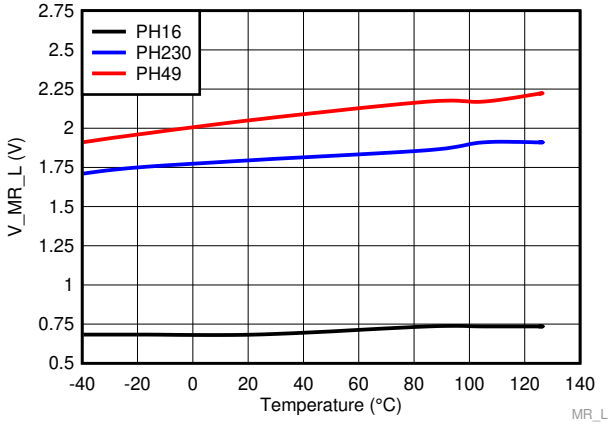


図 30. Manual Reset Logic Low Voltage Threshold Over Temperature for TPS3840PH-Q1

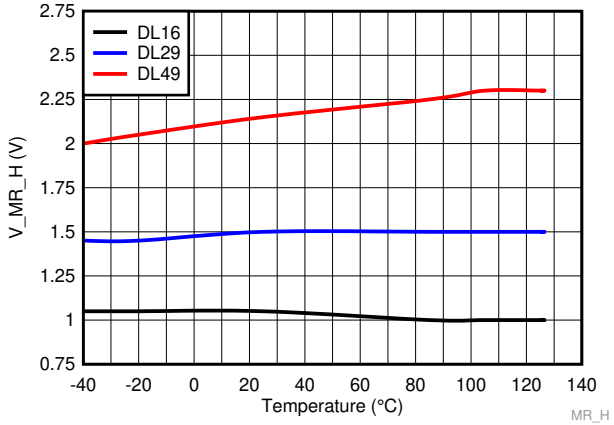


図 31. Manual Reset Logic High Voltage Threshold Over Temperature for TPS3840DL-Q1

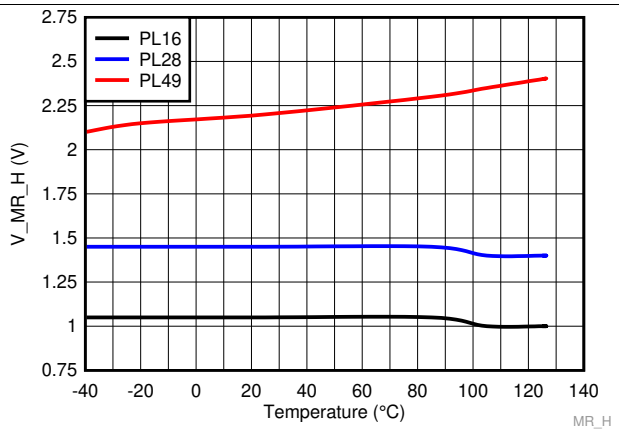


図 32. Manual Reset Logic High Voltage Threshold Over Temperature for TPS3840PL-Q1

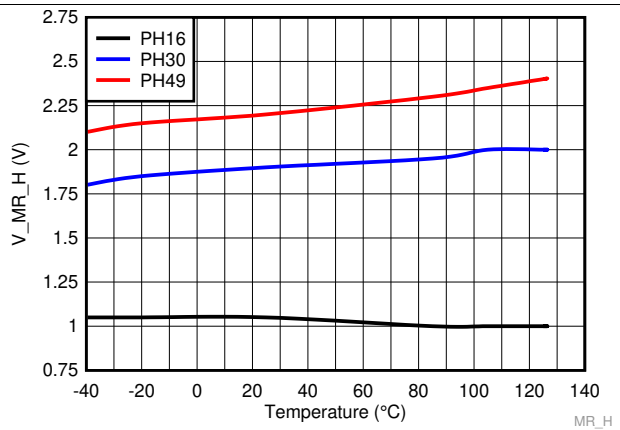


図 33. Manual Reset Logic High Voltage Threshold Over Temperature for TPS3840PH-Q1

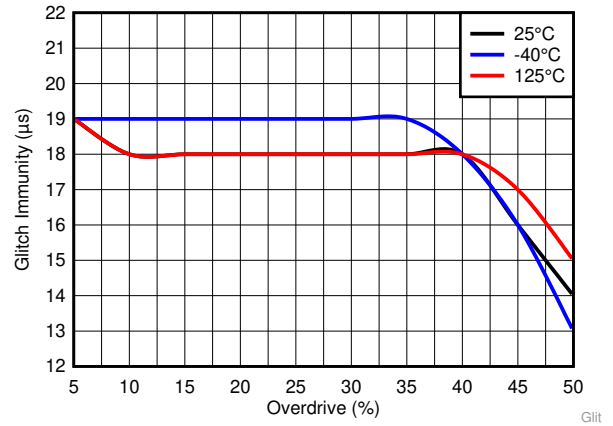


図 34. Glitch Immunity on V_{IT-} vs Overdrive (Data Taken with TPS3840PL28-Q1)

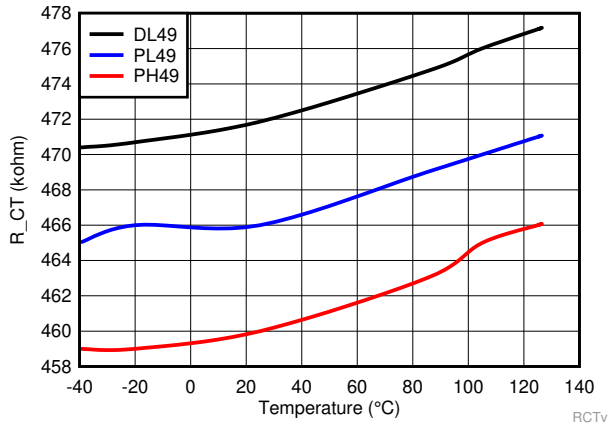


図 35. CT Pin Internal Resistance Over Temperature

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

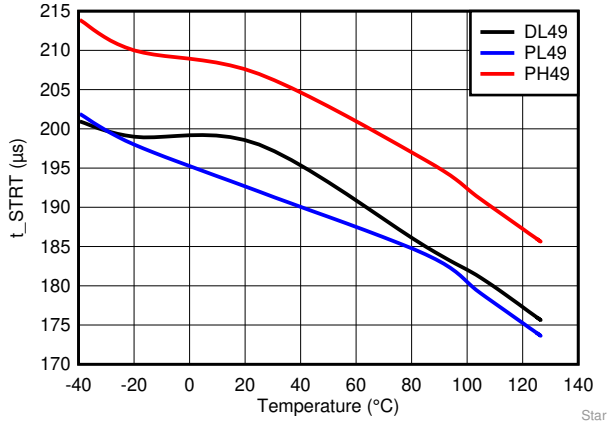


図 36. Startup Delay Over Temperature

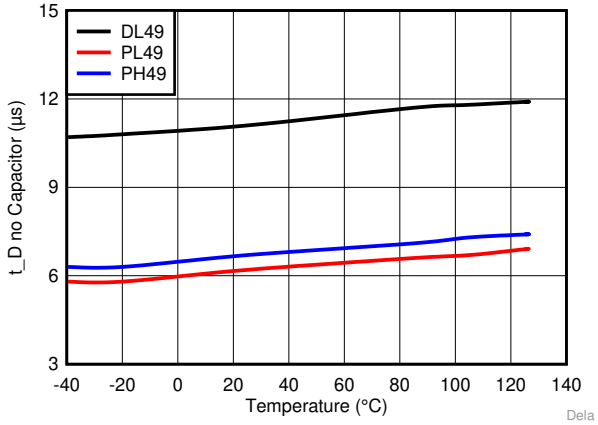


図 37. Reset Time Delay with No Capacitor Over Temperature

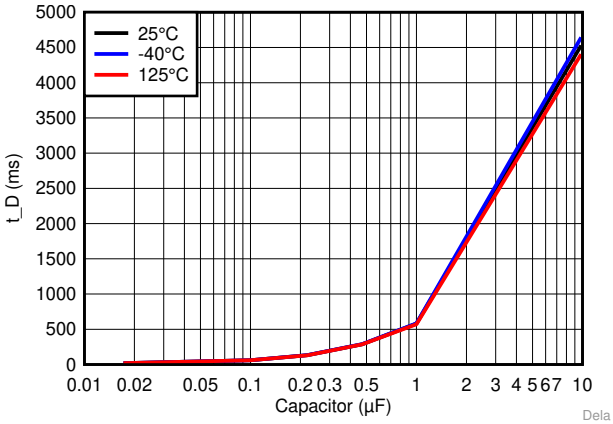


図 38. Reset Time Delay vs Capacitor Value (Data Taken with TPS3840PL16-Q1)

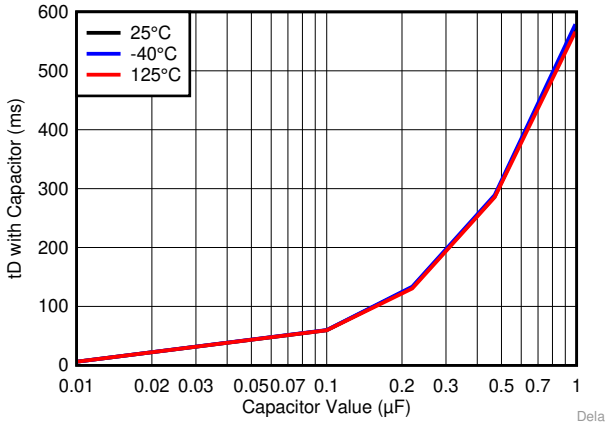


図 39. Reset Time Delay vs Small Capacitor Values (Data Taken with TPS3840PL16-Q1)

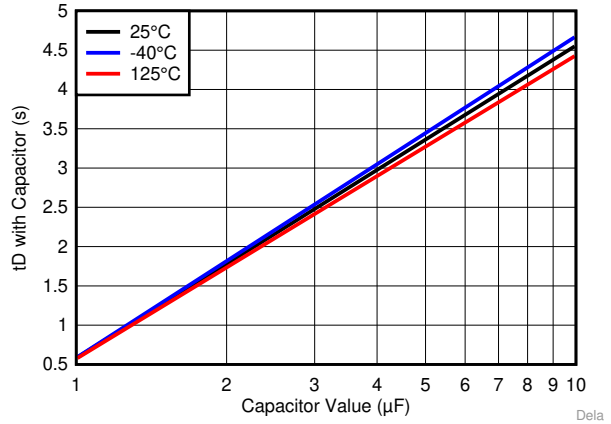


図 40. Reset Time Delay vs Large Capacitor Values (Data Taken with TPS3840PL16-Q1)

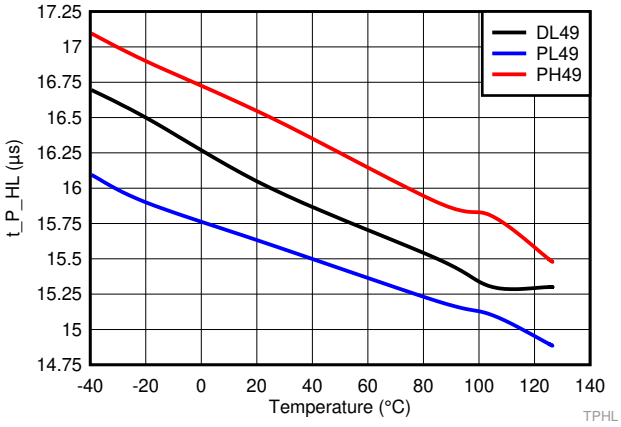


図 41. Propagation Detect Time Delay for VDD Falling Below V_{IT-} (High-to-Low) Over Temperature

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840-Q1 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

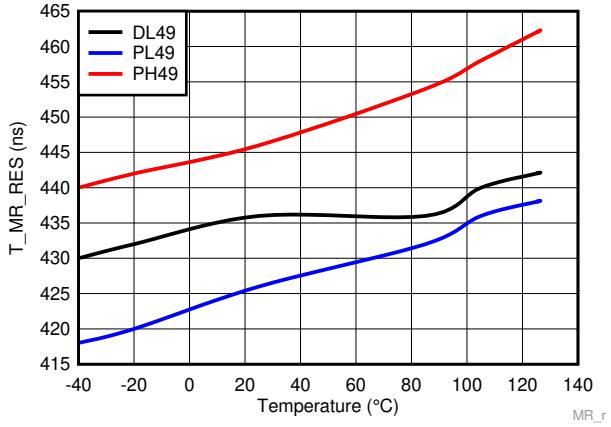


図 42. Propagation Time Delay from $\overline{MR}$ Asserted to Reset Over Temperature

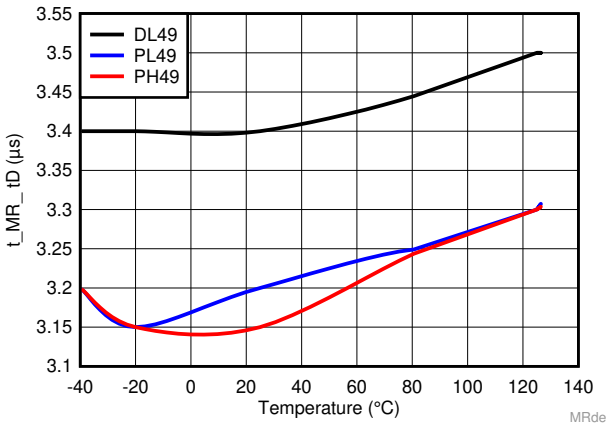


図 43. Propagation Time Delay from $\overline{MR}$ Release to Deasserted Reset Over Temperature

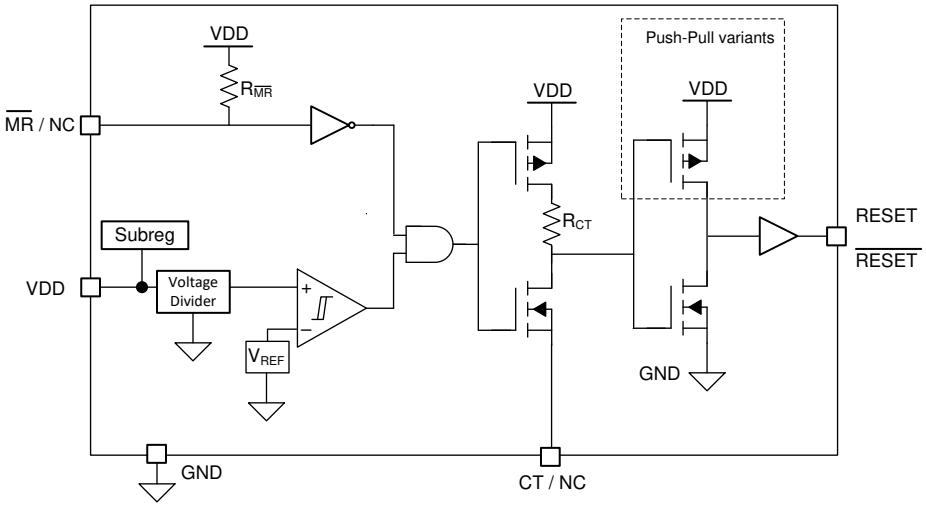
9 Detailed Description

9.1 Overview

The TPS3840-Q1 is a family of wide VDD and nano-quiescent current voltage detectors with fixed threshold voltage. TPS3840-Q1 features include programable reset time delay using external capacitor, active-low manual reset, 1% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages (V_{IT-}) can be factory set from 1.6 V to 4.9 V (see *表 3* for available options). TPS3840-Q1 is available in SOT-23 5 pin industry standard package.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 uF to 1 uF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

Feature Description (continued)

9.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

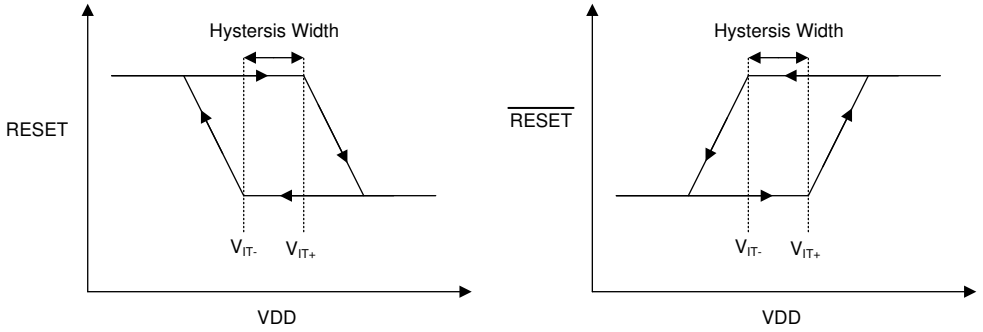


図 44. Hysteresis Diagram

9.3.1.2 VDD Transient Immunity

The TPS3840-Q1 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 1.

$$\text{Overdrive} = | (V_{DD} / V_{IT-} - 1) \times 100\% | \quad (1)$$

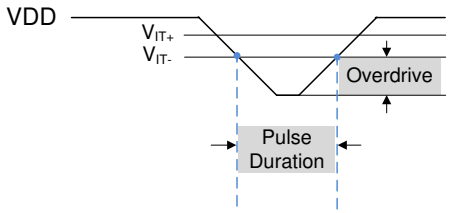


図 45. Overdrive vs Pulse Duration

9.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 50 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between CT pin and GND.

The relationship between external capacitor (C_{CT_EXT}) in F at CT pin and the time delay (t_D) in seconds is given by 式 2.

$$t_D = -\ln (0.29) \times R_{CT} \times C_{CT\_EXT} + t_D \text{ (no cap)} \quad (2)$$

式 2 is simplified to 式 3 by plugging R_{CT} and $t_{D(no\ cap)}$ given in *Electrical Characteristics* section:

$$t_D = 618937 \times C_{CT\_EXT} + 50\ \mu s \quad (3)$$

式 4 solves for external capacitor value (C_{CT_EXT}) in units of F where t_D is in units of seconds

$$C_{CT\_EXT} = (t_D - 50\ \mu s) \div 618937 \quad (4)$$

The reset delay varies according to three variables: the external capacitor variance (C_{CT}), CT pin internal resistance (R_{CT}) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is shown in Equation 5 and Equation 6.

$$s\ t_{D\ (minimum)} = -\ln (0.36) \times R_{CT\ (min)} \times C_{CT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (5)$$

$$t_{D\ (maximum)} = -\ln (0.26) \times R_{CT\ (max)} \times C_{CT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (6)$$

Feature Description (continued)

The recommended maximum delay capacitor for the TPS3840 is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

9.3.3 Manual Reset ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ with pulse duration longer than $t_{\overline{MR}\_RES}$ will causes reset output to assert. After $\overline{MR}$ returns to a logic high ($V_{\overline{MR}\_H}$) and VDD is above V_{IT+}, reset is deasserted after the user programmed reset time delay (t_D) expires.

If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can be left disconnected. If the logic signal controlling $\overline{MR}$ is less than VDD, then additional current flows from VDD into $\overline{MR}$ internally. For minimum current consumption, drive $\overline{MR}$ to either VDD or GND. $V_{\overline{MR}}$ must not be higher than VDD voltage.

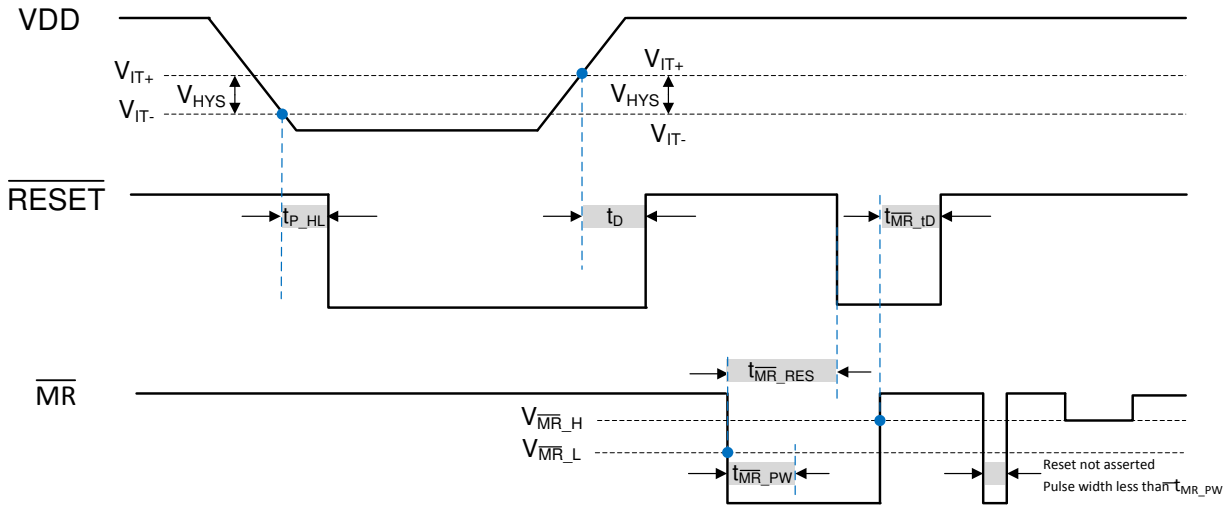


図 46. Timing Diagram $\overline{MR}$ and $\overline{RESET}$ (TPS3840DL-Q1)

9.3.4 Output Logic

9.3.4.1 $\overline{RESET}$ Output, Active-Low

$\overline{RESET}$ (Active-Low) applies to TPS3840D**L**-Q1 (Open-Drain) and TPS3840P**L**-Q1 (Push-Pull) hence the "**L**" in the device name. $\overline{RESET}$ remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the $\overline{MR}$ pin is floating or above $V_{\overline{MR}\_H}$. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then $\overline{RESET}$ is asserted.

When $\overline{MR}$ is again logic high or floating and VDD rise above V_{IT+}, the delay circuit will hold $\overline{RESET}$ low for the specified reset time delay (t_D). When the reset time delay has elapsed, the $\overline{RESET}$ pin goes back to logic high voltage (V_{OH}).

The TPS3840DL-Q1 (Open-Drain) version, denoted with "**D**" in the device name, requires a pull-up resistor to hold $\overline{RESET}$ pin high. Connect the pull-up resistor to the desired pull-up voltage source and $\overline{RESET}$ can be pulled up to any voltage up to 10 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$).

The Push-Pull variants (TPS3840**P**L and TPS3840**P**H), denoted with "**P**" in the device name, does not require a pull-up resistor.

Feature Description (continued)

9.3.4.2 RESET Output, Active-High

RESET (active-high), denoted with no bar above the pin label, applies only to TPS3840PH-Q1 push-pull active-high version. RESET remains low (deasserted) as long as VDD is above the threshold (V_{IT-}) and the manual reset signal ($\overline{MR}$) is logic high or floating. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When $\overline{MR}$ is again logic high and VDD is above V_{IT+} the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to low voltage (V_{OL}).

9.4 Device Functional Modes

表 1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

表 1. Truth Table

VDD	$\overline{MR}$	RESET	$\overline{RESET}$
VDD < V_{POR}	Ignored	Undefined	Undefined
V_{POR} < V_{DD} < V_{IT-} (1)	Ignored	H	L
VDD ≥ V_{IT-}	L	H	L
VDD ≥ V_{IT-}	H	L	H
VDD ≥ V_{IT-}	Floating	L	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and output reset is held asserted until V_{DD} falls below V_{POR}.

9.4.1 Normal Operation (V_{DD} > $V_{DD(min)}$)

When VDD is greater than $V_{DD(min)}$, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-}) and the logic state of $\overline{MR}$.

- $\overline{MR}$ high: the reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{MR}$ low: in this mode, the reset is asserted regardless of the threshold voltage.

9.4.2 VDD Between VPOR and $V_{DD(min)}$

When the voltage on VDD is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the reset signal is asserted.

9.4.3 Below Power-On-Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

10.2 Typical Application

10.2.1 Design 1: Dual Rail Monitoring with Power-Up Sequencing

A typical application for the TPS3840-Q1 is voltage rail monitoring and power-up sequencing as shown in 図 47. The TPS3840-Q1 can be used to monitor any rail above 1.6 V. In this design application, two TPS3840-Q1 devices monitor two separate voltage rails and sequences the rails upon power-up. The TPS3840PL30-Q1 is used to monitor the 3.3-V main power rail and the TPS3840DL16-Q1 is used to monitor the 1.8-V rail provided by the LDO for other system peripherals. The $\overline{\text{RESET}}$ output of the TPS3840PL30-Q1 is connected to the ENABLE input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than V_{IT-} or when $\overline{\text{MR}}$ is driven low by an external source.

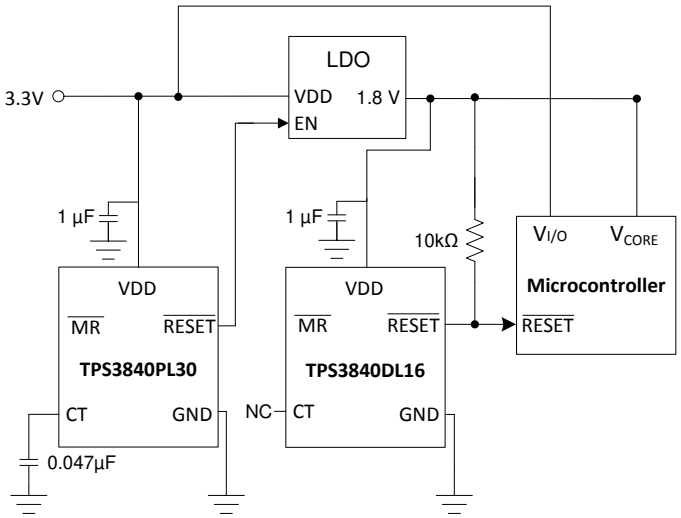


図 47. TPS3840-Q1 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

10.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3-V and 1.8-V rails. The voltage rail needs to sequence upon power up with the 3.3-V rail coming up first followed by the 1.8-V rail at least 25 ms after.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3-V and 1.8-V rails	Two TPS3840-Q1 devices provide voltage monitoring with 1% accuracy with device options available in 0.1 V variations
Voltage Rail Sequencing	Power up the 3.3-V rail first followed by 1.8-V rail 25 ms after	The CT capacitor on TPS38240PL28 is set to 0.047 µF for a reset time delay of 29 ms typical
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	1 µA	Each TPS3840-Q1 requires 350 nA typical

10.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS3840-Q1 can monitor any voltage between 1.6 V and 10 V and is available in 0.1 V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the first TPS3840-Q1 triggers when the 3.3-V rail falls to 3.0 V. The second TPS3840-Q1 triggers a reset when the 1.8-V rail falls to 1.6 V. The secondary constraint for this application is the reset time delay that must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3-V rail, enough time to startup correctly before the 1.8-V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in 式 2. Solving 式 2 for 25 ms gives a minimum capacitor value of 0.04 µF which is rounded up to a standard value 0.047 µF to account for capacitor tolerance.

A 1-µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ±5 mA limit found in the *Recommended Operating Conditions*: $R_{Pull\text{-}up} = V_{Pull\text{-}up} \div 5$ mA. For this design, a standard 10-kΩ pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted. Keep in mind the lower the pull-up resistor, the higher V_{OL}. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired or left floating if not used due to the internal pull-up resistor to VDD.

10.2.1.3 Application Curves

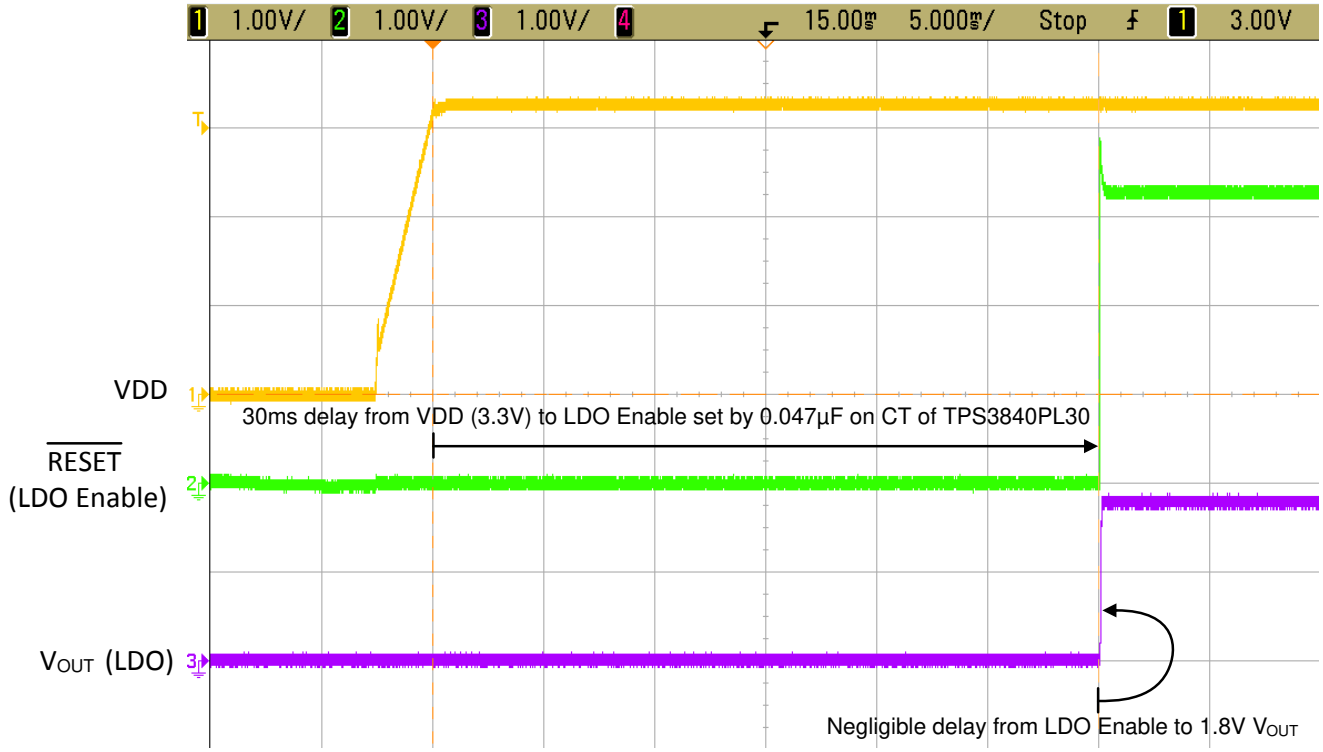


図 48. Startup Sequence Highlighting the Delay Between 3.3V and 1.8V Rails

10.2.2 Design 2: Automotive Off-Battery Monitoring

The initial power stage in automotive applications starts with the 12 V battery. Variation of the battery voltage is common between 9 V and 16 V. Furthermore, If cold-cranking and load dump conditions are considered, voltage transients can occur as low as 3 V and as high as 42V. In this design example, we are highlighting the ability for low power , direct off-battery voltage supervision. 図 49 illustrates an example of how the TPS3840-Q1 is monitoring the battery voltage while being powered by it as well. For more information, read this *application report* on how to achieve nano-amp I_Q voltage supervision in automotive, wide-vin applications.

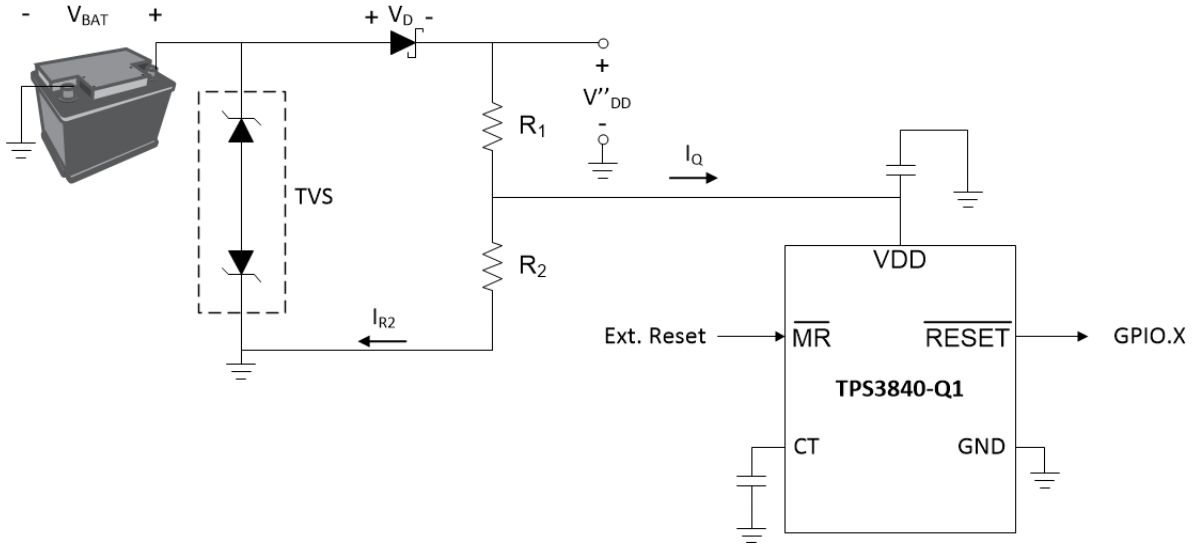


図 49. Fast Start Undervoltage Supervisor with Level-Shifted Input

10.2.2.1 Design Requirements

This design requires voltage supervision on a 12-V power supply voltage rail with possibility of the 12-V rail rising up as high as 42 V. The undervoltage fault occurs when the power supply voltage drops below 7.7 V.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 12-V power supply for undervoltage condition, trigger a undervoltage fault at 7.7 V.	TPS3840-Q1 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. Resistor dividers are calculated based on device variant and desired threshold voltage.
Maximum Input Power	Operate with power supply input up to 42 V.	The TPS3840-Q1 limits VDD to 10 V but can monitor voltages higher than the maximum VDD voltage with the use of an external resistor divider.
Output logic voltage	Open-Drain Output Topology	Due to large variance in battery voltage, an open-drain output is recommended to provide the correct reset signal.
Maximum system current consumption	35 uA when power supply is at 12 V typical	TPS3840-Q1 requires 350 nA (typical) and the external resistor divider will also consume current. There is a tradeoff between current consumption and voltage monitor accuracy but generally set the resistor divider to consume 100 times current into VDD.
Voltage Monitor Accuracy	Typical voltage monitor accuracy of 2.5%.	The TPS3840-Q1 has 1% typical voltage monitor accuracy. By decreasing the ratio of resistor values, the resistor divider will consume more current but the accuracy will increase. The resistor tolerance also needs to be accounted for.
Delay when returning from fault condition	$\overline{\text{RESET}}$ delay of at least 200 ms when returning from a undervoltage fault.	C_{CT} = 0.33 µF sets 204 ms delay

10.2.2.2 Detailed Design Procedure

The primary constraint for this application is monitoring a 12-V rail while preventing the VDD pin on TPS3840-Q1 from exceeding the recommended maximum of 10 V. This is accomplished by sizing the resistor divider so that when the 12-V rail drops to 7.7 V, the VDD pin for TPS3840-Q1 will be at 1.6 V which is the V_{IT-} threshold for triggering a undervoltage condition for TPS3840DL16-Q1 as shown in 式 7. Reasonably sized resistors were selected for the voltage divider. While selecting lower resistor values may increase current, this allows for additional accuracy from the resistor divider.

$$V_{rail\_trigger} = V_{IT-} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

where $V_{rail\_trigger}$ is the trigger voltage of the rail being monitored, V_{IT-} is the falling threshold on the VDD pin of TPS3840, and R_1 and R_2 are the top and bottom resistors of the external resistor divider. V_{IT-} is fixed per device variant and is 1.6 V for TPS3840DL16-Q1. Substituting in the values from 図 49, the undervoltage trigger threshold for the rail is set to 7.7 V. Given that R_1 = 100 kΩ, R_2 = 26.2 kΩ.

Because the undervoltage trigger of 10 V on the rail corresponds to 1.6 V undervoltage threshold trigger of the TPS3840-Q1 device, there is room for the rail to rise up while maintaining less than 10 V on the VDD pin of the TPS3840-Q1. 式 8 shows the maximum rail voltage that still meets the 10 V maximum at the VDD pin for TPS3840-Q1.

$$V_{rail\_max} = 10\ V \times (26.2\ k\Omega \div (100\ k\Omega + 26.2\ k\Omega)) = 48.168\ V \quad (8)$$

This means the monitored voltage rail can go as high as 48.168 V and not violate the recommended maximum for the VDD pin on TPS3840-Q1. This is useful when monitoring a voltage rail that has a wide range that may go much higher than the nominal rail voltage such as in this case. Notice that the resistor values chosen are less than 100kΩ to preserve the accuracy set by the internal resistor divider. Good design practice recommends using a 0.1-µF capacitor on the VDD pin and this capacitance may need to increase when using an external resistor divider.

10.2.2.3 Application Curves: TPS3840EVM

These application curves are taken with the *TPS3840EVM* using the TPS3840-Q1. Please see the *TPS3840EVM User Guide* for more information. The scope of the test below was to ensure that normal operation was maintained under typical cold crank and load dump conditions. This was verified by observing the input changing to its minimum and maximum value and the output remained both defined and accurate.

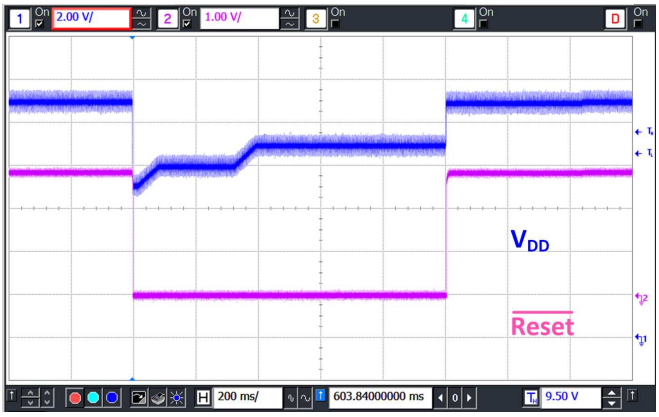


図 50. TPS3840-Q1 Warm-Start Test Pulse

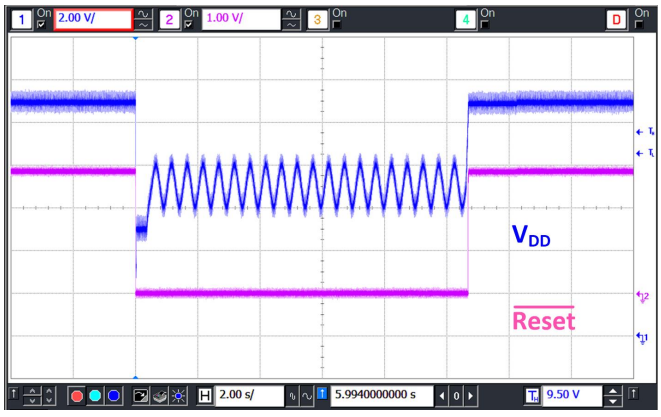


図 51. TPS3840-Q1 Cold-Start Test Pulse

図 52. TPS3840-Q1 Cold Crank Test Pulse

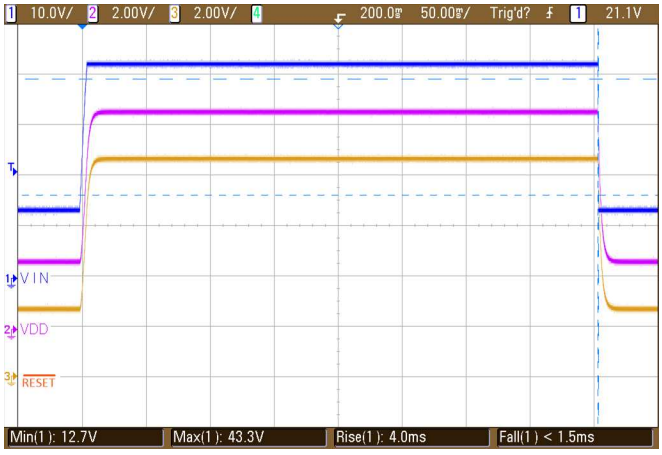


図 53. TPS3840-Q1 Load Dump Test Pulse

11 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 10 V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 12-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 12 V, additional precautions must be taken.

12 Layout

12.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a >0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT} capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to <5 pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.

12.2 Layout Example

The layout example in shows how the TPS3840-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.

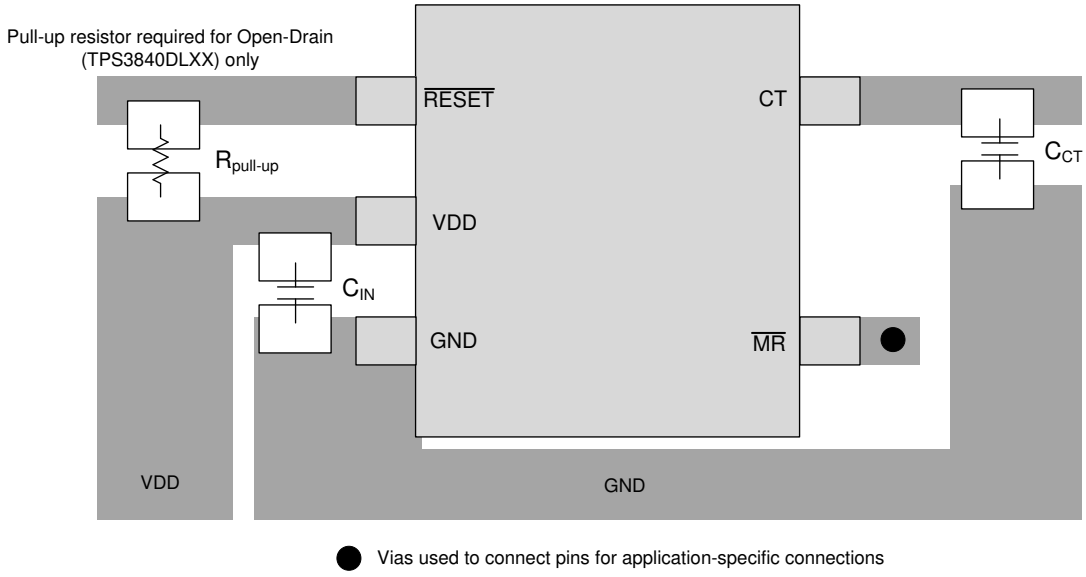


図 54. TPS3840-Q1 Recommended Layout

13 デバイスおよびドキュメントのサポート

13.1 デバイスの項目表記

デバイスの型番から機能を解読する方法を、表 2に示します。

表 2. デバイスの命名規則

説明	項目表記	値
エンジニアリング・プロトタイプ・プレリリース・サンプル	P	エンジニアリング・プロトタイプ・サンプル
型番	TPS3840	TPS3840-Q1
バリアント・コード (出力トポロジ)	DL	オープン・ドレイン、アクティブ LOW
	PH	プッシュプル、アクティブ HIGH
	PL	プッシュプル、アクティブ LOW
検出電圧オプション	## (2 文字)	例:16 は 1.6V のスレッショルドを表します。
パッケージ	DBV	SOT23-5
リール	R	大型リール
車載用接尾辞	Q1	デバイスが AEC-Q100 規格に準拠していることを示します。

表 3 に、TPS3840-Q1 の提供中のバリアントを示します。下記以外のオプションの詳細と入手可能性については、テキサス・インスツルメンツにお問い合わせください。最小注文数量があります。

表 3. デバイスのスレッショルド

製品名			電圧スレッショルド (V_{IT-})	ヒステリシス (V_{HYST})
オープン・ドレイン、アクティブ **LOW**	プッシュプル、アクティブ **LOW**	プッシュプル、アクティブ **HIGH**	標準値 (V)	標準値 (V)
TPS3840DL16-Q1	TPS3840PL16-Q1	TPS3840PH16-Q1	1.6	0.100
TPS3840DL17-Q1	TPS3840PL17-Q1	TPS3840PH17-Q1	1.7	0.100
TPS3840DL18-Q1	TPS3840PL18-Q1	TPS3840PH18-Q1	1.8	0.100
TPS3840DL19-Q1	TPS3840PL19-Q1	TPS3840PH19-Q1	1.9	0.100
TPS3840DL20-Q1	TPS3840PL20-Q1	TPS3840PH20-Q1	2.0	0.100
TPS3840DL21-Q1	TPS3840PL21-Q1	TPS3840PH21-Q1	2.1	0.100
TPS3840DL22-Q1	TPS3840PL22-Q1	TPS3840PH22-Q1	2.2	0.100
TPS3840DL23-Q1	TPS3840PL23-Q1	TPS3840PH23-Q1	2.3	0.100
TPS3840DL24-Q1	TPS3840PL24-Q1	TPS3840PH24-Q1	2.4	0.100
TPS3840DL25-Q1	TPS3840PL25-Q1	TPS3840PH25-Q1	2.5	0.100
TPS3840DL26-Q1	TPS3840PL26-Q1	TPS3840PH26-Q1	2.6	0.100
TPS3840DL27-Q1	TPS3840PL27-Q1	TPS3840PH27-Q1	2.7	0.100
TPS3840DL28-Q1	TPS3840PL28-Q1	TPS3840PH28-Q1	2.8	0.100
TPS3840DL29-Q1	TPS3840PL29-Q1	TPS3840PH29-Q1	2.9	0.100
TPS3840DL30-Q1	TPS3840PL30-Q1	TPS3840PH30-Q1	3.0	0.100
TPS3840DL31-Q1	TPS3840PL31-Q1	TPS3840PH31-Q1	3.1	0.200
TPS3840DL32-Q1	TPS3840PL32-Q1	TPS3840PH32-Q1	3.2	0.200
TPS3840DL33-Q1	TPS3840PL33-Q1	TPS3840PH33-Q1	3.3	0.200
TPS3840DL34-Q1	TPS3840PL34-Q1	TPS3840PH34-Q1	3.4	0.200
TPS3840DL35-Q1	TPS3840PL35-Q1	TPS3840PH35-Q1	3.5	0.200
TPS3840DL36-Q1	TPS3840PL36-Q1	TPS3840PH36-Q1	3.6	0.200
TPS3840DL37-Q1	TPS3840PL37-Q1	TPS3840PH37-Q1	3.7	0.200
TPS3840DL38-Q1	TPS3840PL38-Q1	TPS3840PH38-Q1	3.8	0.200
TPS3840DL39-Q1	TPS3840PL39-Q1	TPS3840PH39-Q1	3.9	0.200

表 3. デバイスのスレッショルド (continued)

製品名			電圧スレッショルド (V_{IT-})	ヒステリシス (V_{HYST})
オープン・ドレイン、アクティブ LOW	プッシュプル、アクティブ LOW	プッシュプル、アクティブ HIGH	標準値 (V)	標準値 (V)
TPS3840DL40-Q1	TPS3840PL40-Q1	TPS3840PH40-Q1	4.0	0.200
TPS3840DL41-Q1	TPS3840PL41-Q1	TPS3840PH41-Q1	4.1	0.200
TPS3840DL42-Q1	TPS3840PL42-Q1	TPS3840PH42-Q1	4.2	0.200
TPS3840DL43-Q1	TPS3840PL43-Q1	TPS3840PH43-Q1	4.3	0.200
TPS3840DL44-Q1	TPS3840PL44-Q1	TPS3840PH44-Q1	4.4	0.200
TPS3840DL45-Q1	TPS3840PL45-Q1	TPS3840PH45-Q1	4.5	0.200
TPS3840DL46-Q1	TPS3840PL46-Q1	TPS3840PH46-Q1	4.6	0.200
TPS3840DL47-Q1	TPS3840PL47-Q1	TPS3840PH47-Q1	4.7	0.200
TPS3840DL48-Q1	TPS3840PL48-Q1	TPS3840PH48-Q1	4.8	0.200
TPS3840DL49-Q1	TPS3840PL49-Q1	TPS3840PH49-Q1	4.9	0.200

13.2 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.3 商標

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All other trademarks are the property of their respective owners.

13.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3840DL16DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ16	Samples
TPS3840DL18DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ18	Samples
TPS3840DL20DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ20	Samples
TPS3840DL25DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ25	Samples
TPS3840DL28DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ28	Samples
TPS3840DL29DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ29	Samples
TPS3840DL30DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ30	Samples
TPS3840DL31DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ31	Samples
TPS3840DL32DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ32	Samples
TPS3840DL37DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ37	Samples
TPS3840DL40DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ40	Samples
TPS3840DL41DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ41	Samples
TPS3840DL42DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ42	Samples
TPS3840DL44DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ44	Samples
TPS3840DL45DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ45	Samples
TPS3840DL46DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ46	Samples
TPS3840DL47DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQ47	Samples
TPS3840PH27DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QH27	Samples
TPS3840PH30DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QH30	Samples
TPS3840PL16DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL16	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3840PL25DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL25	Samples
TPS3840PL28DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL28	Samples
TPS3840PL29DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL29	Samples
TPS3840PL30DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL30	Samples
TPS3840PL31DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL31	Samples
TPS3840PL40DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL40	Samples
TPS3840PL43DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QL43	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3840-Q1 :

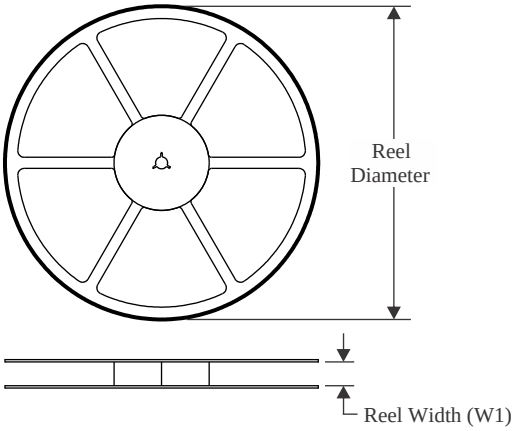
- Catalog : TPS3840

NOTE: Qualified Version Definitions:

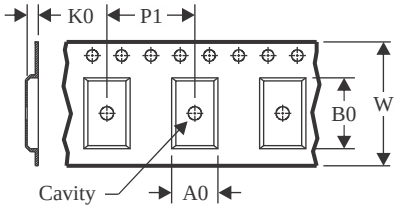
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

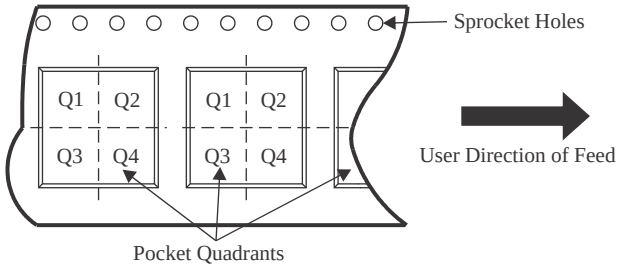


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

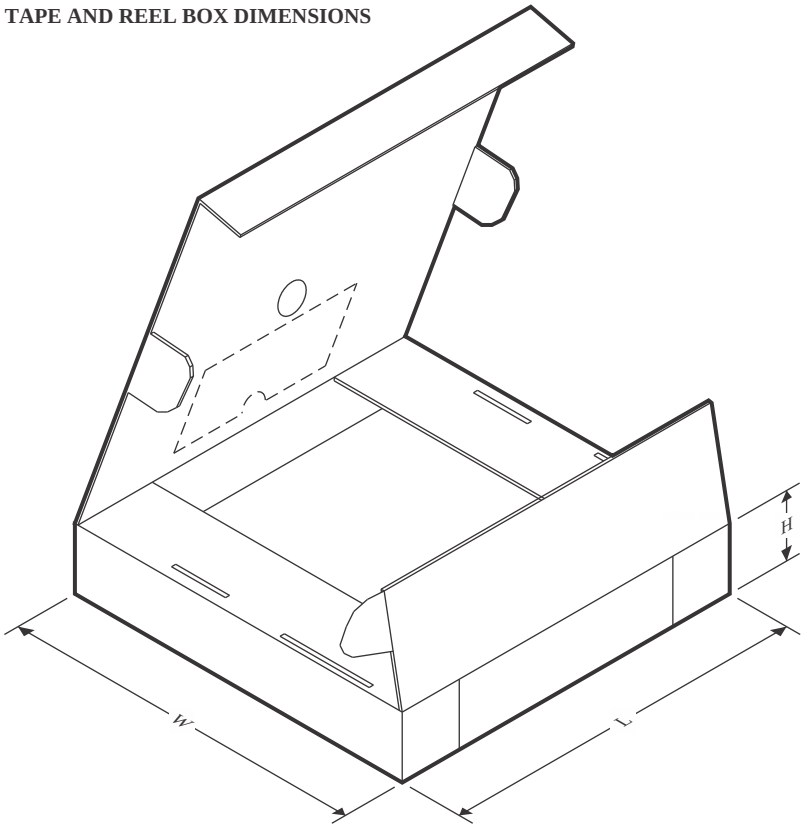


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840DL16DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL18DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL20DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL25DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL28DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL29DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL31DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL32DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL37DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL40DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL41DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL42DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL44DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL45DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL46DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840DL47DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH27DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL16DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL25DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL28DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL29DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL31DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL40DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL43DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840DL16DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL18DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL20DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL25DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL28DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL29DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL30DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL31DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL32DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL37DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL40DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL41DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL42DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL44DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL45DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL46DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL47DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH27DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

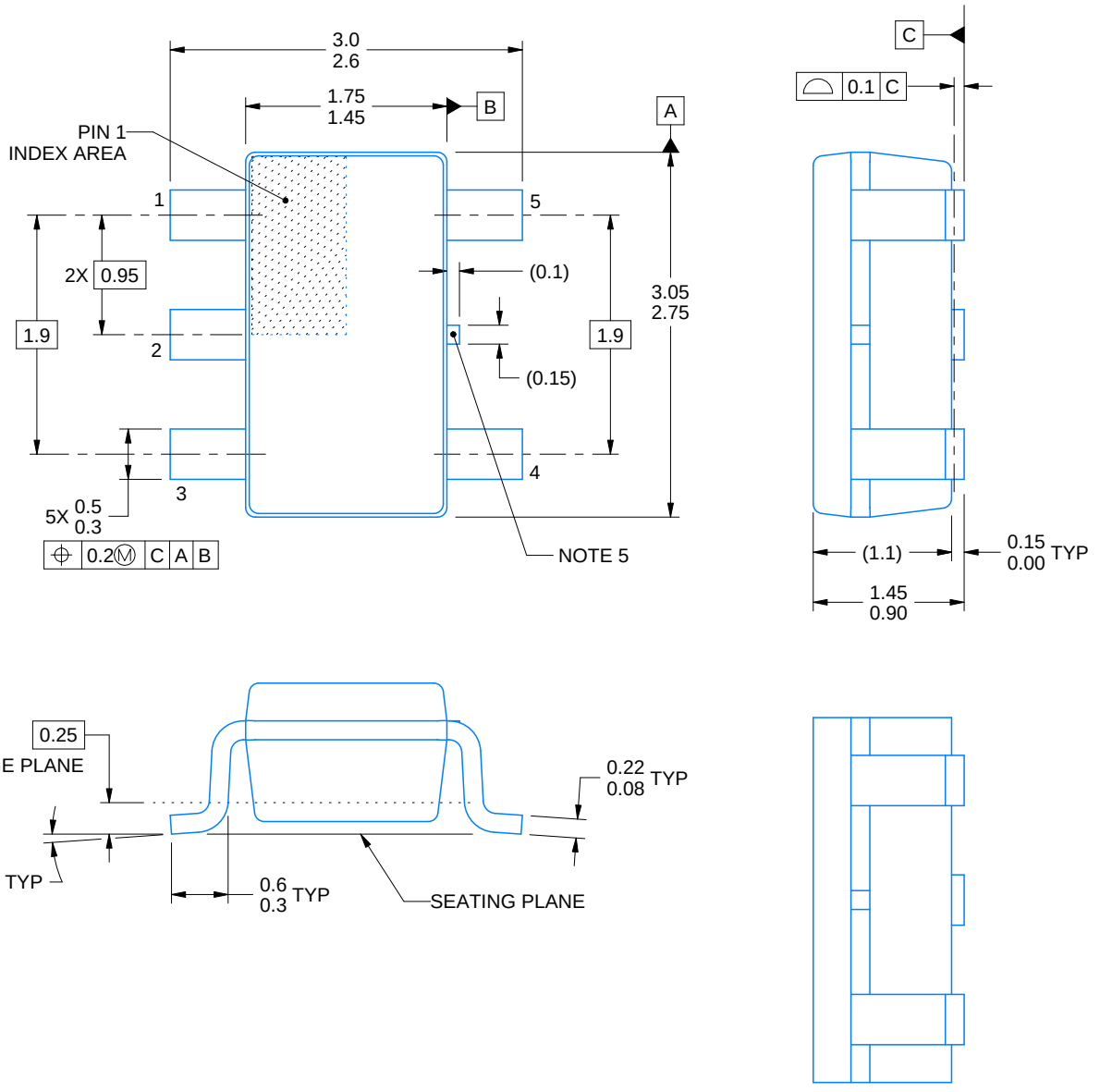
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840PH30DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL16DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL25DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL28DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL29DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL30DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL31DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL40DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL43DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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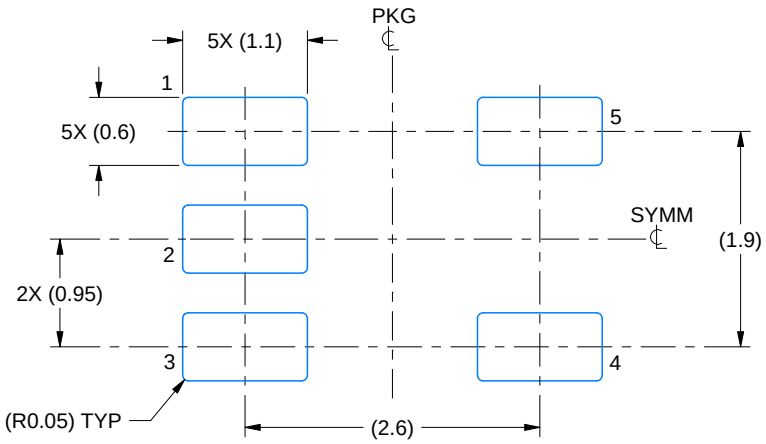
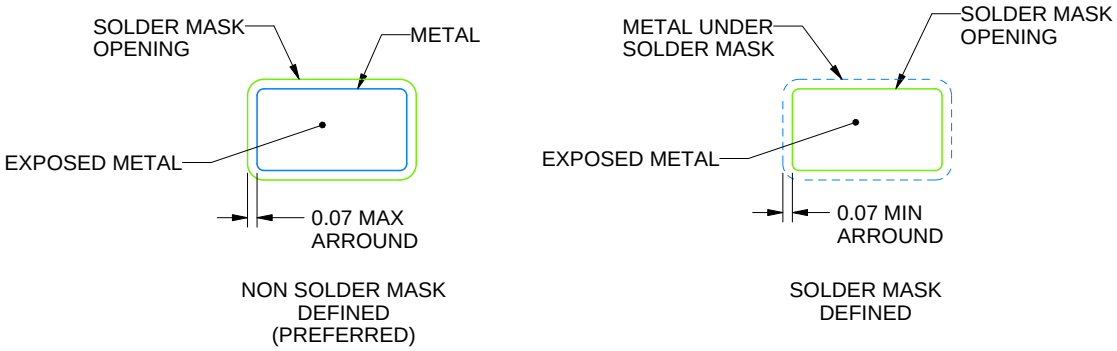
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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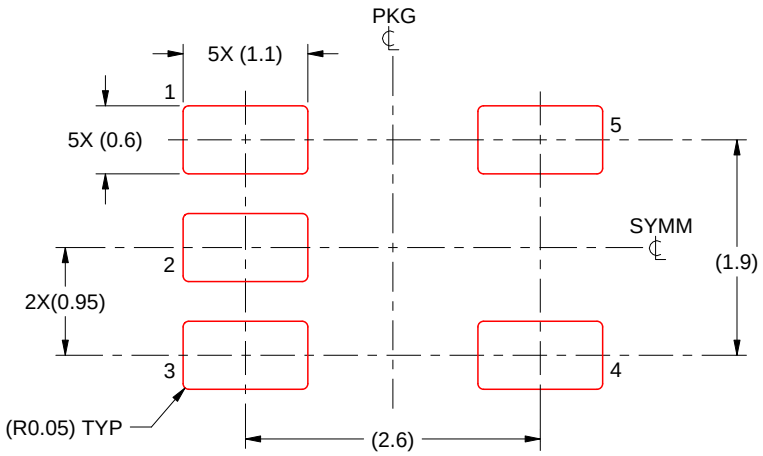
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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