TPSM336x5、3V～36V 入力、1V～15V 出力、1.5A、2.5A 同期整流降圧コンバータ電源モジュール、HotRod™ QFN パッケージ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 多用途な同期整流降圧 DC/DC モジュール:
  - MOSFET、インダクタ、C_{BOOT} コンデンサ、コントローラを内蔵
  - 幅広い入力電圧範囲:3V～36V
  - 最大 40V の過渡入力に対する保護
  - 接合部温度範囲:-40°C～+125°C
  - 4.5mm × 3.5mm × 2mm のオーバーモールド パッケージ
  - RT ピンを使用して 200kHz～2.2MHz の範囲で周波数を調整可能
- 全負荷範囲にわたって極めて高い効率を実現:
  - V_{IN} = 12V、V_{OUT} = 5V、1MHz、I_{OUT} = 2.5A で 88% を上回る効率
  - V_{IN} = 24V、V_{OUT} = 5V、1MHz、I_{OUT} = 2.5A で 87% を上回る効率
  - V_{IN} = 13.5V で最小 1.5µA のスタンバイ I_Q
- 超低 EMI 要件に最適化:
  - デュアル ランダム スペクトラム拡散機能 - DRSS
  - フリップチップ オン リード パッケージ - FCOL
  - インダクタとブート コンデンサの統合
  - CISPR 11、Class B 準拠可能
- 出力電圧および電流オプション:
  - 出力電圧を 1V～15V の範囲で調整可能
- スケーラブルな電源に対応した設計:
  - 次の製品とピン互換:
    - TPSM365R15 (65V、150mA)、TPSM365R6 (65V、600mA)
- WEBENCH® Power Designer により、TPSM336x5 を使用するカスタム設計を作成

2 アプリケーション

- ファクトリ・オートメーション
- 試験および測定機器
- グリッド・インフラ

3 概要

TPSM336x5 は、1.5A または 2.5A、36V 入力の同期整流降圧 DC/DC パワー モジュールで、フリップ チップ オン リード (FCOL) パッケージ、パワー MOSFET、内蔵インダクタ、ブート コンデンサをコンパクトで使いやすい 3.5mm × 4.5mm × 2mm の 11 ピン QFN パッケージに統合しています。小型 HotRod™ QFN パッケージ テクノロジーにより、放熱性能が向上し、高い周囲温度での動作が保証されます。さらに、このデバイスはスペクトラム拡散との組み合わせにより、優れた EMI 性能を実現します。デバイスは、自動または強制 PWM モードでフィードバック デバイダを使用して 1V から 15V までの出力に構成でき、動作します。

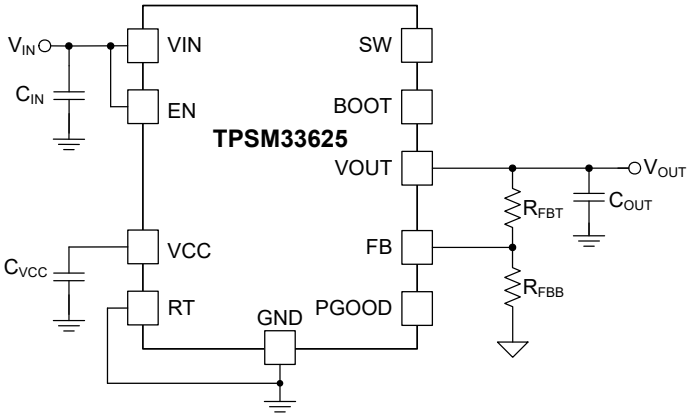
TPSM336x5 は、特に常時オンの産業用アプリケーションの低スタンバイ電力要件を満たすように設計されています。自動モードでは、軽負荷動作時の周波数フォールドバックが可能であり、1.5µA (V_{IN} = 13.5V) の無負荷時消費電流と、軽負荷時の効率向上を実現できます。PWM モードと PFM モードの間のシームレスな移行と小さな MOSFET ON 抵抗により、負荷範囲全体にわたって非常に優れた効率が得られます。

TPSM336x5 はピーク電流モード アーキテクチャと内部補償により、最小の出力容量で安定した動作を維持します。DRSS を使用して、入力 EMI フィルタの外部部品を低減します。MODE / SYNC および RT ピンのバリアントを使用すると、200kHz～2.2MHz の周波数に同期または設定して、ノイズの影響を受けやすい周波数帯域を回避できます。

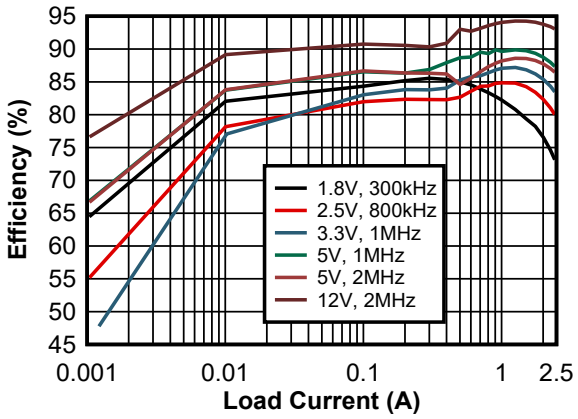
製品情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TPSM33625	RDN (QFN-FCMOD、11)	3.50mm × 4.50mm
TPSM33615		

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的な回路図



効率と出力電流との関係 (V_{IN} = 24V)

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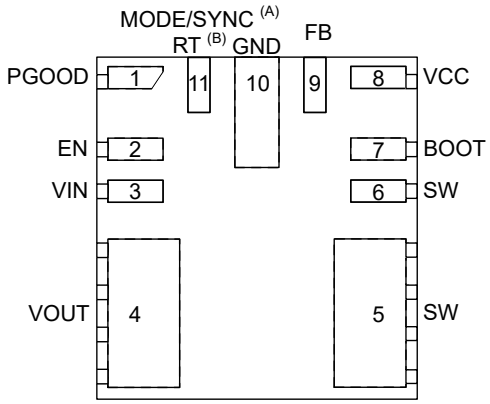
4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER (1)	F_{SW}	OUTPUT VOLTAGE	OUTPUT CURRENT	EXTERNAL SYNC (MODE Configuraiton)	SPREAD SPECTRUM
TPSM33625	TPSM33625RDNR	Adjustable with RT resistor	Adjustable (1 V to 15 V)	2.5 A	No (Default PFM at light load)	Yes
TPSM33625	TPSM33625FRDNR	Fixed 1 MHz	Adjustable (1 V to 15 V)	2.5 A	Yes (PFM/PWM Selectable)	Yes
TPSM33615	TPSM33615RDNR	Adjustable with RT resistor	Adjustable (1 V to 15 V)	1.5 A	No (Default PFM at light load)	Yes
TPSM33615	TPSM33615FRDNR	Fixed 1 MHz	Adjustable (1 V to 15 V)	1.5 A	Yes (PFM/PWM Selectable)	Yes

5 Pin Configuration and Functions



A. Pin 11 factory-set for fixed switching frequency MODE/SYNC variants only.

B. See *Device Comparison Table* for more details. Pin 11 trimmed and factory-set for externally adjustable switching frequency RT variants only.

図 5-1. RDN Package, 11-Pin QFN-FCMOD , Top View (All Variants)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	PGOOD	A	Power-good monitor. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to GND. High = power OK, Low = power bad. PGOOD pin goes low when EN = Low.
2	EN	A	Precision enable input pin. High = ON, Low = OFF. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Can be connected directly to VIN. The module can be turned off by using an open-drain or collector device to connect this pin to GND. An external voltage divider can be placed between this pin, GND, and VIN to create an external UVLO.*Do not float this pin.*
3	VIN	P	Input supply voltage. Connect the input supply to these pins. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND in close proximity to the module. Refer to セクション 8.5.2 for input capacitor placement example.
4	VOUT	P	Output voltage. The pin is connected to the internal output inductor. Connect the pin to the output load and connect external output capacitors between the pin and GND.
5, 6	SW	P	Power module switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
7	BOOT	P	Bootstrap pin for internal high-side driver circuitry. A 100-nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage.
8	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
9	FB	A	Feedback input. For the adjustable output, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to VOUT at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to GND. When connecting with feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See セクション 8.5.2 for a feedback resistor placement.
10	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
11	RT or MODE/SYNC	A	When the part is configured as the RT pin variant, the switching frequency in the part can be adjusted from 200 kHz to 2.2 MHz based on the resistor value connected between RT and GND. When the pin is trimmed as the MODE/SYNC variant, the part can operate in user-selectable PFM/PWM operation. In FPWM, the part can be synchronized to an external clock. Clock triggers on rising edge of applied external clock.*Do not float this pin.*.
A = Analog, P = Power, G = Ground			

6 Specifications

6.1 絶対最大定格

制限値は T_J = -40℃～125℃ までの範囲で適用されます (特に記述のない限り)。(1)

		最小値	最大値	単位
入力電圧	VIN から GND へ	-0.3	40	V
	SW に対する CBOOT	-0.3	5.5	V
	RT から GND へ	-0.3	5.5	V
	EN から GND へ	-0.3	40	V
	FB から GND へ	-0.3	16	V
	PG から GND へ	0	20	V
入力電圧	MODE/SYNC から GND へ	-0.3	5.5	V
出力電圧	VCC から GND へ	-0.3	5.5	V
	SW から GND へ(2)	-0.3	40	V
	VOUT から GND へ	-0.3	16	V
入力電流	PG	–	10	mA
T_J	接合部温度	-40	125	℃
T_A	周辺温度	-40	105	℃
T_{stg}	保管温度	-55	150	℃

(1) 「絶対最大定格」の範囲外の動作は、デバイスの永続的な損傷の原因となる可能性があります。「絶対最大定格」は、これらの条件において、または「推奨動作条件」に示された値を超える他のいかなる条件でも、本製品が正しく動作することを暗に示すものではありません。「絶対最大定格」の範囲内であっても「推奨動作条件」の範囲外で使用した場合、本デバイスは完全に機能するとは限らず、このことが本デバイスの信頼性、機能、性能に影響を及ぼし、本デバイスの寿命を縮める可能性があります。
(2) このピンには、PGND より 2V 低い値から VIN より 2V 高い値までの電圧を最大 200ns の間 (デューティ サイクルは 0.01% 以下) 印加できます。

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Limits apply over T_J = –40°C to 125°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	VIN (Input voltage range after start-up)	3		36	V
Output voltage	Output Adjustment Range(1)	1		15	V
Output current	TPSM33625 IOUT(2)	0		2.5	A
Output current	TPSM33615 IOUT(2)	0		1.5	A
Frequency	F_{SW} set by SYNC	200		2500	kHz
Frequency	F_{SW} set by RT	200		2200	kHz
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature	–40		105	°C

(1) Under no conditions should the output voltage be allowed to fall below zero volts.
(2) Maximum continuous DC current may be derated when operating with high switching frequency or high ambient temperature. Refer to the *Typical Characteristics* section for details.

6.4 Thermal Information

THERMAL METRIC (1)		TPSM33625 / TPSM33615	UNIT
		RDN	
		11 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM33625EVM)	22	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)	54.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report. The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. It does not represent the performance obtained in an actual application.

6.5 電気的特性

制限値は、T_J = -40℃～125℃、V_{IN} = 24V、V_{OUT} = 3.3V、F_{SW} = 1000kHz の範囲で適用されます (特に記述がない限り)。最小値および最大値の制限値は、量産テストを通して、または設計により規定されています。標準値は最も一般的なパラメータ基準値を表しており、参考目的にのみ提供されています。

パラメータ		テスト条件	最小値	代表値	最大値	単位
電源電圧						
V_{IN}	入力電圧立ち上がりスレッショルド	起動前	3.2	3.35	3.5	V
		動作開始後	2.45	2.7	3	V
I_{Q_VIN}	入力動作静止電流 (スイッチングなし)	T_A = 25℃、V_{EN} = 3.3V、V_{FB} = 1.5V		1.2		μA
I_{SDN_VIN}	VIN のシャットダウン時静止電流	V_{EN} = 0V、T_A = 25℃		0.3		μA
イネーブル						
V_{EN_RISE}	EN 電圧立ち上がりスレッショルド		1.16	1.23	1.3	V
V_{EN_HYS}	EN 電圧ヒステリシス		0.275	0.353	0.404	V
V_{EN_WAKE}	EN ウェークアップ スレッショルド		0.5	0.7	1	V
I_{LKG-EN}	イネーブル ピン入力リーク電流	V_{EN} = V_{IN} = 24V		10		nA
内部 LDO VCC						
V_{CC}	内部 LDO VCC 出力電圧	V_{FB} = 0V、I_{VCC} = 1mA	3.1	3.3	3.5	V
FEEDBACK						
V_{FB}	帰還電圧	T_A = 25℃、I_{OUT} = 0A		1.0		V
V_{FB_ACC}	帰還電圧精度	V_{IN} 範囲、V_{OUT} = 1V、I_{OUT} = 0A、F_{SW} = 200kHz	-1		+1	%
I_{FB}	FB ピンへの入力電流	可変構成、V_{FB} = 1.0V		10		nA
CURRENT						
I_{L_HS}	ハイサイド スイッチ電流制限値 (TPSM33625)	デューティ サイクルを 0% に近付ける	4.2	4.9	5.5	A
I_{L_LS}	ローサイド スイッチ電流制限値 (TPSM33625)		2.38	2.9	3.42	A
I_{L_NEG}	負の電流制限値 (TPSM33625)			-2		A
$I_{PEAKMIN}$	最小ピーク電流制限値 (TPSM33625)	自動モード		0.6		A
I_{L_HS}	ハイサイド スイッチ電流制限値 (TPSM33615)	デューティ サイクルを 0% に近付ける	2.58	3	3.42	A
I_{L_LS}	ローサイド スイッチ電流制限値 (TPSM33615)		1.44	1.75	2.06	A
I_{L_NEG}	負の電流制限値 (TPSM33615)			-2		A
$I_{PEAKMIN}$	最小ピーク電流制限値 (TPSM33615)	自動モード		0.4		A
I_{ZC}	ゼロクロスの電流制限値	自動モード		80		mA
V_{HICCUP}	ヒカップ モードに移行するためのレギュレートされる前の FB 電圧に対する FB 電圧の比率	ソフトスタート中以外		40		%
t_W	短絡待機時間 (ソフト スタートの前の「ヒカップ」時間)(1)		30	50	75	ms
ソフト スタート						
t_{SS}	最初の SW パルスから V_{REF} が設定点の 90% に達するまでの時間	V_{IN} ≧ 4.2V	2	3.5	4.6	ms

6.5 電気的特性 (続き)

制限値は、T_J = -40℃～125℃、V_{IN} = 24V、V_{OUT} = 3.3V、F_{SW} = 1000kHz の範囲で適用されます (特に記述がない限り)。最小値および最大値の制限値は、量産テストを通して、または設計により規定されています。標準値は最も一般的なパラメータ基準値を表しており、参考目的にのみ提供されています。

パラメータ		テスト条件	最小値	代表値	最大値	単位
パワー グッド						
PG_{OV}	PG の上限 - 立ち上がり	V_{OUT} 設定の % (可変出力)	104	108	111	%
PG_{UV}	PG の下限 - 立ち下がり	VOUT 設定の % (可変出力)	89	91	94.2	%
PG_{HYS}	OV の PG 上限スレッショルド ヒステリシス	VOUT 設定の %	2	2.4	2.8	%
	UV の PG 上限スレッショルド ヒステリシス	VOUT 設定の %	2	3.3	4.6	%
$V_{IN\_PG\_VALID}$	有効な PG 出力の入力電圧	R_{PGD_PU} = 10kΩ、V_{EN} = 0V			1.5	V
V_{PG_LOW}	Low レベル PG 機能出力電圧	PG ピンに 2mA のプルアップを接続、V_{EN} = 3.3V			0.4	V
$t_{PG\_FLT\_RISE}$	PG High 信号までの遅延時間		1.35	2.5	4	ms
t_{RESET_FILTER}	立ち下がりエッジでの PGOOD グリッチ除去遅延		25	40	75	µs
R_{PGD}	PGOOD オン抵抗	V_{EN} = 3.3V、200uA のプルアップ電流			100	Ω
R_{PGD}	PGOOD オン抵抗	V_{EN} = 0 V、200uA のプルアップ電流			100	Ω
スイッチング周波数						
f_{SYNC_RANGE}	SYNC によるスイッチング周波数範囲 (モード / 同期バリアント)		200		2500	kHz
f_{ADJ_RANGE}	R_T によるスイッチング周波数範囲 (R_T バリアント)		200		2200	kHz
f_{SW_RT1}	R_T によりプログラムされる 2.2MHz のスイッチング周波数	R_{RT}= 0kΩ (RT ピンを GND に接続)	2000	2200	2300	kHz
DeltaFc	内部発振器のスペクトラム拡散による周波数の増加 / 減少	DRSS (デュアル ランダム スペクトラム拡散)		±4%		
同期						
V_{MODE_L}	SYNC/MODE 入力電圧の Low レベル スレッショルド				1	V
V_{MODE_H}	SYNC/MODE 入力電圧の High レベル スレッショルド		1.6			V
t_{PULSE_H}	パルスとして認識されるのに必要な High の継続時間		100			ns
t_{PULSE_L}	パルスとして認識されるのに必要な Low の継続時間		100			ns
t_B	立ち上がりまたは立ち下がりエッジの後の EN のブランキング (1)		4		28	µs
t_{SYNC}	有効なクロック信号として認識されるための HIGH/LOW レベル パルスの最大期間				6	µs
電力段						
V_{BOOT_UVLO}	ハイサイド スイッチがオフになる CBOOT ピンの電圧 (SW 基準)			2.1		V
t_{ON_MIN}	最小 ON パルス幅(1)	FPWM モード、V_{OUT} = 1V、I_{OUT} = 1A		65	75	ns
t_{ON_MAX}	最大 ON パルス幅(1)	ドロップアウト時の HS タイムアウト	6	9	13	µs
t_{OFF_MIN}	最小 OFF パルス幅	V_{IN} = 4V、I_{OUT} = 1A		60	85	ns

(1) パラメータは、設計、統計分析、相関パラメータの製造試験によって規定されています。実製品の検査は行っていません。

6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V(R_{FBT} = 23.2 kΩ), V_{EN} = V_{IN}, F_{SW} = 1000 kHz, I_{OUT} = 0 A,PFM		6.9		µA
I_{IN}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 5 V(R_{FBT} = 40.2 kΩ), V_{EN} = V_{IN}, F_{SW} = 1000 kHz, I_{OUT} = 0 A,PFM		7		µA
OUTPUT VOLTAGE						
V_{FB}	Load regulation	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 0.4 A to full load(FPWM)		3		mV
V_{FB}	Line regulation	V_{OUT} = 3.3 V, V_{IN} = 4 V to 36 V, I_{OUT} = 2.5 A		10		mV
V_{OUT}	Load transient	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 1 A to 2.5 A @ 2 A/µs, $C_{OUT(derated)}$ = 32 uF		100		mV
EFFICIENCY						
η	Efficiency	V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 2.5 A, F_{SW} = 1 MHz		84		%
		V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, F_{SW} = 1 MHz		83		%
		V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, F_{SW} = 1 MHz		87		%
		V_{OUT} = 5 V, V_{IN} = 36 V, I_{OUT} = 2.5 A, F_{SW} = 1 MHz		86		%
η	Efficiency	V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 1.5 A, F_{SW} = 2 MHz		94		%
Thermal Shutdown						
T_{SDN}	Thermal shutdown threshold	Temperature rising	158	168	186	°C
T_{HYST}	Thermal shutdown hysteresis			15	20	°C

6.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C , V_{IN} = 13.5 V.

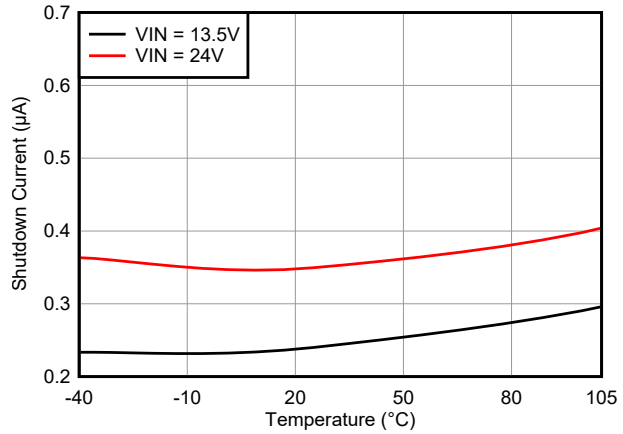


図 6-1. Shutdown Supply Current (I_{SDN_VIN}) Versus Temperature

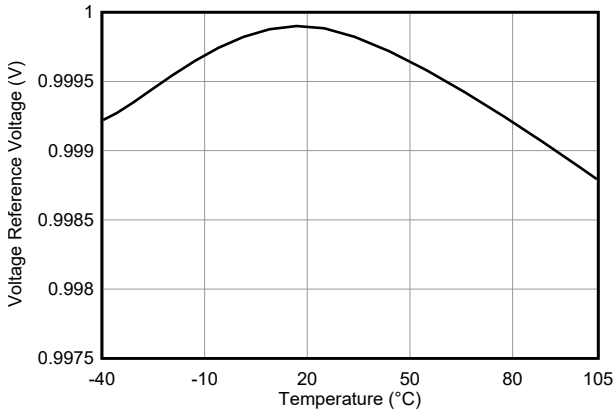


図 6-2. Feedback Voltage (V_{FB}) Accuracy Versus Temperature

7 Detailed Description

7.1 Overview

The TPSM336x5 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 36-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 36-V supply rails, as example. With an integrated buck controller, inductor, boot capacitor, and MOSFETs, the TPSM336x5 delivers up to 2.5-A DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

The TPSM336x5 can operate over a wide range of switching frequencies and duty ratios. If the minimum ON-time or OFF-time cannot support the desired duty ratio, the switching frequency gets reduced automatically, maintaining the output voltage regulation. In addition, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin or an external clock signal, the TPSM336x5 incorporates specific features to improve EMI performance in noise-sensitive applications:

- An optimized package that incorporates flip chip on lead (FCOL) technology and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Dual-Random Spread Spectrum (DRSS) modulation reduces peak emissions.
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range.
- Inductor and boot capacitor integration

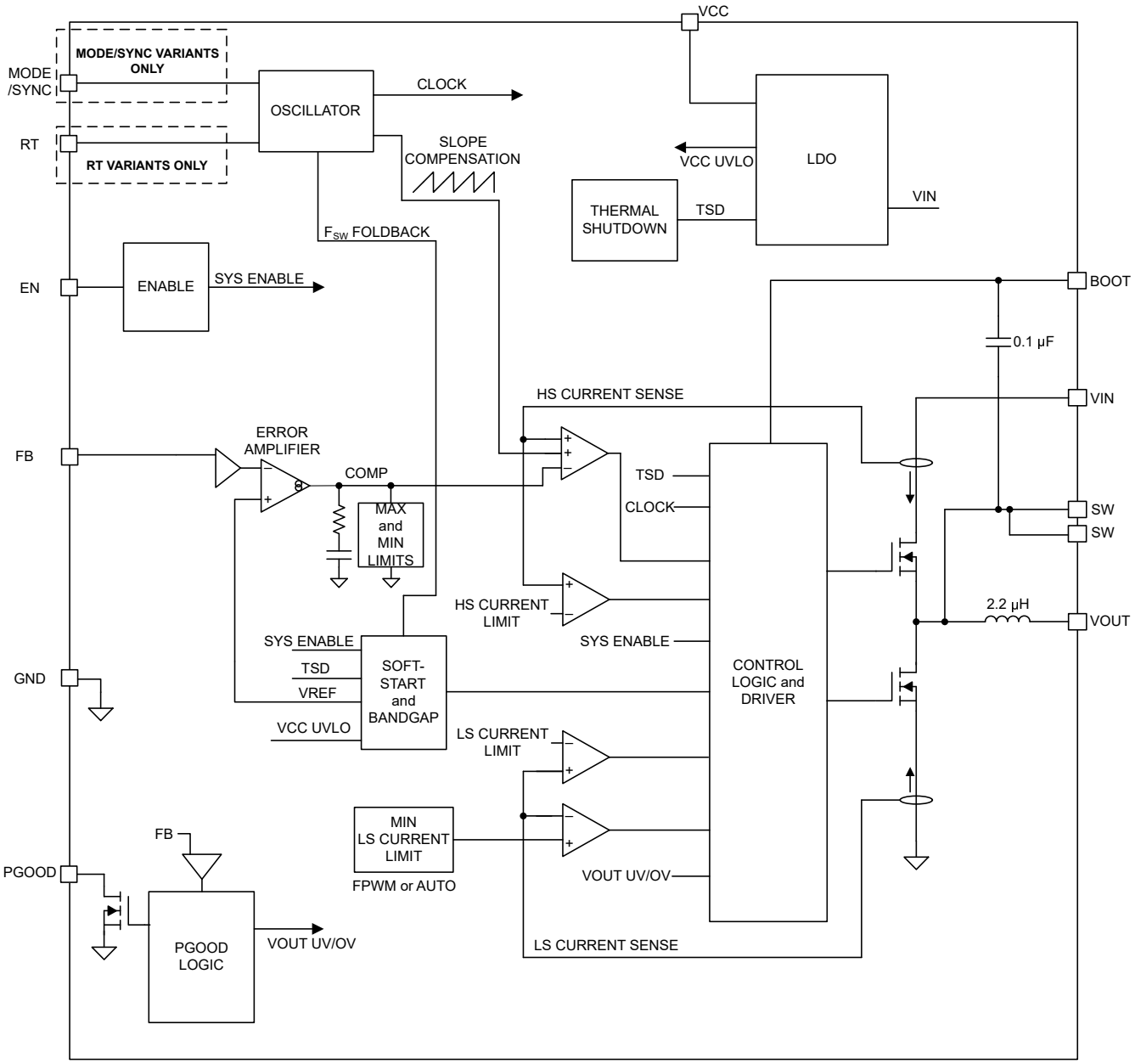
Together, these features can eliminate the need for any common-mode choke, shielding, and input filter inductor, greatly reducing the complexities and cost of the EMI/EMC mitigation measures.

The TPSM336x5 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing:
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for a simple layout, requiring few external components. See *Layout* for a layout example.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range

With a steady-state input voltage range from 3 V to 36 V, the TPSM336x5 module is intended for step-down conversions from typical 12-V to 36-V input supply rails, as example. The schematic circuit in 図 7-1 shows all the necessary components to implement a TPSM336x5-based buck regulator using a single input supply.

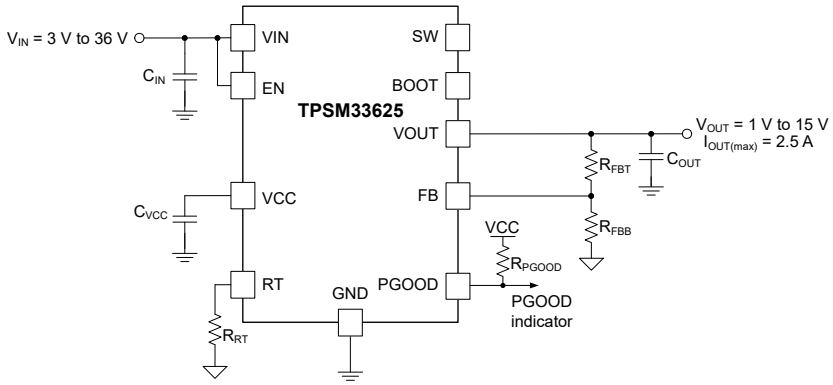


図 7-1. TPSM336x5 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

Take extra care to ensure that the voltage at the VIN pin does not exceed the absolute maximum voltage rating of 40 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

7.3.2 Output Voltage Selection

Adjustable Output Voltage Variants

The TPSM336x5 output voltage can be set by two external resistors, R_{FBT} and R_{FBB}. Connect R_{FBT} between VOUT at the regulation point and the FB pin. Connect R_{FBB} between the FB pin and AGND.

The TPSM336x5 has an adjustable output voltage range from 1.0 V to 15 V. To ensure that the power module regulates to the desired output voltage, the typical minimum value for the parallel combination of R_{FBT} and R_{FBB} is 5 kΩ while the typical maximum value is 10 kΩ as shown in 式 3. 式 2 and 式 3 can be used as a starting point to determine the value of R_{FBT}. Reference 表 7-1 for a list of acceptable resistor values for various output voltages.

$$5\ k\Omega\ <\ R_{FBT}\left|\right|R_{FBB}\ \leq 10\ k\Omega \tag{1}$$

$$\mathrm{R_{FBT}[k\Omega]} = \mathrm{R_{FBB}[k\Omega]} \times \left(\frac{\mathrm{V_{OUT}\,[V]}}{1\,\mathrm{V}} - 1\right) \tag{2}$$

$$\mathrm{R_{FBT}} \leq 10\ \mathrm{k\Omega} \times \frac{\mathrm{V_{OUT}}}{1\,\mathrm{V}} \tag{3}$$

For adjustable output options, an addition feedforward capacitor, C_{FF}, in parallel with the R_{FBT} can be needed to optimize the transient response. See *C_{FF} Selection* for additional information.

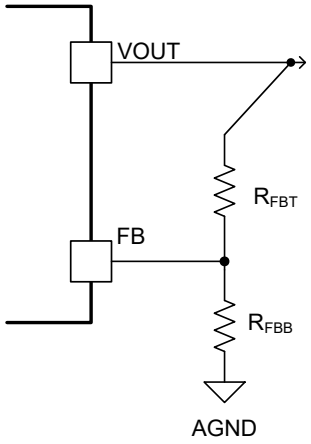


図 7-2. Setting Output Voltage for Adjustable Output Variant

表 7-1. Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)	V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	10	400	300	3.3	23.2	800	40
1.2	2	500	200	5.0	40.2	1000	25
1.5	4.99	500	160	7.5	64.9	1300	20
1.8	8.06	600	120	10	90.9	1500	15
2.0	10	600	100	12	110	2000	5
2.5	15	750	65	13	120	2200	5
3.0	20	750	50	15	140	2200	4

(1) R_{FBB} = 10 kΩ

7.3.3 Input Capacitors

Input capacitors are required to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. 式 4 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \times \left(I_{OUT}^2 \times (1 - D) + \frac{\Delta I_L^2}{12} \right)} \quad (4)$$

where

- $D = V_{OUT} / V_{IN}$ is the module duty cycle.

Ideally, the DC and AC components of the input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude ($I_{OUT} - I_{IN}$) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resulting capacitive component of the AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, 式 5 gives the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \quad (5)$$

式 6 gives the input capacitance required for a particular load current.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \quad (6)$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TPSM336x5 requires a minimum of a 4.7-µF ceramic type input capacitance. Only use high-quality ceramic type capacitors with sufficient voltage and temperature rating. The ceramic input capacitors provide a low impedance source to the power module in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. 表 7-2 includes a preferred list of capacitors by vendor.

表 7-2. Recommended Input Capacitors

VENDOR (1)	DIELECTRIC	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE RATING (V)	CAPACITANCE (µF) (2)
TDK	X7R	C3225X7R1H475K2 50AB	1210	50	4.7
Wurth	X7R	885012209048	1210	50	4.7
Murata	X5R	GRM155R61H104M E14D	0402	50	0.1
Chemi-Con	Electrolytic	EMVY500ADA101M HA0G	HA0	50	100

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.4 Output Capacitors

表 7-1 lists the TPSM336x5 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See 表 7-3 for a preferred list of output capacitors by vendor.

表 7-3. Recommended Output Capacitors

VENDOR (1)	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE (µF) (2)
TDK	X7R	CNA6P1X7R1E226M250AE	1210	25	22
TDK	X7R	CGA6P1X7R1C226 M250AC	1210	16	22
Wurth	X7R	885012209028	1210	25	10
Wurth	X7R	885012209014	1210	16	10

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.5 Enable, Start-Up, and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the TPSM336x5. The part stays shut down as long as the EN pin voltage is less than $V_{EN-WAKE}$.With the voltage at the EN pin greater than $V_{EN-WAKE}$, the device enters device standby mode and the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN-RISE}$, the device finally starts to switch, entering start-up mode with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN-RISE}$–$V_{EN-HYST}$), the regulator stops switching and re-enters device standby mode. Any further decrease in the EN pin voltage, below $V_{EN-WAKE}$, and the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the VIN input pin if remote precision control is not needed. The EN input pin must not be allowed to float.

The various EN threshold parameters and their values are listed in the *Electrical Characteristics*. 図 7-3 shows the precision enable behavior and 図 7-4 shows a typical remote EN start-up waveform in an application. After EN goes high, after a delay of about 1 ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 3.5 ms (t_{ss}). After a delay of about 2.5 ms ($t_{PG\_FLT\_RISE}$), the PGOOD flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN.

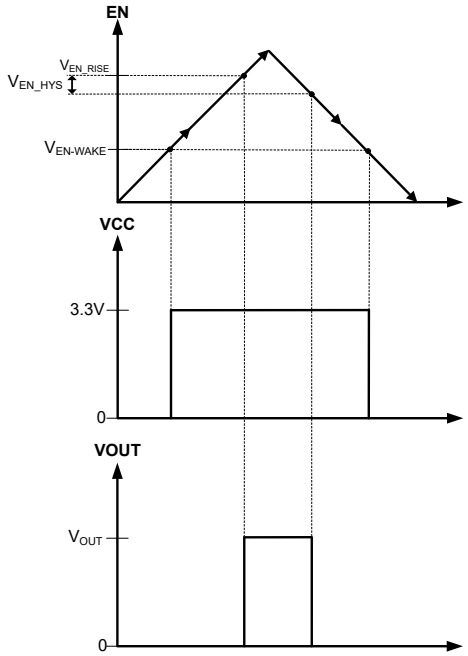


図 7-3. Precision Enable Behavior

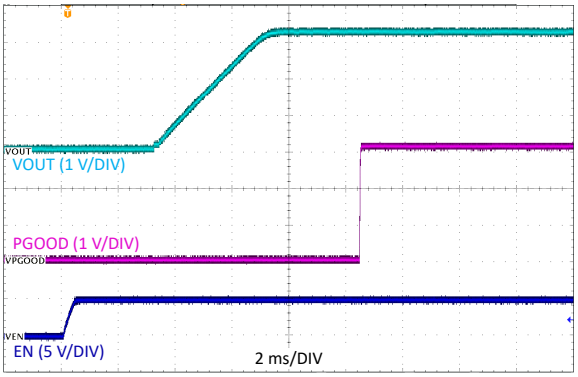


図 7-4. Enable Start-Up V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 2.5 A I_{OUT} = 1.5 A

External UVLO through EN Pin

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 図 7-5. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 式 7and 式 8 are used to calculate R_{ENT} and V_{OFF}, respectively.

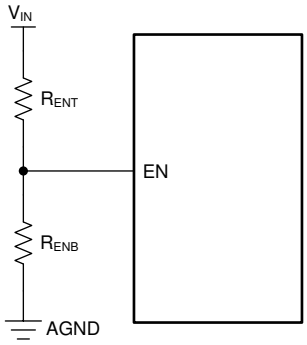


図 7-5. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN\_RISE}} - 1\right) \times R_{ENB} \quad (7)$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN\_HYS}}{V_{EN\_RISE}}\right) \quad (8)$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.
- Refer to electrical characteristics table for other terms.

7.3.6 External CLK SYNC (with MODE/SYNC)

Synchronizing the operation of multiple regulators in a single system, resulting in a well-defined system level performance is desirable. The select variants in the TPSM336x5 with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. An in-phase locking scheme where the rising edge of the clock signal, provided to the MODE/SYNC pin, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL) eliminating any large glitches. The external clock fed into the TPSM336x5 replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

The MODE/SYNC input pin in the TPSM336x5 can operate in one of three selectable modes:

- Auto Mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor.
- FPWM Mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current.
- SYNC Mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off-time or minimum on-time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, it operates as though in FPWM mode: diode emulation is disabled allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

7.3.6.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the device are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC pin control is useful with these systems. To initiate pulse-dependent MODE/SYNC pin control, a valid sync signal must be applied. 表 7-4 shows a summary of the pulse dependent mode selection settings.

表 7-4. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{MODE_H}	FPWM with spread spectrum factory setting
< V_{MODE_L}	Auto mode with spread spectrum factory setting
Synchronization Clock	SYNC mode

図 7-6 shows the transition between auto mode and FPWM mode while in pulse-dependent MODE/SYNC control. The device transitions to a new mode of operation after the time, t_{MODE}. 図 7-6 and 図 7-7 show the details.

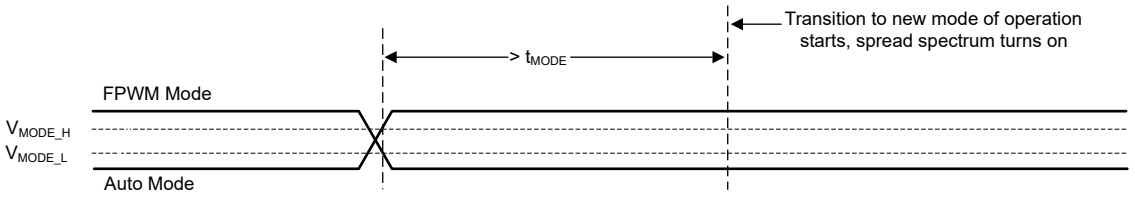


図 7-6. Transition from Auto Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the device enters either auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

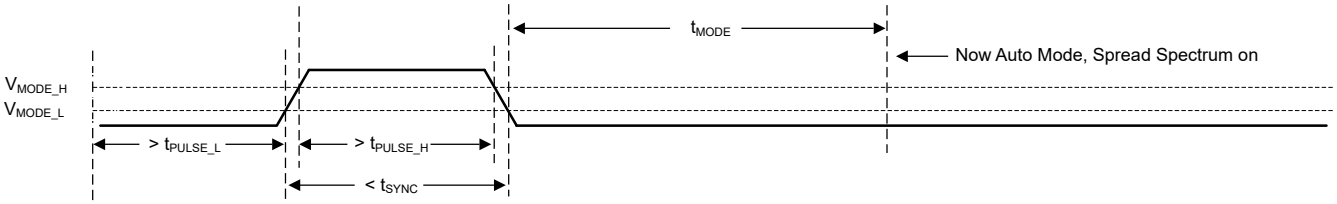


図 7-7. Transition from SYNC Mode to Auto Mode

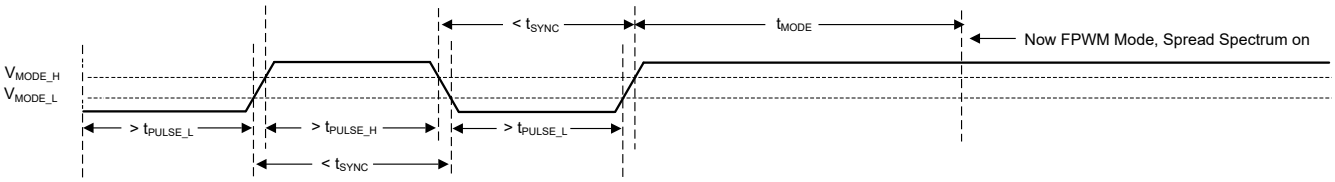


図 7-8. Transition from SYNC Mode to FPWM Mode

7.3.7 Switching Frequency (RT)

The select orderables in the TPSM336x5 family with the RT pin allow power designers to set any desired operating frequency between 200 kHz and 2.2 MHz in their applications. See 図 7-9 to determine the resistor value needed for the desired switching frequency or simply select from 表 7-6. The RT pin and the

MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal. See 表 7-5 for selection on programming the RT pin.

表 7-5. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT to GND	Adjustable according to 図 7-9
Float (Not Recommended)	No Switching

$$RT = \frac{18286}{Fsw^{1.021}} \quad (9)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency (kHz).

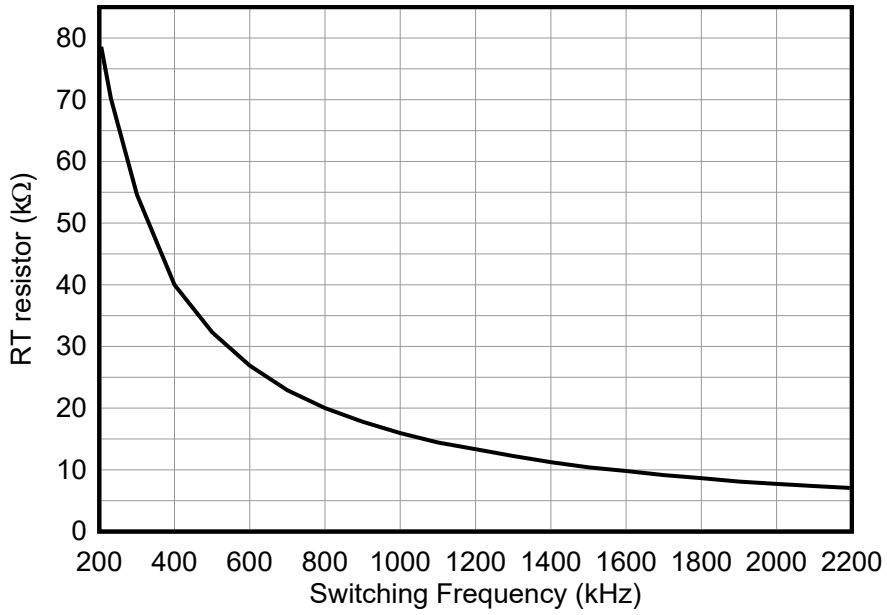


図 7-9. RT Values vs Frequency

The switching frequency must be selected based on the output voltage setting of the device. See 表 7-6 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

表 7-6. Switching Frequency Versus Output Voltage (I_{OUT} = 2.5 A)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
200	81.6	1	1.75	1	1.5	1	1.25	1	1.25
400	40.2	1	2	1	4	1	3	1.25	2.5
600	26.7	1	2.5	1	5	1.25	5	2	4
800	19.8	1	3	1	5.5	1.5	8	2.25	6
1000	15.8	1	3.5	1	6	2	11	2.5	8

表 7-6. Switching Frequency Versus Output Voltage (I_{OUT} = 2.5 A) (続き)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
1200	13.2	1	3.5	1.5	6.25	2.5	11	3	11
1400	11.3	1	3.5	1.5	6.5	3	11.5	3.5	15
1600	9.76	1	3.5	1.5	7	3	12	4	15
1800	8.66	1	3	1.5	7.5	3.5	12.5	5	15
2000	7.77	1	3	1.5	8	3.5	13	5.5	15
2200	7.06	1	3	1.5	8.5	4.5	14	6	15

7.3.8 Power-Good Output Operation

The power-good feature using the PGOOD pin of the TPSM336x5 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to 図 7-10. 表 7-7 gives a more detailed breakdown of the PGOOD operation. Here, $V_{PG_{UV}}$ is defined as the PG_{UV} scaled version of V_{OUT} (target regulated output voltage) and $V_{PG_{HYS}}$ as the PG_{HYS} scaled version of V_{OUT}, where both PG_{UV} and PG_{HYS} are listed in *Electrical Characteristics*. During the initial power up, a total delay of 6 ms (typical) is encountered from the time V_{EN_RISE} is triggered to the time that the power-good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power-good remains valid as long as the input voltage ($V_{IN\_PG\_VALID}$ is ≥ 1.5 V (max)).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

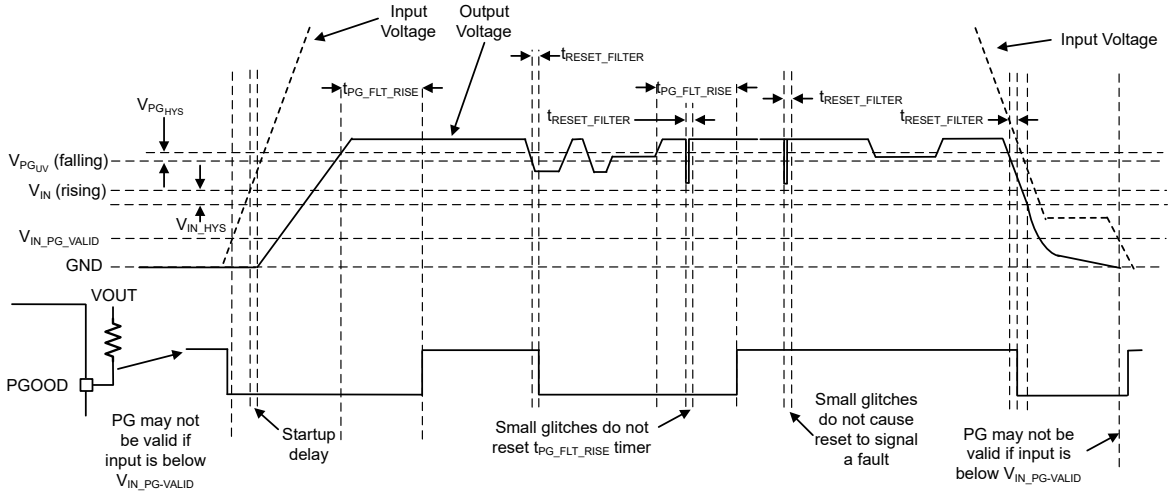


図 7-10. Power-Good Operation (OV Events Not Included)

表 7-7. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PG_{UV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PG_{UV}} + V_{PG_{HYS}} < V_{OUT} < V_{PG_{OV}} - V_{PG_{HYS}}$
$V_{OUT} > V_{PG_{OV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SDN}$	$T_J < T_{SDN}$-T_{HYST} AND output voltage in regulation
$EN < V_{EN\_RISE} - V_{EN\_HYS}$	$EN > V_{EN\_RISE}$ AND output voltage in regulation

7.3.9 Internal LDO, VCC and VOUT/FB Input

The TPSM336x5 uses the internal LDO output and the VCC pin for all internal power supply. The VCC rail typically measures 3.3 V. During start-up, VCC momentarily exceeds the normal operating voltage, then drops to the normal operating voltage.

7.3.10 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to ensure the HS switch is turned ON. There is an internal 0.1-µF capacitor connected between BOOT and SW that operates as a charge pump to boost the voltage on the BOOT terminal to (SW + VCC). The boot diode is integrated on the TPSM336x5 die to minimize physical solution size. The BOOT rail has an UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.1 V. If the BOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

7.3.11 Spread Spectrum

Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The TPSM336x5 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The TPSM336x5 uses a ±4% spread of frequencies which can spread energy smoothly across the FM and TV bands. The device implements dual random spread spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional pseudo-random jumps at the switching frequency

The advantage of DRSS is its equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This advantage reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the TPSM336x5 also allows the user to further reduce the output voltage ripple caused by the spread spectrum modulating pattern.

The spread spectrum is only available while the clock of the device is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on time reaches minimum on time. See the *Electrical Characteristics*.
- The clock is synchronized with an external clock.

7.3.12 Soft Start and Recovery from Dropout

When designing with the TPSM336x5, slow rise in output voltage due to recovery from dropout and soft start must be considered as a two separate operating conditions, as shown in 図 7-11 and 図 7-12. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection

After soft start is triggered, the power module takes the following actions:

- The reference used in the power module to regulate the output voltage is slowly ramped up. The net result is that output voltage, if previously 0 V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a pre-bias start-up.

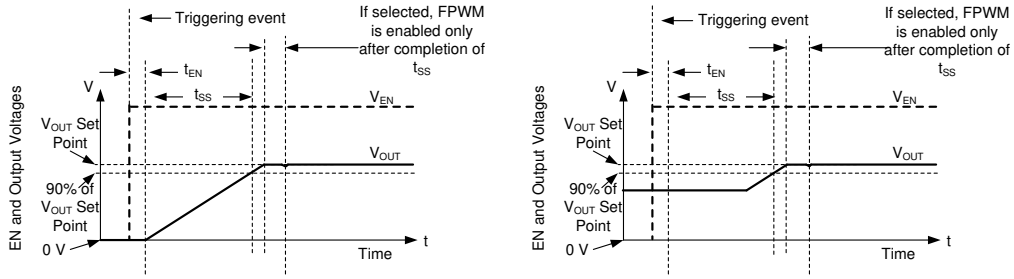


図 7-11. Soft Start With and Without Pre-bias Voltage

7.3.12.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device is set to FPWM, it continues to operate in that mode during its recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the TPSM336x5 can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

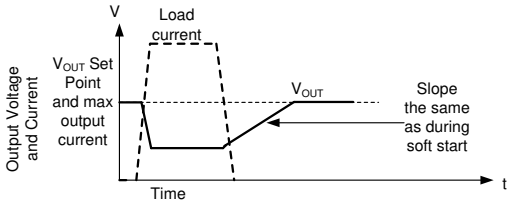


図 7-12. Recovery from Dropout

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below its set point is removed, the output climbs at the same speed as during start-up. 図 7-12 shows an example of this behavior.

7.3.13 Overcurrent Protection (Hiccup Mode)

The TPSM336x5 is protected from overcurrent conditions by using cycle-by-cycle current limiting circuitry on both the high-side (HS) and low-side (LS) MOSFETs. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases with reduced switching frequency.

High-side MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Because the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty cycle is above 35%.

When the LS switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device has a turn-off commanded by the internal error amplifier loop. In the case of the low-side device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

If, during current limit, the voltage on the FB input falls below about 0.4 V (V_{HICCUP}) due to a short circuit, the device enters hiccup mode. In this mode, the device stops switching for t_W or about 50 ms, and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 5 ms (typical) and then shuts down again. This cycle repeats as long as the short-circuit condition persists.

7.3.14 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 153°C (typical). When the junction temperature falls below 153°C (typical), the TPSM336x5 attempts another soft start.

While the TPSM336x5 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.7 V (typical), the power module does not have any output voltage and the device is in shutdown mode. In shutdown mode, the quiescent current drops to typically 250 nA.

7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output EN threshold. When the EN pin voltage is above 1 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3 V typical. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above its precision enable threshold. The TPSM336x5 also employs UVLO protection.

7.4.3 Active Mode

The TPSM336x5 is in active mode whenever the EN pin is above V_{EN_RISE}, V_{IN} is greater than V_{IN} (min), and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{IN} (min).

Depending on the load current, input voltage, and output voltage, the TPSM336x5 is in one of five modes:

- Continuous conduction mode (CCM) with fixed switching frequency (f_{SW}) when load current is above half of the inductor current ripple
- Auto mode - Light Load Operation: PFM where f_{SW} is decreased at very light load
- FPWM mode - Light Load Operation: Continuous conduction mode (CCM) when the load current is lower than half of the inductor current ripple
- Minimum on time: At high input voltage and low output voltages, the f_{SW} is reduced to maintain regulation
- Dropout mode: When f_{SW} is reduced to minimize voltage dropout

7.4.3.1 CCM Mode

The following operating description of the TPSM336x5 refers to *Functional Block Diagram*. In CCM, the TPSM336x5 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The buck module converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (10)$$

In an ideal buck module converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (11)$$

7.4.3.2 Auto Mode – Light-Load Operation

The TPSM336x5 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the TPSM336x5 operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

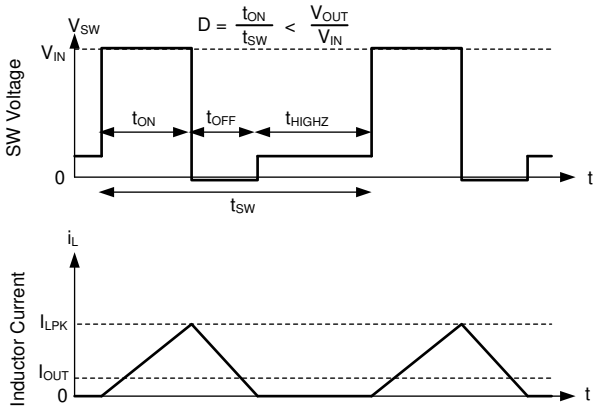
The light-load operation is employed in the TPSM336x5 only in auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation (See 図 7-13)
- Frequency reduction (See 図 7-14)

Note that while these two features operate together to improve light load efficiency, they operate independently of each other.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which potentially requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



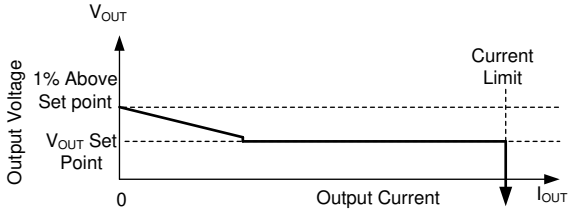
In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple can be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

図 7-13. PFM Operation

The TPSM336x5 has a minimum peak inductor current setting (see $I_{PEAKMIN}$ in セクション 6.5) while in auto mode. After current is reduced to a low value with fixed input voltage, on time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.3.2.2 Frequency Reduction

The TPSM336x5 reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of VOUT/FB and the voltage applied to VOUT/FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



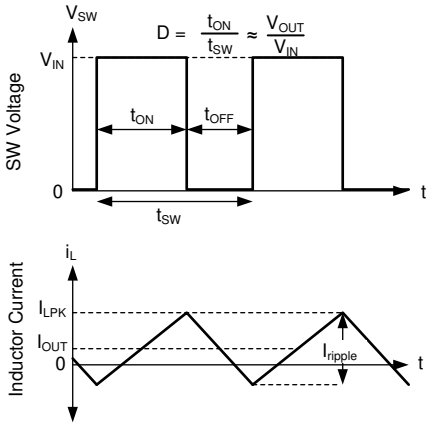
In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

図 7-14. Steady State Output Voltage Versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM mode can be used to reduce or eliminate this offset.

7.4.3.3 FPWM Mode – Light-Load Operation

In FPWM mode, frequency is maintained while the output is lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by negative current limit circuitry, see *セクション 6.5* for negative current limit values.



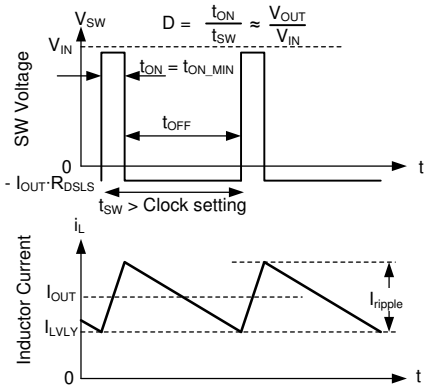
In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

図 7-15. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

7.4.3.4 Minimum On-Time (High Input Voltage) Operation

The TPSM336x5 continues to regulate output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the power module is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on time is fixed at its minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see 図 7-16.

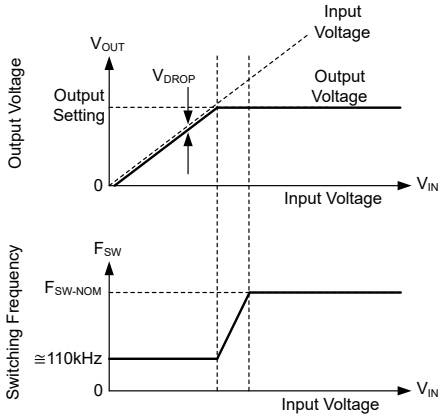


In valley control mode, minimum inductor current is regulated, not peak inductor current.

図 7-16. Valley Current Mode Operation

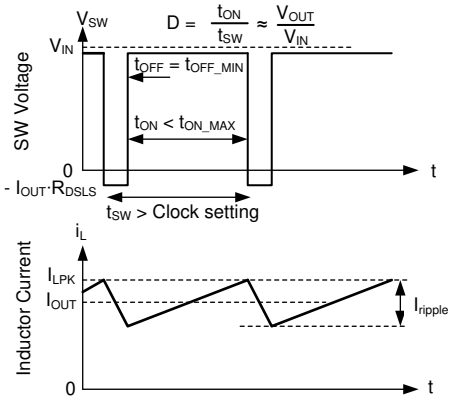
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off time. After this limit is reached as shown in 図 7-18 if clock frequency was to be maintained, the output voltage can fall. Instead of allowing the output voltage to drop, the TPSM336x5 extends the high-side switch on time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on time, t_{ON-MAX}, of approximately 9 µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off time, frequency drops to maintain regulation. As shown in 図 7-17, if input voltage is low enough so that output voltage cannot be regulated even with an on time of t_{ON-MAX}, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer to セクション 7.3.12.1.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

図 7-17. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON-MAX}.

図 7-18. Dropout Waveforms

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM336x5 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM336x5, WEBENCH online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM336x5 power module.

As mentioned previously, the TPSM336x5 also integrates several optional features to meet system design requirements, including precision enable, UVLO, and PGOOD indicator. The application circuit detailed below shows TPSM336x5 configuration options suitable for several application use cases. Refer to the *TPSM33625EVM, TPSM3365FEVM User's Guide* for more detail.

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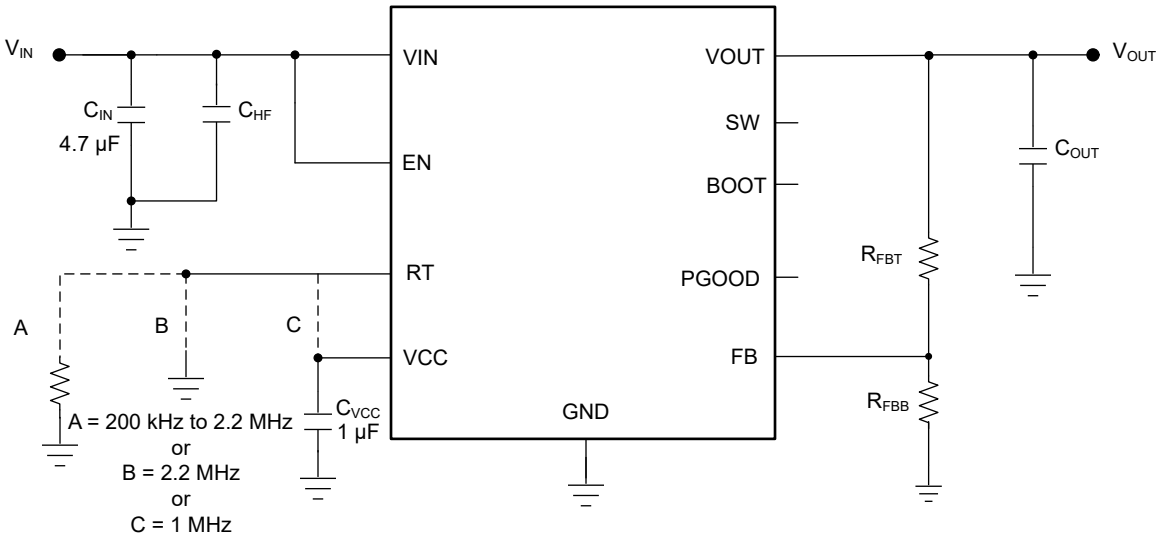
All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

図 8-1 shows a typical application circuit for the TPSM336x5. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of switching frequencies and output capacitance.



A. The RT pin is factory-set for externally adjustable switching frequency RT variants only. See *Switching Frequency (RT)* for details.

図 8-1. Example Application Circuit (TPSM336x5)

8.2.1 Design Requirements

Detailed Design Procedure provides instructions to design and select components according to 表 8-1.

表 8-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5.5 V to 36 V
Output voltage	5 V
Maximum output current	0 A to 2.5 A
Switching frequency	1 MHz

8.2.2 Detailed Design Procedure

The design procedure that follows and the resulting component selection is illustrated in 図 8-2.

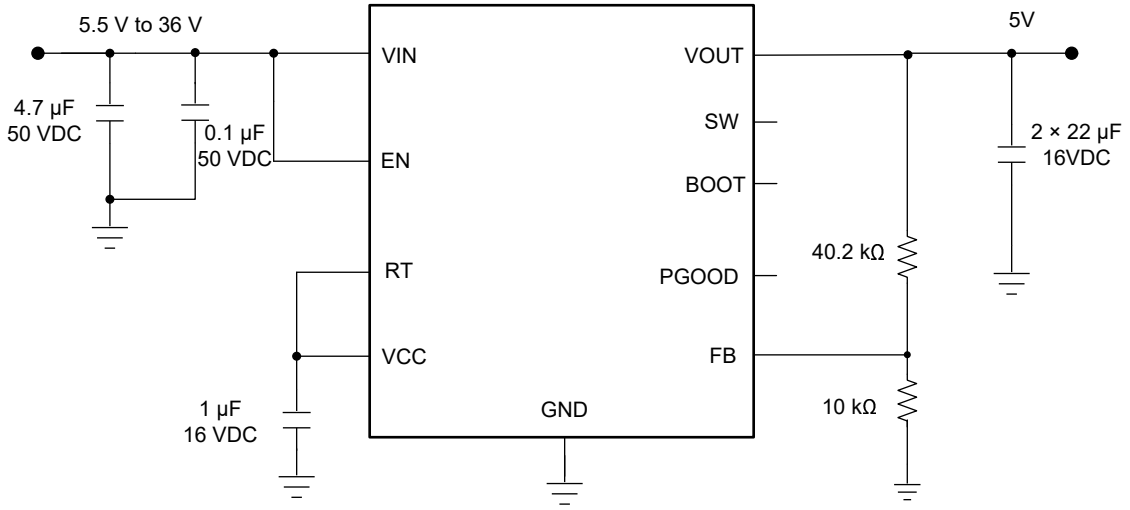


図 8-2. 5-V VOUT Design Example

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM336x5 devices with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial
3. Compare the generated design with other possible solutions from Texas Instruments. The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Choosing the Switching Frequency

The recommended switching frequency for standard output voltages can be found in 表 7-1. For a 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect the RT pin to VCC.

8.2.2.3 Setting the Output Voltage

The adjustable output voltage is externally set with a resistor divider. For more information on how to choose the feedback resistor values, please see *Output Voltage Selection*. The recommended value of R_{FBB} is 10 kΩ. For more information The value for R_{FBT} can be selected from 表 7-1 or calculated using 式 12:

$$R_{FBT}[k\Omega] = R_{FBB}[k\Omega] \times \left(\frac{V_{OUT}[V]}{1V} - 1 \right) \quad (12)$$

For the desired output voltage of 5 V, the formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

8.2.2.4 Input Capacitor Selection

The TPSM336x5 requires a minimum input capacitance of 4.7 µF. An additional 0.1 µF capacitor in parallel is recommended for improved bypassing. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage. For this design, a 4.7 µF and a 0.1 µF, 50 V rated capacitor are used.

It is often desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Refer to 表 7-2 for example input capacitor part numbers to consider.

8.2.2.5 Output Capacitor Selection

For a 5 V output, the TPSM336x5 requires a minimum of 25 µF effective output capacitance for proper operation (see 表 7-1). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

For this design example, select 2 x 22 µF, 16 V, 1210 case size, ceramic capacitors, which have a total effective capacitance of approximately 40 µF at 5 V. Review 表 7-3 for example output capacitor selection.

8.2.2.6 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1 µF, 16 V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see *Power-Good Output Operation*). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3 V; see *Electrical Characteristics* for limits.

8.2.2.7 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor application report* is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of C_{FF} must be limited to ensure that the desired output voltage is established when configuring for adjustable output voltages. 式 13 must be followed to ensure C_{FF} remains below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}}}{1.2 \times 10^{6}} \quad (13)$$

8.2.2.8 Power Good Signal

Applications requiring a power good signal to indicate that the output voltage is present and in regulation must use a pullup resistor between the PGOOD pin and a valid voltage source. This voltage source could be VCC or VOUT, as example.

8.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the TPSM336x5 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the power module above ambient. The internal die and inductor temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the module and PCB combination. The maximum junction temperature for the TPSM336x5 must be limited to 125°C. This establishes a limit on the maximum module power dissipation and, therefore, the load current. 式 14 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The power module efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. Lastly, safe-operation-area curves and module thermal captures developed through bench analysis on the EVM can be used to provide insights on the output power capability. These curves can be found in the *Application Curves* section of the data sheet.

As stated in the *Semiconductor and IC Package Thermal Metrics application report* the values given in *Thermal Information* section are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT,\,max} = \frac{\left(T_J - T_A\right)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{VOUT} \quad (14)$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ (TPSM33625EVM = 22°C/W) is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The IC Power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC resistance. The overall power loss can be approximated by using WEBENCH for a specific operating condition and temperature.

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight Application Report*

- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD™ Thermally Enhanced Package Application Report*
- *PowerPAD™ Made Easy Application Report*
- *Using New Thermal Metrics Application Report*
- *PCB Thermal Calculator*

8.2.2.10 Other Connections

- The RT pin can be connected to AGND for a switching frequency of 2.2 MHz or tied to VCC for a switching frequency of 1 MHz. A resistor connected between the RT pin and GND can be used to set the desired operating frequency between 200 kHz and 2.2 MHz.
- For the MODE/SYNC pin variant, connecting this pin to an external clock forces the device into SYNC operation. Connecting the MODE/SYNC pin low allows the device to operate in PFM mode at light load. Connecting the MODE/SYNC pin high puts the device into FPWM mode and allows full frequency operation independent of load current.
- A resistor divider network on the EN pin can be added for a precision input undervoltage lockout (UVLO)
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.
- A pullup resistor between the PGOOD pin and a valid voltage source to generate a power-good signal.

8.2.3 Application Curves

COUT = 2 × 22 uF (1210,16VDC)

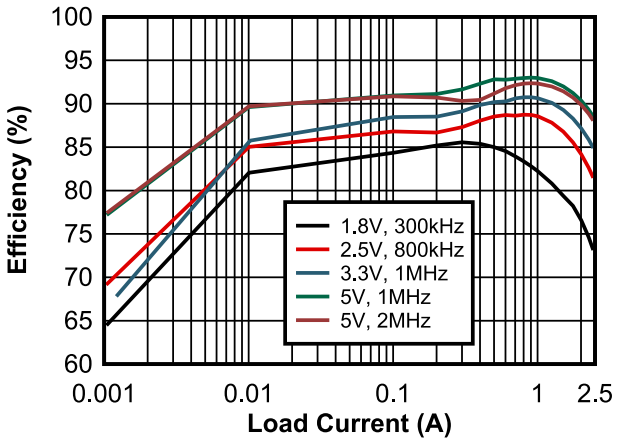


図 8-3. 12VIN Efficiency (Log)

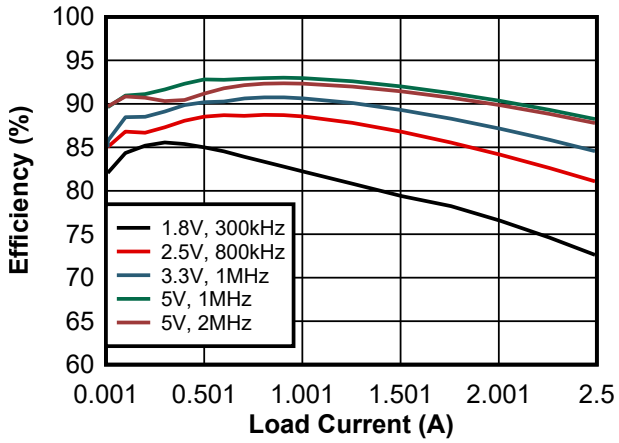


図 8-4. 12VIN Efficiency (Linear)

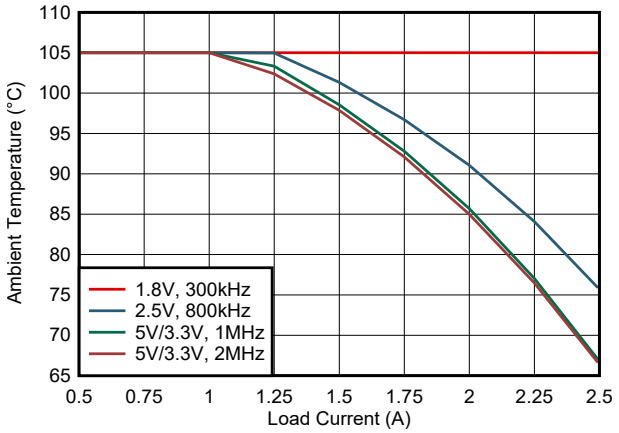


図 8-5. 12VIN: Max Ambient Temperature vs Load Current (Analysis on TPSM33625EVM)

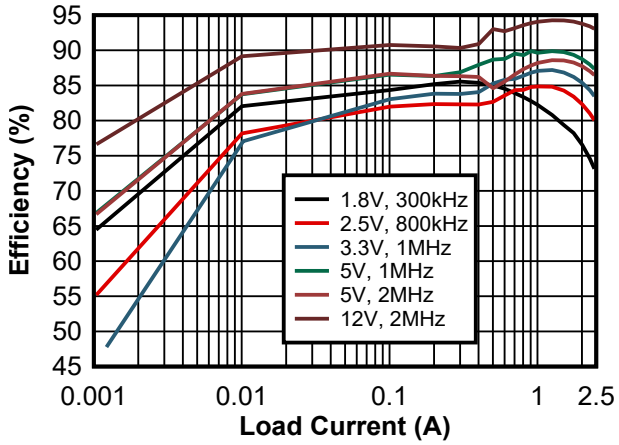


図 8-6. 24VIN Efficiency (Log)

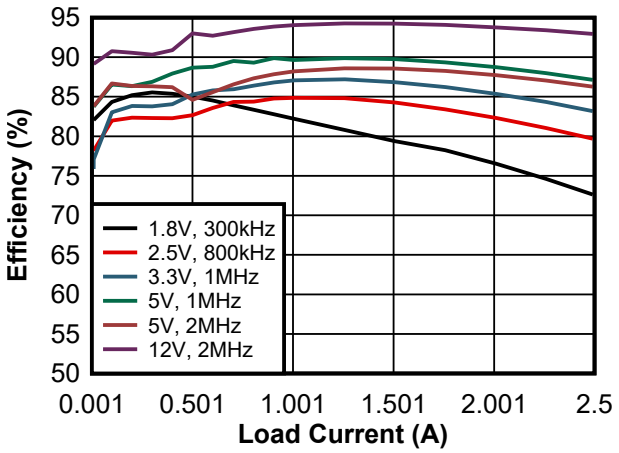


図 8-7. 24VIN Efficiency (Linear)

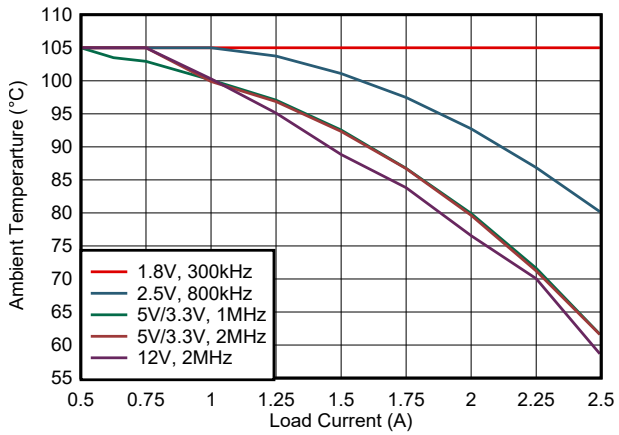


図 8-8. 24VIN: Max Ambient Temperature vs Load Current (Analysis on TPSM33625EVM)

8.2.3 Application Curves (continued)

COUT = 2 × 22 uF (1210,16VDC)

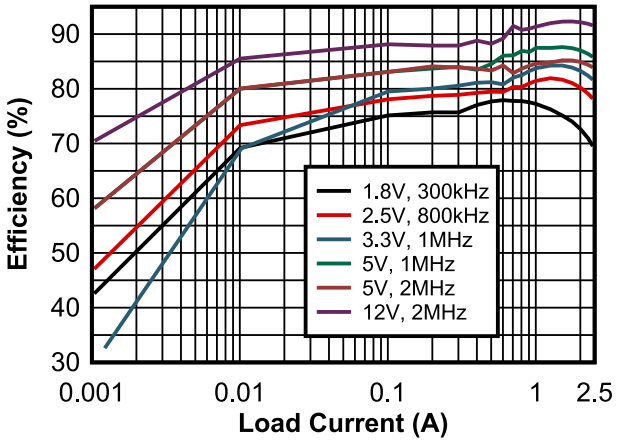


図 8-9. 36VIN Efficiency (Log)

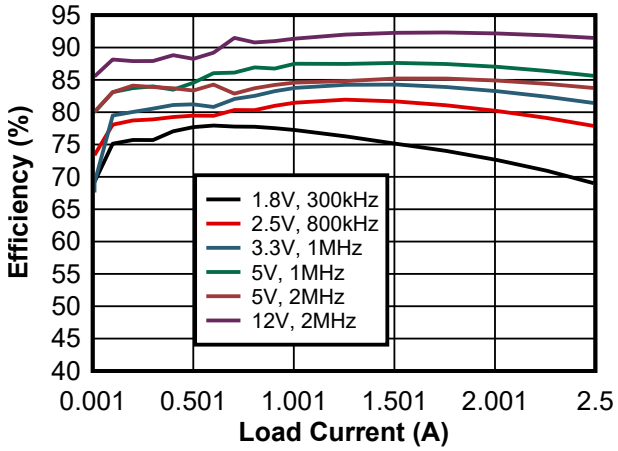


図 8-10. 36VIN Efficiency (Linear)

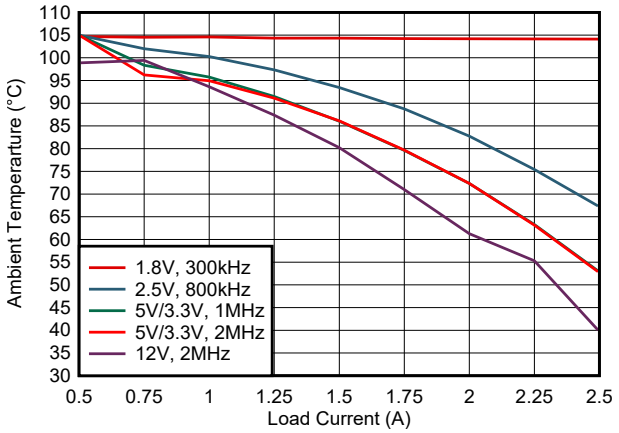
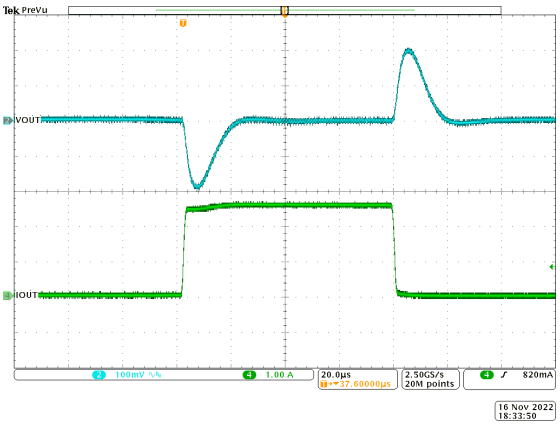


図 8-11. 36VIN: Maximum Ambient Temperature vs Load Current (Analysis on TPSM33625EVM)

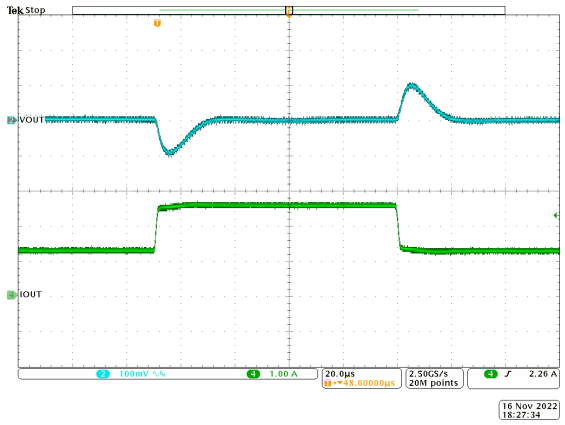


V_{IN} = 24 V
0 A to 2.5 A,1 A/µs

V_{OUT} = 5 V
COUT = 2 × 22 uF
(1210,16VDC)

1 MHz (FPWM)

図 8-12. Load Transient

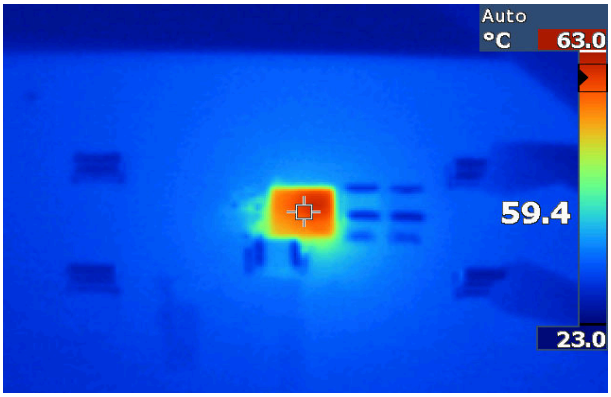


V_{IN} = 24 V
1.25 A to 2.5 A,1 A/µs

V_{OUT} = 5 V

1 MHz (FPWM)

図 8-13. Load Transient



V_{IN} = 12 V

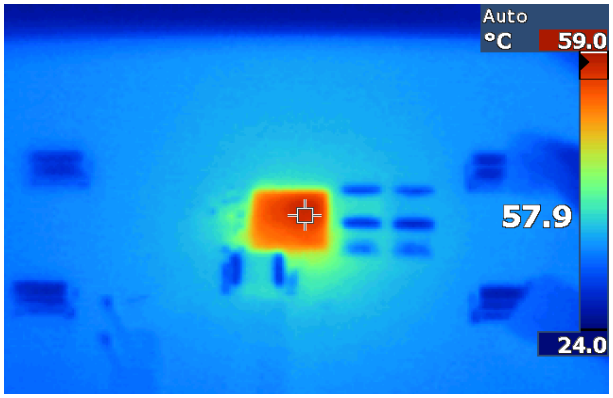
V_{OUT} = 3.3 V

2 A, 500 kHz

図 8-14. EVM Thermal Performance

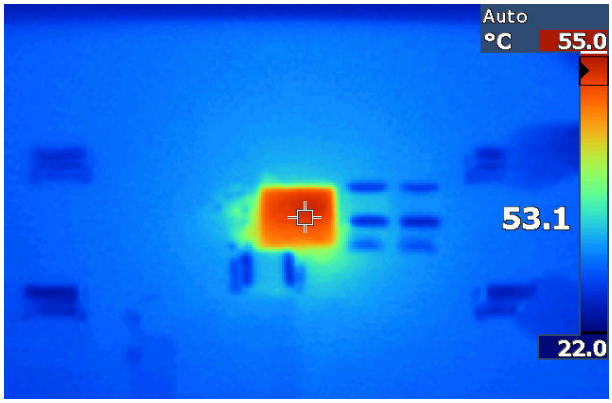
8.2.3 Application Curves (continued)

COUT = 2 × 22 uF (1210,16VDC)



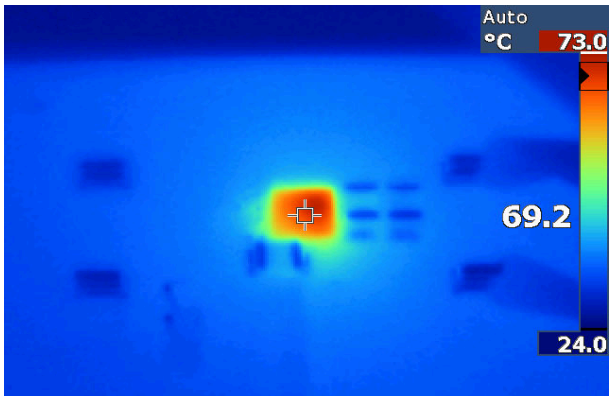
V_{IN} = 12 V V_{OUT} = 3.3 V 2 A, 1 MHz

図 8-15. EVM Thermal Performance



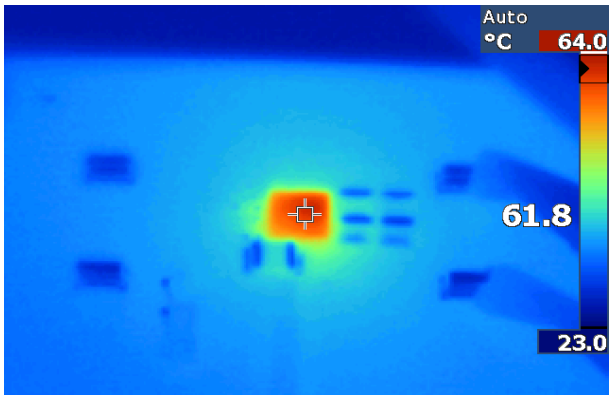
V_{IN} = 12 V V_{OUT} = 3.3 V 2 A, 2.2 MHz

図 8-16. EVM Thermal Performance



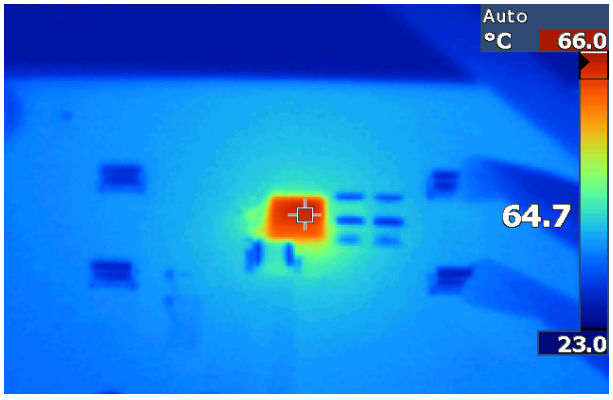
V_{IN} = 24 V V_{OUT} = 3.3 V 2 A, 500 kHz

図 8-17. EVM Thermal Performance



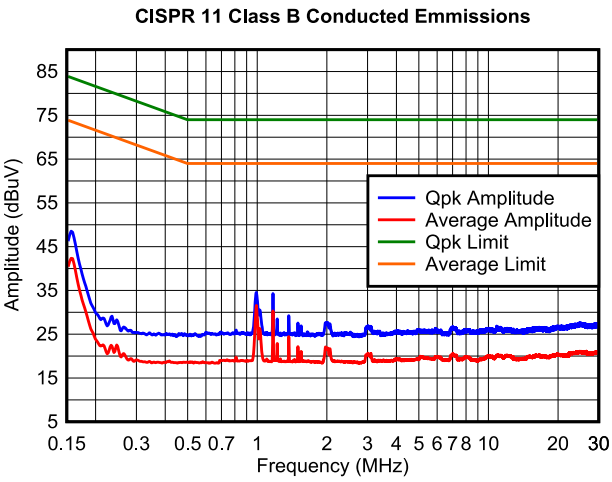
V_{IN} = 24 V V_{OUT} = 3.3 V 2 A, 1 MHz

図 8-18. EVM Thermal Performance



V_{IN} = 24 V V_{OUT} = 3.3 V 2 A, 2.2 MHz

図 8-19. EVM Thermal Performance

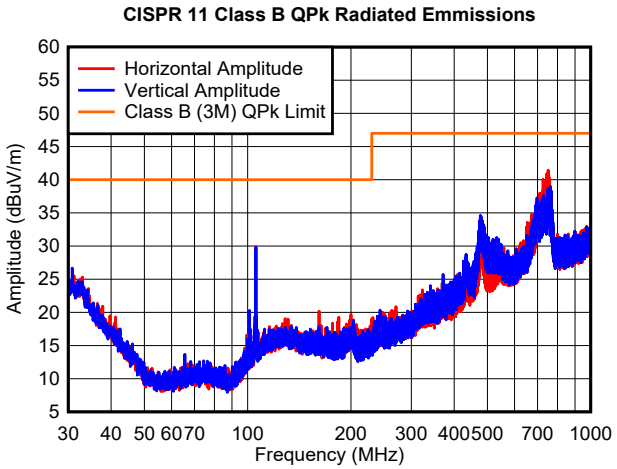


V_{IN} = 24 V V_{OUT} = 5 V Fsw = 1 MHz
Board = TPSM33625EVM Load = 2.5 A

図 8-20. CISPR 11, Class B, CE Scan 150 kHz–30 MHz

8.2.3 Application Curves (continued)

COUT = 2 × 22 uF (1210,16VDC)



V_{IN} = 24 V　　V_{OUT} = 5 V　　Fsw = 1 MHz

Board = TPSM33625EVM (No Filter)　　Load = 2.5 A

図 8-21. CISPR 11 RE, 3-Meter, Scan 30 MHz–1 GHz

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

8.4 Power Supply Recommendations

The TPSM336x5 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with 式 15.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (15)$$

where

- η is the efficiency

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

8.5 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

8.5.1 Layout Guidelines

The PCB layout of any DC/DC module is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the module regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter module, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 図 8-22. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the power module. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. *Layout Exmple* shows a recommended layout for the critical components of the TPSM336x5.

1. *Place the input capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
4. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
5. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the power module and maximizes efficiency.
6. *Provide enough PCB area for proper heat-sinking.* Sufficient amount of copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
7. *Use multiple vias* to connect the power planes to internal layers.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

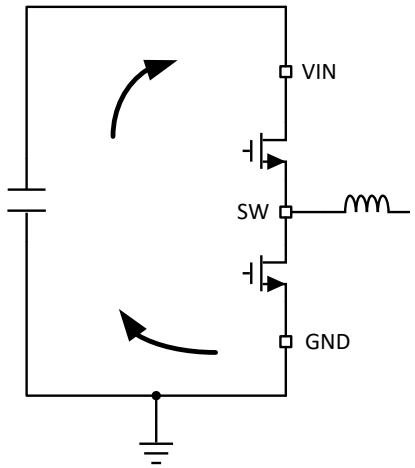


図 8-22. Current Loops with Fast Edges

8.5.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See 図 8-23 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting

from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

8.5.2 Layout Example

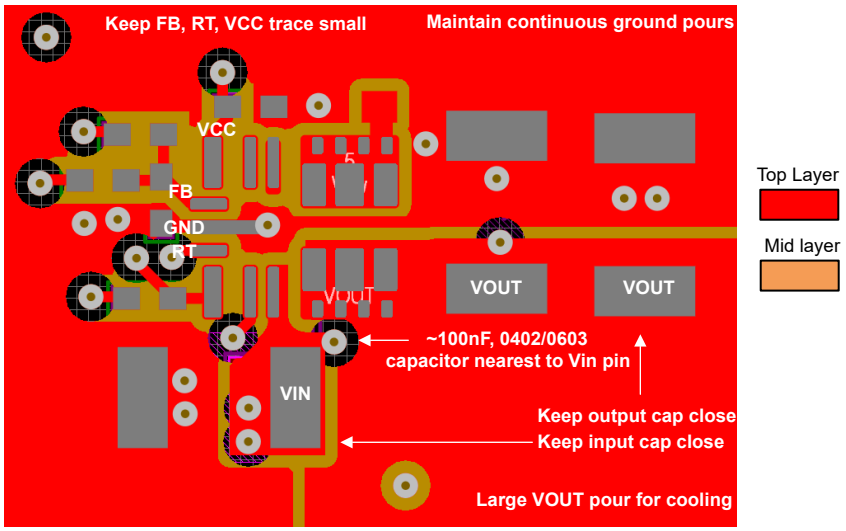


図 8-23. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM336x5 devices with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial
3. Compare the generated design with other possible solutions from Texas Instruments. The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.1.3 Device Nomenclature

図 9-1 shows the device naming nomenclature of the TPSM336x5. See セクション 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E support forum for detail and availability of other options; minimum order quantities apply.

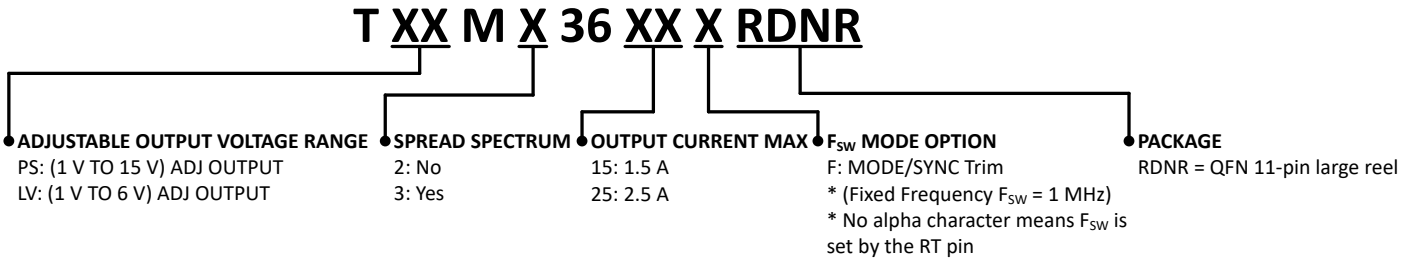

図 9-1. Device Naming Nomenclature

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight Application Report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package Application Report*
- Texas Instruments, *PowerPAD™ Made Easy Application Report*

- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies Application Report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines Application Report*
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (March 2023) to Revision C (February 2024)	Page
• TPSM365R15 をピン互換デバイスとして追加	1
• 効率と出力電流との関係 V_{IN} = 24V 図の 1MHz データを更新	1
• Added MODE/SYNC pin definition	5
• Added absolute maximum rating for MODE/SYNC	6
• Added recommended operations conditions' test condition, TPSM33625/TPSM33615, for output current specification	6
• Changed system characteristics' efficiency specification from 86%, 84%, 88%, 86%, and 95% to 84%, 83%, 87%, 86%, and 94%. Deleted V_{LDOIN} test condition	6
• Changed 表 7-1, 1 Vout, R_{FBT} = 10kΩ from short	14
• Added web link to the WEBENCH Design Center	32
• Updated 式 14 to have V_{OUT} term from h	34
• Updated 1MHz data for 図 8-3, 図 8-4, 図 8-6, 図 8-7, 図 8-9, and 図 8-10	36

- Added web link to the WEBENCH Design Center....43

Changes from Revision A (January 2023) to Revision B (March 2023) **Page**

- ドキュメントに TPSM33615 を追加....1
- Removed TLVM23625 from the orderable part numbers....4
- Added new orderable part numbers....4

Changes from Revision * (December 2022) to Revision A (January 2023) **Page**

- Added TLVM23625 to the orderable part numbers....4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM33615FRDNR	ACTIVE	QFN-FCMOD	RDN	11	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33615F	Samples
TPSM33615RDNR	ACTIVE	QFN-FCMOD	RDN	11	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33615	Samples
TPSM33625FRDNR	ACTIVE	QFN-FCMOD	RDN	11	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33625F	Samples
TPSM33625RDNR	ACTIVE	QFN-FCMOD	RDN	11	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33625	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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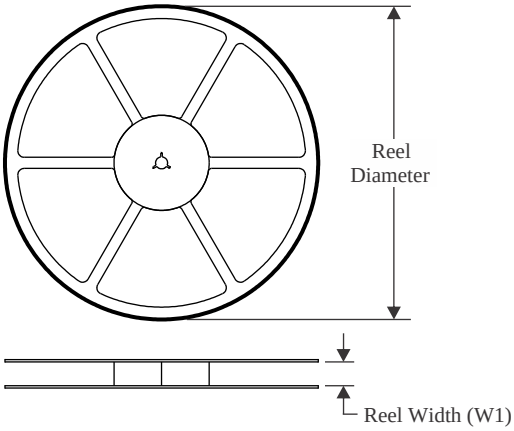
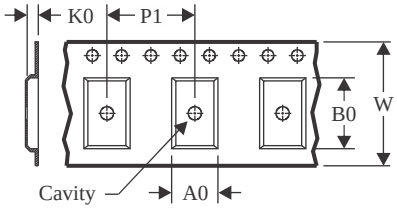
TAPE AND REEL INFORMATION

REEL DIMENSIONS

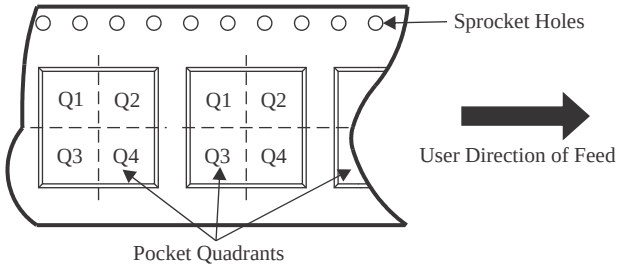


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

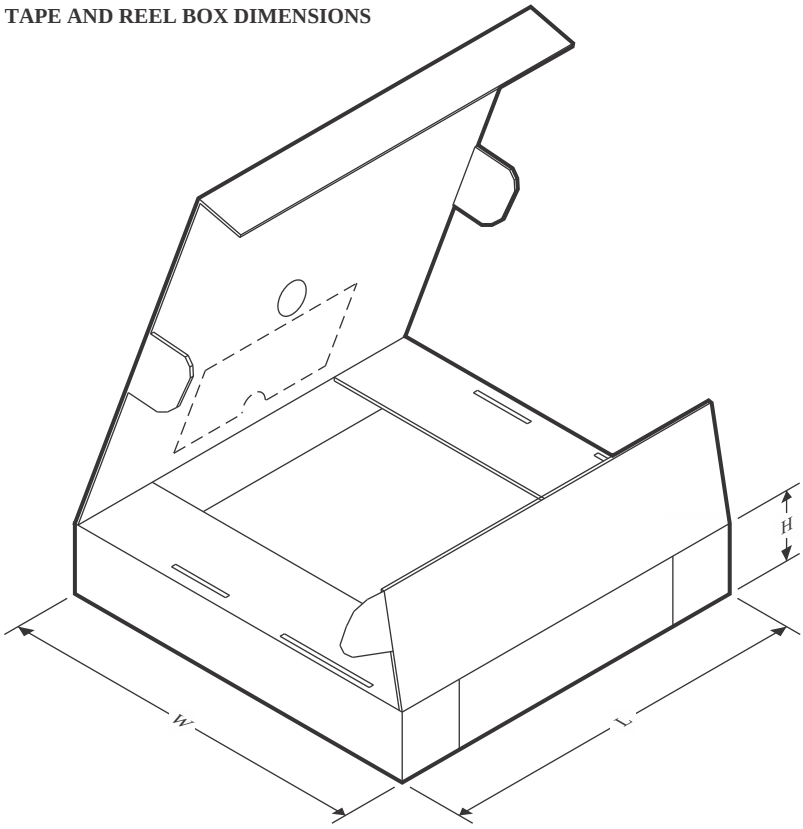
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM33615FRDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM33615RDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM33625FRDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM33625RDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

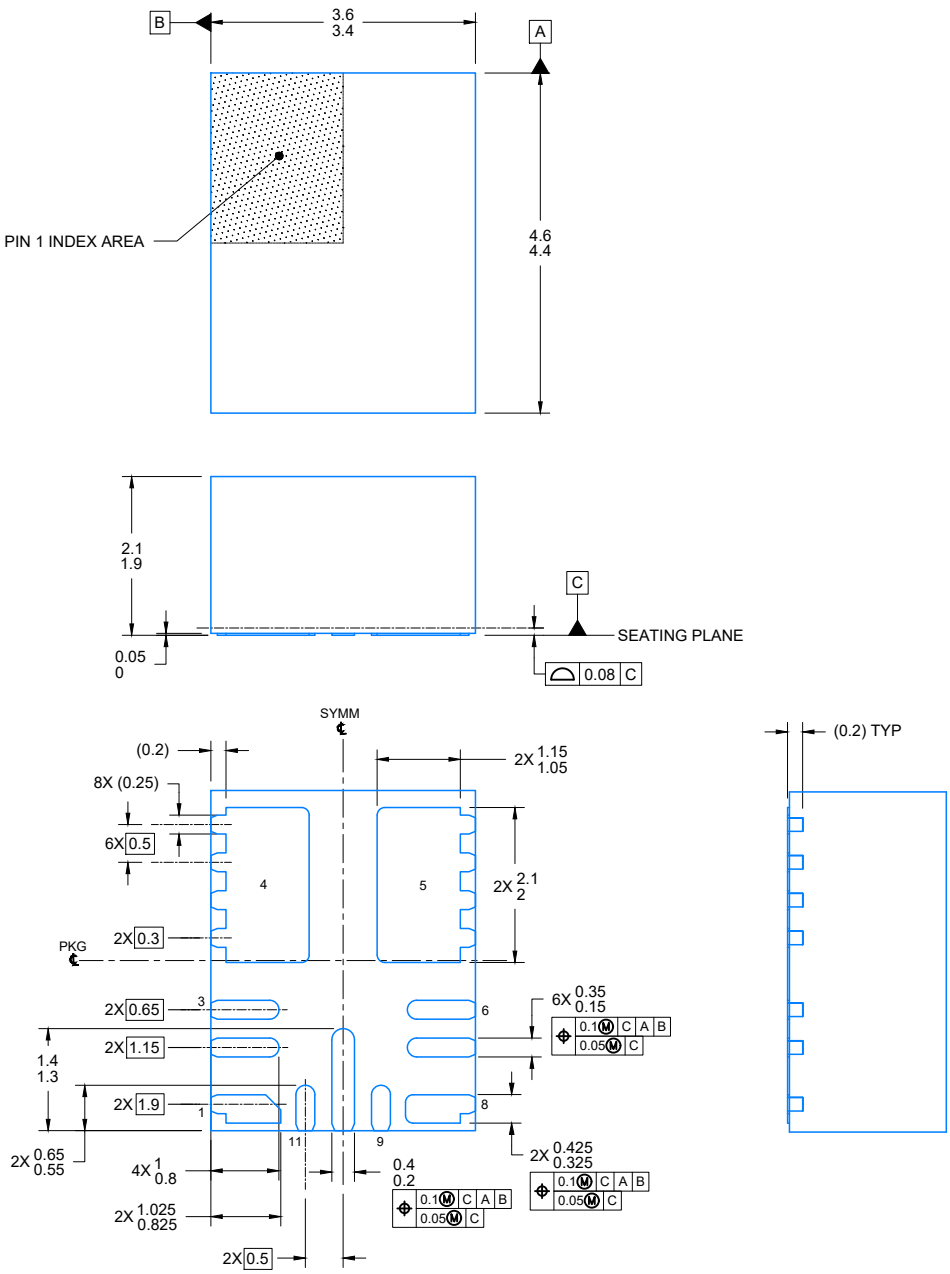
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM33615FRDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM33615RDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM33625FRDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM33625RDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDN0011A

QFN-FCMOD - 2.1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



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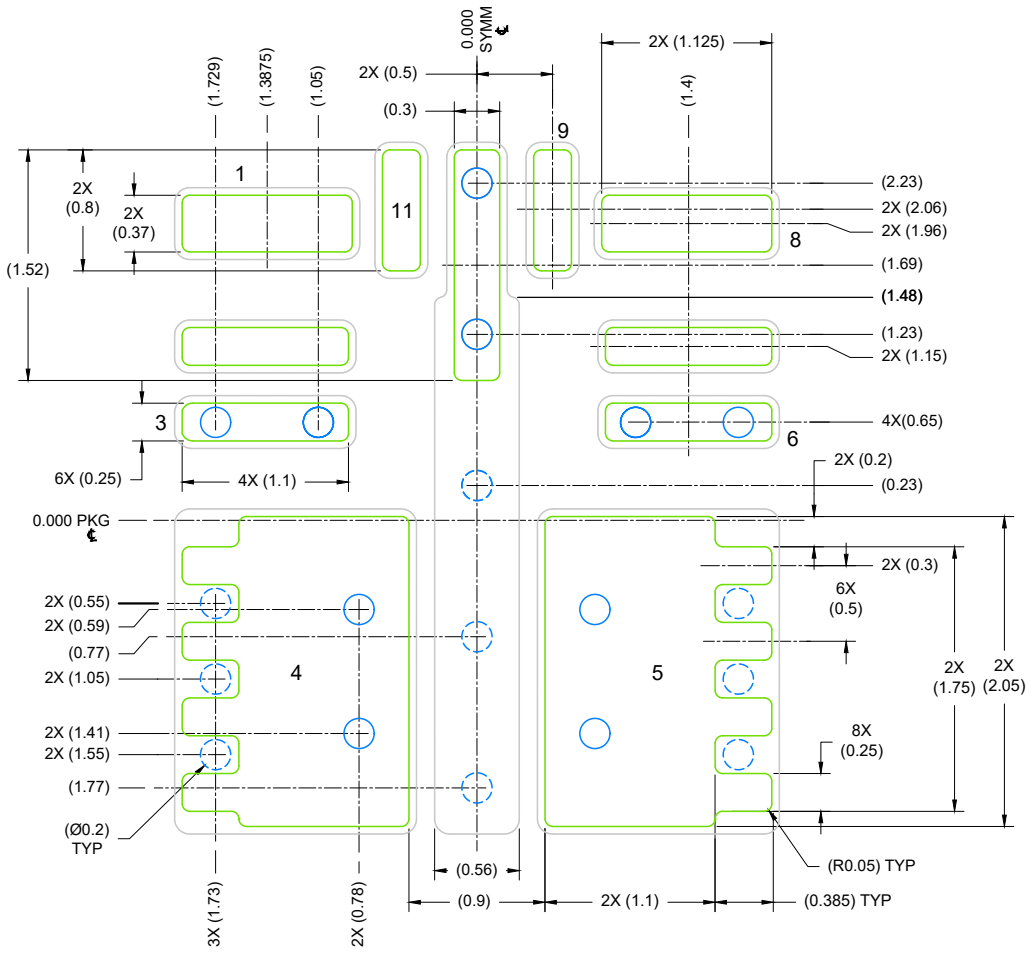
NOTES:

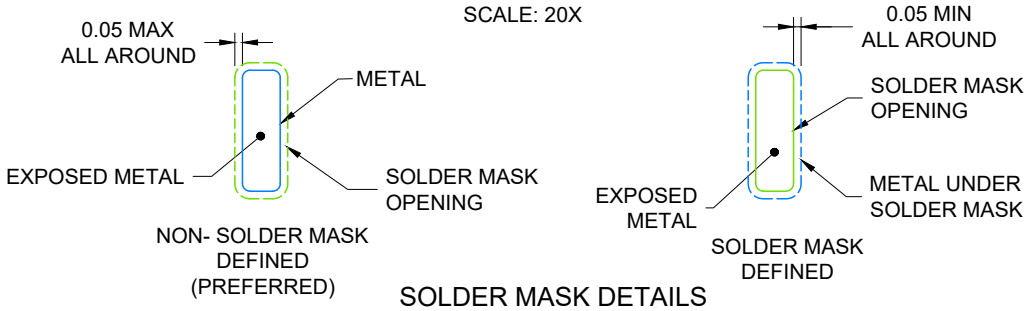
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



SOLDER MASK DETAILS

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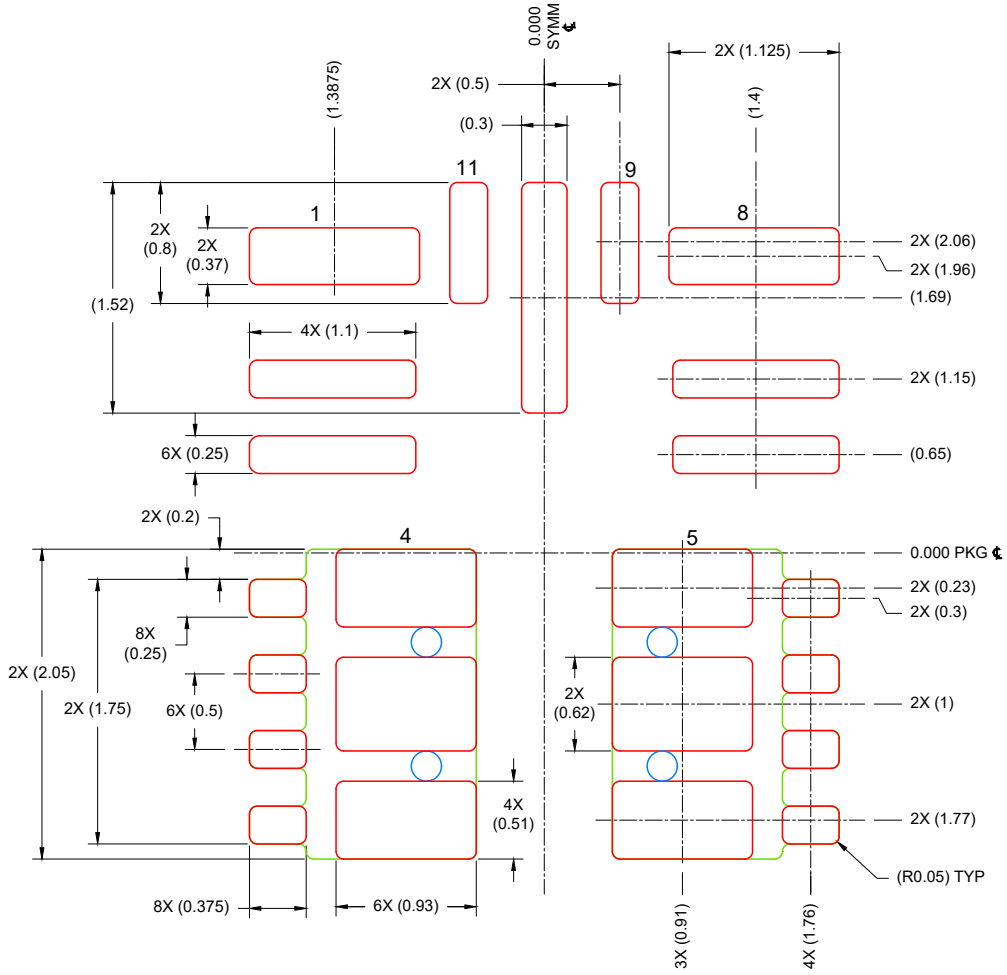
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PIN 4 & 5:
72% SOLDER COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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