

# TUSB522P 3.3V、デュアル・チャネル、USB 3.1 GEN1 リドライバ、イコライザ

## 1 特長

- 3.3V 電源搭載、USB3.1 Gen1、5Gbps、デュアル・チャネル・リドライバ
- 超低消費電力アーキテクチャ:
  - アクティブ: 98mA
  - U2、U3: 1.2mA
  - 切断時: 265μA
  - シャットダウン時: 60μA
- 最適なレシーバ・イコライゼーション:
  - 2.5GHz で 3、6、9dB
- 出力ドライバのディエンファシス: 0、3.5、6dB
- 自動的な LFPS ディエンファシス制御により USB 3.1 の認定要件に合致
- ホスト側またはデバイス側の要件なし
- ホットプラグ対応
- 工業用温度範囲: -40°C ~ 85°C (TUSB522PI)
- 商業用温度範囲: 0°C ~ 70°C (TUSB522P)

## 2 アプリケーション

- 携帯電話
- タブレット
- ノート PC
- デスクトップ PC
- ドッキング・ステーション
- バックプレーンとアクティブ・ケーブル

## 3 概要

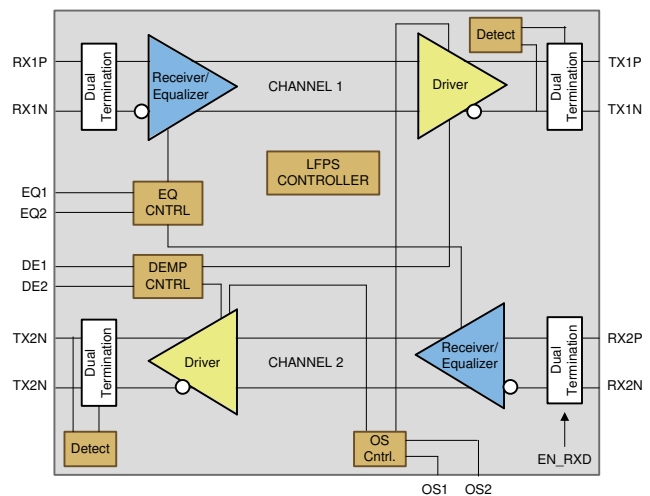
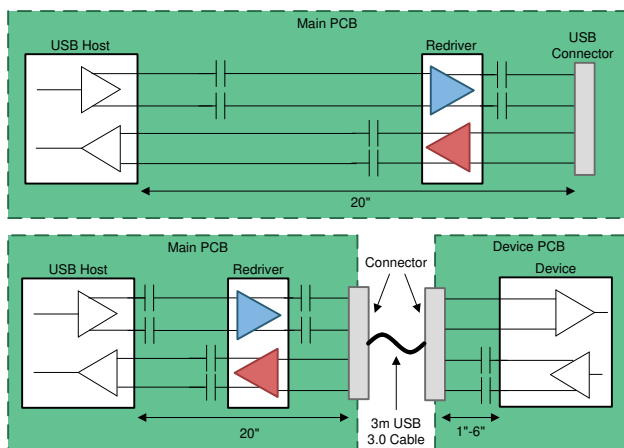
TUSB522P は、5Gbps をサポートする、第 4 世代、デュアル・チャネル、シングル・レーンの USB 3.1 GEN1 リドライバおよびシングル・コンディショナです。このデバイスは超低電力アーキテクチャにより 3.3V 電源で動作し、低消費電力を実現します。USB 3.1 の低電力モードをサポートしているため、アイドル時の消費電力をさらに減らすことができます。

デュアル・チャネル機能により、システムは送信および受信の両方のデータパスで信号の整合性を維持できます。レシーバのイコライゼーションには 3 つのゲイン設定があり、挿入損失やシンボル間干渉によるチャネルの劣化を克服できます。これらの設定は EQ ピンから制御されます。伝送ライン損失を補償するため、出力ドライバはピン DE によるディエンファシスの構成をサポートしています。さらに、自動的な LFPS ディエンファシス制御により、完全な USB 3.1 準拠が可能になります。これらの設定により、最適な性能が実現され、信号の距離が延長され、TUSB522P を USB 3.1 GEN1 のパス内に柔軟に配置できます。

### 製品情報

| 部品番号      | 温度                            | パッケージ <sup>(1)</sup> |
|-----------|-------------------------------|----------------------|
| TUSB522P  | T <sub>A</sub> = 0°C ~ 70°C   | RGE (VQFN, 24)       |
| TUSB522PI | T <sub>A</sub> = -40°C ~ 85°C |                      |

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



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### 概略回路図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

|                                                                                                                                                                                                           |             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision D (May 2019) to Revision E (November 2023)</b>                                                                                                                                   | <b>Page</b> |
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....                                                                                                                                                                      | <b>1</b>    |
| • 周囲温度を含めるよう「製品情報」表を更新 .....                                                                                                                                                                              | <b>1</b>    |
| • In the <i>Pin Functions</i> table deleted "Note: When OS = low." for both DE1 and DE2. ....                                                                                                             | <b>3</b>    |
| • In <i>Recommended Operation Conditions</i> , changed C <sub>AC-USB1</sub> max from 200 nF to 265 nF.....                                                                                                | <b>5</b>    |
| • Reformat Table 7-1 for readability.....                                                                                                                                                                 | <b>11</b>   |
| • Updated Figure 8-1 to include C <sub>AC-USB1</sub> , C <sub>AC-USB2</sub> , L <sub>AB</sub> , L <sub>CD</sub> , L <sub>AC-CAP</sub> , L <sub>ESD</sub> , R <sub>ESD</sub> , and R <sub>RX</sub> , ..... | <b>12</b>   |
| • Added comment that ac-capacitor should be placed between ESD and USB receptacle when designing for short to VBUS protection.....                                                                        | <b>12</b>   |
| • Updated the <i>Design Parameters</i> table to include pre-channel and post-channel min/max limits.....                                                                                                  | <b>13</b>   |
| • Added the <i>ESD Protection</i> section.....                                                                                                                                                            | <b>14</b>   |
| <b>Changes from Revision C (May 2019) to Revision D (May 2019)</b>                                                                                                                                        | <b>Page</b> |
| • Changed pin 11 From: TX1N To: TX2N and pin 12 From: TX1P To: TX2P in Figure 8-2.....                                                                                                                    | <b>13</b>   |
| <b>Changes from Revision B (November 2017) to Revision C (May 2019)</b>                                                                                                                                   | <b>Page</b> |
| • Deleted the RGE0024F mechanical pages.....                                                                                                                                                              | <b>17</b>   |
| <b>Changes from Revision A (October 2016) to Revision B (November 2017)</b>                                                                                                                               | <b>Page</b> |
| • Changed the values in the FOR OS = HIGH column of Table 7-1 to match FOR OS = LOW column. ....                                                                                                          | <b>11</b>   |
| <b>Changes from Revision * (July 2016) to Revision A (October 2016)</b>                                                                                                                                   | <b>Page</b> |
| • デバイスのステータスを「プレビュー」から「量産」に変更.....                                                                                                                                                                        | <b>1</b>    |

## 5 Pin Configuration and Functions

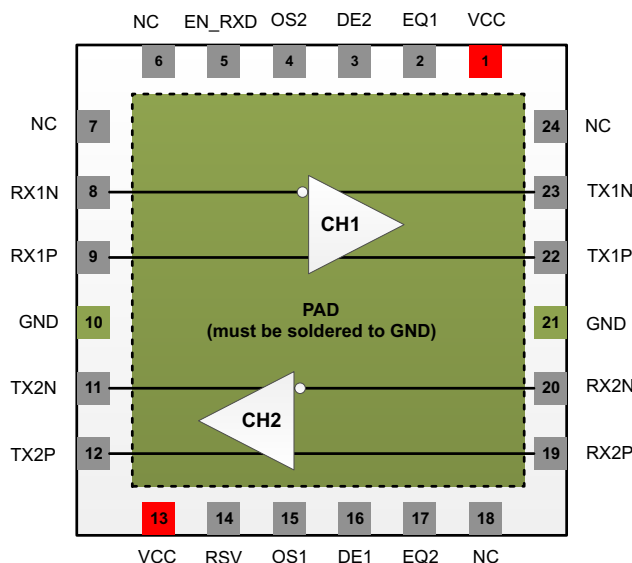


図 5-1. RGE Package, 24-Pin (VQFN) (Top View)

表 5-1. Pin Functions

| PIN  |     | I/O            | DESCRIPTION                                                                                                                                                                  |
|------|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NO. |                |                                                                                                                                                                              |
| RX1N | 8   | Differential I | Differential input for 5Gbps negative signal on Channel 1                                                                                                                    |
| RX1P | 9   | Differential I | Differential input for 5Gbps positive signal on Channel 1                                                                                                                    |
| TX1N | 23  | Differential O | Differential output for 5Gbps negative signal on Channel 1                                                                                                                   |
| TX1P | 22  | Differential O | Differential output for 5Gbps positive signal on Channel 1                                                                                                                   |
| RX2N | 20  | Differential I | Differential input for 5Gbps negative signal on Channel 2                                                                                                                    |
| RX2P | 19  | Differential I | Differential input for 5Gbps positive signal on Channel 2                                                                                                                    |
| TX2N | 11  | Differential O | Differential output for 5Gbps negative signal on Channel 2                                                                                                                   |
| TX2P | 12  | Differential O | Differential output for 5Gbps positive signal on Channel 2                                                                                                                   |
| EQ1  | 2   | I, CMOS        | Sets the receiver equalizer gain for Channel 1. 3-state input with integrated pull-up and pull-down resistors.<br>EQ1 = Low = 3 dB<br>EQ1 = Mid = 6 dB<br>EQ1 = High = 9 dB  |
| DE1  | 16  | I, CMOS        | Sets the output de-emphasis for Channel 1. 3-state input with integrated pull-up and pull-down resistors.<br>DE1 = Low = 0 dB<br>DE1 = Mid = -3.5 dB<br>DE1 = High = -6.2 dB |
| OS1  | 15  | I, CMOS        | Sets the output swing (differential voltage amplitude) for Channel 1. 2-state input with an integrated pull down resistor.<br>OS1 = Low = 0.9 mV<br>OS1 = High = 1.1 mV      |
| EQ2  | 17  | I, CMOS        | Sets the receiver equalizer gain for Channel 2. 3-state input with integrated pull-up and pull-down resistors.<br>EQ2 = Low = 3 dB<br>EQ2 = Mid = 6 dB<br>EQ2 = High = 9 dB  |

表 5-1. Pin Functions (続き)

| PIN    |              | I/O     | DESCRIPTION                                                                                                                                                                                                                  |
|--------|--------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME   | NO.          |         |                                                                                                                                                                                                                              |
| DE2    | 3            | I, CMOS | Sets the output de-emphasis for Channel 2. 3-state input with integrated pull-up and pull-down resistors.<br>DE2 = Low = 0 dB<br>DE2 = Mid = -3.5 dB<br>DE2 = High = -6.2 dB                                                 |
| OS2    | 4            | I, CMOS | Sets the output swing (differential voltage amplitude) for Channel 2. 2-state input with an integrated pull down resistor.<br>OS2 = Low = 0.9 mV<br>OS2 = High = 1.1 mV                                                      |
| EN_RXD | 5            | I, CMOS | Enable. The device has a 660-k $\Omega$ pulldown resistor. Device is active when EN_RXD = High. Drive actively high or install a pullup resistor (recommend 4.7 K $\Omega$ ) for normal operation. Does reset state machine. |
| RSV    | 14           | I, CMOS | Reserved. Can be left as no-connect.                                                                                                                                                                                         |
| VCC    | 1, 13        | P       | Positive power supply. Power supply is 3.3 V.                                                                                                                                                                                |
| GND    | 10, 21, PAD  | G       | Ground. PAD must be connected to Ground. Pins 10, 21 can be connected to Ground or left unconnected.                                                                                                                         |
| NC     | 6, 7, 18, 24 | —       | No connection. These pins can be tied to any desired voltages including connecting them to GND.                                                                                                                              |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                               |                  | MIN  | MAX | UNIT |
|-----------------------------------------------|------------------|------|-----|------|
| Supply Voltage Range <sup>(2)</sup>           | V <sub>CC</sub>  | −0.5 | 4   | V    |
| Voltage Range at any input or output terminal | Differential I/O | −0.5 | 1.5 | V    |
|                                               | CMOS Inputs      | −0.5 | 4   | V    |
| Junction temperature, T <sub>J</sub>          |                  |      | 105 | °C   |
| Storage temperature, T <sub>stg</sub>         |                  | −65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.

### 6.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                      |                                           | MIN       | NOM | MAX | UNIT |
|----------------------|-------------------------------------------|-----------|-----|-----|------|
| V <sub>CC</sub>      | Main power supply                         | 3         | 3.3 | 3.6 | V    |
|                      | Supply Ramp Requirement                   |           |     | 100 | ms   |
| V <sub>(PSN)</sub>   | Supply Noise on V <sub>CC</sub> Terminals |           |     | 100 | mV   |
| T <sub>A</sub>       | Operating free-air temperature            | TUSB522P  |     | 70  | °C   |
|                      |                                           | TUSB522PI |     | 85  | °C   |
| C <sub>AC-USB1</sub> | External AC coupling capacitor            | 75        | 100 | 265 | nF   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TUSB522P   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGE (VQFN) |      |
|                               |                                              | 24 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 51.2       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 55.9       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 28.3       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 2.0        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 28.3       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 9.7        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics, Power Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER          |                                 | TEST CONDITIONS                                                                                                                                                         | MIN | TYP | MAX | UNIT |
|--------------------|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $I_{CC(ACTIVE)}$   | Average active current          | Link in U0 with GEN1 data transmission.<br>RSV, EQ cntrl pins = NC, EN_RXD = $V_{CC}$ ,<br>k28.5 pattern at 5Gbps,<br>$V_{ID}$ = 1000 mVpp, OS = 900 mV and DE = 3.5 dB |     | 98  |     | mA   |
| $I_{CC(U2/U3)}$    | Average current in U2/U3        | Link in U2 or U3                                                                                                                                                        |     | 1.2 |     | mA   |
| $I_{CC(NC)}$       | Average current disconnect mode | Link in Disconnect mode                                                                                                                                                 |     | 265 |     | μA   |
| $I_{CC(SHUTDOWN)}$ | Average shutdown current        | EN_RXD = L                                                                                                                                                              |     | 60  |     | μA   |

## 6.6 Electrical Characteristics, DC

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 |                               | TEST CONDITIONS                   | MIN                 | TYP                  | MAX | UNIT |
|-------------------------------------------|-------------------------------|-----------------------------------|---------------------|----------------------|-----|------|
| <b>3-State CMOS Inputs(EQ1/2, DE1/2)</b>  |                               |                                   |                     |                      |     |      |
| $V_{IH}$                                  | High-level input voltage      |                                   | $V_{CC} \times 0.8$ |                      |     | V    |
| $V_{IM}$                                  | Mid-level input voltage       |                                   |                     | $V_{CC} / 2$         |     | V    |
| $V_{IL}$                                  | Low-level input voltage       |                                   |                     | $V_{CC} \times 0.2$  |     | V    |
| $V_F$                                     | Floating voltage              | $V_{IN}$ = High impedance         |                     | $0.36 \times V_{CC}$ |     | V    |
| $R_{PU}$                                  | Internal pull-up resistance   |                                   |                     | 410                  |     | kΩ   |
| $R_{PD}$                                  | Internal pull-down resistance |                                   |                     | 240                  |     | kΩ   |
| $I_{IH}$                                  | High-level input current      | $V_{IN} = 3.6$ V                  |                     |                      | 26  | μA   |
| $I_{IL}$                                  | Low-level input current       | $V_{IN} = GND$ , $V_{CC} = 3.6$ V | -26                 |                      |     | μA   |
| <b>2-State CMOS Input (OS1/2, EN_RXD)</b> |                               |                                   |                     |                      |     |      |
| $V_{IH}$                                  | High-level input voltage      |                                   | $V_{CC} \times 0.7$ |                      |     | V    |
| $V_{IL}$                                  | Low-level input voltage       |                                   |                     | $V_{CC} \times 0.3$  |     | V    |
| $R_{PD}$                                  | Internal pull-down resistance |                                   |                     | 660                  |     | kΩ   |
| $I_{IH}$                                  | Low-level input current       | $V_{IN} = 3.6$ V                  |                     |                      | 25  | μA   |
| $I_{IL}$                                  | Low-level input current       | $V_{IN} = GND$ , $V_{CC} = 3.6$ V | -10                 |                      |     | μA   |

## 6.7 Electrical Characteristics, AC

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                  |                                                                                               | TEST CONDITIONS                                                                                              | MIN  | TYP  | MAX  | UNIT       |
|--------------------------------------------|-----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|------|------|------|------------|
| <b>Differential Receiver (RXP, RXN)</b>    |                                                                                               |                                                                                                              |      |      |      |            |
| $V_{(RX-DIFF-PP)}$                         | Input differential voltage swing.                                                             | AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel                   | 100  |      | 1200 | mVpp       |
| $V_{(RX-DC-CM)}$                           | Common-mode voltage bias in the receiver (DC)                                                 |                                                                                                              |      | 0.7  |      | V          |
| $R_{(RX-DIFF-DC)}$                         | Differential input impedance (DC)                                                             | Present after a GEN1 device is detected on TXP/TXN                                                           | 72   |      | 120  | $\Omega$   |
| $R_{(RX-CM-DC)}$                           | Receiver DC Common Mode impedance                                                             |                                                                                                              | 18   |      | 30   | $\Omega$   |
| $Z_{(RX-HIGH-IMP-DC-POS)}$                 | Common-mode input impedance with termination disabled (DC)                                    | Present when no GEN1 device is detected on TXP/TXN. Measured over the range of 0-500 mV with respect to GND. | 25   |      |      | k $\Omega$ |
| $V_{(RX-SIGNAL-DET-DIFF-PP)}$              | Input Differential peak-to-peak Signal Detect Assert Level                                    | At 5Gbps, no input channel loss clock pattern                                                                |      | 85   |      | mV         |
| $V_{(RX-IDLE-DET-DIFF-PP)}$                | Input Differential peak-to-peak Signal Detect De-assert Level                                 |                                                                                                              |      | 85   |      | mV         |
| $V_{(RX-LFPS-DET-DIFF-PP)}$                | Low Frequency Periodic Signaling (LFPS) Detect Threshold                                      | Below the minimum is squelched.                                                                              | 100  |      | 300  | mV         |
| $V_{(RX-CM-AC-P)}$                         | Peak RX AC common mode voltage                                                                | Measured at package pin                                                                                      |      |      | 150  | mV         |
| $V_{(detect)}$                             | Voltage change to allow receiver detect                                                       | Positive voltage to sense receiver termination                                                               |      |      | 600  | mV         |
| $C_{(RX-PARASITIC)}$                       | Voltage change to allow receiver detect                                                       | At 2.5 GHz                                                                                                   | 0.17 | 0.63 | 0.99 | pF         |
| $R_{L(RX-DIFF)}$                           | Differential Return Loss                                                                      | 50 MHz – 1.25 GHz at 90 $\Omega$                                                                             |      | –19  |      | dB         |
|                                            |                                                                                               | 2.5 GHz at 90 $\Omega$                                                                                       |      | –14  |      | dB         |
| $R_{L(RX-CM)}$                             | Common Mode Return Loss                                                                       | 50 MHz – 1.25 GHz at 90 $\Omega$                                                                             |      | –13  |      | dB         |
| <b>Differential Transmitter (TXP, TXN)</b> |                                                                                               |                                                                                                              |      |      |      |            |
| $V_{(TX-DIFF-PP)}$                         | Transmitter differential voltage swing (transition-bit)                                       | OS Low, 0dB DE                                                                                               | 0.8  | 0.9  |      | Vpp        |
|                                            |                                                                                               | OS High, 0dB DE                                                                                              |      | 1.1  | 1.2  | Vpp        |
| $V_{(TX-DIFF-PP-LFPS)}$                    | LFPS differential voltage swing                                                               | OS Low, High                                                                                                 | 0.8  |      | 1.2  | Vpp        |
| $V_{(TX-DE-RATIO)}$                        | Transmitter differential voltage De-Emphasis ratio                                            | DE = Low                                                                                                     |      | 0    |      | dB         |
|                                            |                                                                                               | DE = Floating                                                                                                |      | –3.5 |      | dB         |
|                                            |                                                                                               | DE = High                                                                                                    |      | –6.2 |      | dB         |
| $V_{(TX-RCV-DETECT)}$                      | Amount of voltage change allowed during Receiver Detection                                    |                                                                                                              |      |      | 600  | mV         |
| $V_{(TX-CM-IDLE-DELTA)}$                   | Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS |                                                                                                              | –600 |      | 600  | mV         |
| $V_{(TX-DC-CM)}$                           | Common-mode voltage bias in the transmitter (DC)                                              |                                                                                                              |      | 0.7  |      | V          |
| $V_{(TX-CM-AC-PP-ACTIVE)}$                 | Tx AC Common-mode voltage active                                                              | Max mismatch from Txp + Txn for both time and amplitude                                                      |      |      | 100  | mVpp       |
| $V_{(TX-IDLE-DIFF-AC-PP)}$                 | AC Electrical idle differential peak-to-peak output voltage                                   | At package pins                                                                                              | 0    |      | 10   | mV         |
| $V_{(TX-IDLE-DIFF-DC)}$                    | DC Electrical idle differential output voltage                                                | At package pins after low pass filter to remove AC component                                                 | 0    |      | 10   | mV         |
| $V_{(TX-CM-DC-ACTIVE-IDLE-DELTA)}$         | Absolute DC common mode voltage between U1 and U0                                             | At package pin                                                                                               |      |      | 200  | mV         |
| $C_{(TX)}$                                 | TX input capacitance to GND                                                                   | At 2.5 GHz                                                                                                   |      |      | 1.25 | pF         |
| $R_{(TX-DIFF)}$                            | Differential impedance of the driver                                                          |                                                                                                              | 72   |      | 120  | $\Omega$   |
| $R_{(TX-CM)}$                              | Common-mode impedance of the driver                                                           | Measured with respect to AC ground over 0-500 mV                                                             | 18   |      | 30   | $\Omega$   |
| $I_{(TX-SHORT)}$                           | TX short circuit current                                                                      | TX± shorted to GND                                                                                           |      |      | 60   | mA         |
| $C_{(TX-PARASITIC)}$                       | TX input capacitance for return loss                                                          | Package Pins                                                                                                 |      | 0.63 | 1.02 | F          |

## 6.7 Electrical Characteristics, AC (続き)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                          |                                                               | TEST CONDITIONS                                                    | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------------|-----|-----|-----|------|
| R <sub>L(RX-DIFF)</sub>            | Differential Return Loss                                      | 50 MHz – 1.25 GHz at 90 Ω                                          |     | 12  |     | dB   |
|                                    |                                                               | 1.25 – 2.5 GHz at 90 Ω                                             |     | 8   |     | dB   |
| R <sub>L(RX-CM)</sub>              | Common Mode Return Loss                                       | 50 MHz – 1.25 GHz at 90 Ω                                          |     | 13  |     | dB   |
|                                    |                                                               | 1.25 –2.5 GHz                                                      |     | 11  |     | dB   |
| AC Characteristic                  |                                                               |                                                                    |     |     |     |      |
| Xtalk                              | Differential Cross Talk between TX and RX signal Pairs        | At 2.5 GHz                                                         |     | –40 |     | dB   |
| V <sub>(CM-TX-AC)</sub>            | AC Common-mode voltage swing in active mode                   | Within U0 and within LFPS                                          |     |     | 100 | mVpp |
| V <sub>(TX-IDLE-DIFF -AC-PP)</sub> | Differential voltage swing during electrical idle             | Tested with a high-pass filter                                     | 0   |     | 10  | V    |
| R <sub>L(TX-DIFF)</sub>            | Differential Return Loss                                      | f = 50 MHz - 1.25 GHz                                              |     | 12  |     | dB   |
|                                    |                                                               | 1.25 –2.5 GHz                                                      |     | 8   |     | dB   |
| R <sub>L(TX-CM)</sub>              | Common Mode Return Loss                                       | f = 50 MHz - 1.25 GHz                                              |     | 16  |     | dB   |
|                                    |                                                               | 1.25 –2.5 GHz                                                      |     | 13  |     | dB   |
| t <sub>j</sub>                     | Total Jitter                                                  | Minimum input and output trace at 2.5 GHz, V <sub>CC</sub> = 3.3 V |     | 15  |     | ps   |
| V <sub>(TX-CM-ΔU1-U0)</sub>        | Absolute delta of DC CM voltage during active and idle states |                                                                    |     |     | 100 | mV   |
| V <sub>(TX-IDLE-DIFF-DC)</sub>     | DC Electrical idle differential output voltage                | Voltage must be low pass filtered to remove any AC component       | 0   |     | 12  | mV   |

## 7 Detailed Description

### 7.1 Overview

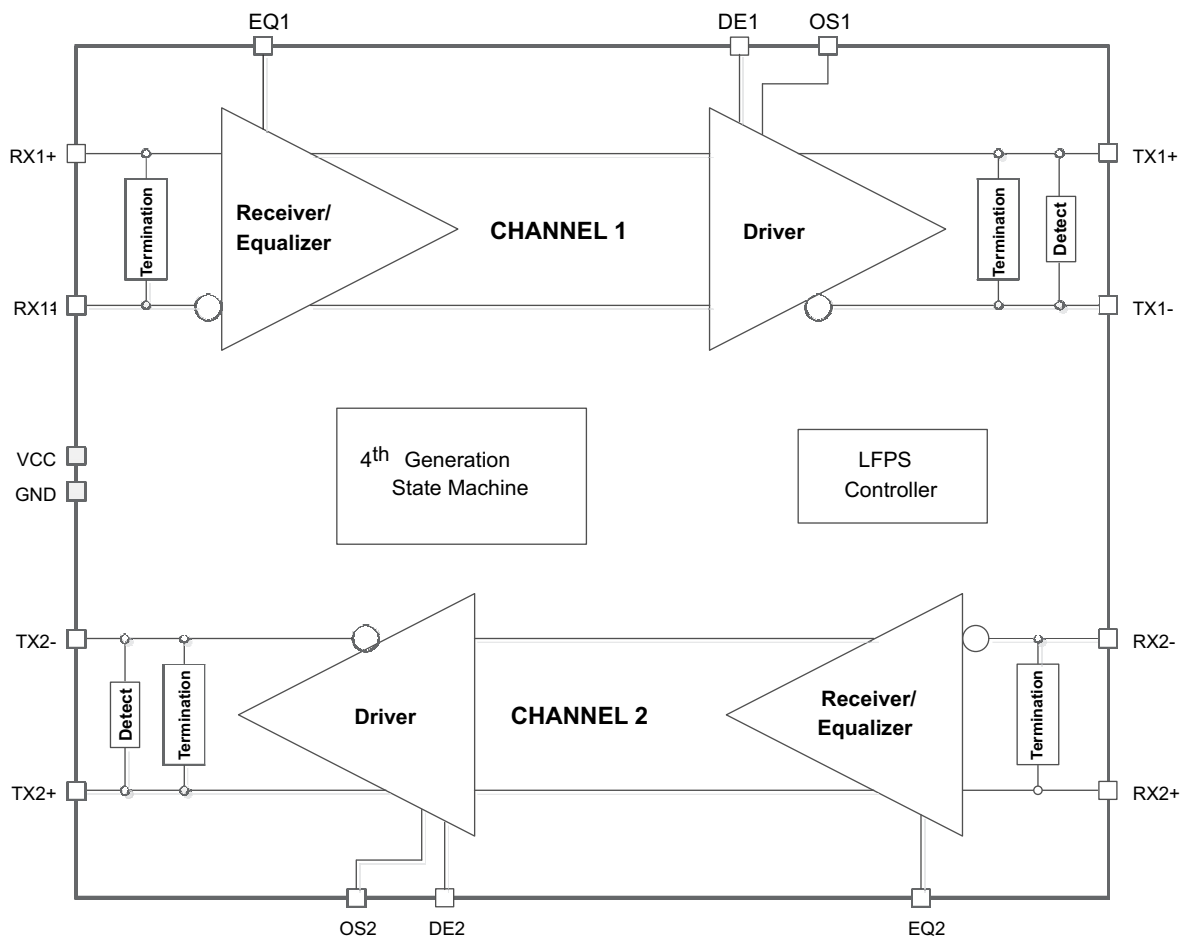
The TUSB522P is designed to overcome channel loss due to inter-symbol interference and crosstalk when 5Gbps USB3.1 GEN1 signals travel across a PCB or cable. The dual channel architecture is a one-chip, low-power solution, extending the possible channel length for transmit and receive data paths in an application. For a Host application, this enables the system to pass both transmitter compliance and receiver jitter tolerance tests.

The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. The equalization should be set based on the amount of insertion loss in channel 1 or 2 before the TUSB522P receivers. Likewise, the output drivers support configuration of De-Emphasis. Independent equalization and de-emphasis control for each channel can be set using EQ1/2 and DE1/2 pins.

The TUSB522P advanced state machine makes it transparent to hosts and devices. After power up, the TUSB522P periodically performs receiver detection on the TX pairs. If it detects a USB3.1 GEN1 receiver, the RX termination is enabled, and the TUSB522P is ready to re-drive.

The device ultra-low-power architecture operates at a 3.3-V power supply and achieves Enhanced performance. The automatic LFPS De-Emphasis control further enables the system to be USB3.1 compliant.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Receiver Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB522P. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TUSB522P receivers. The gain setting may differ for channel 1 and channel 2.

### 7.3.2 De-Emphasis Control and Output Swing

The differential driver output provides selectable de-emphasis and output swing control in order to achieve USB3.1 compliance. The TUSB522P offers a unique way to adjust output de-emphasis and transmitter swing based on the OS1/2 and DE1/2 pins. The level of de-emphasis required in the system depends on the channel length after the output of the re-driver. The output swing and de-emphasis levels may differ for channel 1 and channel 2.

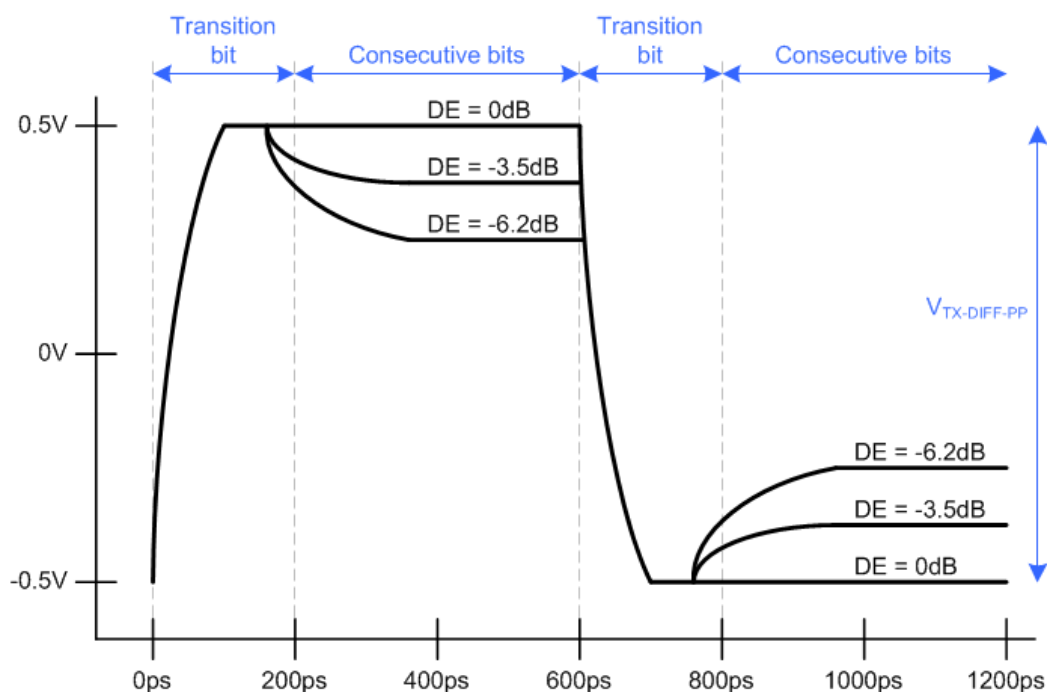


図 7-1. Transmitter Differential Voltage, OS = Floating

### 7.3.3 Automatic LFPS Detection

The TUSB522P features an intelligent low frequency periodic signaling (LFPS) controller. The controller senses the low frequency signals and automatically disables the driver de-emphasis, for full USB3.1 compliance.

## 7.4 Device Functional Modes

### 7.4.1 Device Configuration

**表 7-1. Control Pin Settings (Typical Values)**

| PIN     | DESCRIPTION                                            | LOGIC STATE | TYP  | UNITS |
|---------|--------------------------------------------------------|-------------|------|-------|
| EQ1/EQ2 | Receiver equalization amount                           | Low         | 3    | dB    |
|         |                                                        | Floating    | 6    | dB    |
|         |                                                        | High        | 9    | dB    |
| OS1/OS2 | Transmit output swing amplitude for the transition bit | Low         | 0.9  | Vpp   |
|         |                                                        | High        | 1.1  | Vpp   |
| DE1/DE2 | Transmit de-emphasis amount                            | Low         | 0    | dB    |
|         |                                                        | Floating    | –3.5 | dB    |
|         |                                                        | High        | –6.2 | dB    |

### 7.4.2 Power Modes

The TUSB522P has 3 primary power modes:

#### 7.4.2.1 U0 Mode (Active Power Mode)

During active power mode, U0, the device is transmitting USB SS data or USB LFPS signaling. The U0 mode is the highest power state of the TUSB522P. Anytime super-speed traffic is being received, the TUSB522P remains in this mode.

#### 7.4.2.2 U2/U3 (Low Power Mode)

While in this mode, the TUSB522P periodically performs far-end receiver detection.

#### 7.4.2.3 Disconnect Mode - RX Detect

In this state, the TUSB522P periodically checks for far-end receiver termination on both TX. Upon detection of the far-end receiver's termination on both ports, the TUSB522P will transition to U0 mode.

#### 7.4.2.4 Shutdown Mode

Shutdown mode is entered when the EN\_RXD pin is driven low. This is lowest power setting for the device.

## 8 Application and Implementation

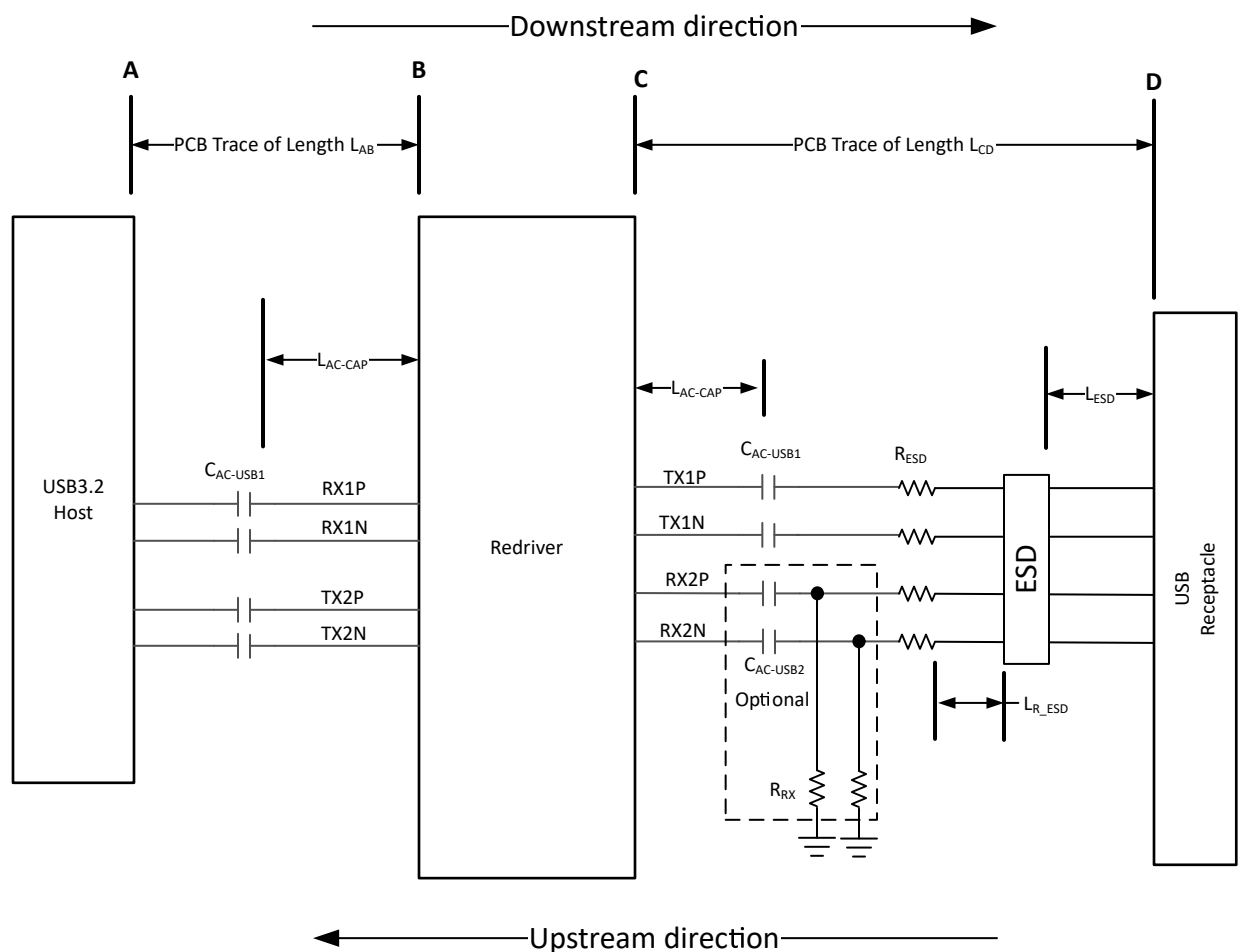
注

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## 8.1 Application Information

The TUSB522P is a dual-channel single-lane re-driver and signal conditioner designed to compensate for ISI jitter caused by attenuation through passive mediums such as traces or cables. The TUSB522P has two independent channels to allow optimization in both upstream and downstream directions through three EQ and six De-Emphasis settings.

## 8.2 Typical Application



### ❏ 8-1. Embedded Host Application

The C<sub>AC-USB1</sub> and C<sub>AC-USB2</sub> should be placed between ESD and USB receptacle for systems designing for short to VBUS protection.

## 8.2.1 Design Requirements

For this design example, use the parameters provided in 表 8-1.

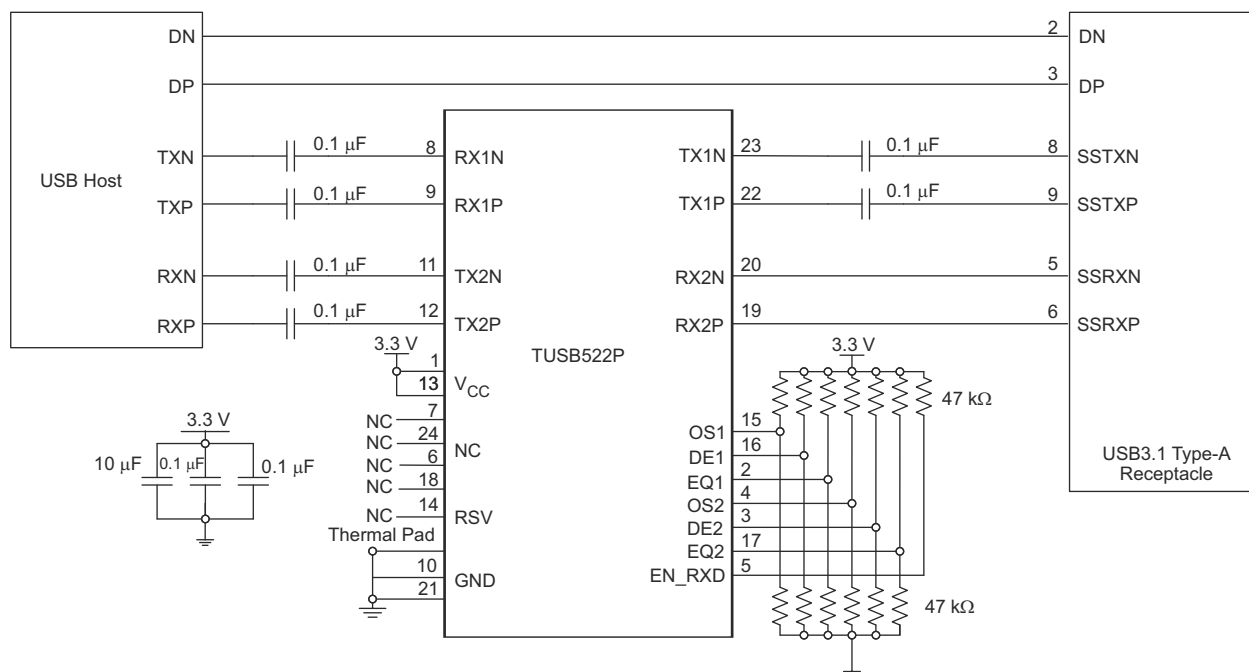
**表 8-1. Design Parameters**

| PARAMETER                                                                            | VALUE                                                                                                                                                                 |
|--------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pre-channel A to B PCB trace length <sup>(1)</sup> , $L_{AB}$ .                      | 1 inches $\leq L_{AB} \leq$ 20 inches                                                                                                                                 |
| Post-channel C to D PCB trace length <sup>(1)</sup> , $L_{CD}$ .                     | $\leq$ 6 inches                                                                                                                                                       |
| Minimum distance of the AC capacitors from TUSB522P, $L_{AC-CAP}$                    | 0.25 inches                                                                                                                                                           |
| Maximum distance of ESD component from the USB receptacle, $L_{ESD}$                 | 0.6 inches                                                                                                                                                            |
| Maximum distance of series resistor ( $R_{ESD}$ ) from ESD component, $L_{R\_ESD}$ . | 0.25 inches                                                                                                                                                           |
| $C_{AC-USB1}$ AC-coupling capacitor (75 nF to 265 nF)                                | 100 nF                                                                                                                                                                |
| $C_{AC-USB2}$ AC-coupling capacitor (297 nF to 363 nF)                               | Options:<br><ul style="list-style-type: none"> <li>RX1 or RX2 are DC-coupled to USB receptacle</li> <li>330 nF AC-couple with <math>R_{RX}</math> resistor</li> </ul> |
| Optional $R_{RX}$ resistor (220-k $\Omega$ $\pm$ 5%)                                 | Not used                                                                                                                                                              |
| Optional $R_{ESD}$ (0- $\Omega$ to 2.2- $\Omega$ )                                   | Not used                                                                                                                                                              |
| $V_{CC}$ supply (3-V to 3.6-V)                                                       | 3.3-V                                                                                                                                                                 |
| EQ1 for RX1P/N (3, 6, or 9dB)                                                        | 9 dB (EQ1 = High)                                                                                                                                                     |
| De-Emphasis 2 for TX2P/N (0, -3.5, and -6.2 dB)                                      | -6.2 dB (OS2 = Low, DE2 = High)                                                                                                                                       |
| EQ2 for RX2P/N (3, 6, or 9 dB)                                                       | 6 dB (EQ2 = Floating)                                                                                                                                                 |
| De-Emphasis 1 for TX1P/N (0, -3.5, and -6.2 dB)                                      | -3.5 dB (OS1 = Low, DE1 = Floating)                                                                                                                                   |
| Output Swing 1 (0.9 or 1.1 Vppd)                                                     | 900 mV (OS1 = Low)                                                                                                                                                    |
| Output Swing 2 (0.9 or 1.1 Vppd)                                                     | 900 mV (OS2 = Low)                                                                                                                                                    |

(1) Maximum trace length assumes an insertion loss of 0.2 dB/inch/GHz. If insertion loss is more than 0.2 dB/inch/GHz, then maximum trace length must be reduced accordingly.

## 8.2.2 Detailed Design Procedure

The TUSB522P differential receivers and transmitters have internal BIAS and termination. Due to this, the TUSB522P must be connected to the USB Host and receptacle through ac-coupling capacitors. In this example, as depicted in 図 8-2, 100 nF capacitors are placed on TX2P, TX2N, RX1P, RX1N, TX1P and TX1N. No ac-coupling capacitors are placed on the RX2P and RX2N pins because it is assumed the device downstream of the TUSB522P will have ac-coupling capacitors on its transmitter as defined by the USB 3.1 specification. The system designer may desire to support short to VBUS protection. If this is the case, then a 330 nF ac-coupling capacitor should be placed on RX2P/N pins.



**図 8-2. Embedded Host Application Schematic**

### 8.2.2.1 ESD Protection

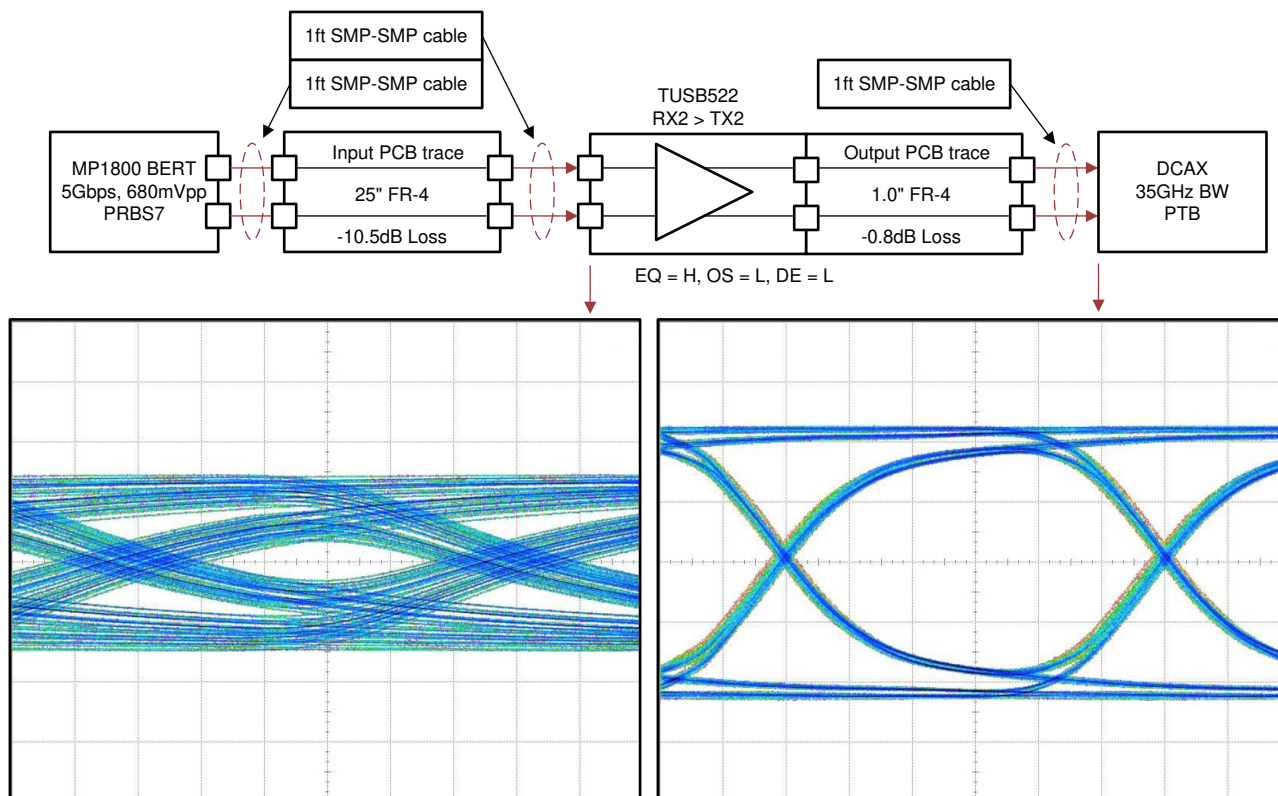
It may be necessary to incorporate an ESD component to protect the TUSB522P from electrostatic discharge (ESD). It is recommended that the ESD protection component has working peak voltage of  $\geq 1.3$  V, a breakdown voltage of  $\geq 2.3$  V, and a clamp voltage of  $\leq 4.0$  V. A clamp voltage greater than 4.0 V may require a  $R_{ESD}$  on each differential pin. The ESD component should be placed near the USB connector.

**表 8-2. Recommended ESD Protection Component**

| Manufacturer | Part Number  | Required $R_{ESD}$ to pass IEC 61000-4-2 Contact $\pm 8$ -kV |
|--------------|--------------|--------------------------------------------------------------|
| Nexperia     | PUSB3FR4     | 2.2- $\Omega$                                                |
| Nexperia     | PESD2V8Y1BSF | 2.2- $\Omega$                                                |

## 8.2.3 Application Curves

BERT > 24"6mil > char-board > RX2-to-TX2 > char-board > Scope



## 8.3 Power Supply Recommendations

The TUSB522P is designed to operate with a 3.3-V power supply. Levels above those listed in the *Absolute Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-μF capacitor should be used on each power pin.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance ( $\pm 15\%$ ).
- Keep away from other high speed signals.
- Intra-pair routing should be kept to within 2mils.
- Length matching should be near the location of mismatch.
- Each pair should be separated at least by 3 times the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be  $\geq 135$  degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do not route differential pairs over any plane split.
- Adding test points will cause impedance discontinuity; and will therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
- The 100-nF capacitors on the TXP and SSTXN nets must be placed close to the USB connector (Type A, Type B, and so forth).

- The ESD and EMI protection devices (if used) must also be placed as close as possible to the USB connector.
- Place voltage regulators as far away as possible from the differential pairs.
- To minimize crosstalk, TI recommends keeping high-speed signals away from each other. Each pair must be separated by at least 5 times the signal trace width. Separating with ground also helps minimize crosstalk.

#### 8.4.2 Layout Example

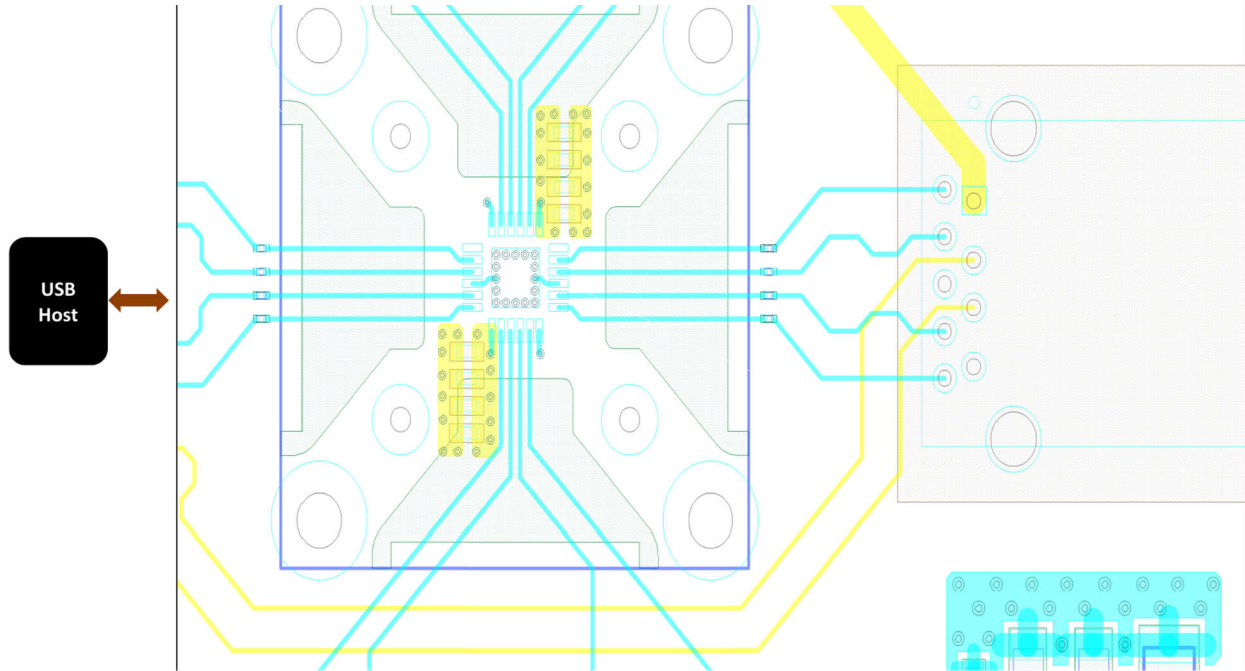


図 8-3. Example Layout

## 9 Device and Documentation Support

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

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### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TUSB522PIRGER    | ACTIVE        | VQFN         | RGE                | 24   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TUSB<br>522P            | <a href="#">Samples</a> |
| TUSB522PIRGET    | ACTIVE        | VQFN         | RGE                | 24   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TUSB<br>522P            | <a href="#">Samples</a> |
| TUSB522PRGER     | ACTIVE        | VQFN         | RGE                | 24   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 70      | TUSB<br>522P            | <a href="#">Samples</a> |
| TUSB522PRGET     | ACTIVE        | VQFN         | RGE                | 24   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 70      | TUSB<br>522P            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB522PIRGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TUSB522PIRGET | VQFN         | RGE             | 24   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TUSB522PRGER  | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TUSB522PRGET  | VQFN         | RGE             | 24   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

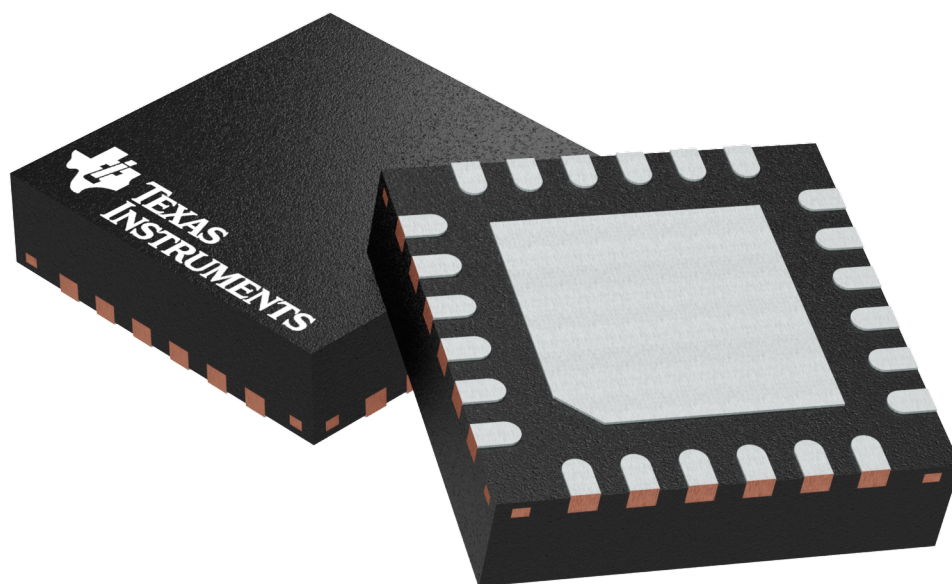
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB522PIRGER | VQFN         | RGE             | 24   | 3000 | 356.0       | 356.0      | 35.0        |
| TUSB522PIRGET | VQFN         | RGE             | 24   | 250  | 210.0       | 185.0      | 35.0        |
| TUSB522PRGER  | VQFN         | RGE             | 24   | 3000 | 356.0       | 356.0      | 35.0        |
| TUSB522PRGET  | VQFN         | RGE             | 24   | 250  | 210.0       | 185.0      | 35.0        |

**RGE 24**

**GENERIC PACKAGE VIEW**

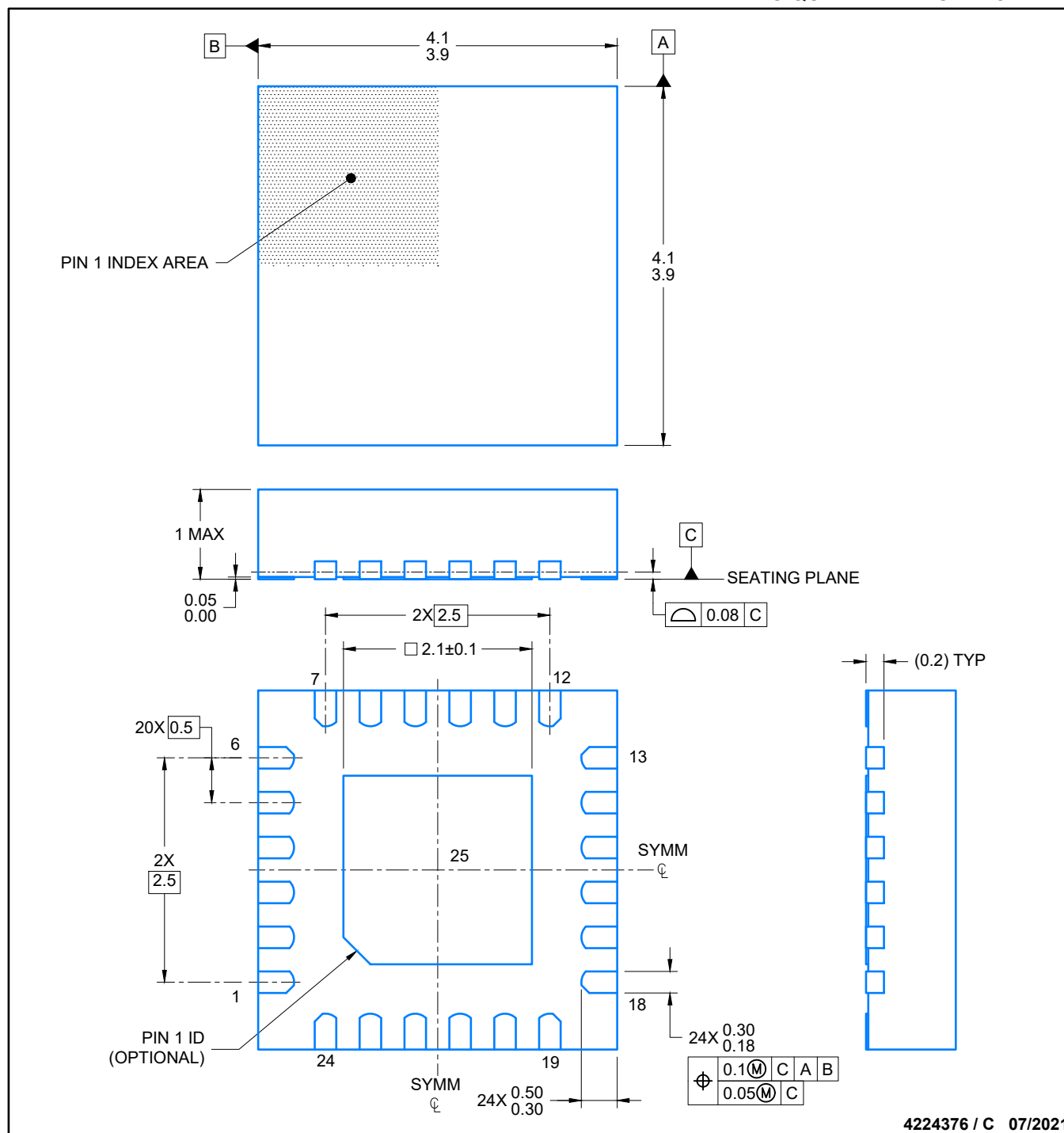
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



4224376 / C 07/2021

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

### VQFN - 1 mm max height

0.07 MAX  
ALL AROUND

METAL

SOLDER MASK  
OPENING

NON SOLDER MASK  
DEFINED  
(PREFERRED)

0.07 MIN  
ALL AROUND

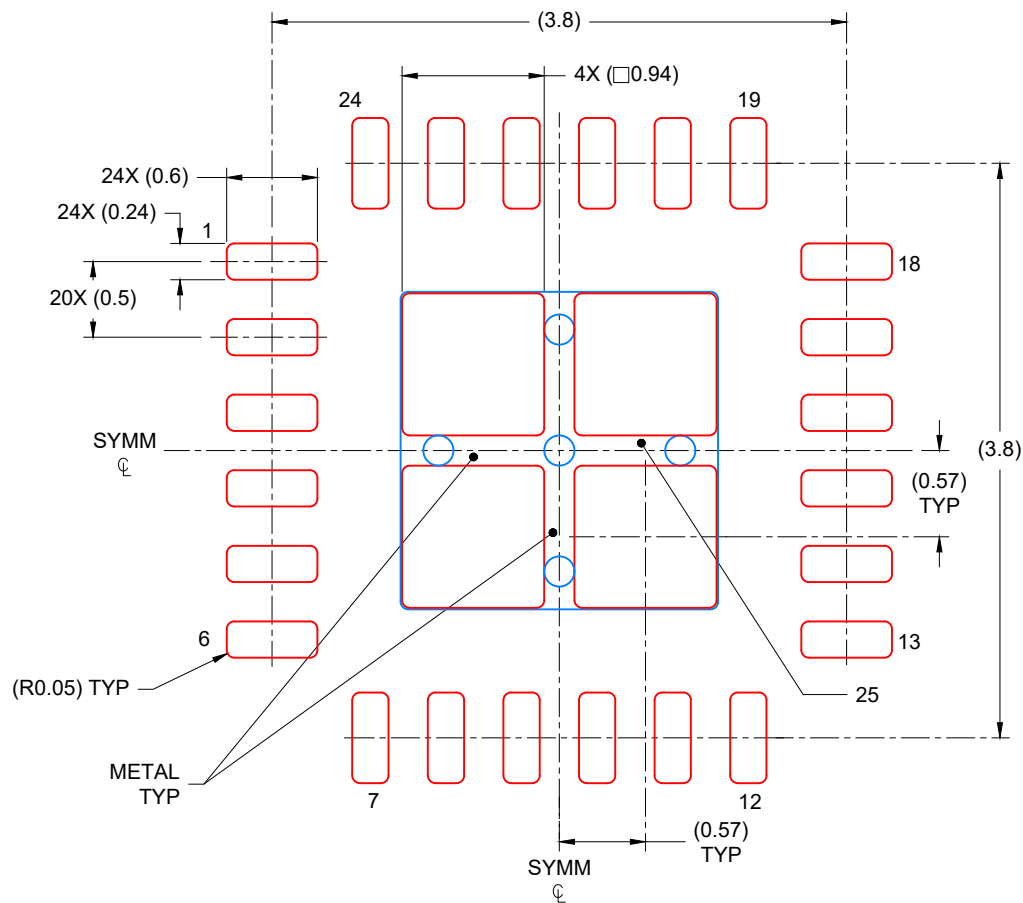
SOLDER MASK  
OPENING

METAL UNDER  
SOLDER MASK

SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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