

# EVM User's Guide: DLPLCRC964EVM

## DLPLCRC964 Evaluation Module Quick Start Guide



### Description

The DLP® LightCrafter™ DLPC964 Evaluation Module (EVM) offers a reference design to enable faster development of the DLPC964 controller architecture in support of the DLP991U DMD. This platform receives high-speed bit-plane data from an external source via the AMD Aurora 64B/66B interface and formats the bit-plane data prior to loading into a DLPLCR99EVM for display on the DLP991U DMD.

### Get Started

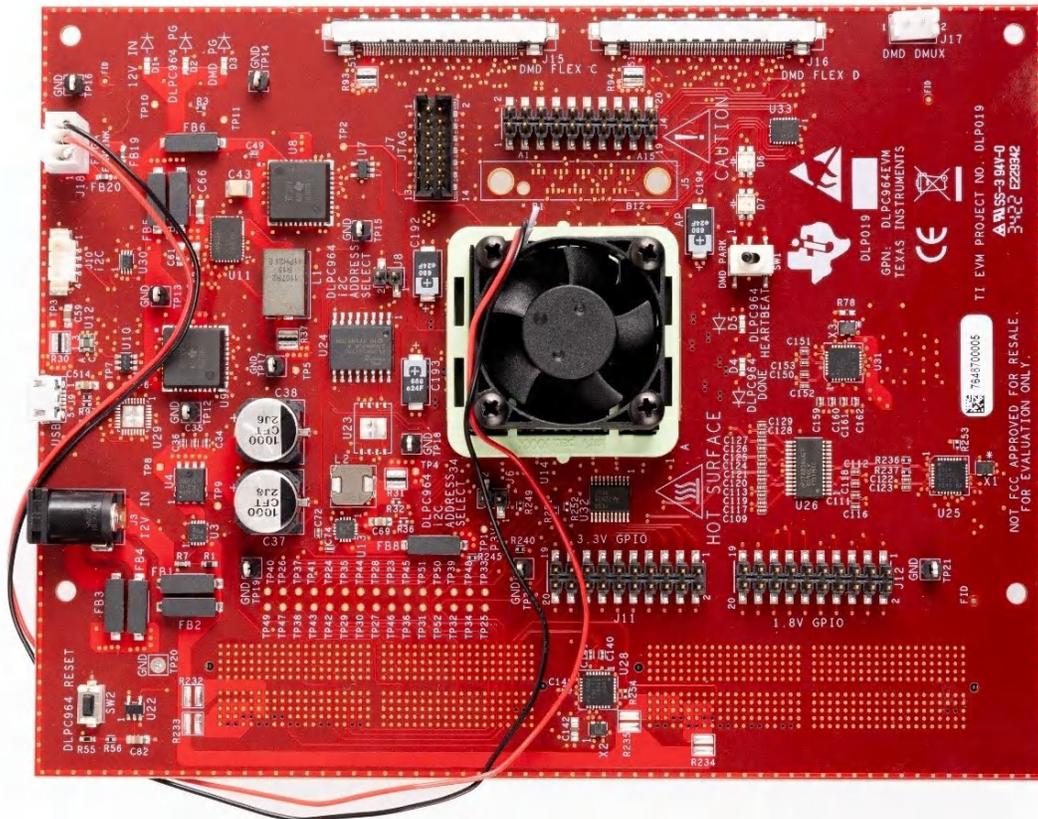
1. To order the DLPLCRC964EVM, visit the [DLPLCRC964EVM Product Page](#).
2. Please refer to the [TI E2E DLP products forum](#) for more assistance.

### Features

- Controller EVM for the DLPLCR99EVM
- 12 HSS input Aurora 64B/66B data lanes at 10Gbps per lane
- 32 HSS DMD output data lanes at 3.6 Gbps per data lane

### Applications

- Digital direct imaging (LDI)
- Maskless lithography
- Additive manufacturing and 3D printing
- Industrial printing
- Dynamic gray scale marking and coding
- High-speed imaging and display



DLP LightCrafter DLPC964 Evaluation Module

# 1 Evaluation Module Overview

## 1.1 Introduction

The TI DLP DLPC964 GUI allows for evaluation of the DLPLCRC964EVM (DLPC964 controller board), DLPLCR99EVM (DLP991U DMD board) and Apps FPGA (AMD EVM) application. The DLPLCRC964EVM contains fixed internal test patterns that can be loaded the DLP991U DMD and provides necessary interfaces for displaying these patterns on a DLP991U DMD. The front-end AMD EVM is used to interfacing with the DLPC964 controller for sending high speed pattern data to the DLP991U DMD EVM.

This guide explains the hardware and software features of the DLP LightCrafter DLPC964 EVM system. The EVM architecture and connectors are described along with a quick start guide on how to assemble a supporting DMD EVM and an AMD Xilinx™ Evaluation board to the DLPLCRC964EVM to display and run test patterns. This guide also explains how to operate the DLP LightCrafter DLPLCRC964EVM using a Graphical User Interface (GUI). Specific details for each DLP component can be found in [Section 6](#).

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### Note

The DLPLCR99EVM (DMD EVM), AMD Xilinx™ Virtex™-7 Evaluation board (Apps FPGA), optics, illumination source, and power supply are sold separately from the DLPLCRC964EVM kit.

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## 1.2 Kit Contents

The DLPLCRC964EVM is a flexible, ready-to-use evaluation module. When the DLPLCRC964EVM is coupled with the DLPLCR99EVM and an Apps FPGA board, the DLPLCRC964EVM enables the capability of sending customer created patterns to the DLPC964 Controller and then to the attached DLP991U DMD for display. The DLP LightCrafter DLPC964EVM and supported DLP991U DMD EVM are offered for purchase separately so that customers can determine which elements are needed for application.

The following items are not included with the EVM and need to be purchased separately if needed for evaluation:

- Supported DMD EVM board ([DLPLCR99EVM](#))
- APPS FPGA board - example: AMD Evaluation Board (with separate power supply)
- Power supply - see [Section 2.1.1](#) for more details
- USB cable: Type A to Micro-B USB cable

## 1.3 Specification

The DLPLCRC964EVM contains the electronics capable of controlling the supported DLP991U DMD. This EVM offers several interface options including USB, I<sup>2</sup>C, HPC FMC connectors, and Flex Cables connectors. [Figure 1-1](#) shows the EVM Hardware Block diagram of the DLPLCRC964EVM.

The major components of DLPLCRC964EVM are:

- DLPC964 Digital DMD Controller
- Power Management Unit to support the DLPC964 subsystem
- DLPC964 configuration Flash memory
- USB 2.0 interface
- Flex Cables - Four are needed to supported the DLP991U DMD EVM board
- HPC FMC Connectors - Two for an attached Apps FPGA or other front end board

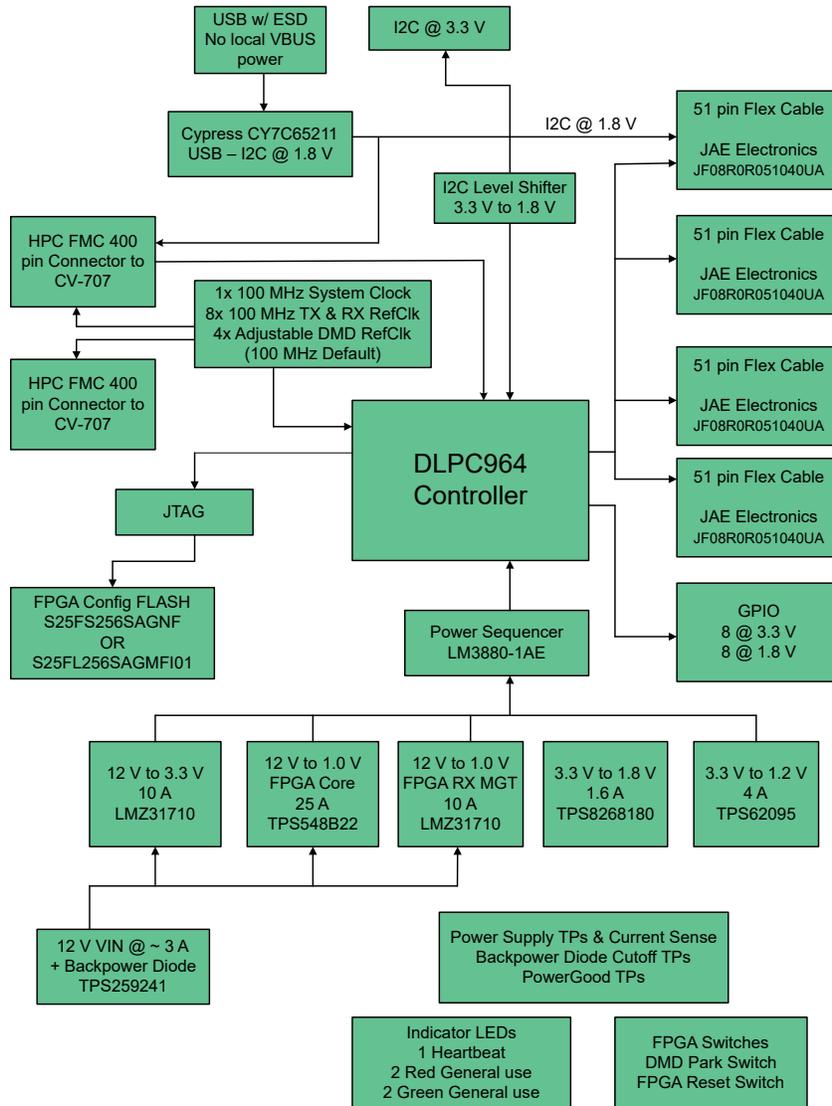


Figure 1-1. DLP LightCrafter DLPC964 EVM Block Diagram

## 1.4 Device Information

The DLP LightCrafter DLPC964 EVM is one third of a complete DMD imaging electronics subsystem. The DLP LightCrafter DLPC964 EVM consists of the DLPC964 board which includes a DLPC964 Digital Controller, USB interface, power management circuits, and supported digital logic.

Also needed to complete the imaging subsystem is a compatible DLPLCR99EVM (DLP DMD EVM). The DLPLCR99EVM is compatible with the DLPLCR964EVM and the AMD Xilinx Virtex-7 EVM or other front end to send patterns to the DLPC964 controller. The DLPLCR99EVM consists of a DMD, a DMD board (PCB) containing on-board DMD power circuits, DMD mounting hardware, and Flex Cables for connections to the DLPLCR964EVM and DLPLCR99EVM.

Figure 1-2 outlines the major hardware components of a DLPLCR964EVM System Hardware.

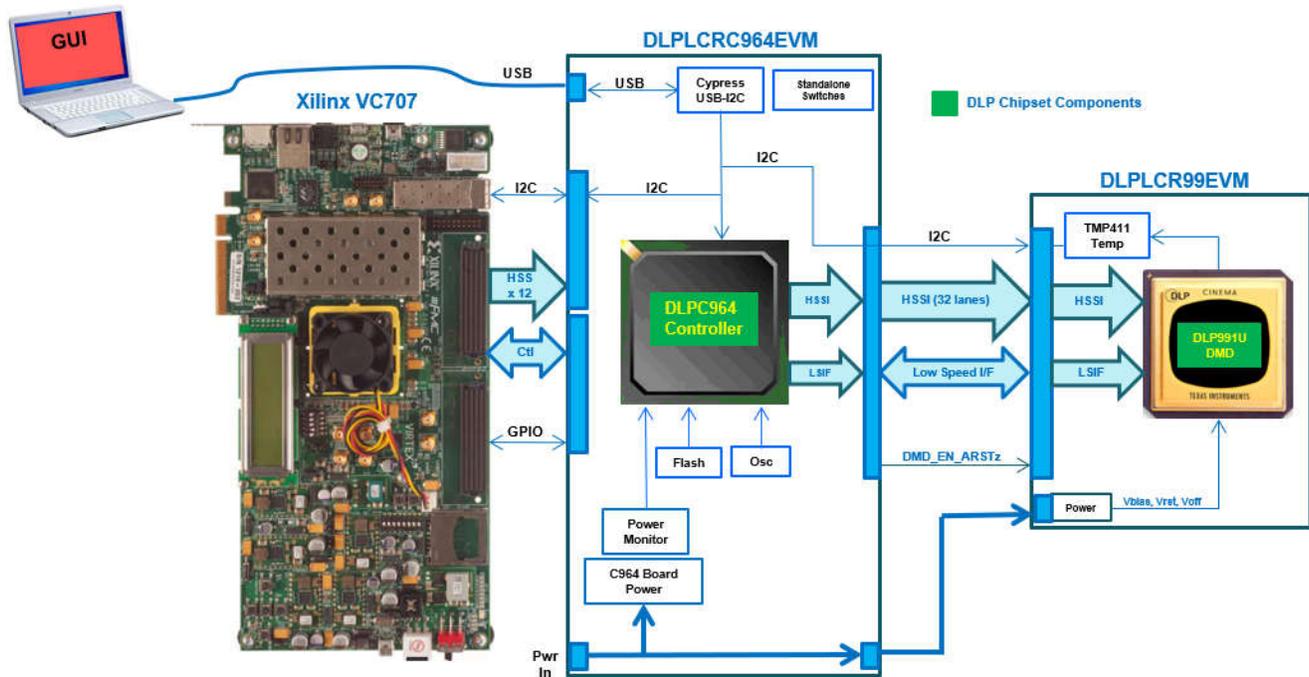


Figure 1-2. DLPLCR964EVM Hardware Components

## 2 Hardware

### 2.1 DLPLCRC964EVM Power Supply Requirements

#### 2.1.1 External Power Supply Requirements

The DLP LightCrafter DLPC964 EVM doesn't include a power supply. The external power supply requirements are:

- Nominal voltage: 12V DC -5%/+10%
- Current: 5A
- DC connector size:
  - Inner diameter: 2.5mm
  - Outer diameter: 5.5mm
  - Shaft: 9.5mm female, center positive
- A recommended power supply is [Digi-Key part number 102-3811-ND](#) or equivalent.

#### Note

External Power Supply Regulatory Compliance Certifications: TI recommends selection and use of an external power supply which meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory and safety certification requirements such as, UL, CSA, VDE, CCC, PSE.

### 2.2 DLPLCRC964EVM Connections

Figure 1-3 depicts the DLPLCRC964EVM switches and connectors with the respective locations.

#### Note

The DLPLCR99EVM, Apps FPGA, power supply, and USB cable are NOT included with the module.

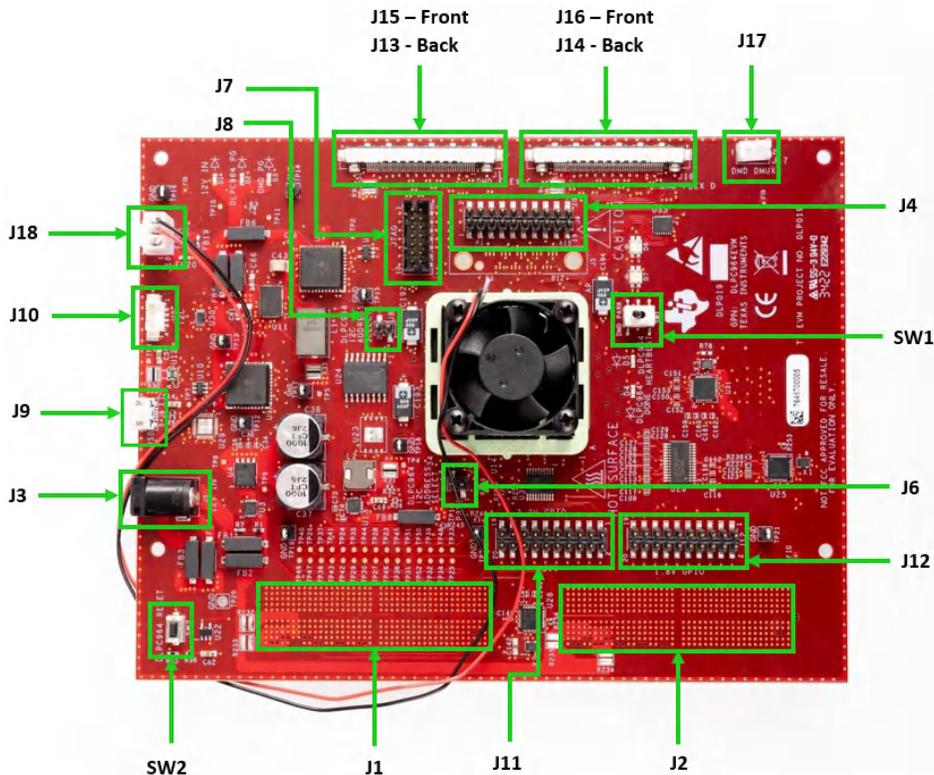


Figure 2-1. DLPLCRC964EVM Connectors (Top View)

### 2.2.1 J1, J2 - HPC FMC Connector (Male)

The 400 position HPC FMC male connectors J1 and J2 are used to connect a front end Apps FPGA (AMD Evaluation Board) to the DLPLCRC964EVM Board. The Apps FPGA is used to help enable customers with interfacing to the DLPC964 Controller for sending high speed pattern data to the DLP991U DMD.

The matching part numbers are:

- Samtec part number: SEAF-40-05.0-S-10-2-A-K-TR
- Digi-Key part number: SAM8009CT-ND

If using ribbon cables to connect between the front end Apps FPGA and DLPLCRC964EVM Board, the matching part numbers are:

- Samtec part number: ASP-134488-01 or ASP-134602-01
- Digi-Key part number: SAM8730-ND or 612-ASP-134602-01CT-ND

### 2.2.2 J3 - Input Power

Connector J3 accepts a +12 VDC input power to the DLPLCRC964EVM board. The power socket J3 pins are shown in [Table 2-1](#).

The matching part numbers are:

- CUI Devices part number: PP3-002A
- Digi-Key part number: CP3-1000-ND

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#### Note

The power supply and cable are not included inside the DLPLCRC964EVM kit and needs to be purchased separately. Please see [Section 2.1.1](#) for more details.

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**Table 2-1. Power Connector Pins**

Description	Pin	Supply Range
Input supply	1	12+ V DC -5%/+10%
Ground	2	0V
Ground	3	0V

### 2.2.3 J4 - TestMux Connector

The TESTMUX connector J4 pins are shown in [Table 2-2](#).

**Table 2-2. TESTMUX Connector Pins**

Description	Pin	Supply Range
Ground	1	0V
Ground	2	0V
TESTMUX_0	3	1.8V
TESTMUX_8	4	1.8V
TESTMUX_1	5	1.8V
TESTMUX_9	6	1.8V
TESTMUX_2	7	1.8V
TESTMUX_10	8	1.8V
TESTMUX_3	9	1.8V
TESTMUX_11	10	1.8V
TESTMUX_4	11	1.8V
TESTMUX_12	12	1.8V
TESTMUX_5	13	1.8V
TESTMUX_13	14	1.8V
TESTMUX_6	15	1.8V
TESTMUX_14	16	1.8V
TESTMUX_7	17	1.8V
TESTMUX_15	18	1.8V
Ground	19	0V
Ground	20	0V

### 2.2.4 J6, J8 - I<sup>2</sup>C Address Selectors

The I<sup>2</sup>C\_ADDR\_SEL[1:0] input pins allow the user to select the DLPC964 I<sup>2</sup>C Secondary address. [Table 2-3](#) describes the relationship between the I<sup>2</sup>C\_ADDR\_SEL[1:0] pins and the DLPC964 I<sup>2</sup>C Secondary address.

**Note**

If pins are left unconnected, the default I<sup>2</sup>C address is 0x0C.

**Table 2-3. DLPC964 I<sup>2</sup>C Secondary Address Selection Table**

I <sup>2</sup> C_ADDR_SEL[1]	I <sup>2</sup> C_ADDR_SEL[0]	I <sup>2</sup> C Secondary address
0	0	0x0F
0	1	0x0E
1	0	0x0D
1	1	0x0C

## 2.2.5 J7 - JTAG Boundary Scan

Connector J7 provides a direct connection for an AMD JTAG programming cable. J7 is used when customers want to load firmware configuration files into the FPGA (DLPC964 Controller). The JTAG Boundary connector J7 pins on the DLPLC964EVM pins are listed in [Table 2-4](#).

Two matching fourteen position connector part numbers are:

- Molex part number: 051110-1451
- Digi-Key part number: WM18047-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 087396-8051
- Digi-Key part number: WM23602CT-ND

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### Note

For instructions on programming the DLPC964 Controller, see [Section 3.1.5.2](#) for more details.

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**Table 2-4. JTAG Boundary Scan Connector Pins**

Description	Pin	Supply Range
Ground	1	0V
Supply Voltage	2	1.8V
Ground	3	0V
TMS	4	1.8V
Ground	5	0V
TCK	6	1.8V
Ground	7	0V
TDO	8	1.8V
Ground	9	0V
TDI	10	1.8V
Ground	11	0V
NC	12	N/A
Ground	13	0V
NC	14	N/A

### 2.2.6 J9 - Micro-B USB Connector

Connector J9 is used to connect the USB cable from users PC running the DLPC964 GUI. The Micro-B USB connector J9 pins are shown in [Table 2-5](#).

#### Note

The USB Micro-B to USB type A cable is not included inside the DLPLCRC964EVM kit and needs to be purchased separately.

**Table 2-5. Micro-B USB Receptacle Connector Pins**

Description	Pin	Supply Range
VBUS	1	5.0V
DMINUS	2	5.0V
DPLUS	3	5.0V
NC	4	0V
Ground	5	0V
Ground	6	0V
Ground	7	0V
Ground	8	0V
Ground	9	0V

### 2.2.7 J10 - I<sup>2</sup>C Connector

The connector J10 is used for 3.3V external I<sup>2</sup>C operations. The I<sup>2</sup>C connector J10 pins are shown in [Table 2-6](#).

Two matching four-pin, 1.25mm connector part numbers are:

- Molex part number: 0510210400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0500798100
- Digi-Key part number: 0500798100

**Table 2-6. I<sup>2</sup>C Connector Pins**

Description	Pin	Supply Range
I <sup>2</sup> C SCL	1	3.3V
I <sup>2</sup> C SDA	2	3.3V
3.3V supply	3	3.3V
Ground	4	0V
Ground	5	0V
Ground	6	0V

### 2.2.8 J11 - 3.3V GPIO Connector

The pins for J11 are available for customers definition. The 3.3V GPIO connector J11 pins are shown in [Table 2-7](#).

**Table 2-7. 3.3V GPIO Connector Pins**

Description	Pin	Supply Range
GPIO_3P3_0	1	3.3V
Ground	2	0V
GPIO_3P3_1	3	3.3V
Ground	4	0V
GPIO_3P3_2	5	3.3V
Ground	6	0V
GPIO_3P3_3	7	3.3V
Ground	8	0V
GPIO_3P3_4	9	3.3V
Ground	10	0V
GPIO_3P3_5	11	3.3V
Ground	12	0V
GPIO_3P3_6	13	3.3V
Ground	14	0V
GPIO_3P3_7	15	3.3V
Ground	16	0V
3.3V Supply	17	3.3V
Ground	18	0V
3.3V Supply	19	3.3V
Ground	20	0V

## 2.2.9 J12 - 1.8V GPIO Connector

The pins for J12 are available for customers definition. The 1.8V GPIO connector J12 pins are shown in [Table 2-8](#).

**Table 2-8. 1.8V GPIO Connector Pins**

Description	Pin	Supply Range
GPIO_1P8_0	1	1.8V
Ground	2	0V
GPIO_1P8_1	3	1.8V
Ground	4	0V
GPIO_1P8_2	5	1.8V
Ground	6	0V
GPIO_1P8_3	7	1.8V
Ground	8	0V
GPIO_1P8_4	9	1.8V
Ground	10	0V
GPIO_1P8_5	11	1.8V
Ground	12	0V
GPIO_1P8_6	13	1.8V
Ground	14	0V
GPIO_1P8_7	15	1.8V
Ground	16	0V
1.8V Supply	17	1.8V
Ground	18	0V
1.8V Supply	19	1.8V
Ground	20	0V

### 2.2.10 J13, J14, J15, J16 - DMD EVM Board Flex Cable Connectors

Connectors J13, J14, J15, and J16 are used to connect the DLPLCRC964EVM to the DLPLCR99EVM. All four Flex Cables must be connected so there can be a proper data interface to the DMD board and DMD.

Two matching fifty-one position connector part numbers are:

- JAE Electronics part number: FI-RE51HL
- Digi-Key part number: 670-1205-ND

The corresponding terminal (crimp) part numbers are:

- JAE Electronics part number: FI-RC3-1A-1E-15000
- Digi-Key part number: 670-1195-1-ND

### 2.2.11 J17 - DMD\_DMux Connector

The DMD\_DMux connector J17 is connected to the DMUX\_LATCHED signal on the DLP991U DMD EVM board. The J17 connector pins are shown in [Table 2-9](#).

Two matching two-pin, 2.5mm connector part numbers are:

- JST Sales America Inc. part number: EHR-2
- Digi-Key part number: 455-1000-ND

The corresponding terminal (crimp) part numbers are:

- JST Sales America Inc. part number: SEH-001T-P0.6
- Digi-Key part number: 455-1042-1-ND

**Table 2-9. DMD\_DMUX Connector Pins**

Description	Pin	Supply Range
DMD_DMUX	1	3.3V
Ground	2	0V

### 2.2.12 J18 - FanSink Connector

Connector J18 is a 3-pin +12 VDC fan connector used to control the temperature of the DLPC964 Controller from overheating. The FanSink connector J18 pins on the DLPLCRC964EVM are listed in [Table 2-10](#).

Two matching three-pin, 2.54mm connector part numbers are:

- Molex part number: 0022013037
- Digi-Key part number: 900-0022013037-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0008650804
- Digi-Key part number: WM2756CT-ND

#### Note

Before powering on the DLPLCRC964EVM, make sure J18 is connected to the FanSink to prevent damaging the DLPC964 Controller.

**Table 2-10. Fan Connector Pins**

Description	Pin	Supply Range
Ground	1	0V
Power	2	12V
Power	3	NC

### 2.2.13 Switches

This section describes the switches on the DLPLCRC964EVM with the respective locations.

### 2.2.13.1 SW1 - DMD park (PARK\_Z)

SW1 is a toggle switch that issues a park command to the DMD that stops the DLPC964 logic. When ON, SW1 forces the DMD micromirrors to the parked state.

#### Note

TI highly recommends switching SW1 ON prior to removing power via J3 to prevent damage to the EVM board. Please see [Section 2.4.2](#) for more information.

**Table 2-11. SW1 ON/OFF State**

SW1 State	Description
ON (facing toward DLPC964 controller)	Sets PARK_Z low and un parks the attached DMD.
OFF (facing away from DLPC964 controller)	Sets PARK_Z high and issues a park on the DMD micromirrors.

### 2.2.13.2 SW2 - DLPC964 Reset

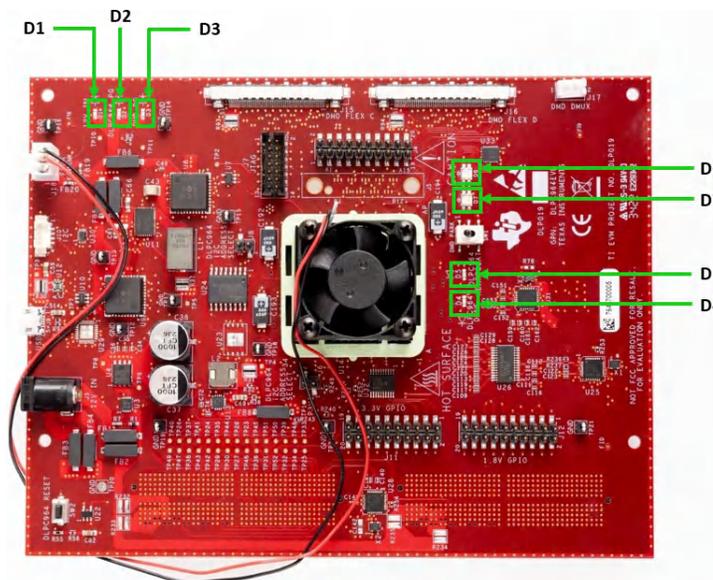
SW2 is a contact switch that resets the DLPC964 Controller code running on the DLPLC964EVM. When SW2 is released, the DLPC964 Controller boots from reset.

### 2.2.14 DLP LightCrafter DLPC964 LEDs

This section describes the power and status LEDs of the DLPLC964EVM.

#### 2.2.14.1 DLPLC964EVM Power and Status LEDs

Figure 1-4 depicts the DLPLC964EVM LEDs with the respective locations.



**Figure 2-2. DLPLC964EVM LEDs (Top View)**

**Table 2-12. DLP LightCrafter DLPC964 EVM LED Reference**

Connector Reference	EVM Function	Description or Use
D1	12V Power	External +12 VDC present.
D2	DLPC964 Power Good (PG)	All voltages are stable and present from controller board.
D3	DMD Power Good (PG)	All voltages are stable and present from DMD board.
D4	DLPC964 Done	DLPC964 initialization complete.
D5	DLPC964 Heartbeat (Flashing)	Flashes when the DLPC964 is running.
D6	Phased-Locked Loop (PLL)	Indicator that the Phase-Locked Loop (PLL) clock circuitry of the controller is locked.
D7	DMD HSSI sync error	Indicator on whether a DMD HSSI sync error was detected.

## 2.3 EVM Assembly

This chapter is going to describe how to assemble the EVM hardware.

### 2.3.1 DLPLCRC964EVM and DMD EVM Assembly

This section explains how to assemble the standalone DLPLCRC964EVM and DLPLCR99EVM.

The DLPLCRC964EVM requires a DLPLCR99EVM and four Flex Cables for assembling standalone system.

- The Flex Cable connectors are labeled J13, J14, J15, and J16 which can be seen in [Figure 1-3](#).
- The Flex Cable connectors are going to be connected between the EVM boards.
- The ends of each Flex Cable are identical.
- Either end can be connected to the connector ports J13, J14, J15, and J16 of the DLPLCRC964EVM. The other end of the flex cable is going to be connected to the DLPLCR99EVM.

The Flex Cables that come with the DLPLCR99EVM kit have a length of 16". If desired, then there are shorter Flex Cables offered by JAE Electronics. Please see the other two Flex Cable connector options below:

- [JF08R0R051030UA](#) - 12" cable length
- [JF08R0R051020UA](#) - 8" cable length

[Figure 2-1](#) depicts how to successfully connect the Flex Cables between the DLPLCRC964EVM and DLPLCR99EVM.



**Figure 2-3. Standalone DLPLCRC964EVM and DLPLCR99EVM**

### 2.3.2 Connecting an Apps FPGA Board to the DLPLCRC964EVM

This section explains how to assemble the Apps FPGA front end to the DLPLCRC964EVM and DLPLCR99EVM. If desired, customers can connect a front end board (AMD EVM) to the DLPLCRC964EVM board to send fast test patterns to the DLPC964 Controller.

Locate the AMD EVM female HPC FMC connectors and the DLPLCRC964EVM HPC FMC connectors (J1 and J2). Please line up both HPC FMC connectors and verify that the connectors are lined up correctly before applying pressure to connect the boards together as shown in [Figure 2-4](#).

#### Note

After initially applying pressure to connect both boards, apply pressure at one end and then the other to make sure connectors are fully connected together.

The 300mm Samtec HPC FMC ribbon cables ([HDR-169468-01](#)) are an alternative for these connections. Two cables are needed.

- Attach the HPC FMC female connector end of the cables to the male HPC FMC connectors on the DLPLCRC964EVM board.
- Attach the HPC FMC male connector end of the cables to the female HPC FMC connectors on the Apps FPGA board.

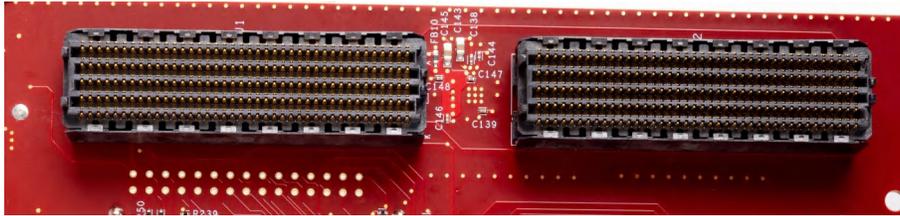


Figure 2-4. DLPLCRC964EVM Female HPC FMC Connector



Figure 2-5. AMD EVM Female HPC FMC Connector



Figure 2-6. Fully Assembled DLPLCRC964EVM with AMD EVM

## 2.4 Quick Start

This chapter explains how to properly power-up and power down the DLPLCRC964EVM.

### 2.4.1 Power-up of the DLPLCRC964EVM

The DLPLCRC964EVM is ready to use after assembling with a supported DMD EVM and a front end board such as the AMD VC-707 EVM. The following steps show how to power, display an image, and connect the EVM to a PC.

Before powering up the DLPLCRC964EVM / AMD EVM board, follow the instructions on programming the configuration PROM for either the standalone system or the AMD EVM and standalone system.

- [Programming the DLPC964 Controller](#)
- [Programming the Apps FPGA \(AMD EVM\)](#)

#### Power-Up Instructions:

1. Make sure switch SW1 is OFF and facing away from the DLPC964 Controller [DMD in parked state].
2. Power on the AMD EVM.

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#### Note

Allow sufficient time for the AMD EVM board to configure (DS1 and DS10 illuminates, indicating successful power up on the Apps FPGA).

3. Connect a 12V, 5A DC power supply to the barrel jack connector J3 shown in [Figure 1-3](#).
4. Flip SW1 ON to face toward the DLPC964 Controller (DMD in unparked state).
5. 12V power (D1), DLPC964 Power Good (D2), and DMD Power Good (D3) LEDs illuminate indicating that power is present on the DLPLCRC964EVM and DLPLCR99EVM boards.
6. DLPC964 Done (D4) illuminates indicating that the DLPC964 has completed initialization.
7. Phased-Locked Loop (D6) & DMD HSSI sync error (D7) illuminate indicating that there are no DMD HSSI sync errors and that the DLPC964 PLL is locked.
8. DLPC964 heartbeat (D5) flashes on and off indicating that the DLPLCRC964EVM is running.

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#### Note

The DLPLCR99EVM DMD board or a properly configured AMD EVM board must be present for the DLPC964 to initialize.

9. Connect a USB cable from a PC to connector J9 on the DLPLCRC964EVM, as seen in [Figure 1-3](#). The first time the cable is connected on a PC, the DLPLCRC964EVM enumerates. The required drivers are installed as part of the DLPLCRC964EVM GUI installation.
10. Open and run the DLP LightCrafter DLPC964 GUI. When the GUI application opens, look at the bottom left. The GUI is going to display *Hardware Connected*.
11. The DLPLCRC964EVM can be controlled through the GUI software available for download from the [DLPLCRC964EVM Tools Folder](#).

### 2.4.2 Power-down of the DLPLCRC964EVM

Follow steps 1 through 3 to properly power down the DLPLCRC964EVM:

1. Flip switch SW1 so the switch is facing away from the DLPC964 Controller [DMD in parked state]
2. Remove power from the barrel jack connector J3 of the DLPLCRC964EVM
3. Power off the AMD EVM (if connected)

### 3 Software

This chapter introduces the Windows DLPC964 GUI software used to control the DLPLC964EVM.

#### 3.1 Operating the DLPLC964EVM

##### 3.1.1 DLPLC964EVM GUI and Apps FPGA Software

The [DLPLC964EVM-SW](#) includes a DLPC964 GUI application to control the DLPC964 Controller, Apps FPGA, GUI source code, and Apps FPGA VHDL source code.

For details on the Apps FPGA VHDL source code, please see [DLPC964 Apps FPGA User's Guide](#).

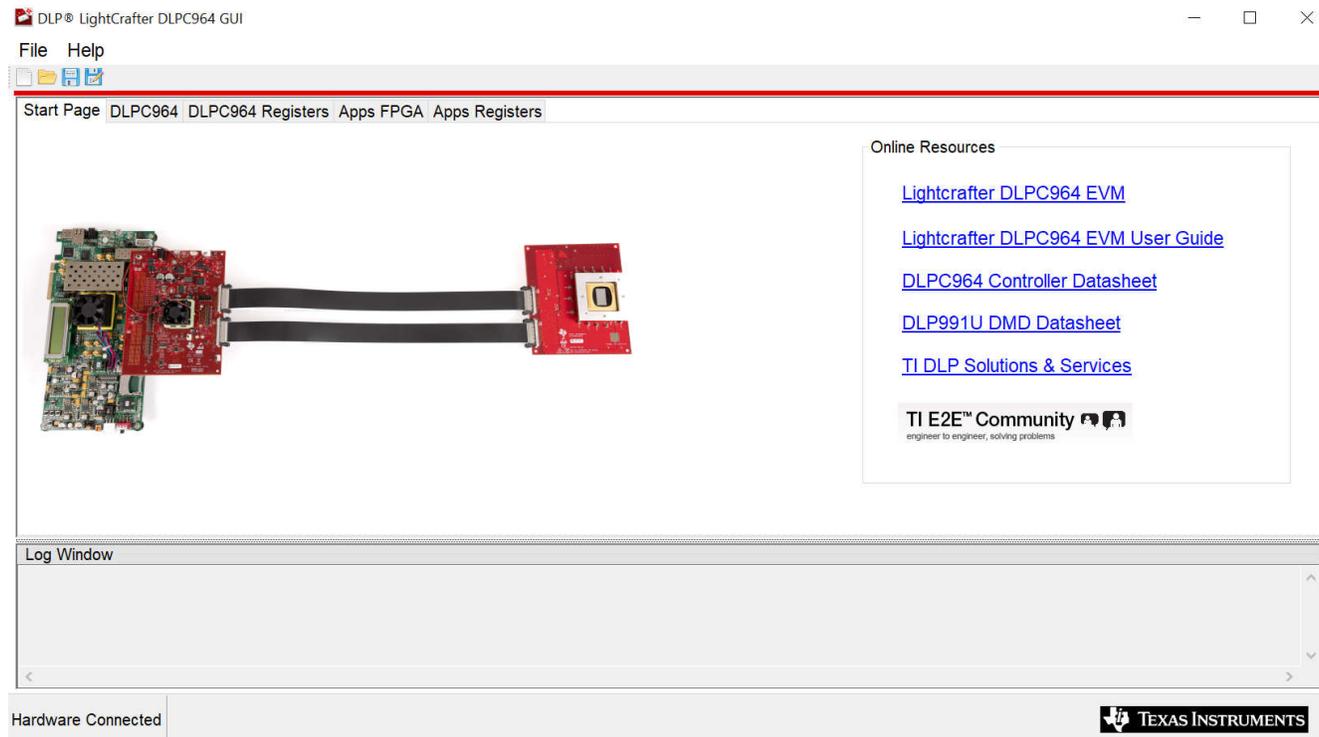
##### 3.1.2 PC Software

Upon execution of the DLPC964 GUI application, the panel shown in [Figure 4-1](#) is displayed. The GUI interface contains the following:

- Menu Bar (top)
- Main window with five sub-windows
- Hardware Connected - information bar (bottom)
- Log window (bottom)
- Online Resources

The five sub-windows are:

- Start Page
- DLPC964 Tab
- DLPC964 Registers Tab
- Apps FPGA Tab
- Apps FPGA Registers Tab



**Figure 3-1. DLPC964 GUI**

### 3.1.3 Menu Bar

The DLPC964 GUI Menu bar consists of two items:

#### 1. File Menu

- **New Log** empties the Status sub-window to record a new command log sequence.
- **Open Log** opens a dialogue box to select an existing command log sequence file from the disk.
- **Save Log** saves the current contents of the Status sub-window to the current script file. If the file is not yet saved the save as dialogue opens.
- **Save Log As** opens a dialogue box to save the current command log sequence with a new name.

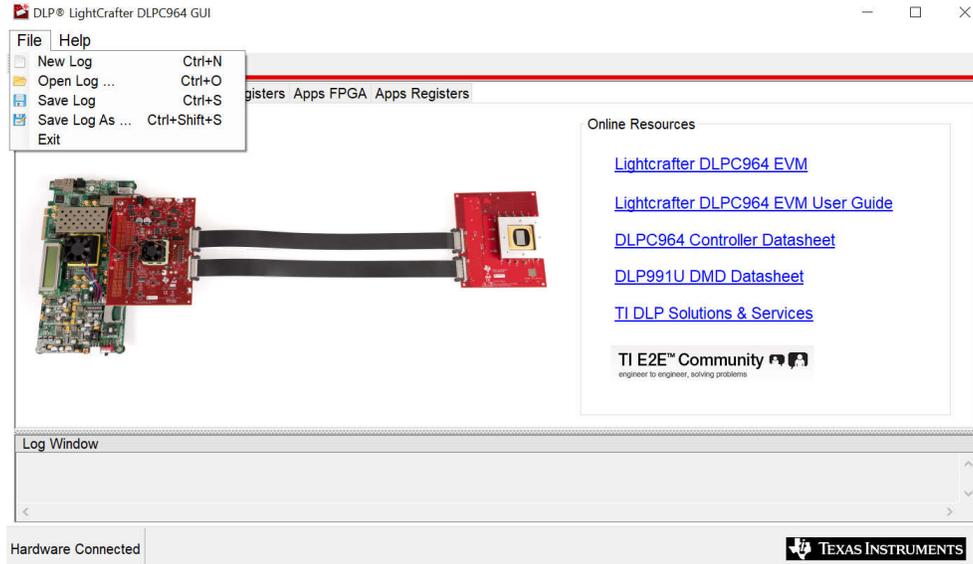


Figure 3-2. Menu Log Items

#### 2. Help Menu

- About DLP® LightCrafter DLPC964 GUI displays the Software Version (X.X.X) and USB DLL Version information box:



Figure 3-3. DLPC964 GUI About Box

### 3.1.4 Main Window

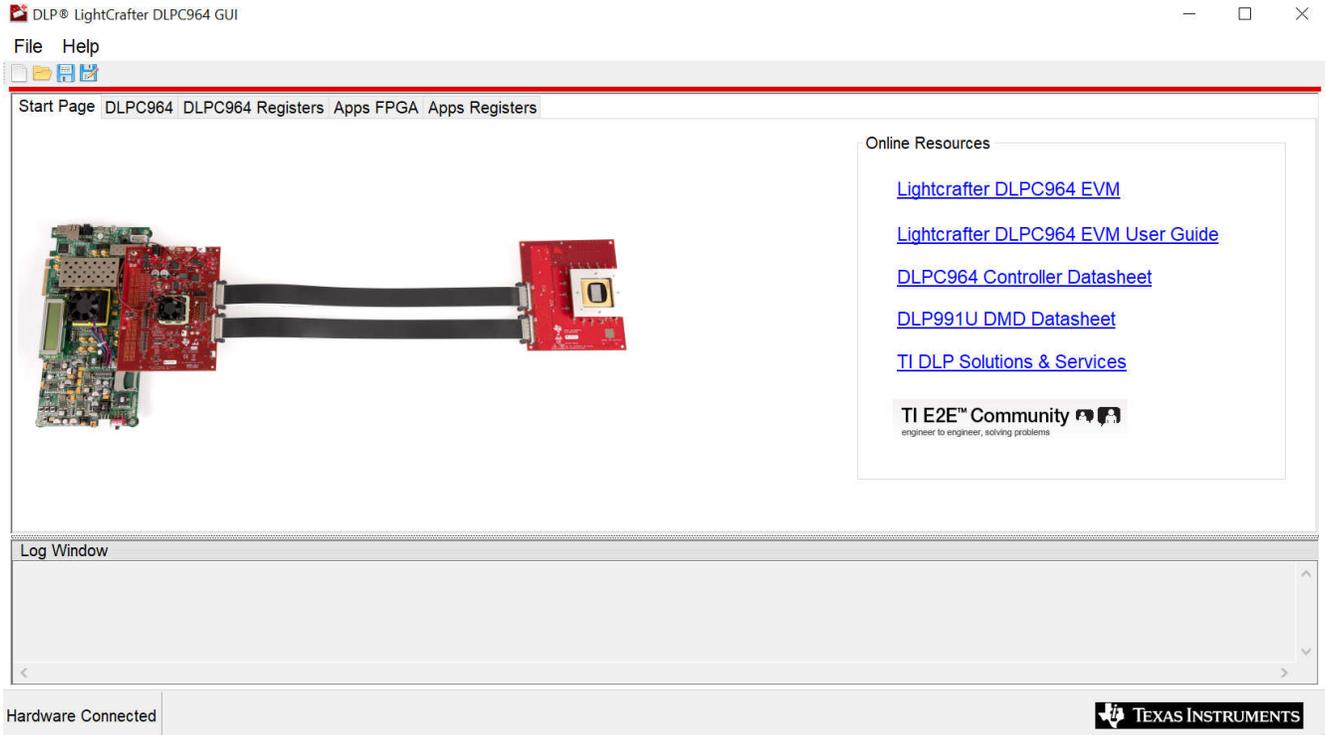
The main window consists of five sub-windows:

#### 3.1.4.1 Start Page

The Start Page is the first window that users see upon executing the DLPC964 GUI.

This window has the image of a standard setup for the Apps FPGA (AMD EVM) with DLPLC964EVM and DLPLCR99EVM.

There are also online resources to help enable customers in getting Evaluation Module Kits started.



**Figure 3-4. DLPC964 GUI Start Window**

If the DLPC964 GUI states that Hardware is not connected, then check:

- The USB connection on J9 and/or the USB connection via the user's PC.
- The DLPC964 driver in Device Manager with the .inf file provided from the GUI software installation.

#### Note

The .inf file is located under: C:\Program Files\Texas Instruments\DLPC964REF-SW-VX.X.XX\Driver\Win10\64.

### 3.1.4.2 DLPC964 Tab

The **DLPC964 tab** read the status of the DLPC964 features and functions. HSSI, HSS, PLL, select test patterns and configure test pattern settings.

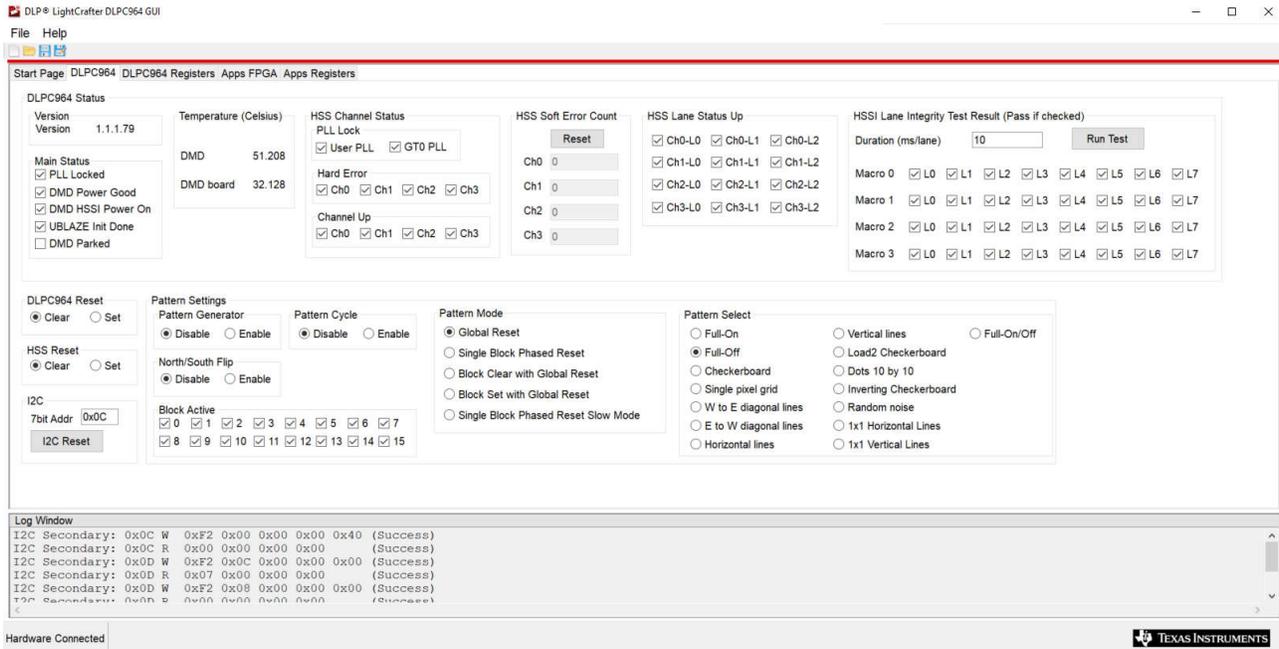


Figure 3-5. DLPC964 Tab

#### 3.1.4.2.1 DLPC964 Status

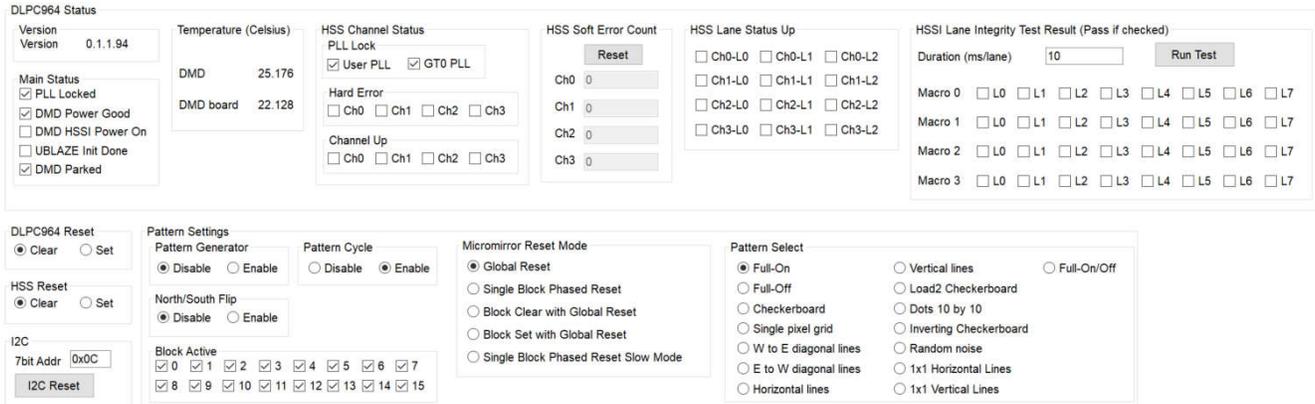


Figure 3-6. DLPC964 Status

- **DLPC964 Version** - Contains the build number and version information for the DLPC964 Firmware.
- **DLPC964 Temperature** - Displays the temperature of the DMD in Celsius
  - **DMD** - DMD internal temperature
  - **DMD Board** - Surface temperature of physical DMD board
- **Main Status** - Contains the status of the DLPC964 PLL Lock, DMD POWERGOOD, DMD High Speed Interface, UBLAZE, and DMD Parked.
- **HSS Channel Status** - Indicates the status of the Aurora 64B/66B inputs to the DLPC964 Controller.
  - **PLL Lock**
    - **User PLL** - When unchecked, the user clock is not lock. When checked, user clock is locked.
    - **GT0 PLL** - The source for the MMCM to generate the user clock and determines if the PLL is lock.
  - **Hard Error** - Indicates if the HSS requires a reset to recover from a hard error condition.
  - **Channel Up** - Determines if the Aurora Channels 0-3 are up and running.

- **HSS Soft Error Count** - Contains the Aurora 64B/66B Channel 0-3 total soft error count.
- **HSS Lane Status Up** - Indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC964 Controller.
- **HSSI Lane Integrity Test Results** - The Lane Integrity Test contains the testing results of DMD High Speed Serial Interface for Channels 0-3. Each lane for this interface (7:0) can be checked for passing results.

**Note**

If the Channels are not passing, this results in a DMD Interface D-Sync Error.

**3.1.4.2.2 DLPC964 Reset**



**Figure 3-7. DLPC964 Reset**

The **DLPC964 Reset** command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the pattern that is currently selected from Pattern Select. You can choose to reset all the blocks (**Global**), or you can choose to reset blocks individually using **Single Block Mode**.

**3.1.4.2.3 HSS Reset**



**Figure 3-8. HSS Reset**

The HSS Reset command causes the HSS input and output buses to reset the data going to the DLPC964.

**3.1.4.2.4 I<sup>2</sup>C 7-bit Addr**



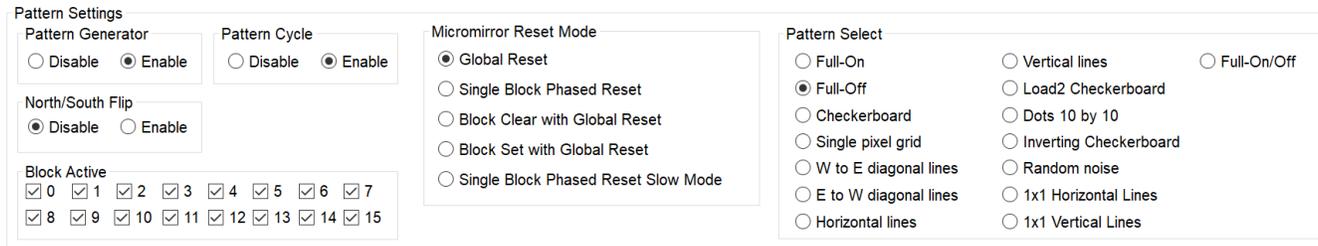
**Figure 3-9. DLPC964 I<sup>2</sup>C 7-bit Addr**

This allows for an alternate I<sup>2</sup>C address to be reset.

**Note**

When J6 and J8 are left unconnected, the default I<sup>2</sup>C address is 0x0C. To communicate with the alternate I<sup>2</sup>C addresses, please see [Table 2-3](#) for information regarding the jumpers that must be populated.

### 3.1.4.2.5 Pattern Settings



**Figure 3-10. DLPC964 Pattern Settings**

- **Pattern Generator** - When enabled, patterns are displayed onto the DMD. When disabled, no patterns are going to be displayed on DMD.
- **Pattern Cycle** - When enabled, the DMD cycles through the first eight predefined patterns, each being displayed every 2 seconds. When disabled, a single selected pattern is sent to the DMD.
- **North/South Flip** - Having this enabled flips the image being displayed on the DMD vertically.
- **Pattern Select**
  - **Full-On** - Full white background where all mirrors on the DMD are going to be in the on position.
  - **Full-Off** - Full black background where all mirrors on the DMD are going to be in the off position.
  - **Checkerboard** - Black and white checkerboard (64 x 64 pixels).
  - **Single pixel grid** - The border is on to help visualize the extent of the DMD array.
  - **W to E diagonal lines** - Used to check for row data issues.
  - **E to W diagonal lines** - Used to check for row data issues.
  - **Horizontal lines** - Used to check for issues with row loads.
  - **Vertical lines** - Used to check for issues with data bus lines.
  - **Load2 Checkerboard** - A black and white checkerboard pattern (32 x 32 pixels).
  - **Dots 10 by 10** - Single white pixels are spaced 10 pixels evenly in the X and Y direction.
  - **Inverting Checkerboard** - Inverted version of the checkerboard pattern.
  - **Random Noise** - Randomized noise pattern for customer tilt angle testing.
  - **1x1 Horizontal lines** (every row alternating black/white) - used to check for issues with row loads.
  - **1x1 Vertical lines** (every column alternating black/white) - used to check for issues with data bus lines.
  - **Full-On/Off** - Toggles between the Full-On and Full-Off pattern.
- **Micromirror Reset Mode**
  - **Global Reset** - In global reset mode, all enabled blocks are going to be loaded with data sequentially. Once all blocks have been loaded, the MCP\_Start signal resets all the blocks at the same time.
  - **Single Block Phased Reset** - In single reset mode, a single block is loaded at a time and once the DLPC964 has loaded the DMD with the data sent, the MCP\_Start signal resets that single block.
  - **Block Clear with Global Reset** - This mode shows how the Clear block load type is used in the DLPC964 system. A clear load type does not require any data since the block puts all of the mirrors in the off state (0). Since the clear load type does not have any data to be sent after, the command valid signal is not needed so only the DMD load signal is sent. The MCP\_Start signal follows the same pattern as Global Mode.
  - **Block Set with Global Reset** - This mode shows how the Set block load type is used in the DLPC964 system. A set load type does the opposite of the clear load type and also does not require any data. The set load type sets all the mirrors in the on state (1). Just like the clear load type, there is no need for the command valid signal, only the DMD load signal. The MCP\_Start signal follows the same pattern as Global Mode.
  - **Single Block Phased Reset Slow Mode** - Slow mode (or disabling the fast mode) causes the DLPC964 to receive data across a single channel only (4x 10Gbps lanes compared to 12x). To do this, each segment of a block must be sent sequentially across 1 Aurora 64B/66B channel instead of parallel. The segments must be sent in the following order: D (0x3) C (0x2) B (0x1) A (0x0). Once all four segments are sent, the MCP\_Start signal can be issued. The MCP\_Start signal behaves the same as in Single Mode.
- **Block Active** - There are 16 blocks [0-15] in the DLP991U DMD. The blocks that are checked inside the GUI are going to determine what blocks are going to be reset and loaded with new data from the DMD.

### 3.1.4.3 DLPC964 Registers Tab

The DLPC964 Registers tab uses the I<sup>2</sup>C Interface to communicate with the DLPC964 controller registers. This tab shows the DLPC964 controller register list and settings for each register which use Get/Set buttons to read/write to specific registers.

#### Note

Access to the DLPC964 registers must not begin until INIT\_DONE has transitioned high (logic 1).

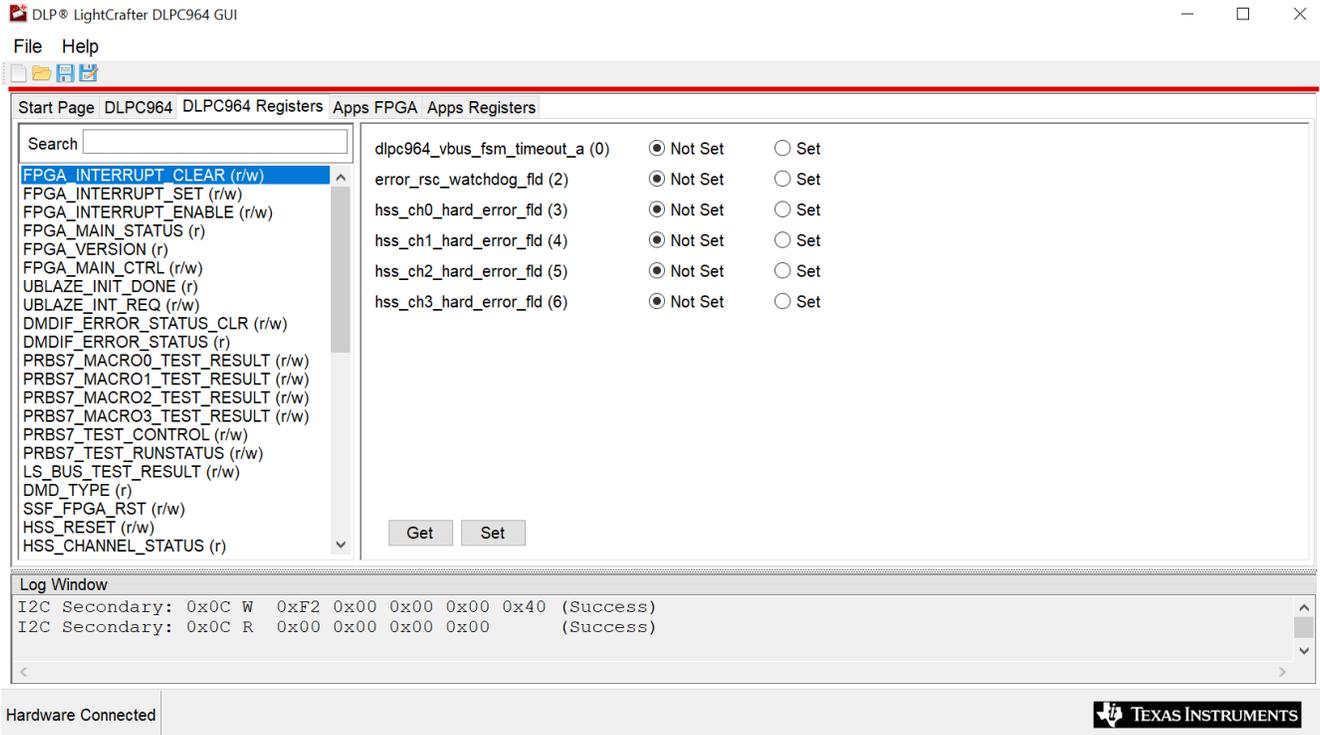


Figure 3-11. DLPC964 Register List

### Register Definitions

The following designations are used throughout this section of the document:

- R - designates read only
- W - designates write only
- R/W - designates read and write
- S - designates status of register
- I - designates interrupt only
- P - designates pulse only

Please visit the [DLPC964 data sheet](#) for detailed descriptions of each DLPC964 register offered in the DLPC964 GUI.

### 3.1.4.4 Apps FPGA Tab

The **Apps FPGA tab** reads the status of Apps FPGA features and functions, select test patterns and configure pattern settings.

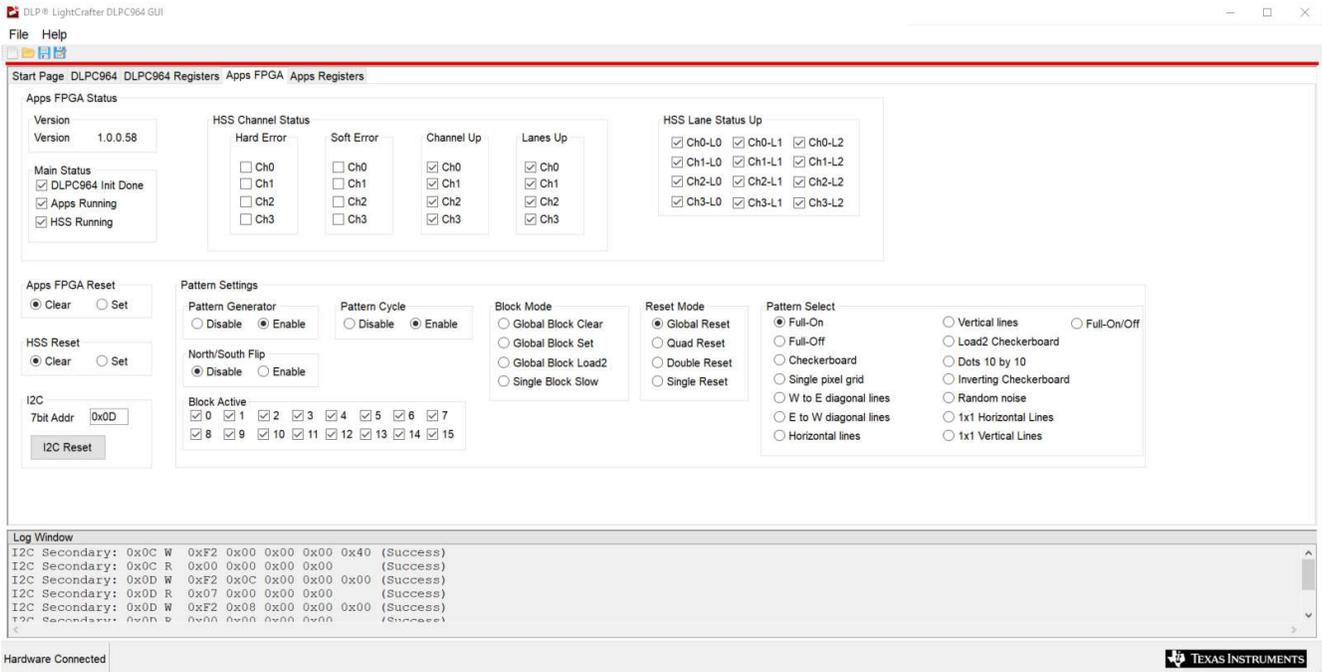


Figure 3-12. Apps FPGA Tab

#### 3.1.4.4.1 Apps FPGA Status

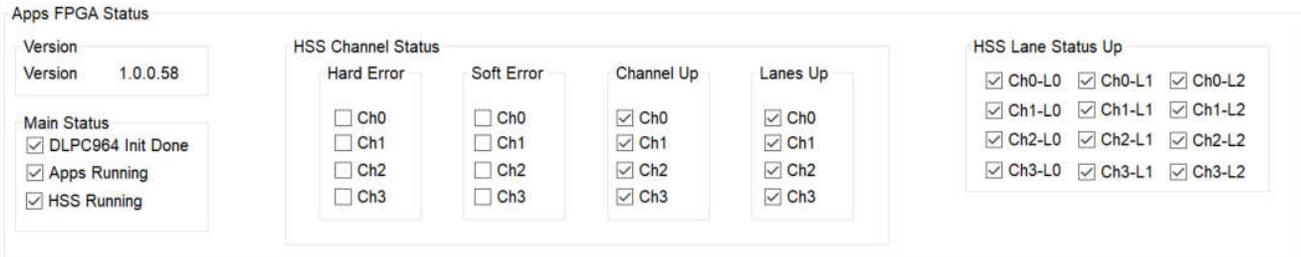
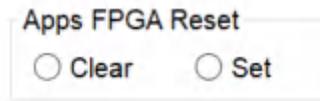


Figure 3-13. Apps FPGA Status

- **Apps FPGA Version** - Contains the build number and version information for the Apps FPGA Firmware.
- **Main Status** - This contains the status for the DLPC964, Apps FPGA, and HSS status determining if each one is up and running.
- **HSS Channel Status** - HSS Channel Status indicates the status of the Aurora 64B/66B inputs to the DLPC964 Controller.
  - **Hard Error** - Input Aurora Channel 0-3 hard error and indicates failure in the GTH.
  - **Soft Error** - The HSS Soft Error Count indicates corrupted data received on each individual channel.
  - **Channel Up** - Determines if the HSS Aurora Channels 0-3 are initialized.
  - **Lanes Up** - Determines if the HSS Aurora Lane Channels 0-3 are initialized.
- **HSS Lane Status Up** - The HSS Lane Status Up indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC964 Controller.

### 3.1.4.4.2 Apps FPGA Reset



**Figure 3-14. Apps FPGA Reset**

The **Apps FPGA Reset** command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the pattern that is currently selected from Pattern Select. You can choose to reset all the blocks (**Global**), or you can choose to reset blocks individually using **Single Block Mode**.

### 3.1.4.4.3 HSS Reset (Apps)



**Figure 3-15. HSS Reset**

The HSS Reset command causes the HSS input and output buses to reset the data of the Aurora 64B/66B interface.

### 3.1.4.4.4 Apps I<sup>2</sup>C 7-bit Addr



**Figure 3-16. DLPC964 I2C 7-bit Addr**

This allows for an alternate I<sup>2</sup>C address to be reset.

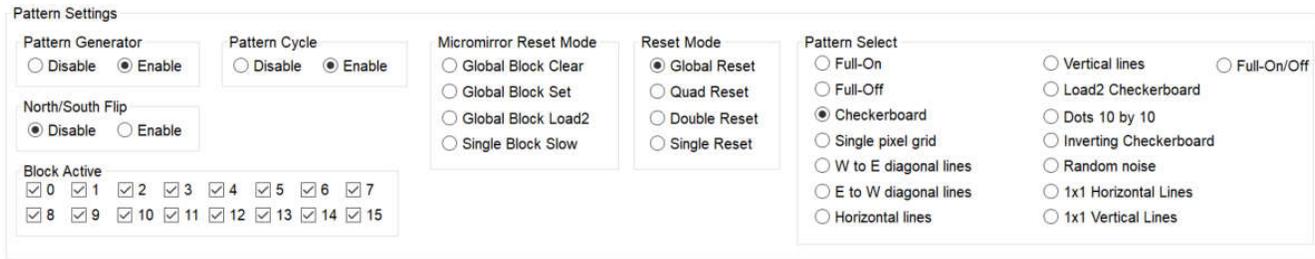
---

**Note**

When J6 and J8 are left unconnected, the default I<sup>2</sup>C address is 0x0D. To communicate with the alternate I2C addresses, please see [Table 2-3](#) for information regarding the jumpers that must be populated.

---

### 3.1.4.4.5 Pattern Settings (Apps)



**Figure 3-17. Apps FPGA Pattern Settings**

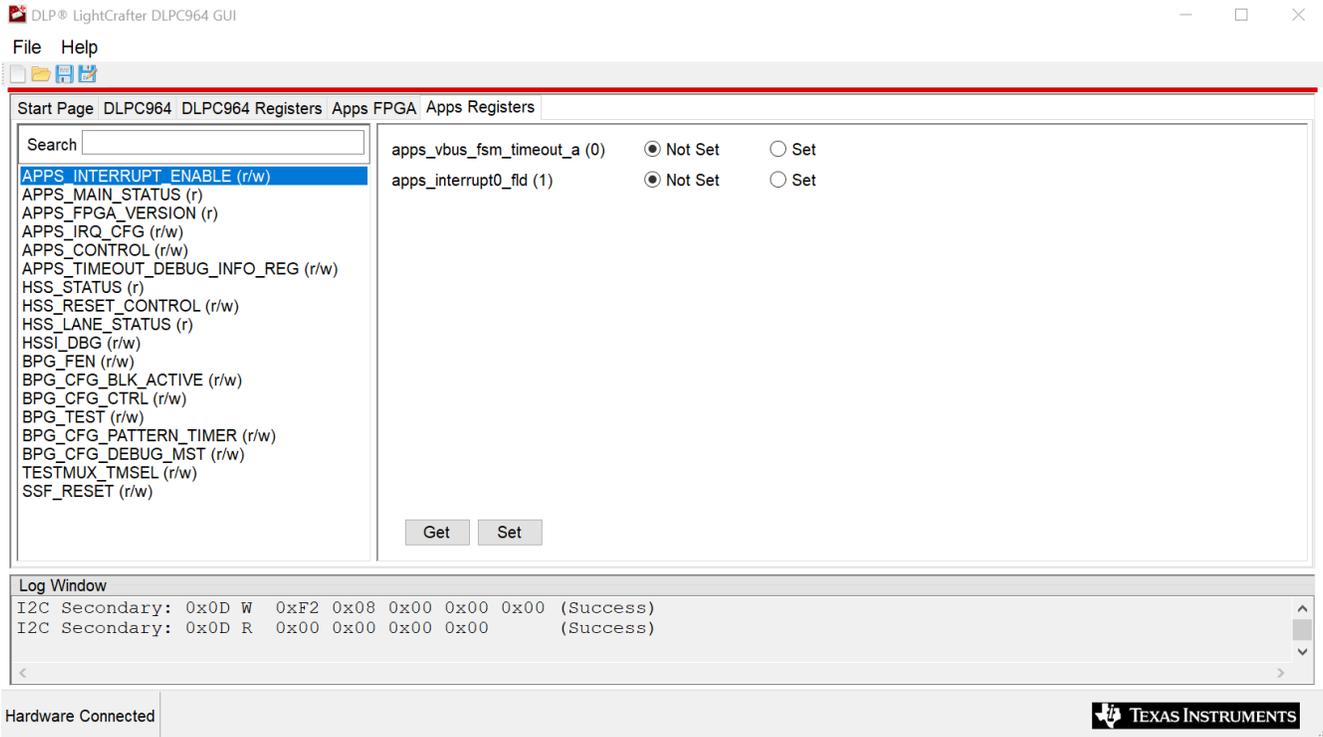
- **Pattern Generator** - When enabled, patterns are displayed onto the DMD. When disabled, no patterns are going to be displayed on DMD.
- **Pattern Cycle** - When enabled, the DMD cycles through the first 8 predefined patterns, each being displayed every 2 seconds. When disabled, a single selected pattern is sent to the DMD.
- **North/South Flip** - Having this enabled flips the image being displayed on the DMD vertically.
- **Pattern Select**
  - **Full-On** - Full white background where all mirrors on the DMD are going to be in the on position.
  - **Full-Off** - Full black background where all mirrors on the DMD are going to be in the off position.
  - **Checkerboard** - Black and white checkerboard (64 x 64 pixels).
  - **Single pixel grid** - The border is on to help visualize the extent of the DMD array.
  - **W to E diagonal lines** - Used to check for row data issues.
  - **E to W diagonal lines** - Used to check for row data issues.
  - **Horizontal lines** - Used to check for issues with row loads.
  - **Vertical lines** - Used to check for issues with data bus lines.
  - **Load2 Checkerboard** - A black and white checkerboard pattern (32 x 32 pixels).
  - **Dots 10 by 10** - Single white pixels are spaced 10 pixels evenly in the X and Y direction.
  - **Inverting Checkerboard** - Inverted version of the checkerboard pattern.
  - **Random Noise** - Randomized noise pattern for customer tilt angle testing.
  - **1x1 Horizontal lines** (every row alternating black/white) - Used to check for issues with row loads.
  - **1x1 Vertical lines** (every column alternating black/white) - Used to check for issues with data bus lines.
  - **Full-On/Off** - Toggles between the Full-On and Full-Off pattern.
- **Micromirror Reset Mode**
  - **Global Block Clear** - This mode shows how the Clear block load type is used in the DLPC964 system. A clear load type does not require any data since the block puts all of the mirrors in the off state (0). Since the clear load type does not have any data to be sent, the command valid signal is not needed so only the DMD load signal is sent. The MCP\_Start signal follows the same pattern as Global Mode.
  - **Global Block Set** - This mode shows how the Set block load type is used in the DLPC964 system. A set load type does the opposite of the clear load type and also does not require any data. The set load type sets all the mirrors in the on state (1). Just like the clear load type, there is no need for the command valid signal, only the DMD load signal. The MCP\_Start signal follows the same pattern as Global Mode.
  - **Global Block Load2** - Enabling the Load2 operation tells the DMD to load 1 line of data received into 2 rows of the DMD. The role of the DLPC964 Apps FPGA during a Load2 operation is to verify that 68 lines, at most, are sent over the Aurora HSSI channels. Asserting LOAD2 causes the DLPC964 controller and attached DMD to load 2 rows for every row of data sent, reducing the pattern load time to half of a full DMD load. This function does not reduce the MCP timing.
  - **Single Block Slow** - Slow mode (or disabling the fast mode) causes the DLPC964 Apps FPGA to send data across a single Aurora 64B/66B channel only (4x 10Gbps lanes compared to 12x). To do this, each segment of a block must be sent sequentially across 1 channel instead of parallel. The segments must be sent in the following order: D (0x3) C (0x2) B (0x1) A (0x0). Once all four segments are sent, the MCP\_Start signal can be issued. The MCP\_Start signal behaves the same as in Single Mode.
- **Block Active** - There are 16 blocks [0-15] in the DLP991U DMD. The blocks that are checked inside the GUI are going to determine what blocks are going to be reset and loaded with new data to the DMD.

### 3.1.4.5 Apps FPGA Registers Tab

The Apps FPGA Registers tab uses the I<sup>2</sup>C Interface to communicate with the Apps FPGA registers. This tab shows the Apps FPGA register list and settings for each register which use Get/Set buttons to read/write to specific registers.

**Note**

Access to the Apps FPGA registers must not begin until INIT\_DONE has transitioned high (logic 1).



**Figure 3-18. Apps FPGA Register List**

### Register Definitions

The following designations are used throughout this section of the document:

- R - designates read only
- W - designates write only
- R/W - designates read and write
- S - designates status of register
- I - designates interrupt only
- P - designates pulse only

Please visit the [DLPC964 data sheet](#) for detailed descriptions of each Apps FPGA register offered in the DLPC964 GUI.

### 3.1.5 Programming Firmware

#### 3.1.5.1 Connecting to the DLPC964 GUI

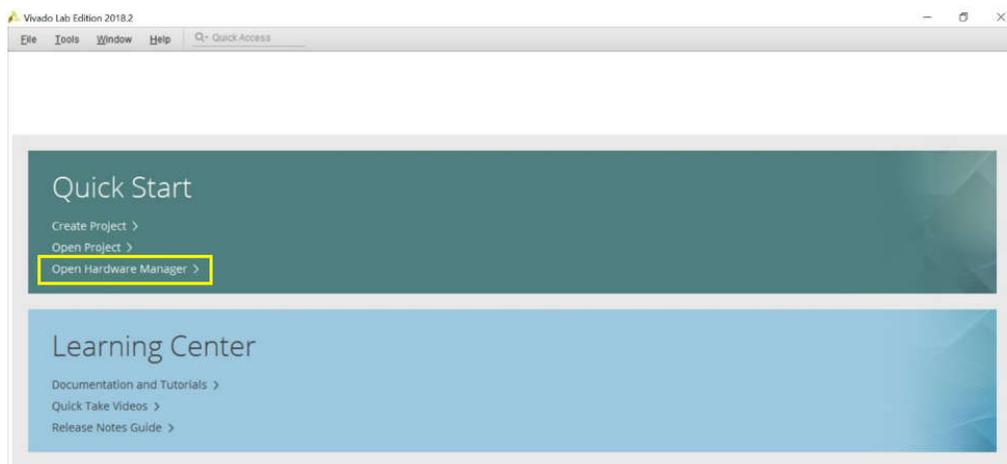
1. Connect the boards as shown in previous slides. There are two configurations:
  - a. Apps FPGA with DLPC964 controller board and DLP991U DMD board.
  - b. Standalone DLPC964 controller board with DLP991U DMD board.
2. Power DLPC964 controller board using 12V DC input.
3. Power on AMD EVM (if present).
4. Connect USB from DLPC964 controller board to PC.
5. Run TI DLP DLPC964 GUI.
6. GUI displays *Hardware Connected* message in bottom left corner of status bar.

#### 3.1.5.2 Programming the DLPC964 Controller

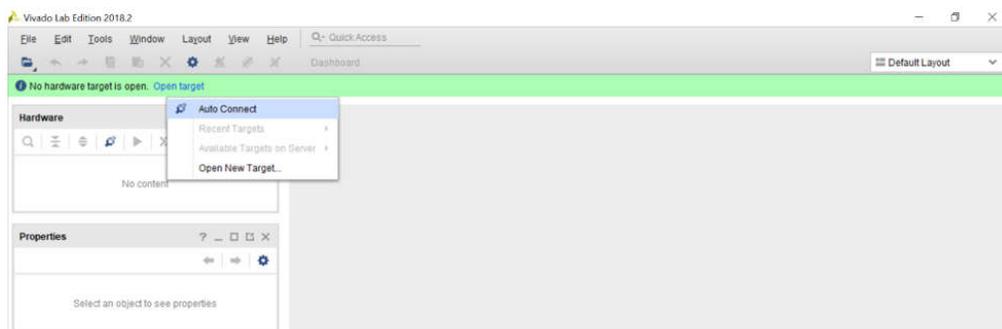
1. Launch the [Vivado Lab Solutions 2018.2](#) application. Once the application opens, select *Open Hardware Manager* from the main window.

#### Note

Click the link above to download Vivado Lab Solutions 2018.2. Once the web page is loaded, find the archived 2018.2 folder and then navigate to the Vivado Lab Solutions 2018.2 downloadable link and download the installation.



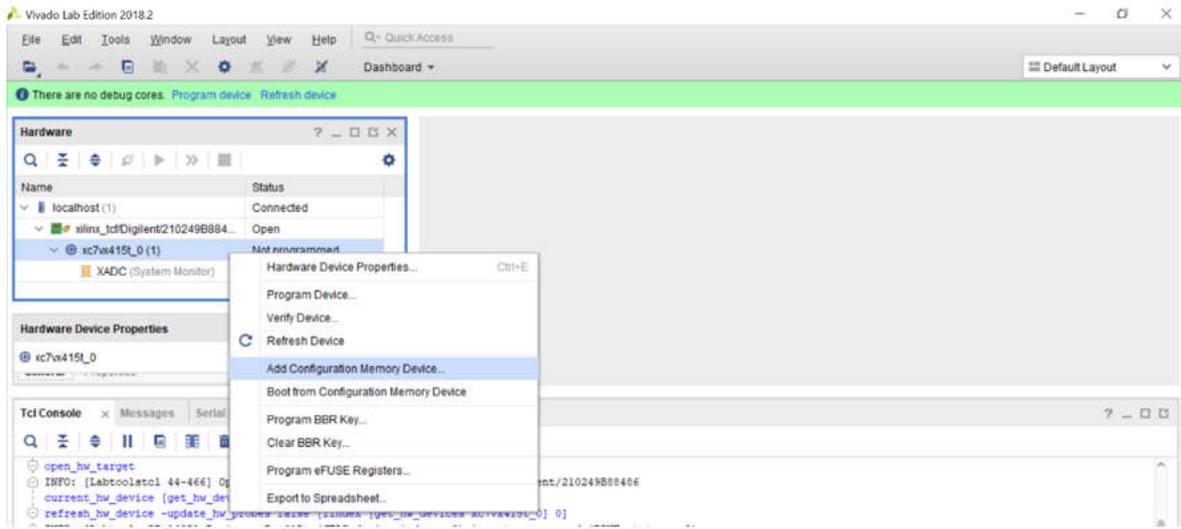
2. Once the Hardware Manager is open, check that the JTAG is connected to jumper J7 on the DLPLC964EVM board and that the port is connected to a PC. Once JTAG is properly connected, plug the 12V DC power supply into the barrel jack on the board and power on.
3. Once JTAG is properly connected and the board is powered on, the next step is selecting the target device that is going to be programmed.
4. In the *Hardware Manager* window, select *Open Target > Auto Connect* to find the target device being programmed.



- Once the target device is detected, the target device is going to be displayed in the bottom left corner, showing current status of device.



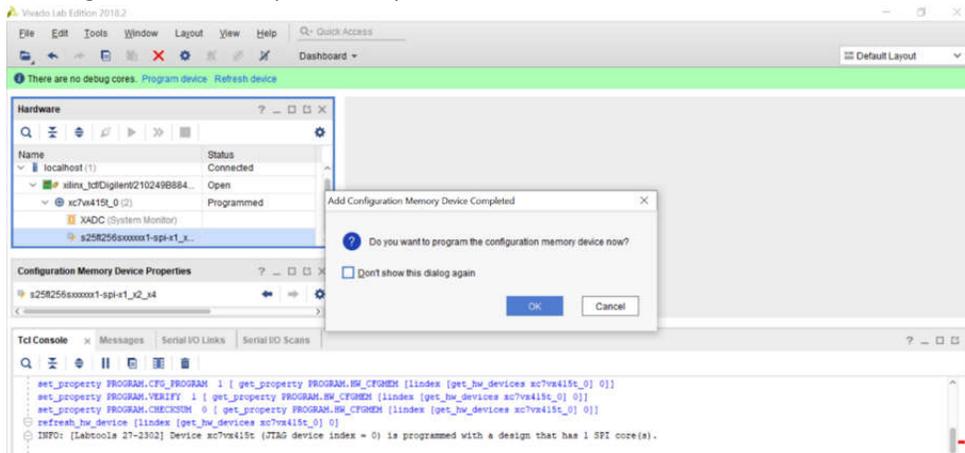
- Right-click on the FPGA and select “Add Configuration Memory Device.”



- Select the correct flash device that is connected to the FPGA device on the DLPLCRC964EVM board. Input the parameters below to select the correct flash device.

Manufacturer = Spansion	Type = SPI
Density = 256Mb	Width = x1_x2_x4
Part Number = s25fl256sxxxxx1	

- Once the appropriate flash device is selected, a dialog box is going to pop up asking if the user wants to program the configuration device (SPI Flash). Click OK.

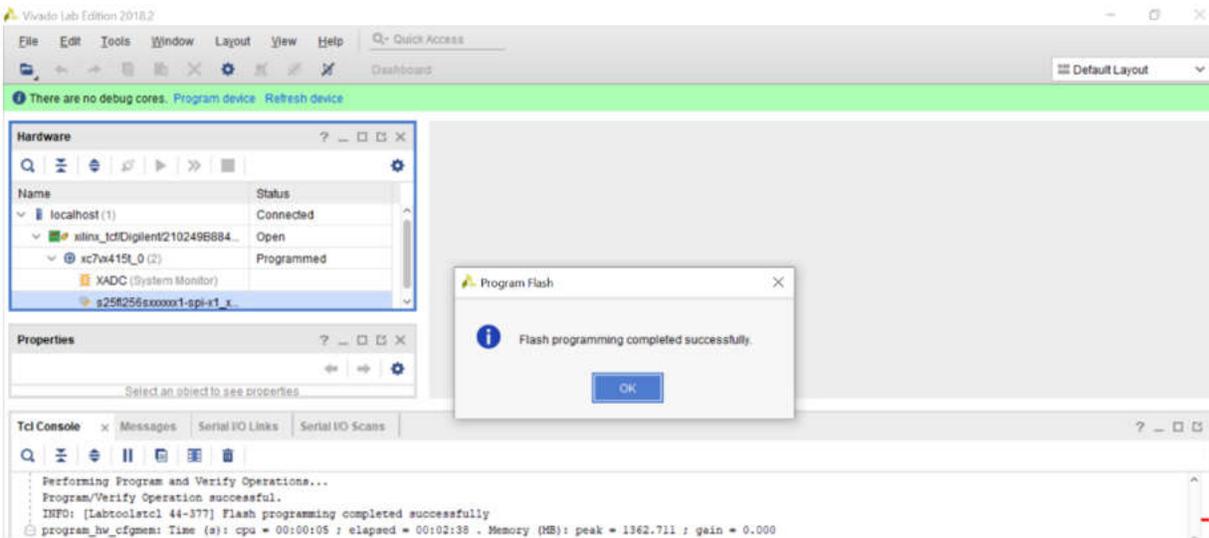


- Go to Configuration file and select the appropriate .mcs file needed to program the flash device.

### Note

The .mcs can be downloaded from the [DLPLCRC964EVM Tool Page](#). Locate and download the [DLPR964-FW package](#) which includes the appropriate .mcs to program the DLPC964 Controller.

- After clicking OK, the Vivado Hardware Manager is going to program the flash of the board and verify that the flash was programmed successfully.



- Complete a power cycle on the DLPLCRC964EVM board. Unplug power from the barrel jack connector J3 and then plug power back into barrel jack connector. After the FPGA is programmed successfully, DLPC964 Done (D4) is going to illuminate green and the DLPC964 Heartbeat (D5) has a heartbeat that flashes on/off.

### 3.1.5.3 Programming the Apps FPGA (AMD EVM)

#### 3.1.5.3.1 Programming the Apps FPGA with Bitstream Loading

Follow the instructions below for loading the DLPC964 Apps binary onto the FPGA via a bitstream using [Vivado Lab Solutions 2018.2](#):

---

**Note**

Click the link above to download Vivado Lab Solutions 2018.2. Once the web page is loaded, find the archived 2018.2 folder and then navigate to the Vivado Lab Solutions 2018.2 downloadable link and download the installation.

---

---

**Note**

The FPGA needs to be reloaded each time power is lost or disconnected from the AMD EVM.

---

1. Plug in the Micro-B USB cable into the side of the VC707 and the other end into the computer running Vivado.
2. Start Vivado Lab Solutions 2018.2 on the computer.
3. Select *Open Hardware Manager* from the main window..
4. Click *open target* located in the top left of the hardware manager then *Auto Connect*.
  - a. If the AMD EVM is the only FPGA plugged into the computer, then Vivado automatically connects to the AMD EVM.
5. Right-click on the FPGA and select *Program Device*.
6. Navigate to the appstop.mcs file and select *Program*.

#### 3.1.5.3.2 Programming Apps FPGA by Flash

Follow the instructions below for loading the DLPC964 Apps binary onto the flash via a bitstream using [Vivado Lab Solutions 2018.2](#):

---

**Note**

Click the link above to download Vivado Lab Solutions 2018.2. Once the web page is loaded, find the archived 2018.2 folder and then navigate to the Vivado Lab Solutions 2018.2 downloadable link and download the installation.

---

---

**Note**

The bitstream is always loaded onto the FPGA upon power-up of the AMD EVM.

---

1. Plug in the micro USB into the side of the AMD EVM and the other end into the computer running Vivado.
2. Make sure to set SW11 to 00010 (1 = on, Position 1 → Position 5, left to right).



**Figure 3-19. FPGA Configuration Mode**

3. Set SW2 to 00000000 (1 = on, Position 1 → Position 8, left to right).



**Figure 3-20. GPIO Dip Switches (VC707)**

4. Start Vivado Lab Studios 2018.2 on the computer.
5. Select *Open Hardware Manager* from the main window.
6. Click *open target* located in the top left of the hardware manager then *Auto Connect*.
  - a. If the AMD EVM is the only FPGA plugged into the computer, then Vivado automatically connects to the AMD EVM. Otherwise, the process is slightly more involved.
7. Right-click on the FPGA and select *Add Configuration Memory Device*.
8. Find the Flash name *mt28gu01gaax1e-bpi-x16* and click *OK*.
9. Select *OK* again and select the configuration file (*appstop.mcs*).
  - a. Make sure all other settings match.
10. Once setup, click *OK*. The programming can take a few minutes.
11. Once completed, power cycle the AMD EVM, and the DLPC964 Apps Bitstream automatically loads onto the AMD EVM.

## 4 Hardware Design Files

### 4.1 Schematics

The schematics are available for download on the [DLPLCRC964EVM Tool Folder](#).

### 4.2 PCB Layout

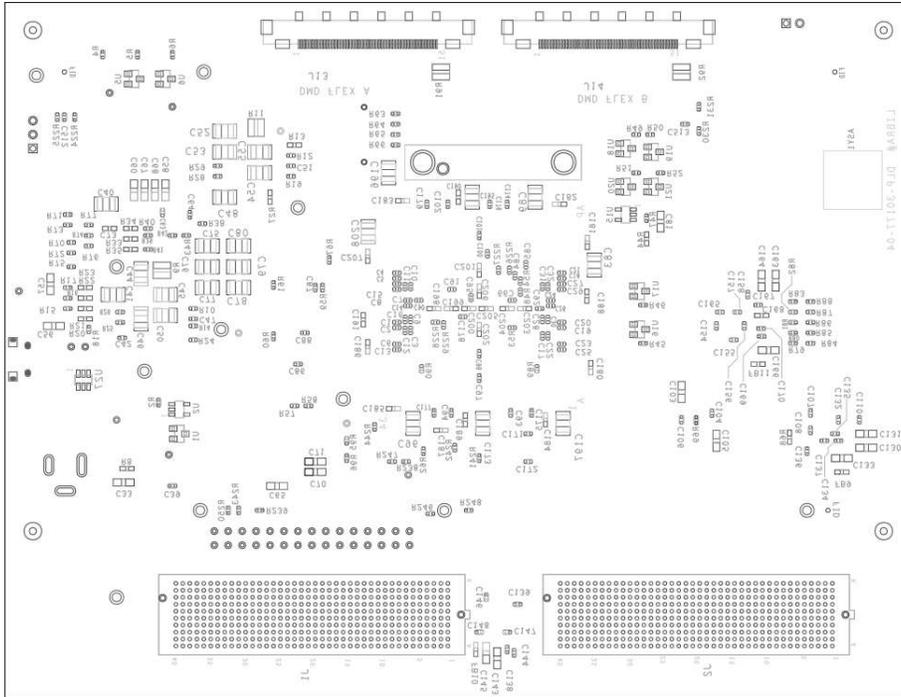


Figure 4-1. DLPLCRC964EVM PCB (Front)

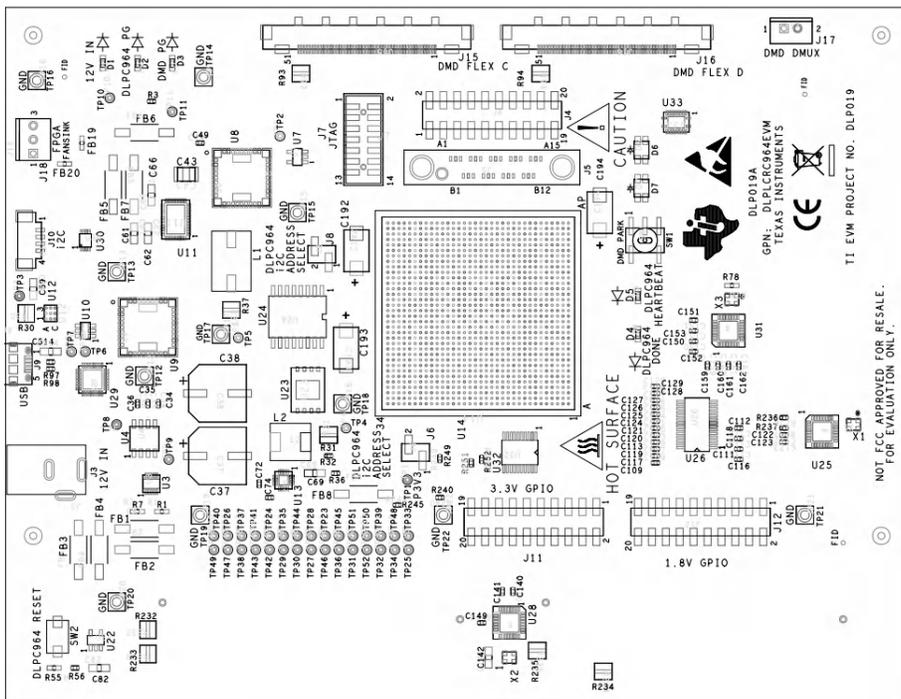


Figure 4-2. DLPLCRC964EVM PCB (Back)

### 4.3 Bill of Materials

Table 4-1 lists the Bill of Materials for the DLPLCRC964EVM.

**Table 4-1. DLPLCRC964EVM Bill of Materials**

Reference	Quantity	Part	MFG	MFG Part Number
C1,C2,C3,C4,C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15,C16,C17,C18, C19,C20,C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C31,C32	32	0.1u	American Technical Ceramics	530L104KT16T
C33	1	22u	Samsung	CL21A226MOCLRNC
C34,C35,C36,C39,C42,C49,C64,C84, C85,C86,C87,C88,C90,C91,C92,C93, C94,C95,C97,C98,C99,C100,C101, C102,C104,C106,C107,C108,C109, C111,C112,C113,C116,C117,C118, C119,C120,C121,C122,C123,C124, C125,C126,C127,C128,C129,C132, C134,C135,C136,C139,C140,C141, C144,C146,C147,C148,C150,C151, C152,C153,C154,C155,C156,C157, C159,C160,C161,C162,C165,C167, C168,C169,C171,C172,C174,C175, C176,C177,C178,C179,C513	82	0.1u	Samsung	CL05A104KA5NNNC
C37,C38	2	1000u	Panasonic	EEE-FT1C102GP
C40,C45,C46,C48,C50,C52,C53, C54,C77,C78,C79,C80,C89,C96, C173,C196,C197	17	100u	Cal-Chip Electronics	GMC32X5R107M16NT
C41,C43,C83,C195	4	47u	KEMET	C1210C476M4PACTU
C44,C55	2	220u	Murata	GRM32ER60J227ME05L
C47,C51	2	0.01u	KEMET	C0402C103K5RACTU
C56,C57,C58,C69,C81,C82,C514	7	1u	Yageo	CC0805KKX7R9BB105
C59,C60,C61,C62,C65, C66,C67,C68,C70,C71	10	22u	Samsung	CL21A226MOCLRNC
C63	1	2200p	Yageo	AC0402KRX7R8BB222
C72,C110,C138,C158	4	0.01u	KEMET	C0402C103K5RACTU
C73,C180,C181,C182,C183,C184, C185,C186,C187,C188,C189,C190, C191,C198,C199,C200,C201,C202, C203,C204,C205,C206,C207	23	4.7u	Murata	GRM188R61E475KE11D
C74	1	3900p	Kyocera	KGM05AR71H392JH
C75,C76,C208	3	330u	Murata	GRM32ER60G337ME05L
C103,C105,C130,C131,C133,C142, C143,C145,C163,C164,C166	11	10u	Samsung	CL21A106KAYNNNE
C137,C149,C170	3	0.047u	Murata	GRM155C71H473KE19D
C192,C193,C194	3	680u	Panasonic	2R5TPF680M6L
C512	1	36p	Yageo	CC0402JRNPO9B360
D1,D2,D3	3	LED_BLUE_SMT	Lite-On	LTST-C193TBKT-5A
D4,D5	2	LED_GREEN_SMT	Lite-On	LTST-C193KGKT-5A
D6,D7	2	DUAL_LED_GRN_RED_SM T	Lite-On	LTST-C155GEKT
FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8	8	FB	Laird	35F0121-1SR-10

**Table 4-1. DLPLCRC964EVM Bill of Materials (continued)**

Reference	Quantity	Part	MFG	MFG Part Number
FB9,FB10,FB11,FB19,FB20	5	FB	Laird	HI0603P600R-10
J1,J2	2	FMC 400POS CONNECTOR	SAMTEC	SEAM-40-11.0-S-10-2-A-K-TR
J3	1	PJ-002AH	CUI	PJ-002AH
J4,J11,J12	3	TSM-110-01-L-DV-P	Samtec	TSM-110-01-L-DV-P
J6,J8	2	TSM-102-01-L-SV	Samtec	TSM-102-01-L-SV
J7	1	JTAG	Molex	878321420
J9	1	10118194-0001LF	Amphenol	10118194-0001LF
J10	1	53398-0471	Molex	533980471
J13,J14,J15,J16	4	FI-RE51S-HF-R1500	JAE	FI-RE51S-HF-R1500
J17	1	B2B-EH	JST	B2B-EH-A(LF)(SN)
J18	1	22-23-2031	Molex	22232031
L1	1	150n	Eaton	FP1107R2-R15-R
L2	1	1uH	TDK	SPM6530T-1R0M120
R1,R27	2	1 Meg	Vishay Dale	CRCW06031M00DHEAP
R2,R47,R56,R62,R67,R238,R239,R240, R241,R242,R243,R244,R245, R246,R247,R248,R249,R250	18	10k	Samsung	RC1005F103CS
R3,R15,R16,R17,R18,R57,R76,R77	8	2.2K	Panasonic	ERJ-2RKF2201X
R4,R5,R6	3	1.8K	Panasonic	ERJ-2GEJ185X
R7	1	150k	Panasonic	ERJ-3EKF1503V
R8	1	130K	Yageo	RC0603FR-07130KL
R9,R11,R30,R31,R37,R91,R92,R93,R94	9	10m	Rohm	LTR18EZPFU10L0
R10,R12,R38,R72,R73,R74,R81,R83, R84,R85,R87,R97,R98,R230, R231,R236,R237	17	0	Samsung	RC1005J000CS
R13,R21,R22,R23,R78	5	100K	TE Connectivity	CRG0603F100K
R14	1	316	Vishay Dale	CRCW0402316RFKED
R19	1	2.15K	Panasonic	ERJ-2RKF2151X
R20,R33,R34,R35,R68	5	100K	TE Connectivity	CRG0603F100K
R24,R39	2	90.9K	Panasonic	ERJ-2RKF9092X
R25,R26,R28,R29,R43,R70,R71,R75, R79,R80,R82,R86,R88	13	0	Samsung	RC1005J000CS
R32	1	80.6K	Panasonic	ERJ-2RKF8062X
R36	1	160k	Panasonic	ERJ-2GEJ164X
R40	1	133k	Yageo	AC0402FR-07133KL
R41	1	42.2K	Panasonic	ERJ-2RKF4222X
R42	1	61.9K	Panasonic	ERJ-2RKF6192X
R44,R55	2	20K	Yageo	ERJ-3EKF2002V
R45,R46,R49,R50,R51,R52	6	270	Panasonic	ERJ-2RKF2700X
R48,R53,R63,R64,R65,R66	6	4.7K	Samsung	RC1005J472CS
R54	1	330	Panasonic	ERJ-2RKF3300X
R58,R61,R224,R225	4	22	Panasonic	ERJ-2GEJ220X
R59,R60	2	2.2K	Panasonic	ERJ-2RKF2201X
R69,R89,R90,R226,R227, R228,R229,R251	8	100	Samsung	RC1005F101CS
R95	1	80.6K	Panasonic	ERJ-2RKF8062X

**Table 4-1. DLPLCRC964EVM Bill of Materials (continued)**

Reference	Quantity	Part	MFG	MFG Part Number
R96	1	160k	Panasonic	ERJ-2GEJ164X
R232,R233,R234,R235	4	10m	Rohm	LTR18EZPFU10L0
R252	1	100	Samsung	RC1005F101CS
SW1	1	SW SPST	C&K COMPONENTS	GT12MSCBE
SW2	1	EVQ-PE105K	Panasonic	EVQ-PE105K
TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8, TP9,TP10,TP11,TP23,TP24,TP25, TP26,TP27,TP28,TP29,TP30,TP31, TP32,TP33,TP34,TP35,TP36,TP37, TP38,TP39,TP40,TP41,TP42,TP43, TP44,TP45,TP46,TP47,TP48,TP49, TP50,TP51,TP52	41	Testpoint		
TP12,TP13,TP14,TP15,TP16, TP17,TP18,TP19,TP21,TP22	10	GND Testpoint	Keystone	5006
TP20	1	GND Testpoint	Keystone	5006
U1	1	N-CHANNEL MOSFET	Diodes Inc	DMN67D8L
U2,U7	2	SN74LVC1G07	Texas Instruments	SN74LVC1G07DBVR
U3	1	TPS259241	Texas Instruments	TPS259241DRCT
U4	1	CSD17579	Texas Instruments	CSD17579Q5AT
U5,U6,U16,U17,U18,U19,U20,U21	8	N-CHANNEL MOSFET	FAIRCHILD SEMI	FDV303N
U8,U9	2	LMZ31710	Texas Instruments	LMZ31710RVQR
U10	1	LM3880-1AE	Texas Instruments	LM3880QMFE-1AE/NOPB
U11	1	TPS548B22	Texas Instruments	TPS548B22RVFT
U12	1	TPS8268180	Texas Instruments	TPS8268180SIPT
U13	1	TPS62095	Texas Instruments	TPS62095RGTR
U14	1	DLPC964ZUM	DLP	DLPC964ZUM
U15,U22	2	SN74LVC1G17	Texas Instruments	SN74LVC1G17DBVRG4
U23	1	S25FS256SAGNF	Cypress	S25FS256SAGNFI000
U24	1	S25FL256SAGMFI01	Cypress	S25FL256SAGMFI011
U25	1	CDCM61002	Texas Instruments	CDCM61002RHBR
U26	1	DS90LV110T	Texas Instruments	DS90LV110TMT/NOPB
U27	1	TPD4E1U06	Texas Instruments	TPD4E1U06DBVR
U28	1	CDCM61001	Texas Instruments	CDCM61001RHBT
U29	1	CY7C65215	Cypress	CY7C65215-32LTXI
U30	1	TCA9406	Texas Instruments	TCA9406DCUR
U31	1	CDCM61004	Texas Instruments	CDCM61004RHBT
U32	1	TXB0108PWR	Texas Instruments	TXB0108PWR
U33	1	SN74AUC245	Texas Instruments	SN74AUC245RGYR
X1,X2	2	ASDMB-25.000MHZ	Abracon	ASDMB-25.000MHZ-LY-T
X3	1	DSC6111JE1A- PROGRAMMABLE	Microchip	DSC6111JE1A- PROGRAMMABLE

## 5 Additional Information

### 5.1 Abbreviations and Acronyms

The following lists abbreviations and acronyms used in this manual:

<b>Apps FPGA</b>	AMD Xilinx Virtex 7 FPGA on the VC-707 EVM or similar board for customer applications
<b>BOM</b>	Bill of Materials
<b>BPG</b>	Bitplane Pattern Generator
<b>DLL</b>	Dynamic Link Library
<b>DMD</b>	Digital Micromirror Device
<b>EVM</b>	Evaluation Module (Board)
<b>FMC</b>	FPGA Mezzanine Connector
<b>FPGA</b>	Field Programmable Gate Array
<b>FW</b>	Firmware
<b>GPIO</b>	General Purpose Input Output
<b>GUI</b>	Graphical User Interface
<b>HPC</b>	High Pin Count
<b>HSS</b>	High Speed Serial
<b>HSSI</b>	High Speed Serial Interface
<b>HW</b>	Hardware
<b>I<sup>2</sup>C</b>	Inter-Integrated Circuit
<b>LED</b>	Light Emitting Diode
<b>MCP</b>	Mirror Clocking Pulse
<b>NC</b>	Not Connected
<b>PC</b>	Personal Computer
<b>PCB</b>	Printed Circuit Board
<b>PG</b>	Power Good
<b>PLL</b>	Phase-Locked Loop
<b>PROM</b>	Programmable Read-Only Memory
<b>SW</b>	Switch
<b>USB</b>	Universal Serial Bus
<b>VHDL</b>	Verification and Hardware Description Language

### 5.2 Trademarks

LightCrafter™ is a trademark of Texas Instruments.

Xilinx™ and Virtex™ are trademarks of Xilinx, Inc.

DLP® is a registered trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 5.3 References

1. [Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit](#)
2. [VC707 Evaluation Board for Virtex-7 FPGA](#)
3. [DLPC964 Apps FPGA User's Guide](#)

## 5.4 Safety

### 5.4.1 Caution Labels

**CAUTION**



To minimize the risk of fire or equipment damage, make sure that air is allowed to circulate freely around the DLPLCRC964EVM controller board while operating.

**CAUTION**



**ATTENTION  
STATIC SENSITIVE DEVICES**

HANDLE ONLY AT  
STATIC SAFE WORK STATIONS

The DLPLCRC964EVM contains ESD-sensitive components.  
Handle with care to prevent permanent damage.

## 6 Related Documentation from Texas Instruments

Component data sheets, technical documents, design documents, and ordering information can be found at the following links:

- [DLPC964 Digital Controller Product Folder](#)
- [DLP LightCrafter DLPC964 EVM Tool Folder](#)
- [DLP991UFLV DMD Product Folder](#)
- [DLP LightCrafter DLP991UFLV DMD EVM Product Folder](#)
- [DLPC964 Apps FPGA Guide](#)

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (October 2023) to Revision A (March 2024)</b>	<b>Page</b>
• Added <i>Specifcation</i> and <i>Device Information</i> sections.....	2
• Added sections to describe the hardware of DLPLCRC964EVM.....	5
• Added sections to describe how to operate DLPLCRC964EVM with DLPC964 GUI.....	17
• Added <i>Hardware Design Files</i> for DLPLCRC964EVM.....	33
• Added additional information and resources for DLPLCRC964EVM.....	37

## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
  - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
  - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
  - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
  - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
  - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

### **WARNING**

**Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.**

**User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.**

**NOTE:**

**EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.**

### 3 Regulatory Notices:

#### 3.1 United States

##### 3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

##### 3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

#### **FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

#### 3.2 Canada

##### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### **Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### **Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

#### 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_02.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page)

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#### 3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

- 
- 4 *EVM Use Restrictions and Warnings:*
    - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
    - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
    - 4.3 *Safety-Related Warnings and Restrictions:*
      - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
      - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
    - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
  5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
  6. *Disclaimers:*
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