参考資料

TI Designs: TIDA-01639
スタンドアロンのデジタル・フィルタを備えた絶縁シャント電流測定のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、絶縁変調器とスタンドアロンのデジタル・フィルタを使用して、絶縁シャント・センサによるクラス0.5の三相エネルギー測定システムを実装しています。同期フィルタを内蔵する必要がないため、より広範なホスト・マイクロコントローラ(MCU)を選択できます。このデザインでは、絶縁変調器で検出した電流と、ホスト・マイクロコントローラで検出した位相電圧とを同期させることで、SimpleLink™ ARM® Cortex®M4ホストMCUを使用する高度な計測アルゴリズムにも対応します。このデザインは、電流センサと電源に変圧器や他の磁気的な部品を使用していないため、磁気的なタンパ攻撃に耐性があります。このサブシステムのデザインはテスト済みであり、ハードウェアを含みます。

リソース

TIDA-01639	デザイン・フォルダ
AMC1106M05	プロダクト・フォルダ
AMC1210	プロダクト・フォルダ
TLV9001	プロダクト・フォルダ
MSP432P4111	プロダクト・フォルダ
TPS3850	プロダクト・フォルダ
TVS0500	プロダクト・フォルダ
TPD1E04U04	プロダクト・フォルダ

TI E2E™ Community

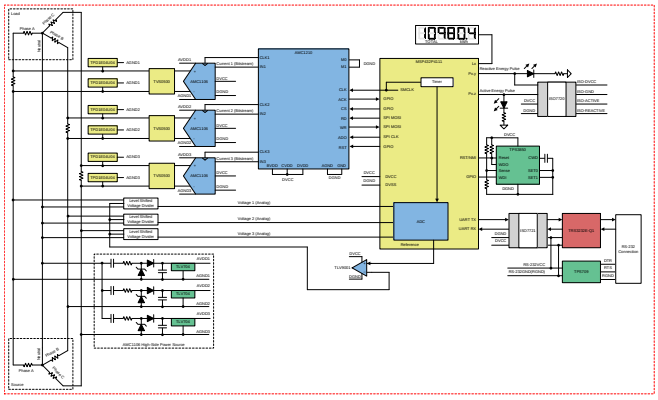
E2E™ エキスパートに質問

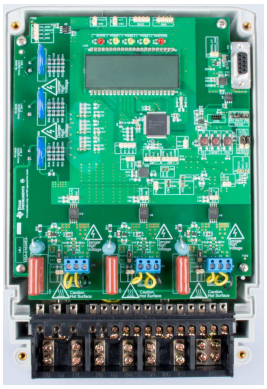
特長

- クラス0.5の三相計測と、ガルバニック絶縁(最高600V_{RMS}、ピーク絶縁電圧4kV_{RMS})のシャント電流センサ
- ガルバニック絶縁のシャント電流センサと、キャップドロップ電源により、磁気的な耐性を実現
- スタンドアロンのデジタル・フィルタにより、デジタル・フィルタなしのホスト・マイクロコントローラを使用できるため、設計の移植性が向上
- すべての位相にわたって同期された電圧と電流のサンプリングとARM® Cortex®M4ホストMCUにより、高度な計測アルゴリズムにも対応
- 有効および無効エネルギー、実効(RMS)電流および電圧、力率、ライン周波数の計算

アプリケーション

- 電気メーター
- 電力品質メーター





1 System Description

Three-phase electricity meters measure the energy consumption at a businesses or industrial sites. To properly sense energy consumption, voltage and current sensors translate mains voltage and current to a voltage range that an ADC can sense. For three-phase electricity meters, it is necessary for the current sensors to be isolated so they can properly sense the energy consumption of multiple phases without damaging the ADC. As a result, current transformers, which inherently have isolation, have historically been used for the current sensors for three-phase electricity meters. One disadvantage of current transformers (and many transformers in general) is that they can be paralyzed by applying a strong enough magnetic field so that the sensed energy consumption is less than the actual energy consumption. Due to this weakness of current transformers against magnetic fields, it is common for people to try to tamper with a meter by placing a strong magnet outside the electricity meter to try to paralyze the current transformers to steal electricity. This reference design prevents magnetic tampering by using isolated shunts as current sensors instead of current transformers.

In this reference design, a class 0.5 three-phase transformerless energy measurement system is implemented with isolated shunt sensors by using isolated delta-sigma modulators. The inputs to these delta-sigma modulators are supplementally protected using ESD and TVS surge protection diodes. The delta-sigma modulators have their output circuitry capacitively isolated from input circuitry, which thereby provides transformerless data isolation. The high-side of each modulator is powered by a capacitive-drop supply that is also transformerless. Because a transformer is not used in this design (whether a power supply transformer or current transformer), the TIDA-01639 is inherently magnetically immune, thereby preventing electricity theft due to magnetic tampering. In addition, using the high-side cap-drop power supply has the following additional advantages:

- Reduces the entire system cost
- Inherently low conducted and radiated emissions
- Reduces the current consumption drawn from the low-side power supply since the high-side is separately powered from mains instead of being derived from the low-side controller power supply

A standalone digital filter device takes the different bitstreams from the isolated modulators and uses its digital filters to produce ADC sample readings that correspond to the voltages sensed across the shunts. The use of the standalone filter device enables the flexibility of selecting a host MCU that does not have digital filters integrated. The host MCU communicates with the standalone filter device via SPI to get the current samples. Since the host MCU only needs to communicate with one standalone digital filter device to get access to all the current samples, a communication multiplexing scheme is not needed to get the ADC samples of the different phases.

The host MCU also senses the phase voltage. Since the ADC of the host MCU that is used to sense voltage cannot sense below 0 V and the mains have both positive and negative voltages, an op amp is used to level shift the signal fed into the MCU ADC so that these signals are above 0 V.

In addition to communicating to the standalone digital filter device and sensing the phase voltage, the host MCU also performs the following tasks:

- Calculates metrology parameter values
- Drives the liquid crystal display (LCD) of the board

- Communicates to a PC GUI through the isolated RS-232 circuitry of the board

In regard to metrology, the test software supports calculation of various parameters for up to three-phase energy measurement. The key parameters calculated during energy measurements are: RMS current and voltage; active and reactive power and energies; power factor; and frequency. These parameters can be viewed either from the calibration GUI or LCD. Since the host MCU has access to all of the voltage and current channels of all the phases, the design also supports adding advanced metrology algorithms that need raw ADC data.

Another advantage of using shunts is that it does not share the same degradation in metrology results that current transformers show when harmonics are present in a system. As a result, these isolated shunt current sensors may also be used for equipment that perform harmonic analysis, such as power quality meters or power quality analyzers.

1.1 Key System Specifications

表 1. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	3
Accuracy class	Class 0.5
Current sensor	Shunt
Voltage ADC type	SAR (MSP432P4111)
Delta-sigma (for current channels) modulation clock frequency	6,000,000 Hz
Digital filter sample oversampling ratio (SOSR) from filter unit	128
Digital filter integrator oversampling ratio (IOSR) from integrator unit	8
Digital filter effective oversampling ratio (EOSR)	1024
Digital filter output sample rate	5,859.4 samples per second
Ratio of skipped samples in software to total samples	0/5
Effective sample rate (for both current and voltage)	5,859.4 kHz samples per second
Phase compensation implementation	Software
Phase compensation resolution	198.68 ns = 0.0120° at 50 Hz or 0.0144° at 60 Hz
Selected CPU clock frequency	48 MHz
System nominal frequency	50 or 60 Hz
Measured parameters	• Active, reactive, apparent power and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency
Utilized LEDs	Total active energy and total reactive energy
Isolated modulator high-side power	Option 1: Power derived from mains using cap-drop supply; Option 2: External power

2 System Overview

2.1 Block Diagram

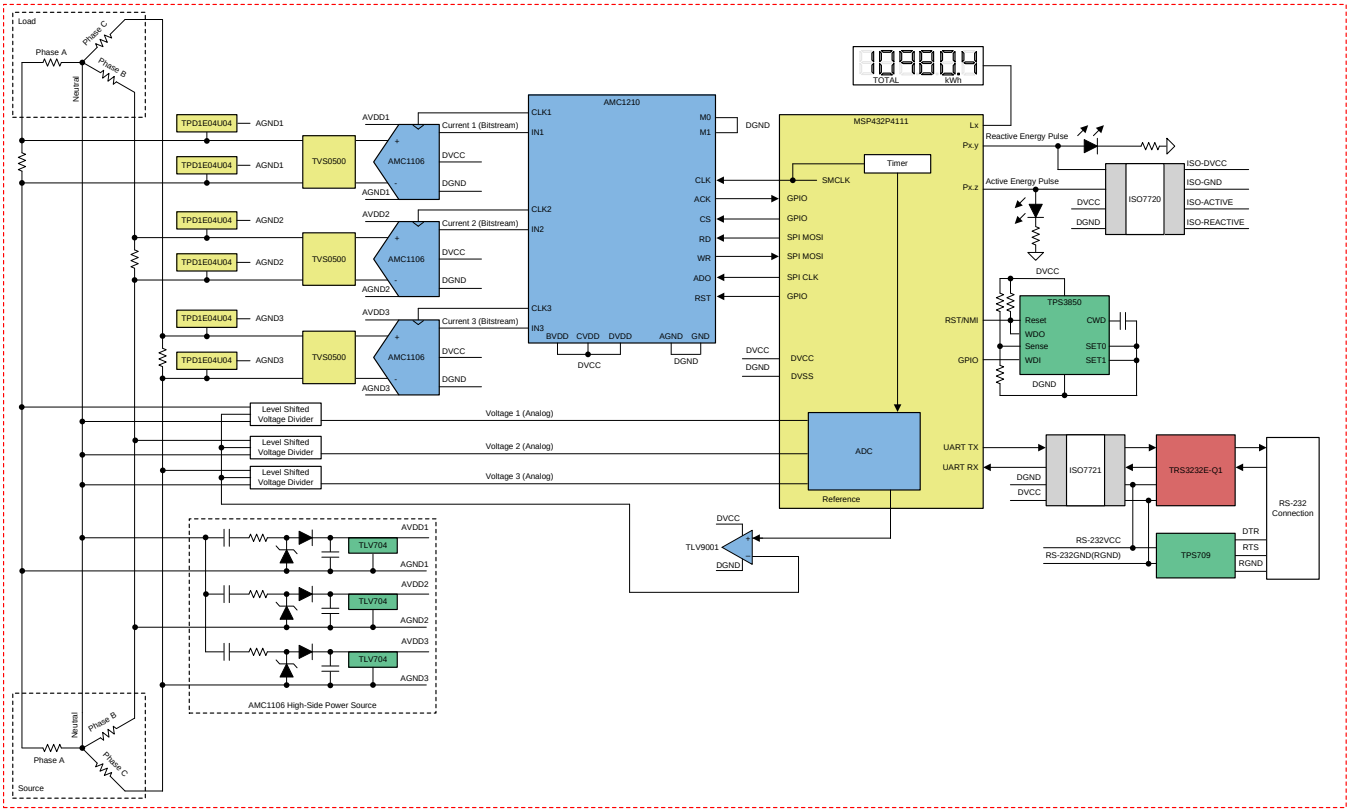


図 1. TIDA-01639 Block Diagram

図 1 depicts a block diagram that shows the high-level interface used for a MSP432P4111-based three-phase energy measurement application with isolated shunts using AMC1106 isolated modulator devices and an AMC1210 digital filter device. 図 1 particularly shows a three-phase, four-wire star connection to the AC mains. In this reference design, each phase has a shunt current sensor and an AMC1106 device for measuring the voltage across the shunt current sensor. The resistance of the shunt is selected based on the current range required for energy measurements and also the minimization of the maximum power dissipation of the shunt.

In this design, the modulator clock used by the AMC1106 devices is provided from the SMCLK clock signal output of the MSP432 that is connected to the CLK pin of the AMC1210. The AMC1210 is configured to output the clock fed to its CLK pin to its CLK1, CLK2, and CLK3 pins, which are connected to the corresponding modulator clock inputs of the isolated modulators. By configuring the AMC1210 to output the modulator clock that is at its CLK pin to the CLK1, CLK2, and CLK3 pins, it reduces layout complexity since it enables connecting the three isolated modulator clocks to one clock without having to route this clock across the PCB of the design.

The shunt input to each AMC1106 is supplementally protected by a TVS0500 surge protection device and the TPD1E04U04 ESD protection diodes. Once the modulator clock is provided to the AMC1106 devices, the AMC1106 devices output bitstreams that correspond to the voltages they sense across their shunt inputs. The bitstream from each AMC1106 is fed into a different digital filter of the AMC1210 device. Once the bitstreams are output by the AMC1106, the following steps occur:

1. The digital filters take the bitstream and generate ADC samples to correspond to the voltage sensed across the shunt by the AMC1106 devices.
2. For each new ADC sample, the AMC1210 asserts its ACK pin, which alerts the MSP432 that new samples are available.
3. After being alerted of new samples, the AMC1210 uses one of its SPI interfaces to get the current samples from the AMC1210.

Since each high side of the AMC1106 devices is referenced from a different line, a different power supply is needed for the high-side of each AMC1106 device. Each implemented power supply provides power to the associated AMC1106 device by using a cap-drop power supply from the line of that phase and neutral. In contrast, for powering the controller-side of the AMC1106 chips, all AMC1106s are powered from the same source that powers the MSP432 and AMC1210 devices.

The 14-bit SAR ADC of the MSP432 senses the phase voltages in this design. In the Magnetically Immune Transformerless Power Supply for Isolated Shunt Current Measurement reference design, it was shown that a 10-bit ADC is sufficient for measuring phase voltage so the 14-bit SAR ADC in this design is more than sufficient for measuring phase voltage. The SAR ADC of the MSP432 can sense voltages from 0-V_{REF} V , where V_{REF} is the voltage of the selected reference used by the SAR ADC for conversion. For a given Mains voltage input to a voltage front-end circuit, 図 2 shows an example output voltage waveform that can be sensed by the SAR ADC of the MSP432 if a 1.2 V V_{REF} value is used. To generate the desired output voltage from the votlage front-end circuit, a voltage divider is used to divide down the Mains voltage to a range that can be sensed by the SAR ADC of the MSP432. Since the output of the voltage divider has half of its waveform below 0 V and the SAR ADC of the MSP432 cannot sense below 0 V, a level shifter is also necessary to level shift the voltage fed to the SAR ADC above 0 V. To maximize the useable range of the ADC, the ideal level shift amount is equal to V_{REF} / 2 . The level shift is implemented by the reference voltage used by the SAR ADC being output by the MSP342 and fed into a TLV9001 op amp, which acts as a buffer. The output of the op amp then drives a voltage divider that is used to create the V_{REF} / 2 shift voltage. An op amp is needed for this level shifter implementation because the reference voltage output from the MSP432 cannot directly drive the voltage divider used to create the V_{REF} / 2 voltage.

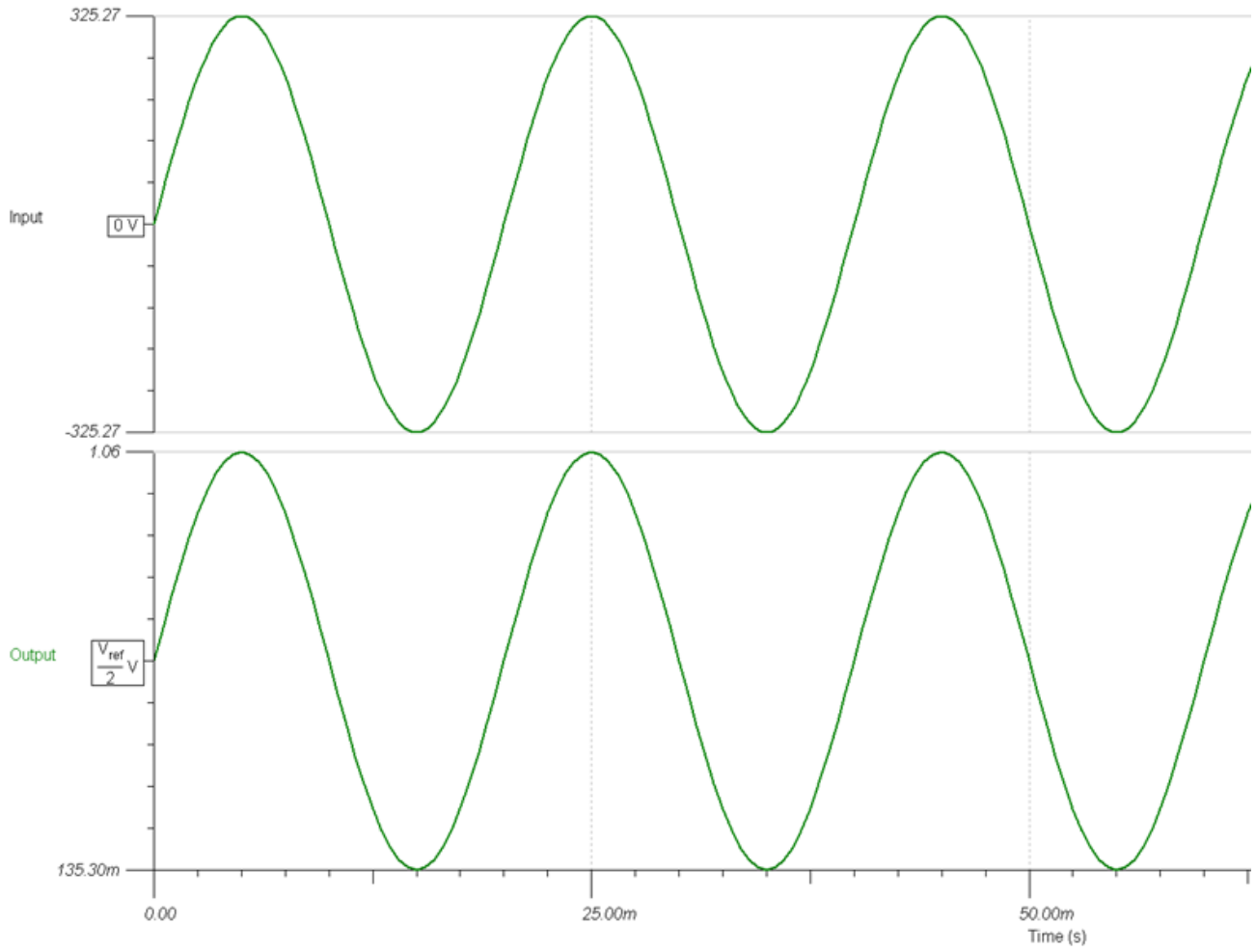


図 2. Voltage Front-End Input Voltage and Output Voltage Waveforms

For the proper calculation of power readings, the voltage and current samples must be synchronized. This synchronization is done by having the modulator clock used by the AMC1106 and AMC1210 also fed to an internal timer of the MSP432. The output of this timer is used to automatically trigger in hardware the SAR ADC to sample the voltages of the different phases. The timer is setup to count up to the effective OSR number of the AMC1210 so that the timing mimics the timing of the AMC1210, and there is one voltage sample produced for each current sample.

In this design, a TPS3850 device is also used as a SVS and watchdog for the MSP432. Although the MSP432 has an internal watchdog and SVS that suffices for this application, the TPS3850 standalone watchdog is used because there is additional security in having a watchdog and SVS that is independent of the MCU.

Other signals of interest in 図 1 are the active and reactive energy pulses used for accuracy measurement and calibration. The ISO7720 provides an isolated connection for these pulses for connecting to non-isolated equipment. In addition to isolated pulses, the design supports isolated RS-232 communication through the use of the TPS70933, ISO7721, and TRS3232E-Q1 devices.

2.2 Highlighted Products

2.2.1 AMC1106M05

The AMC1106 device is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. On the high-side of the AMC1106, the modulator can be supplied by a 3.3-V or 5-V power supply (AVDD). The isolated digital interface operates from a 3.0-V, 3.3-V, or 5-V power supply (DVDD).

The AMC1106 is used to provide isolated current measurement for the shunt current sensors of the design. This isolated current measurement is accomplished by the AMC1106 providing a modulation bit-stream output that is capacitively isolated from the analog signal fed from the shunts to the AMC1106, as 図 3 shows.

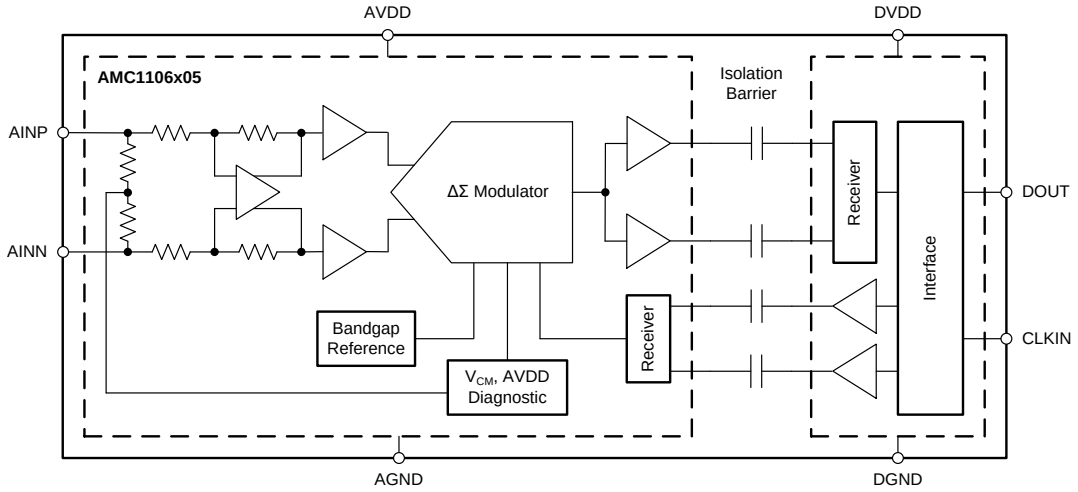


図 3. AMC1106 Functional Block Diagram

In 図 3, the shunt current measurement is made by measuring the voltage across terminals AINP and AINN of the AMC1106, which are connected to the shunt outputs. If the input voltage value exceeds ±50 mV, there is degradation in the accuracy of readings. The third terminal of the shunt is then connected to AGND of the AMC1106. To perform measurements, 3.3 V or 5 V must be fed between AVDD and AGND.

To properly power the controller side, pins DVDD and DGND on the AMC1106 must be connected to DVCC and DVSS of the MSP432. In addition, the modulation clock used by the AMC1210 digital filters must be connected to CLKIN. This modulation clock must be between 5 to 20 MHz for the AMC1106 to properly work and can be generated from the SMCLK clock output of the MSP432. With a proper clock fed into CLKIN of an AMC1106 device, a delta-sigma bit-stream is output from the DOUT pin of the AMC1106. This DOUT pin must be connected to the bit-stream input of the corresponding digital filter within the AMC1210 device.

2.2.2 AMC1210

The AMC1210 is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each input can receive an independent delta-sigma modulator bit stream. The bit streams are processed by four individually-programmable digital decimation filters. The AMC1210 also offers a flexible interface and a comprehensive interrupt unit, allowing customized digital functionality and immediate digital threshold comparisons for over-current monitoring.

In this reference design, the AMC1210 device is used to decimate the bitstreams from the AMC1106 devices. The AMC1210 has four independent filter modules. 図 4 shows the block diagram of a AMC1210 filter module. The portion within the red box represents the parts of the filter module that are used in this reference design.

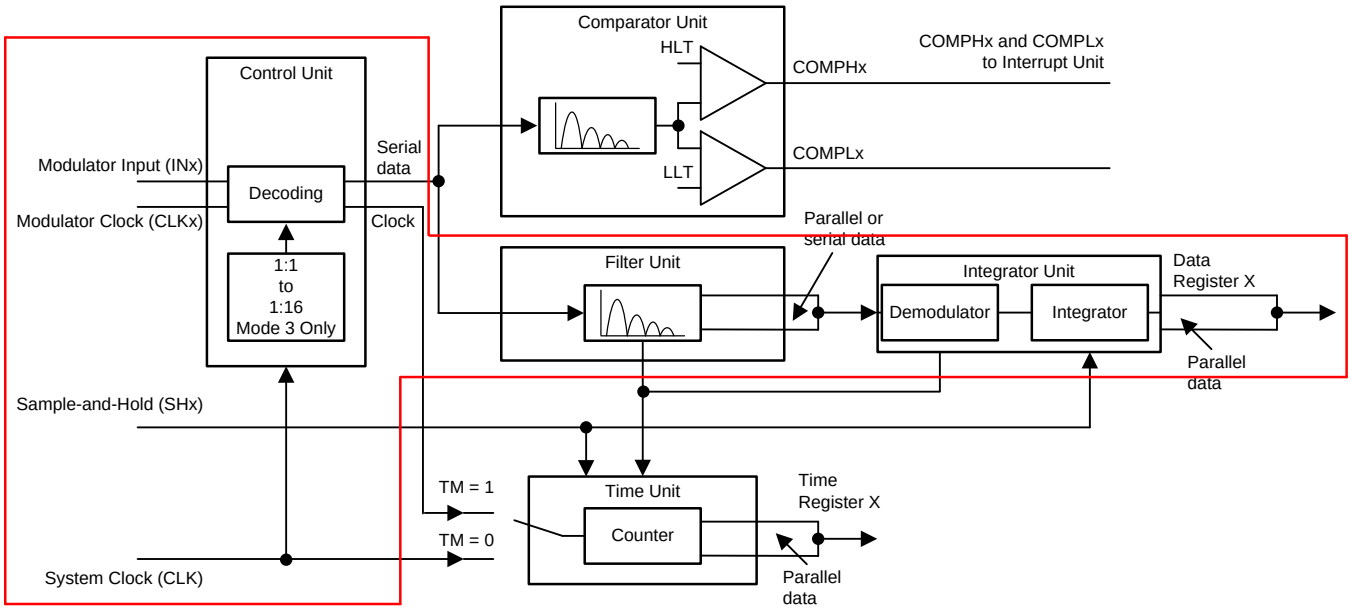


図 4. AMC1210 Filter Module Block Diagram

The AMC1210 has the capability to internally output the system clock, which is fed into the CLK pin of the device, onto each of the CLKx pins. By connecting the CLKx pins of the AMC1210 to the CLKIN pin of the AMC1106, configuring the AMC1210 to internally output the clock on its CLK pin to its CLKx pins connects the isolated modulators to the modulator clock. This feature can be used so that the modulator clock only has to be fed from its source to the CLK pin of the AMC1210 and not to the individual modulators.

Within the filter module, the type of filter (sinc^1, sinc^2, or sinc^3) can be selected as well as a sample OSR value up to 128. The output from the filter unit can then be fed into the integrator unit. The integrator unit allows summation of a defined number of samples from the filter unit. After the user-defined number of samples, which is called the integrator OSR, from the filter unit has been summed, the ACK pin on the AMC1210 is asserted to alert the MCU that new samples are ready. The integrator can be used to divide down the effective sample rate so that less processing is necessary from the host MCU. As an example, with an integrator OSR of 8, sample filter OSR of 128, the timing of an OSR = 1024 filter can be mimicked. With a 6 MHz modulation clock frequency, the resulting effective OSR produces a smaller effective sample rate of 5,859.375 Hz instead of the resulting sample rate of 46,875 if the integrator unit is not used.

To save cost, internal ADCs of a host MCU can be used to measure the phase voltage instead of using additional isolated modulators and an extra AMC1210 device to measure phase voltage. To calculate power readings properly, the voltage and current sampling have to be synchronized. This voltage and current synchronization can be done by using a timer to trigger voltage conversions and having the timer's timing to mimic the timing of the AMC1210 so that there is a voltage sample produced for each current sample.

2.2.3 TLV9001

The TLV900x family includes single (TLV9001), dual (TLV9002), and quad-channel (TLV9004) low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective solution for space-constrained applications. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the TLV600x devices. The robust design of the TLV900x family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions. Micro-size packages, such as SOT-553 and WSON, are offered for all channel variants (single, dual, and quad), along with industry-standard packages such as SOIC, MSOP, SOT-23 and TSSOP packages.

The TLV9001 buffers the internal reference used by the SAR ADC of the MSP432 so that it can be fed into a voltage divider to create a V_{REF} / 2 DC voltage signal. The reference voltage output from the MSP432 cannot directly drive the V_{REF} / 2 voltage divider, which is why the TLV9001 device is used. The V_{REF} / 2 voltage signal is used to level shift the output from the Mains voltage divider so that the resulting signal fed into the SAR of the MSP432 is within its acceptable input voltage range.

For this design, the TLV9001 device was specifically selected for the reference buffer in this design because of its low cost. In addition, the low offset voltage of this op amp for the given cost enables the accurate generation of the V_{REF} / 2 offset needed for level shifting the signal fed into the SAR ADC.

2.2.4 MSP432P4111

The SimpleLink™ MSP432P4111 MCUs are optimized MCUs that deliver ultra-low-power performance with FPU and DSP extensions. This device has an Arm® 32-Bit Cortex®-M4F CPU with Floating-Point Unit and Memory Protection Unit, a real-time clock, LCD driver, port mappable GPIOs, an AES encryption and decryption accelerator, and multiple serial communication options. The MSP432P4111 device is part of the SimpleLink MCU platform, which consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz, and host MCUs. All of these devices share a common, easy-to-use development environment with a single-core software development kit (SDK) and rich tool set.

The MSP432 in this design senses the phase voltages, retrieves current samples from the AMC1210, and calculates metrology parameters. In addition, the device also keeps track of time with its RTC module, drives the LCD on the board with its internal LCD driver module, and uses one of its UART interfaces to communicate to a PC GUI using the isolated RS-232 circuit of the board.

2.2.5 TPS3850

The TPS3850 combines a precision voltage supervisor with a programmable window watchdog timer. The TPS3850 window comparator achieves 0.8% accuracy (–40°C to +125°C) for the undervoltage ($V_{IT–(UV)}$) threshold. The TPS3850 also includes accurate hysteresis on the threshold, making the device ideal for use with tight tolerance systems. The supervisor RESET delay can be set by factory-programmed default delay settings, or programmed by an external capacitor. The factory-programmed RESET delay features a 15% accuracy, high-precision delay timing. The TPS3850 includes a programmable window watchdog timer for a wide variety of applications. The dedicated watchdog output (WDO) enables increased resolution to help determine the nature of fault conditions. The window watchdog timeouts can be set by factory-programmed default delay settings, or programmed by an external capacitor. The watchdog can be disabled via logic pins to avoid undesired watchdog timeouts during the development process. The TPS3850 is available in a small 3.00-mm × 3.00-mm, 10-pin VSON package.

For electricity meters, some manufacturers prefer to have external SVS and watchdog timer devices to reset any microcontrollers in the system, even if the microcontrollers already have an internal SVS and watchdog timer. External SVS and watchdog timers are sometimes preferred over using the SVS and watchdog timer within a microcontroller because the external option can be more secure than the internal option since the external devices function independently of the microcontroller. Although the SVS and watchdog timer of the MSP432 suffices for this application, the TPS3850 external SVS and watchdog timer device is added to this design for an additional level of security.

In this design, the TPS3850H01 variant is specifically used, which enables the undervoltage threshold value to be programmed by external resistors. This variant was also selected because it does not function as a window comparator like the other TPS3850 variants. This variant only monitors the undervoltage threshold and does not have an overvoltage threshold. If the monitored voltage falls below the undervoltage threshold, the RESET pin of the TPS3850 is asserted low. In addition to serving as an SVS device, the device functions as an external watchdog as well. A pulse is output by the MSP342 and fed to the WDI pin of the TPS3850. If the time between successive falling edges on the WDI pin is not within the allowed lower and upper watchdog window boundaries, the WDO pin of the TPS3850 is asserted low. The RESET and WDO output pins of the TPS3850 are connected to each other and the reset of the MSP432 so that the MSP432 is reset whenever the WDO or RESET pins of the TPS3850 are asserted low.

2.2.6 TVS0500

The TVS0500 robustly shunts up to 43 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to 2 kV IEC 61000-4-5 open circuit voltage coupled through a 42 Ω impedance. The TVS0500 uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 10 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness. In addition, the TVS0500 is available in a small 2 mm × 2 mm SON footprint which is ideal for space constrained applications, offering a 70 percent reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance ensure a minimal effect on the protected line. To ensure robust protection over the lifetime of the product, TI tests the TVS0500 against 5000 repetitive surge strikes at high temperature with no shift in device performance. In this design, the TVS0500 is placed in the current front-end circuitry to protect the analog input pins of the AMC1106.

2.2.7 TPD1E04U04

The TPD1E04U04 is a unidirectional TVS ESD protection diode for HDMI 2.0 and USB 3.0 circuit protection. The TPD1E04U04 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device features a 0.5-pF IO capacitance making it ideal for protecting high-speed interfaces up to 6 Gbps such as HDMI 2.0 and USB 3.0. The low dynamic resistance and ultra-low clamping voltage ensure system level protection against transient events for sensitive SoCs. The TPD1E04U04 is offered in the industry standard 0402 (DPY) and 0201 (DPL) packages. In this design, the TPD1E04U04 is placed in the current front-end circuitry for additional protection of the analog input pins of the AMC1106.

2.2.8 TLV704

The TLV70433 low-dropout (LDO) regulator is an ultra-low quiescent current device designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. The TLV70433 operates over a wide operating input voltage of 2.5 V to 24 V. Thus, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients. The TLV70433 is used as the LDO within the cap-drop high-side power supplies of the AMC1106 devices. Cap-drop supplies can only support a small load current. The TLV70433 was selected for the cap-drop LDO because it has a small quiescent current, which allows more of the limited load current of the cap-drop supply to be used to power the high-side of the AMC1106 devices.

2.2.9 TRS3232E-Q1

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232E-Q1 device. The TRS3232E-Q1 device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

The TRS3232E-Q1 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/µs driver output slew rate.

2.2.10 ISO7721

To add isolation to the RS-232 connection to a PC, the isolated RS-232 portion of this reference design uses capacitive galvanic isolation, which has an inherent lifespan advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The variant of the ISO7721 used in the RS-232 circuitry of this reference design provides galvanic isolation up to 3.0 kV_{RMS} for one minute per UL. This digital isolator has two isolated channels where one is a forward channel and the other is a reverse channel. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. This chip supports a signaling rate of 100 Mbps. The chips can operate from a 3.3-V and 5-V supply and logic levels.

2.2.11 TPS709

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this reference design uses the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 V to 12 V, depending on the driver implementation. The 5 V to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

The TPS70933 linear regulator is an ultra-low quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA (typical).

2.2.12 ISO7720

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC. The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. The ISO7720 device has both channels in the same direction while the ISO7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x family of devices is available in 16-pin SOIC wide-body (DW) and 8-pin SOIC narrow-body (D) packages.

To test the active energy and reactive energy accuracy of a meter, pulses are output at a rate proportional to the amount of energy consumed. A reference meter can then determine the accuracy of the e-meter by calculating the error based on these pulses and how much energy is provided to the meter. In this reference design, pulses are output through headers for the cumulative active and reactive energy consumption. Using the ISO7720 provides an isolated version of these headers for connection to non-isolated equipment. In this design, the D package of the ISO7720 is used, which provides an isolation voltage of 3000 V_{RMS} for these signals. These isolated active and reactive signals can be set to have either a 3.3- or 5-V maximum voltage output by applying the selected maximum voltage output between the VCC (ISO_VCC) and GND (ISO_GND) of the isolated side.

2.3 System Design Theory

2.3.1 Design Hardware Implementation

2.3.1.1 TPS3850H01 SVS and Watchdog Timer

The TPS3850H01 is an external supply voltage supervisor (SVS) and watchdog timer that is used to externally reset the MSP432. The MSP432 has an internal watchdog timer and SVS device that can be used as well, which will suffice for this application; however, meter manufacturers sometimes use external SVS and watchdog timer devices instead of an internal SVS and watchdog timer of the microcontroller because they add an additional layer of security since they are independent of the microcontroller, and therefore, are less affected by any issues that affect the microcontroller itself.

The TPS3850H01 device variant is specifically an undervoltage monitor. Whenever the monitored voltage is below the undervoltage threshold, the RESET pin of the TPS3850 is asserted low. When the monitored voltage rises above the undervoltage threshold plus hysteresis voltage value, the RESET pin of the TPS3850 is pulled back high after a t_{RST} user-defined delay elapses. The TPS3850H01 variant does not have an overvoltage monitoring feature like the other TPS3850 variants, which enables the voltage rail that is supervised to detect under voltage conditions when monitoring supply ranges that may vary over a wide range of voltages (such as 2 V to 3.6 V).

For the TPS3850H01 variant, the undervoltage threshold can be set by connecting a resistor divider to the SENSE pin of the TPS3850H01. The values of the two resistors in the voltage divider as well as the monitored supply voltage determine the undervoltage threshold. 図 5 shows the TPS3850H01 circuit used in this design with R71 (324 kΩ) and R75 (80.6 kΩ) being the two resistors that determine the undervoltage threshold

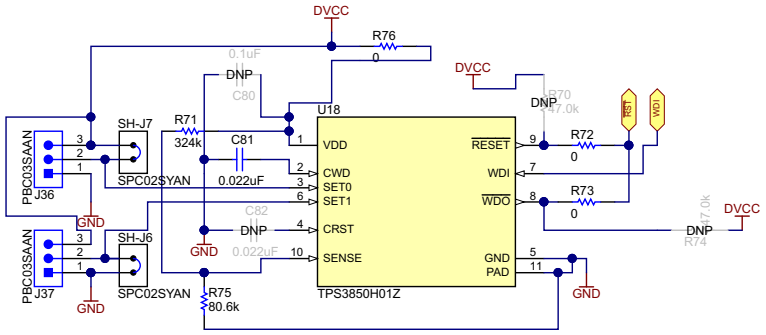


図 5. TPS3850H01 Circuit

The threshold voltage is calculated with 式 1:

$$V_{MON} = V_{IT(ADJ)} \times \left(1 + \frac{R_{71}}{R_{75}}\right) \quad (1)$$

where

- The typical value of $V_{IT(ADJ)}$ is 0.4 V (taken from the TPS3850 datasheeet)

Given the nominal values for R71 and R75 used in this design, the undervoltage threshold is approximately 2.0 V.

In addition to acting as an undervoltage monitor, the TPS3850H01 device is also configured to act as a watchdog timer. A pulse is output by the MSP342 and fed to the WDI pin of the TPS3850. If the time between successive falling edges on the WDI pin is not within the allowed lower and upper watchdog window boundaries, the WDO pin of the TPS3850 is asserted low for t_{RST}. t_{RST} is programmed by either connecting a capacitor, connecting a pullup resistor, or not connecting anything to the CRST pin of the TPS3850. In this design, nothing is connected to the CRST pin, which results in a typical t_{RST} time of 200 ms.

The time between successive falling edges on the WDI pin should be between a lower ($t_{WDL(max)}$) and upper ($t_{WDU(min)}$) time interval. If the time between successive falling edges is not within this window, then the WDO pin is asserted low for a time of t_{RST}. $t_{WDU(min)}$ is determined based on $t_{WDU(typ)}$, which is programmed by either connecting a capacitor, connecting a pullup resistor, or not connecting anything to the CWD pin of the TPS3850. $t_{WDL(max)}$ is determined by $t_{WDU(typ)}$ as well as the state of the SET0 and SET1 pins. The state of the SET0 and SET1 pins are set by connecting the pins to either GND(0) or VDD(1). 図 6 shows the formula for $t_{WDL(max)}$ in the green box, and the formula for $t_{WDU(min)}$ in the red box. The calculation of $t_{WDL(max)}$ is derived from the $t_{WDU(max)}$ calculation, which is in the blue box.

Input			Watchdog Lower Boundary (t_{WDL})			Watchdog Upper Boundary (t_{WDU})			Unit
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	0	$t_{WDU(min)}$ x 0.125	t_{WDU} x 0.125	$t_{WDU(max)}$ x 0.125	0.85 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.15 x $t_{WDU(typ)}$	S
	0	1	$t_{WDU(min)}$ x 0.75	t_{WDU} x 0.75	$t_{WDU(max)}$ x 0.75	0.85 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.15 x $t_{WDU(typ)}$	S
	1	0	Watchdog disabled				Watchdog disabled		
	1	1	$t_{WDU(min)}$ x 0.5	t_{WDU} x 0.5	$t_{WDU(max)}$ x 0.5	0.85 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.15 x $t_{WDU(typ)}$	S

図 6. Watchdog Timer Window Calculations

In the TPS3850 circuit, a 0.022-µF capacitor is connected to the CWD pin to set $t_{WDU(typ)}$. $t_{WDU(typ)}$ is calculated with 式 2:

$$t_{WDU(typ)} = 77.4 \times C_{CWD} + 0.055 \quad (2)$$

where

- C_{CWD} is in units of microfarads in this formula

Based on a nominal capacitor value of 0.022 µF, a 1.7578 seconds $t_{WDU(typ)}$ value results. If SET0 = 0 and SET1 = 0, $t_{WDU(min)}$ = 1.49413 s, $t_{WDU(max)}$ = 2.02147 s, and $t_{WDL(min)}$ = 0.2527 s for the nominal capacitor value. As a result, if we are assuming the nominal 0.22-µF capacitor value, the time between successive falling edges on the WDI pin should be from 0.2527–1.49413 seconds to prevent the WDO output of the TPS3850 from being asserted low. If the capacitor has a tolerance of ±10%, the watchdog timer interval is decreased from 0.2527–1.49413 s to approximately 0.277–1.349 s. In the test software, the WDI pin of the TPS3850 is asserted so that the time between successive edges is normally approximately 1 second, which is within the 0.277–1.349 second watchdog timer window. If there is an issue with the MSP432 where the WDI pin is not asserted at the appropriate time, the WDO pin is asserted low.

In this design, the SET0 and SET1 state is set by adding jumpers to the J36 and J37 headers at the appropriate locations. To maximize the window between the lower and upper watchdog time intervals when the MSP432 is running, SET0 and SET1 are both connected to GND by placing jumpers at the appropriate locations on the J36 and J37 headers. When programming the MSP432 on this board, it is necessary to disable the watchdog feature of the TPS3850, which is done by setting SET0 = 1 and SET1 = 0.

The WDO output and RESET pins of the TPS3850 are connected together in this design. Since the WDO and RESET pins are open-drain, by connecting these pins together and then connecting the shared connection to the RST pin of the MSP432, the TPS3850 is able to reset the MSP432 whenever the WDO or RESET pin of the TPS3850 is asserted low. Because the WDO and RESET pins are open-drain, a pullup resistor is needed from this shared connection to VDD. Since the pins are connected to each other, only one pullup resistor is needed. This pullup resistor is set to be 47-kΩ based on the recommended JTAG circuit of the MSP432. The pullup resistor is not shown in 図 5 since this is located in the JTAG portion of the schematic instead.

2.3.1.2 Analog Inputs

The design of the front end consists of the three AMC1106 chips used for measuring current, a 14-bit SAR ADC module (referred to as the ADC14 module) integrated within the MSP432 for measuring the phase voltages, and a MSP432 timer for synchronizing the AMC1210 with the SAR ADC of the MSP432.

For maximum accuracy, the AMC1106 requires that the input analog signal voltage does not exceed ±50 mV. In addition, the AMC1106 has differential inputs; therefore, the AC current signal from mains can be directly interfaced without the requirement for level shifters.

In contrast, the ADC14 module of the MSP432 has single-ended inputs that cannot accept voltages below 0 V. Therefore, the ADC14 requires that the sensed voltage is between 0-V_{REF} volts, with the option to select the V_{REF} source and voltage in the software. As a result, after the mains voltage is divided down for sensing, the voltage front-end circuitry requires a level shifter to properly interface to the ADC14 module.

2.3.1.2.1 Voltage Analog Front-End

The voltage from the mains is usually 230 V or 120 V and must be brought down to within 0-V_{REF} volts. Because Mains is a signal with negative and positive voltages but the selected SAR ADC cannot take negative voltages, the voltage front-end circuit requires that a level shifter is used in addition to the voltage division scheme that is used. The analog front-end for voltage in this design consists of spike protection varistors, voltage divider and shifter network, and a RC low-pass filter that functions like an anti-alias filter.

図 7 shows the analog front-end used in this design for one-phase for the voltage inputs for a mains voltage of 230 V. The voltage is brought down and shifted to a range within 0-V_{REF} volts, where V_{REF} is selected to be the 1.2-V reference produced by the internal reference module of the MSP432. In this circuit, only one op amp is needed for all three phases. One Mains voltage divider and reference voltage divider is needed for each phase (three in total).

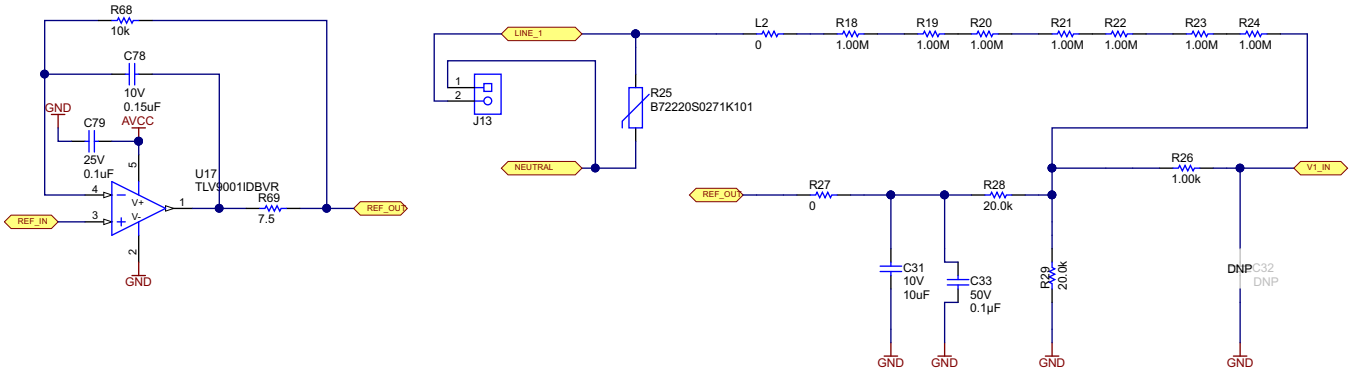


図 7. Analog Front-End for Voltage Inputs

In the voltage analog front-end circuit, the voltage reference used by the SAR ADC is output by the MSP432 and fed to a TLV9001 op amp, which acts as a buffer. The output from the op amp is then fed to a voltage divider to generate a V_{REF} / 2 offset voltage that the signals fed to the SAR ADC are shifted by. The op amp is used to drive the reference voltage divider circuit instead of using the direct reference voltage output from the microcontroller because the reference voltage output of the microcontroller can only drive loads less than 10 µA of current, as 図 8 shows. This 10-µA maximum load current is not enough to drive the reference voltage divider, which is why an op amp is used as a buffer by connecting the reference voltage output to the input of the op amp and connecting the output of the op amp to the reference voltage divider.

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{O(REF+)}$ VREF maximum load current, VREF+ terminal	REFVSEL = (0, 1, 3), AV_{CC} = $AV_{CC(MIN)}$ for each reference level, REFON = REFOUT = 1		-1000		10	µA

図 8. Maximum Load Current of Reference Voltage Output on MSP432

To calculate the voltage that is fed to the SAR ADC of the MSP432 (V1_IN in 図 7 or V_{ADC} in the following formulas) when using the voltage front-end circuit as 図 7 shows, the following equations are used:

$$R_S = R_{18} + R_{19} + R_{20} + R_{21} + R_{22} + R_{23} + R_{24} \quad (3)$$

$$R_{eq1} = \frac{R_S \times R_{29}}{R_S + R_{29}} \quad (4)$$

$$V_{offset} = V_{reference}\left(\frac{R_{eq1}}{R_{eq1} + R_{28}}\right) \approx V_{reference}\left(\frac{R_{29}}{R_{29} + R_{28}}\right) \quad (5)$$

$$V_{peak} = V_{RMS} \times \sqrt{2} \quad (6)$$

$$R_{eq2} = \frac{R_{28} \times R_{29}}{R_{28} + R_{29}} \quad (7)$$

$$V_{ADC\_Swing} = V_{peak}\left(\frac{R_{eq2}}{R_{eq2} + R_S}\right) \quad (8)$$

$$V_{ADC} = V_{offset} \pm V_{ADC\_Swing} \quad (9)$$

To determine the voltage swing from the offset voltage, V_{ADC_Swing}, the voltage that is fed into the SAR ADC of the MSP432 can be thought as a voltage divider with the Mains voltage as the voltage source to the following series resistors: R_s (R18 + R19 + R20 + R21 + R22 + R23 + R24)and R_{eq2} (the equivalent resistor for the parallel combination of R28 and R29). V_{ADC_Swing} is the voltage across R_{eq2} within the Mains voltage divider. If we apply a 230 V_{RMS} signal to the voltage front-end circuit in 図 7 and a 1.2-V reference is used, based on the formulas above V_{offset} ≈ 0.6 V and V_{ADC_Swing} ≈ ±0.464 V. As a result, the voltage fed to the SAR ADC is from 0.136 V to 1.064 V, which is within the 0- to 1.2-V input range for the SAR ADC for the selected 1.2-V reference.

In the V_{offset} formula, an ideal op amp with zero offset voltage is assumed; however, a real op amp has an offset adds to V_{offset}. For the V_{REF} voltage divider and op-amp implementation, the TLV9001 device was specifically selected for the reference buffer in this design because of its low cost and the low offset voltage of this op amp for the given cost, which enables the accurate generation of the V_{REF} / 2 offset needed for level shifting the signals fed into the SAR ADC.

In the design files of this reference design, a voltage front-end simulation file is included, which can be used to simulate the expected waveforms that are fed into the SAR ADC given the selected op amp and input Mains voltage. 図 9 shows the V1_IN simulation waveform obtained with the simulation file and the conditions used for the calculations in this section. From these results, it can be observed that the simulation waveform closely matches the calculations in 式 3 to 式 9 of the range of voltages that are fed into the SAR ADC.

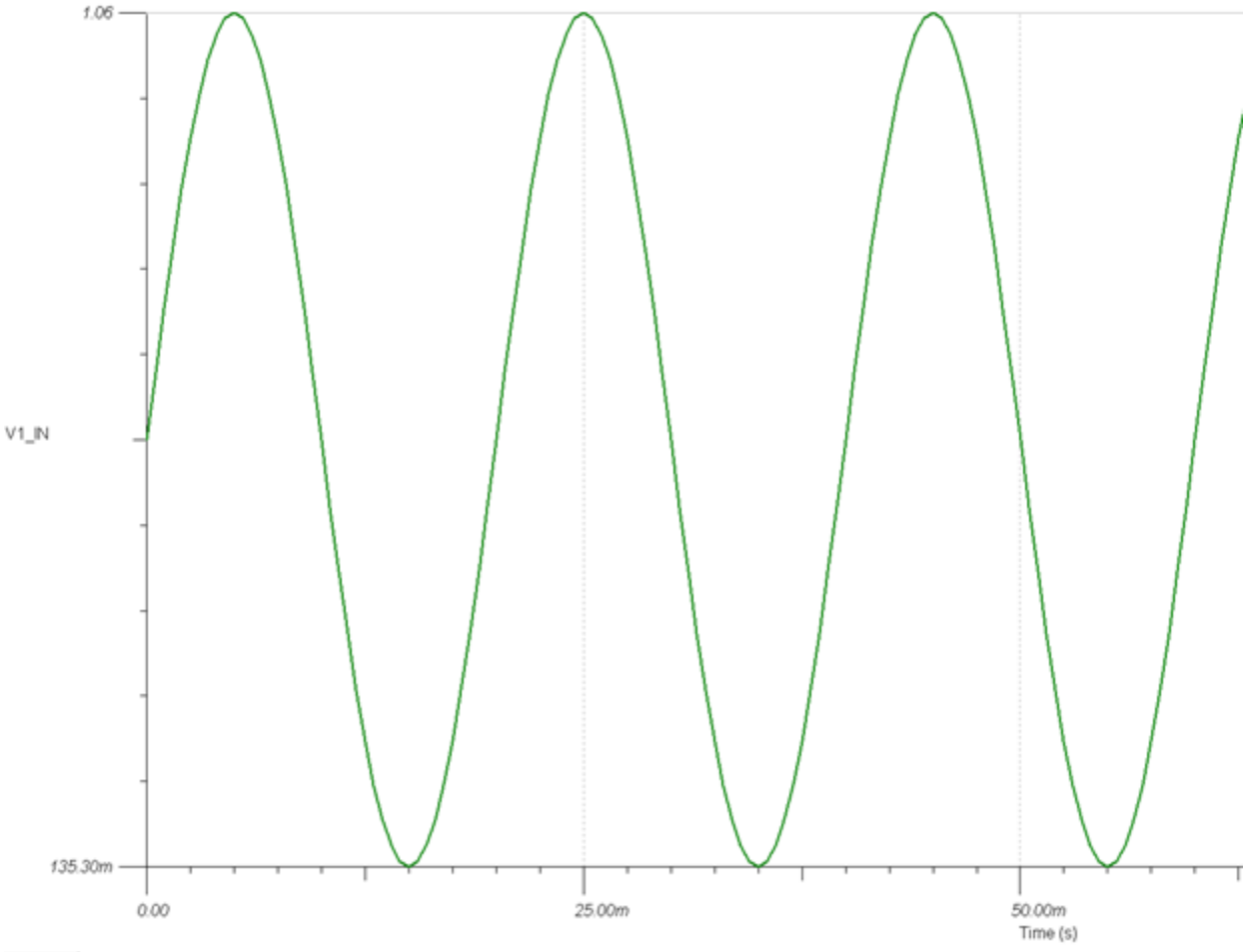


図 9. Simulated Waveform for Voltage Front-end Circuit

Using this voltage front-end circuit and selected values of V_{ADC_Swing} , Mains peak voltage ($V_{peak)}$, and R_S, the resistor values to be used in the voltage front-end circuit can be calculated by first calculating R_{eq2} from the formulas in 式 3 to 式 9. If R_S>>R_{29}, the offset voltage that the SAR ADC waveform is shifted by (V_{offset}) can be approximated using a voltage divider equation, where the reference voltage is the voltage source and only R28 and R29 are the series resistors. Given this approximation, select the same resistance value for R28 and R29 to generate a V_{REF} / 2 offset voltage, which means that R28 and R29 should be selected to have twice the resistance value of the calculated R_{eq2} value.

An alternative implementation for level shifting is to try to create the desired V_{REF} / 2 level shift voltage by an AVCC based voltage divider, as 図 10 shows, instead of a V_{REF} based voltage divider. This AVCC based implementation does not require an op amp; however, with this AVCC-based implementation, in many cases the resistance value options available for the resistors in the AVCC voltage divider cannot accurately create the ideal V_{REF} / 2 offset voltage like the V_{REF} voltage divider

and op-amp implementation. As an example, 図 10 was designed for a 2-V reference so a 1.0 V V_{offset} value would be ideal; however, given the selected resistor values and a 3.3-V AVCC value, an offset of approximately 1.1 V results instead of 1.0 V. As a result, the AVCC voltage divider implementation has an offset in ADC readings that could cause voltage readings longer to settle and also cause not being able to use the full ADC range when compared to the V_{REF} voltage divider and op-amp implementation. These disadvantages of the AVCC voltage divider implementation for level shifting is why the V_{REF} voltage divider and op-amp implementation in 図 7 is utilized for the PCB revision used in this design instead of the AVCC based voltage divider and no op-amp implementation in 図 10.

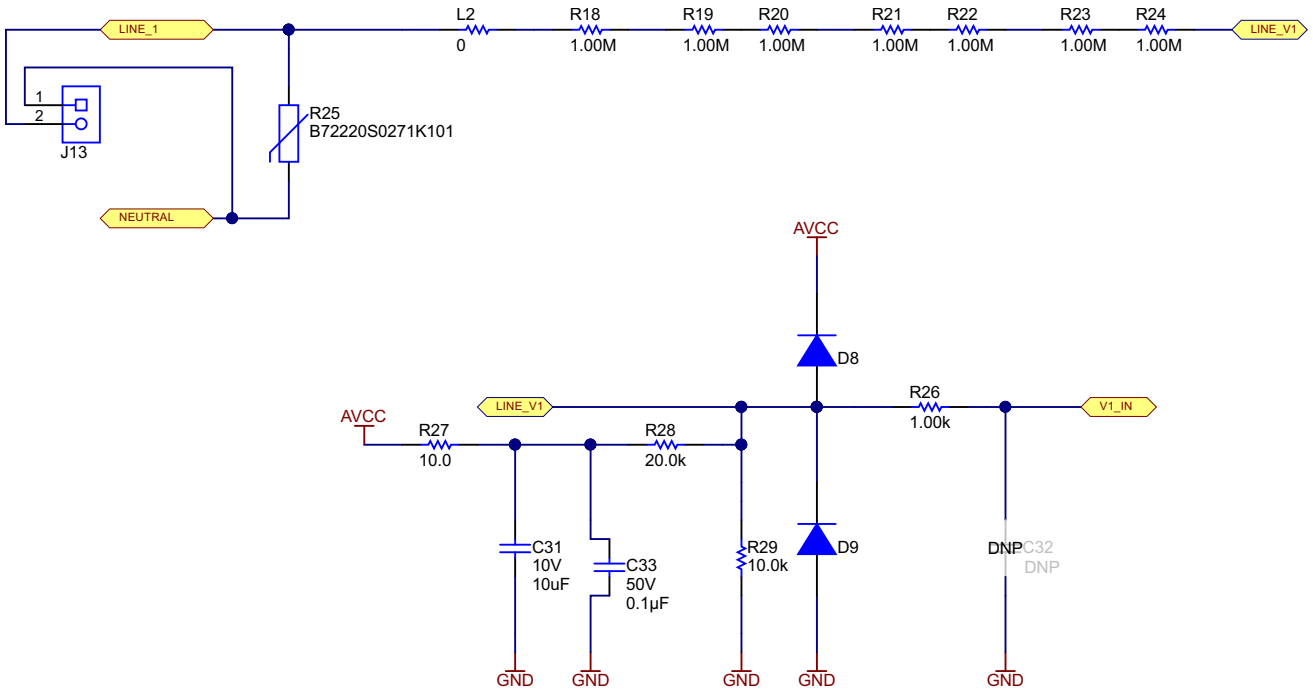


図 10. Alternative Analog Front-End for Voltage Inputs Not Used in Design

2.3.1.2.2 Current Front-End

2.3.1.2.2.1 AMC1106 High-Side Power Supply

To sense the voltage across the shunt, the high-side of each AMC1106 device must be powered. Because each AMC1106 should be referenced from a different line, a different power supply is required for each AMC1106. In this design, there are two options for powering the high-side of the AMC1106 devices: an onboard half-bridge cap-drop power supply or an off-board, custom power supply.

There are multiple advantages to using the onboard cap-drop high-side power supply. First, this cap-drop power supply does not have any magnetic components so the power supply should be magnetically immune to magnetic fields instead of only being magnetically tolerant to a certain limit. Additionally, cap-drop supplies are relatively inexpensive compared to alternative power supply options. Also, LDO-based cap-drop power supplies inherently have low conducted and radiated emissions compared to SMPS power supplies. Finally, because the power to each AMC1106 high side is derived directly from mains instead of from the controller-side power supply, less current is drawn from the controller-side power supply allowing the specifications on the controller-side power supply maximum current drive capability to be relaxed.

図 11 shows the implementation of the half-bridge cap-drop high-side power supply in the design. In this implementation, VIN1, which is the regulated output from the TLV70433 LDO, is fed directly into the AVDD pin of the AMC1106 to provide power to it. As an alternative to using the onboard cap-drop power supply, the design has the option to instead power the AMC1106 by providing the necessary 3.3 V or 5 V from an external isolated voltage supply to the associated terminal block (J26 in 図 11).

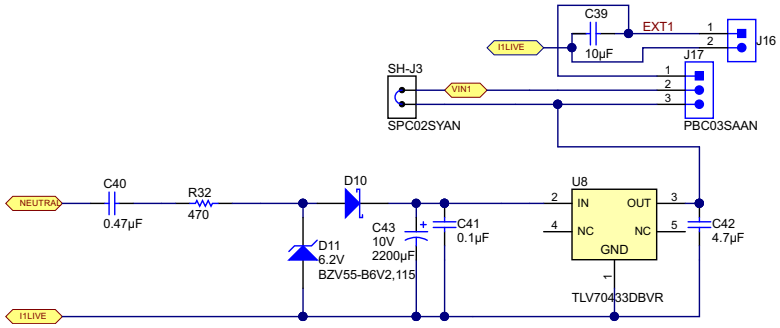


図 11. AMC1106 High-Side Power Options

Minimizing the modulation clock frequency reduces the current consumption of the AMC high-side, thereby allowing the relaxation of the maximum current drive specification on the cap-drop supply. For this design, the modulation clock frequency is selected to be 6 MHz because this is the minimum clock frequency that can be derived from the clocks of the MSP432 clocks that is still above the 5-MHz minimum modulation clock frequency necessary for the AMC1106 to function. In this design, the onboard cap-drop power supplies are able to power the high-side of the AMC devices for voltages as low as 80 V_{RMS} at 50 and 60 Hz .

2.3.1.2.2.2 Current Sensing

The analog front-end for current inputs is different from the analog front-end for the voltage inputs. 図 12 shows the analog front-end used for a current channel.

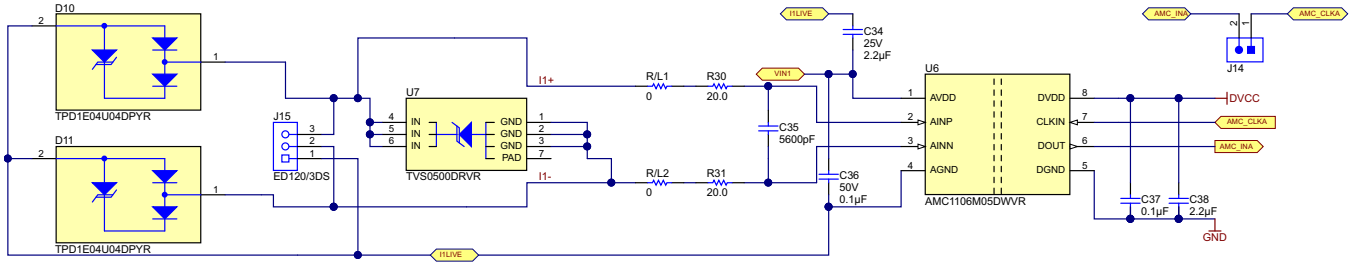


図 12. Analog Front-End for Current Inputs

The analog front-end for current consists of supplemental TPD1E04U04 ESD protection diodes, a supplemental TVS0500 surge protection diode, footprints (R/L1 and R/L2) that could be replaced with inductors for EMI suppression (these footprints are populated with 0-Ω resistors by default), an anti-alias filter (R30, R31, and C35), and the AMC1106 isolated delta-sigma modulator.

In 図 12, the three-terminal shunt used for current measurement is to be connected to J15. The value of this shunt is selected based on balancing maximizing the peak analog voltage input into the AMC1106 with minimizing the power dissipation of the shunt. In particular, for optimal accuracy, the peak DC voltage fed into the AMC must be as close as possible to 50 mV without surpassing this voltage. This peak voltage is dependent on the rated maximum current of the system and the resistance of the selected

shunt. For example, this design uses 400-µΩ shunts . With these 400-µΩ shunts and a maximum RMS current of 90 A, the maximum DC voltage fed into the AMC is $90 \times \sqrt{2} \times (400 \times 10^{-6}) \approx 50$ mV. To minimize the power dissipation in the shunt, a smaller value shunt can also be used. In this design, 220-µΩ shunts are also used. However, by using smaller value shunts, the voltage fed into the AMC is also reduced. As a result, there is a tradeoff in accuracy. Based on the requirements of the system, the tradeoff in accuracy from using a shunt with a small resistance and the reduced power dissipation from choosing the smaller shunt must be taken into account when selecting the proper shunt value.

2.3.2 How to implement software for metrology testing

The MSP432 software used for evaluating this design is test software. This section discusses the features of the test software, which should provide insights on how to implement custom software for metrology testing. The first subsection discusses the setup of the AMC1210 and various peripherals on the MSP432. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

2.3.2.1 Setup

2.3.2.1.1 Clock

The MSP432 is configured to have its CPU clock (MCLK) set at 48 MHz and its subsystem master clock (SMCLK) set to 6 MHz. The clock source for MCLK and SMCLK is an external 48-MHz crystal. An external 32.768-kHz crystal is used as the clock source for the auxiliary clock (ACLK) of the device. This ACLK clock is set to a frequency of 32.768 kHz.

2.3.2.1.2 Port Map

The MSP432 has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP432 device in particular, the EUSCIB0 SPI module's SPI clock, SOMI, and SIMO functionality are all available options to port to ports P2, P3, and P7. In addition, the SMCLK clock output and SAR ADC triggering timer output are also available for output to ports P2, P3, and P7. In the test software, this port mapping feature is used for providing flexibility in the PCB layout.

Using the port mapping controller, the following mappings are used:

- PMAP_UCB0SIMO (EUSCIB0 SPI SIMO) → Port P2.2 (connected to the AD0 pin of the AMC1210)
- PMAP_UCB0CLK (EUSCIB0 SPI Clock) → Port P2.3 (connected to the WR pin of the AMC1210)
- PMAP_UCB0SOMI (EUSCIB0 SPI SOMI) → Port P2.4 (connected to the RD pin of the AMC1210)
- PMAP_SMCLK (SMCLK clock output) → Port P2.6 (connected to CLK pin of the AMC1210 so that it can be used as the modulator clock of the AMC1210 and AMC1106 devices; however, please note that this mapping is not enabled initially and is only enabled after the AMC1210 and SAR ADC have been initialized)
- PMAP_TA0CCR1A (timer output used to trigger SAR ADC)→ Port P2.7 (this is not connecting to anything on the AMC1210 and is only used for debugging purposes)

2.3.2.1.3 UART Setup for GUI Communication

The MSP432 is configured to communicate to the PC GUI through the RS-232 connection on this reference design. The MSP432 communicates to the PC GUI using a UART module configured for 8N1 at 9600 baud.

2.3.2.1.4 Real Time Clock (RTC)

The real-time clock module of the MSP432 is configured to give precise one second interrupts and update the time and date as necessary. Based off of these one second interrupts, a flag is updated to let the foreground process know when to output a high logic level on the WDI pin. After setting the WDI pin high, a timer is triggered that is used to toggle the logic level on the WDI pin back to a low logic state. Providing this pulse on the WDI pin of the TPS3850 is used to prevent the TPS3850 from resetting the MSP432.

2.3.2.1.5 LCD Controller

The LCD controller on the MSP432P4111 can support up to 8-mux displays and 320 segments or 4-mux displays and 176 segment displays. In the current design, the LCD controller is configured to work in 4-mux mode using 144 segments. The eight segment lines not used in the 4-mux mode of this design are used for the port mapping functionality. In this reference design, the LCD is configured for a refresh rate set to ACLK / 64, which is 512 Hz. For contrast control, external resistors are added between the R23, R13, R03 pins and GND, as 図 13 shows.

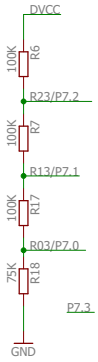


図 13. LCD External Resistors

2.3.2.1.6 Direct Memory Access (DMA)

The direct memory access (DMA) module transfers packets between the MSP432 and AMC1210 with minimal bandwidth requirements from the MSP432 CPU. Two DMA channels are used for communicating to the AMC1210. One channel (channel 0) is used to send data to the AMC1210 and the other channel (channel 1) is used to receive data from the AMC1210. Once a complete packet has been received from the AMC1210, an interrupt is generated to complete any necessary post-transfer processing. 図 19 shows the packets that are sent and received using the DMA of the MSP432.

2.3.2.1.7 ADC Setup

To get synchronized voltage and current samples, the AMC1210 device and the ADC14 module of the MSP432 must be properly initialized. 図 14 shows the process that is followed in this design to initialize and synchronize the AMC1210 and the ADC14 module of the MSP432. Before setting up the AMC1210 and the ADC14 module of the MSP432, the modulator clock of the AMC1106 is disabled to prevent the AMC1210 from generating new samples while trying to set it up. After this, the ADC14 module of the MSP432 is setup, the AMC1210 device is setup, and then the ADC14 module and AMC1210 are synchronized and started. The following sections provide details on this process.

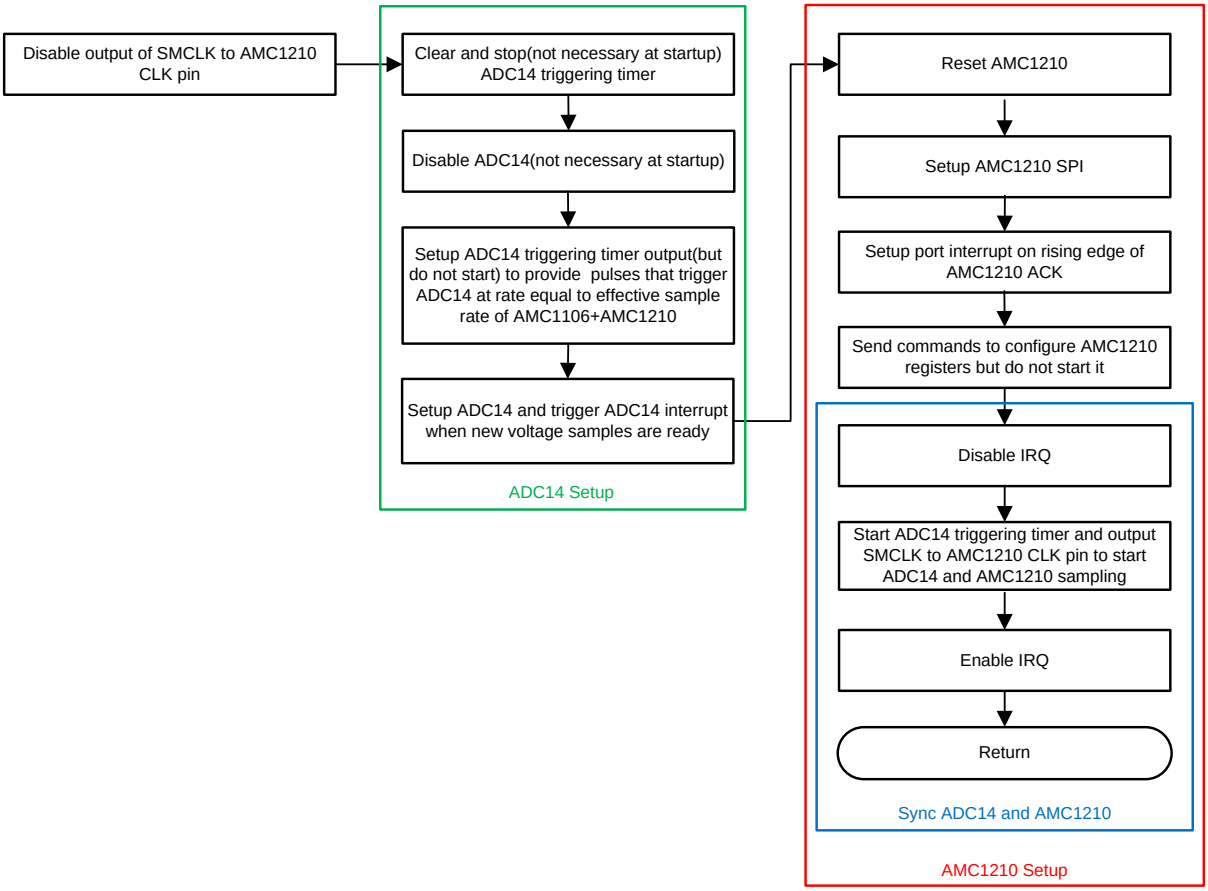


図 14. ADC Initialization and Synchronization Process

2.3.2.1.7.1 ADC14 Setup

The ADC14 is used to sample the three phase voltages and is triggered by the output of a timer. When setting up the ADC14, the ADC14 and triggering timer settings are reset in case the ADC14 and timer were previously initialized. After resetting the ADC14 and triggering timer, the triggering timer and its output that is used to trigger the timer are first initialized. Specifically, timer A0 is the triggering timer and its OUT1 (also referred to as TA0.1, TA0CCR1A, or TA0 CCR1 compare output OUT1) output is the specific output that triggers the SAR ADC using pulses.

To synchronize the voltage and current samples, the clock source of Timer A0 is set to the SMCLK clock, which is also used as the modulator clock by the AMC1106 devices and the AMC1210. Timer A0 counts SMCLK clock cycles until the number of clock cycles counted equals the effective oversampling ratio (EOSR) of the AMC1210, where the EOSR is the ratio of the modulation clock frequency to the effective sample rate of the AMC1210. As a result of counting up to the EOSR number of SMCLK clock cycles, the frequency of the pulses on the OUT1 pin is equal to the effective sample rate of the AMC1210.

The falling edge of the OUT1 pulses will occur right after timer A0 has just counted EOSR SMCLK clock cycles. The OUT1 rising edge, which is what actually triggers the SAR ADC, is set to occur before the OUT1 falling edge occurs in the present cycle. The location of the rising edge does not affect the OUT1 pulse frequency like the OUT1 falling edge so the OUT1 rising edge can occur anywhere within the present cycle before the OUT1 falling edge occurs as long as the time interval between rising edges is always fixed, similar to the example waveform as 図 15 shows. It is important that the interval between OUT1 rising edges is fixed to ensure that the delay between voltage and current samples is also fixed and not variable, which is necessary for accurately calculating power and energy-based metrology readings. By having both the rising edge and falling edge of the ADC triggering output set in hardware using a timer instead of doing it manually in software, a fixed time between rising edges on the triggering output is created. To ensure that there is one set of voltage ADC samples for each pulse on OUT1, the total time to sample all the phase voltages should be less than the time between two pulses on the OUT1 pin. Since in this design the OUT1 pulses trigger the SAR ADC and the total sample time for the phase voltages is less than the time between OUT1 pulses, the sample rate of the SAR ADC is equal to the sample rate of the current samples from the AMC1210, which is necessary for synchronizing the voltage and current samples.

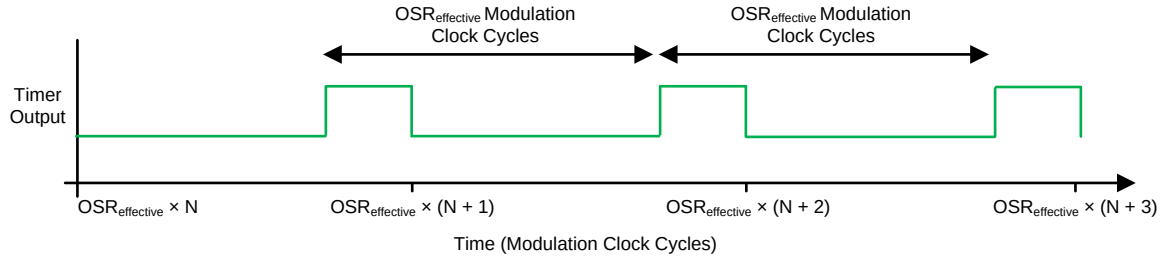


図 15. Example Waveform for Triggering Timer Output

Please note that after setting up the triggering timer , the timer is not started until after the ADC14 and AMC1210 are initialized and ready to be synchronized with each other. When setting up the ADC14, the ADC14 is configured to be in autoscan mode, which is a mode that allows the ADC14 to sample all the voltage channels sequentially every time conversions are triggered by the timer output. In the test software, the clock to the ADC14 is set to 3 MHz. Also, the conversion time for each sample is set so that the time it takes to sample all three voltage samples is much smaller than the time it takes to get one sample from the AMC1210. Specifically, the sample and hold time for each converter is 4 cycles and the conversion time is 16 cycles, which results in an approximate 20-cycle (approximately 7 µs) delay between conversion results of adjacent converters. The ADC14 is configured to generate an interrupt when a complete sequence of voltage samples are ready.

In the design, the ADC14 selects its reference voltage to be the 1.2-V reference from the REF_A module of the MSP432. This reference voltage is also output on a pin of the MSP432 so that it can be fed into the TLV9001 op amp for level shifting the voltage waveforms fed into the SAR ADC.

Additionally, the ADC14 is configured so that its 14-bit results are scaled to 16-bit twos complement numbers. This configuration allows the ADC results from the ADC14 to be treated as a 16-bit signed number when performing mathematical operations.

In this application, the following are the relevant ADC14 channel associations:

- A2 → Voltage V1 (Phase A)
- A1 → Voltage V2 (Phase B)
- A0 → Voltage V3 (Phase C)

2.3.2.1.7.2 AMC1210 Setup

After the ADC14 is initialized, the AMC1210 is then reset to get the device in a known state before initializing it. Next, the EUSCIB0 SPI module of the MSP432 is configured for communication to the AMC1210. The EUSCIB0 SPI module is specifically configured as a master device that uses 3 wire mode (the chip select signal is manually asserted high and low in the test software instead of using the chip select feature of the SPI module) and has a 3-MHz SPI clock that is derived from the 6-MHz SMCLK clock. In addition, the MSP432 is also configured to generate a port interrupt whenever a rising edge occurs on the ACK pin, which would indicate that the AMC1210 has new current samples that are available.

With the communication interface of the MSP432 to the AMC1210 setup, the MSP432 then sends commands to the AMC1210 to configure it. Please note that the modulation clock is not output by the MSP432 to the AMC1210 and AMC1106 until the ADC14 and AMC1210 synchronization function is called, which means that current sampling will not be started until after the AMC1210 registers are initialized to their proper values. By sending commands to the AMC1210 to initialize the AMC1210 registers, the AMC1210 is configured for the following:

- Three of the four AMC1210 digital filters are enabled. Filter module 1 is connected to the AMC1106 for Phase C, filter module 2 is connected to the AMC1106 for Phase B, and filter module 3 is connected to the AMC1106 for Phase A. Filter module 4 is not used in this design but is brought out to a header on the board if it is desired to connect to an additional, external isolated modulator device.
- Each digital filter has a separate register that is used to store the most recent current samples. This data register is configured to be 32-bits instead of 16-bits.
- Each of the three AMC1210 digital filters are set to output the modulator clock that is fed to the "CLK" pin of the AMC1210 to the different CLKx pins of the AMC1210 once the modulator clock is finally output by the MSP432. Outputting the modulator clock to the different CLKx pins, allows the modulator clock to be output to the different AMC1106 devices without having to route this clock across the PCB.
- Each filter unit of the digital filter is set to use a $SINC^3$ digital filter with a sampling oversampling ratio (SOSR) of 128. The output from a filter unit of the digital filter is fed to its corresponding integrator unit. The integrator unit is configured to sum a user-defined number of samples from the filter unit, referred to as the integrator oversampling ratio (IOSR), to produce one effective sample. The IOSR for each digital filter is set to 8. With a SOSR of 128 and a IOSR of 8, an EOSR of 1024 results. Given a modulator clock frequency of 6 MHz, the 1024 EOSR value means that the effective sample rate of the AMC1210 is 6,000,000 / 1024 = 5859.4 Hz.
- Every time a new effective sample is ready from the AMC1210, the ACK pin of the AMC1210 is set to logic high until all of the current samples are read from the AMC1210 by the MSP432.

Once all of the AMC1210 registers have been initialized, the sync_voltage_and_current function is called.

2.3.2.1.7.3 ADC14 and AMC1210 Synchronization

After the ADC14 module and AMC1210 registers are initialized, the sync_voltage_and_current is called. This function first starts by disabling interrupts. Disabling interrupts is done to ensure that the timing of when the voltage starts with respect to current is not affected by interrupts so that this timing is always the same every time this function is called. After disabling interrupts, the triggering timer of the ADC14 is started, which enables the SAR ADC for sensing voltage. Next, the modulation clock is output by the MSP432 so that the AMC1106 and AMC1210 could start current sensing. After starting the ADC14 and AMC1210 devices on the MSP432, interrupts are then enabled again.

2.3.2.2 Foreground Process

The foreground process includes the initial setup of the MSP432 hardware and software and the AMC1210 registers immediately after a device RESET. 図 16 shows the flowchart for this process.

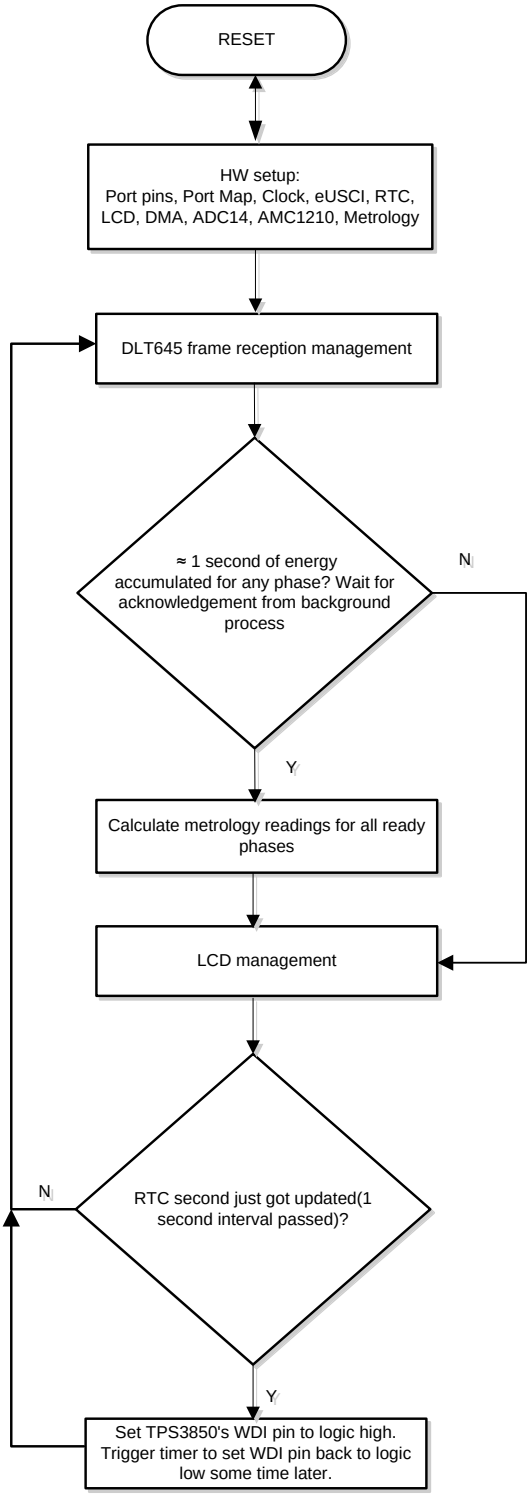


図 16. Foreground Process

The initialization routines involve the setup of the MSP432 general purpose input/output (GPIO) port pins and associated port map controller; MSP432 clock system; MSP432 USCI_A0 for UART functionality; MSP432 RTC module for clock functionality; MSP432 LCD; MSP432 DMA; MSP432 ADC14 module; AMC1210 registers; and MSP432 metrology variables.

After the hardware is setup, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters. This notification is accomplished through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for approximately one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage dot products are accumulated in 48-bit registers. In contrast, processed current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power of the foreground process, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in 2.3.2.2.1.

The foreground process also updates the LCD. The LCD display item is changed every two seconds. See 3.1.4.2.1 for more information about the different items displayed on the LCD.

In addition, the foreground process checks if a one-second RTC flag is set. This flag is set at a rate of once a second within the RTC ISR. If this flag is asserted, the MSP432 sets its GPIO pin that is connected to the WDI pin of the TPS3850 to a logic high. Once this GPIO pin is set to logic high, a timer is triggered, which is used to let the MSP432 know when to set the GPIO pin state back to logic low.

2.3.2.2.1 Formulae

This section briefly describes the formulas used for the voltage, current, power, and energy calculations. As previously described, voltage and current samples are obtained at a sampling rate of 5859.4 Hz. All of the samples that are taken in approximately one second frames are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained with the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample count}}} - v_{offset,ph} \quad (10)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample count}}} - i_{offset,ph}$$

where

- ph = Phase parameters that are being calculated [that is, Phase A (= 1), B (= 2), or C (= 3)],
- $V_{ph}(n)$ = Voltage sample at a sample instant n,
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter,
- $I_{ph}(n)$ = Each current sample at a sample instant n,
- $I_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter,
- Sample count = Number of samples within the present frame,
- $K_{v,ph}$ = Scaling factor for voltage,
- $K_{i,ph}$ = Scaling factor for current. (11)

Power and energy are calculated for active and reactive energy samples of one frame. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample Count}} v(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{ACT\_Offset,ph} \quad (12)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n-1}^{\text{Sample Count}} V_{90,ph}(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{React\_Offset,ph} \quad (13)$$

$$P_{APP,ph}{}^2 = \sqrt{P_{ACT,ph}{}^2 + P_{REACT,ph}{}^2}$$

where

- $V_{90}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°,
- $K_{ACT,ph}$ = Scaling factor for active power,
- $K_{REACT,ph}$ = Scaling factor for reactive power,
- $P_{ACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the active power measurements from other phases and the neutral,
- $P_{REACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the reactive power measurements from other phases and the neutral. (14)

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, the mains frequency is first measured accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated by the following 式 15, 式 16, and 式 17:

$$P_{ACT,Cumulative} = \sum_{ph=1}^{3} P_{ACT,ph} \quad (15)$$

$$P_{REACT,Cumulative} = \sum_{ph=1}^{3} P_{REACT,ph} \quad (16)$$

$$P_{APP,Cumulative} = \sum_{ph=1}^{3} P_{APP,ph} \quad (17)$$

Using the calculated powers, energies are calculated with the following formulas in 式 18:

$$E_{ACT,ph} = P_{ACT,ph} \times Samplecount$$
$$E_{REACT,ph} = P_{REACT,ph} \times Samplecount$$
$$E_{APP,ph} = P_{APP,ph} \times Samplecount \quad (18)$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following 式 19, 式 20, and 式 21:

$$E_{ACT,Cumulative} = \sum_{ph=1}^{3} E_{ACT,ph} \quad (19)$$

$$E_{REACT,Cumulative} = \sum_{ph=1}^{3} E_{REACT,ph} \quad (20)$$

$$E_{APP,Cumulative} = \sum_{ph=1}^{3} E_{APP,ph} \quad (21)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz with 式 22:

$$Frequency\ (Hz) = \frac{Sample\ Rate\ (samples / second)}{Frequency\ (samples / cycle)} \quad (22)$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated with 式 23:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{ if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{ if inductive load} \end{cases} \tag{23}$$

2.3.2.3 Background Process

図 17 shows the different events that occur when sampling voltage and current, where the items in olive green and turquoise are done by the hardware settings and not the test software.

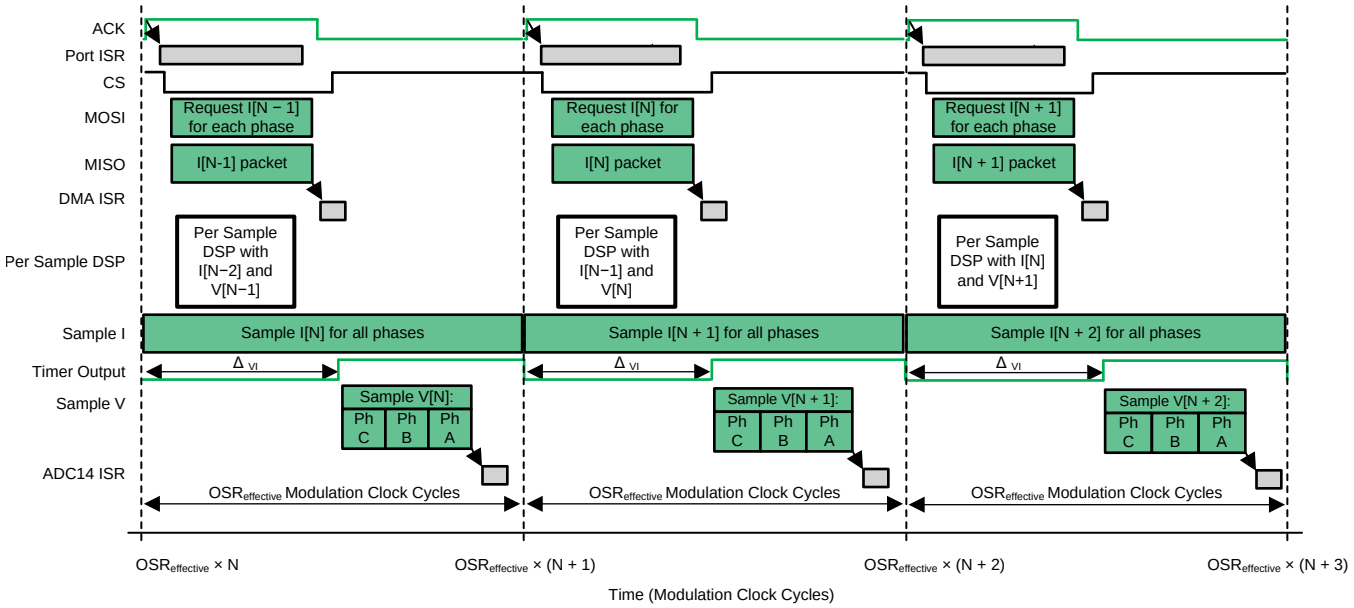


図 17. Voltage and Current Sampling Events

To go over the process mentioned in 図 17, new current samples for each phase are ready every EOSR, or 1024 for this design, modulation clock cycles. Suppose the most recently ready current sample from the AMC1210 corresponds to the N^{th}-1 current sample, or I[N – 1]). Once new samples are ready, the ACK pin is asserted high by the AMC1210. The rising edge on the ACK pin on the AMC1210 causes a GPIO port interrupt on the MSP432, which triggers the Port ISR on the MSP432. Within the Port ISR, the background process is run. 図 18 shows the background process, which mainly deals with timing critical events in the test software.

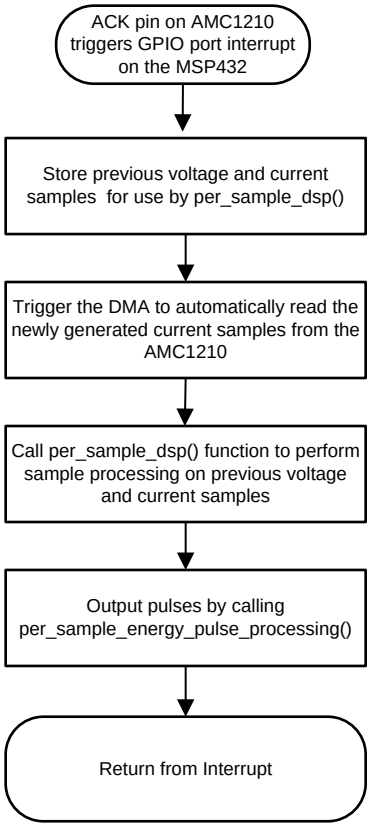


図 18. Background Process

In the background process, the previously obtained voltage samples (V[N-1]) and previously obtained current samples (I[N-2]) are stored so that they can be used later by the per_sample_dsp function, which is responsible for updating the intermediate dot product quantities used to calculate metrology parameters. After the previously obtained voltage and current samples are stored, communication to the AMC1210 is enabled by asserting the chip select signal low. The DMA is then configured to both send a request for the AMC1210's newest current samples (I[N-1]) and also to receive the data packet response from the AMC1210. The request and reception of the current samples is done automatically by the DMA module instead of it being done by the software.

図 19 shows the packet that is transmitted by the DMA of the MSP432 and the response packet from the AMC1210 that is received and assembled by the DMA as well. When requesting the ADC data from the AMC1210, the first packet that has to be sent to the AMC1210 is the command byte, which lets the AMC1210 know whether a read or write operation is being performed and on which AMC1210 register is this operation being performed. The value of this byte is set to 0x9D, which lets the AMC1210 know that we are requesting a read operation on the register that stores the ADC data for filter module 1. To read the response from the AMC1210, it is necessary for a dummy write to be performed for each byte that is to be read. The dummy byte write is necessary to enable the SPI clock, which is necessary to read a byte from the AMC1210. For each dummy byte write, a value of 0x00 is written to the SPI transmit register for EUSCIB0.

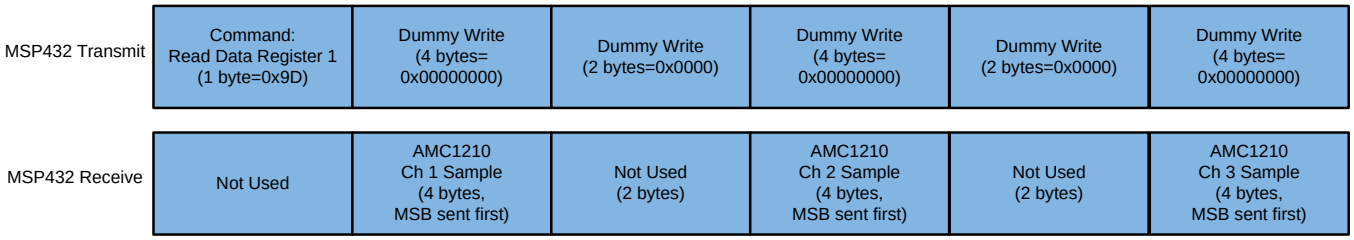


図 19. AMC1210 ADC Sample Request Packet

After the command byte is sent, writing four dummy bytes allows the MSP432 to receive the 4-byte ADC value from the first filter module of the AMC1210. After the first register has been read, the AMC1210 automatically outputs the values of subsequent registers until the chip select line is asserted back high, which resets the communication. In the register map of the AMC1210, the next register after an ADC data register is a two-byte time register, which we do not use. As a result, another two dummy writes are performed; however, because we do not need to use the results of the time register, we ignore these two corresponding bytes in the receive packet. The next register after the time register for filter module 1 is the ADC data register for filter module 2. To read the ADC data for filter module 2, we write another four dummy bytes. The next two dummy bytes are then written, which would cause us to receive the value of the time register for filter module 2. Since we do not need the contents of this time register, we ignore it in the received packet. The final four bytes are then written, which gets the ADC data for filter module 3. Whenever the DMA has received the entire I[N-1] packet from the AMC1210 図 19 shows, the DMA ISR is automatically called. Also, the ACK pin of the AMC1210 is automatically asserted low since all the current samples have been read. Within the DMA ISR, the I[N-1] packet is parsed so that it could be used when the per_sample_dsp function is called at the next interrupt. In addition, the chip select line is pulled back high to properly reset the AMC1210 communication before the next time current samples are ready from the AMC1210.

In parallel to receiving the newest current samples from the AMC1210 using the DMA, the AMC1106 and AMC1210 are currently sampling the next current samples (I[N]) and the test software also performs per sample processing on the last voltage (V[N-1]) and current samples (I[N-2])obtained from the AMC1210. This per sample processing is used to update the intermediate dot product quantities that are used to calculate the metrology parameters. After sample processing, the background process uses the "per_sample_energy_pulse_processing" for the calculation and output of energy-proportional pulses. Once the per_sample_energy_pulse_processing is completed, the test software exits from the port ISR.

In addition to the current sensing and background process calculations, the timer that triggers the SAR ADC is simultaneously counting cycles of the SMCLK clock. The timer's count is reset every 1024 modulation clock cycles so that the SAR ADC is triggered at a frequency equal to the frequency of current samples. Within the 1024 modulation clock cycles, the timer is set to have the output that triggers the SAR ADC go high. When this output goes high, the voltage sampling of the SAR begins, as 図 20 shows.

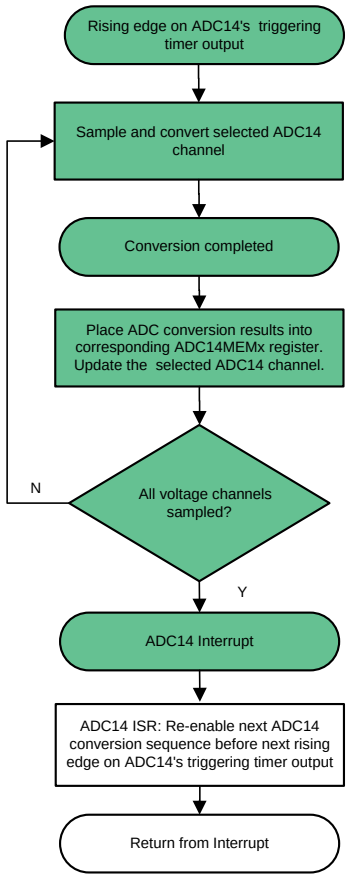


図 20. ADC14 Sampling Process

図 20 shows the ADC14 sampling process of the MSP432, where the items in turquoise represent items that are done automatically by the configuration of the ADC14 so they do not require CPU intervention. In the ADC14 sampling process, the first voltage channel is sampled. After the ADC results for this channel has been obtained, it is automatically placed in memory. Then the second voltage channel is sampled and its results are placed in memory. Finally the third SAR ADC channel is sampled and the results are placed in memory. After the third channel's results have been placed in memory, the ADC14's ISR is triggered. Within this ISR, the ADC14 has to be enabled again so that the voltages are automatically sampled again at the next rising edge on the SAR ADC's triggering timer's output.

2.3.2.3.1 per_sample_dsp()

図 21 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. The ADC14 is configured to represent the 14-bit voltage results as a 16-bit signed result. Because 16-bit voltage samples are used, the voltage samples are further processed and accumulated in dedicated 48-bit registers. Current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

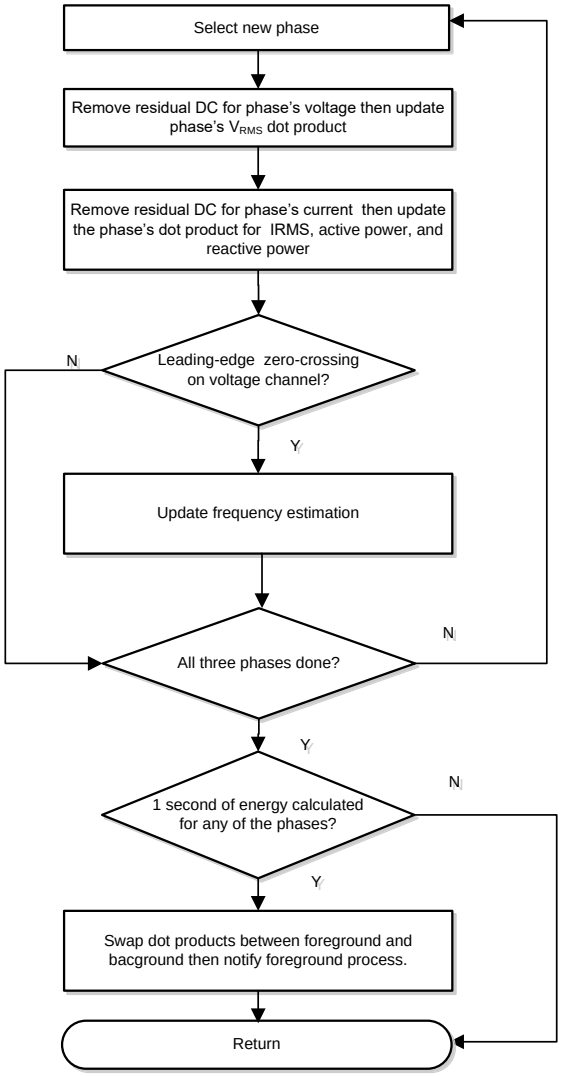


図 21. per_sample_dsp function

After sufficient samples (of approximately one second) are accumulated, the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; and power factor. In the test software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products. Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the corresponding phase's frequency (in samples per cycle) .

The following sections describe the various elements of electricity measurement in the per_sample_dsp() function.

2.3.2.3.1.1 Voltage and Current Signals

The output of the AMC1210 digital filters and ADC14 converter is a signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

2.3.2.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltages are accumulated in a 48-bit register. In contrast, the instantaneous currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one second's worth of samples have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. 図 22 shows the samples near a zero cross and the process of linear interpolation.

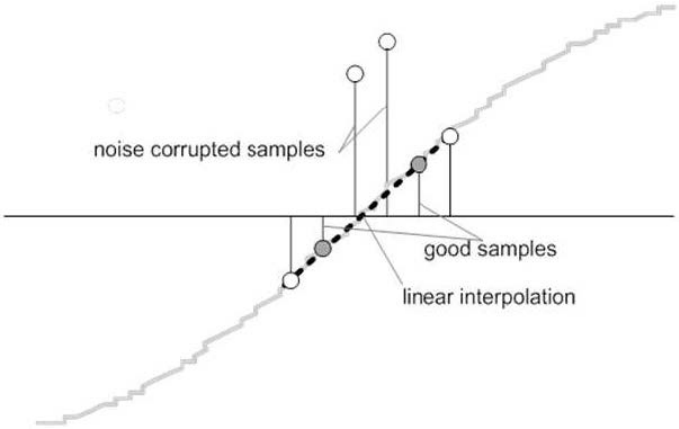


図 22. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

2.3.2.3.2 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSP432 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. If the absolute average power (calculated by the foreground process) is below a certain residual cutoff threshold for power (the residual cutoff threshold is set in the design to be 2.5 W and 2.5 var), then no energy is accumulated and the pulse generation function returns. If the absolute average power is above the residual cutoff threshold, the average power accumulates at every ACK port ISR interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The tick is usually defined in pulses per kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh / 6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses.

In the reference design, the LED that is labeled "Active" correspond to the active energy consumption for the cumulative three-phase sum. "Reactive" corresponds to the cumulative three-phase reactive energy sum.

図 23 shows the flow diagram for pulse generation.

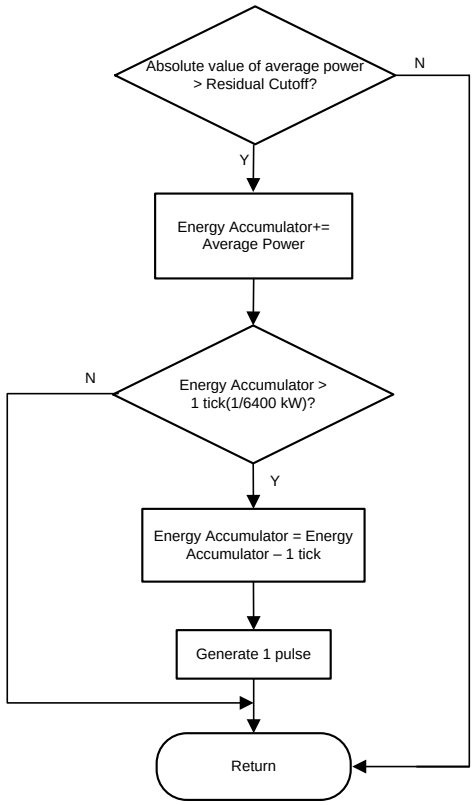


図 23. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and a 1-kWh threshold is defined as:

1-kWh threshold = 1 / 0.001 × 1 kW × (Number of interrupts per sec) × (Number of seconds in one hour) = 1000000 × 5859.4 × 3600 = 0x132F4AD71400

2.3.2.3.3 Phase Compensation

To ensure accurate measurements, the relative phase shift between voltage and current samples must be compensated. This phase shift may be caused by the passive components of the voltage and current input circuit, the sequential sampling on the voltage channel, or the delay from when the ADC14 and AMC1210 start sampling. The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 5859.4 Hz sample rate used in this application corresponds to a 0.0120° degree resolution at 50 Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Cautions and Warnings

At high currents, the terminal block can get warm. In addition, note that the AMC1106 devices are referenced with respect to the different phase voltages, so take the proper precautions.

WARNING

Hot Surface! Contact can cause burns. Do not touch. Take the proper precautions when operating.

CAUTION

High Voltage! Electric shocks are possible when connecting the board to live wires. The board must be handled with care by a professional. For safety, use of isolated test equipment with overvoltage or overcurrent protection is highly recommended.

3.1.2 Hardware

The following figures of the reference design best describe the hardware: 図 24 is the top view of the energy measurement system, and 図 25 shows the location of various pieces of the reference design based on functionality.

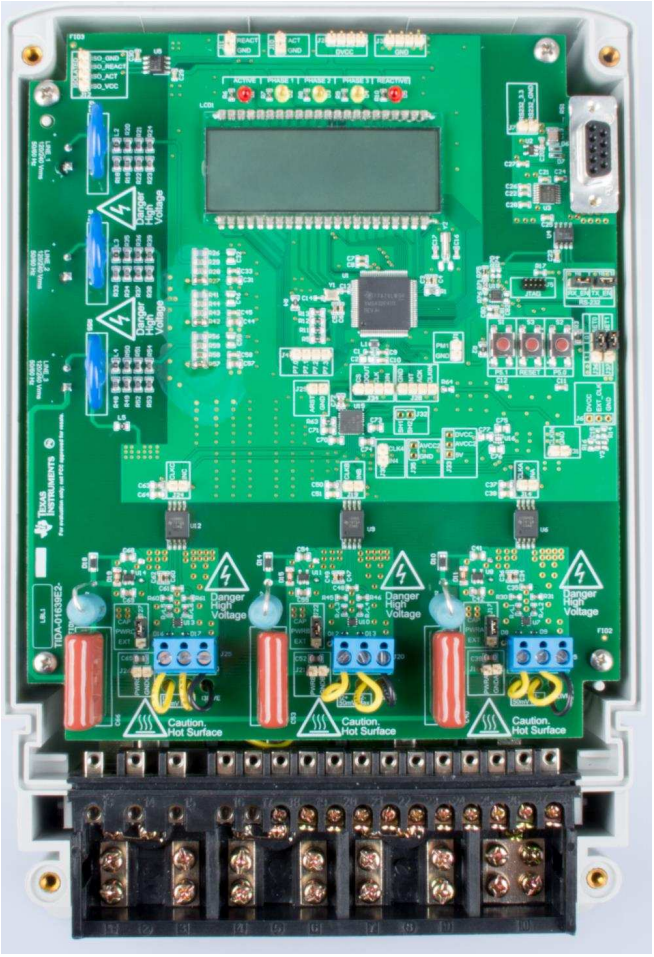


図 24. Top View of TIDA-01639 Design

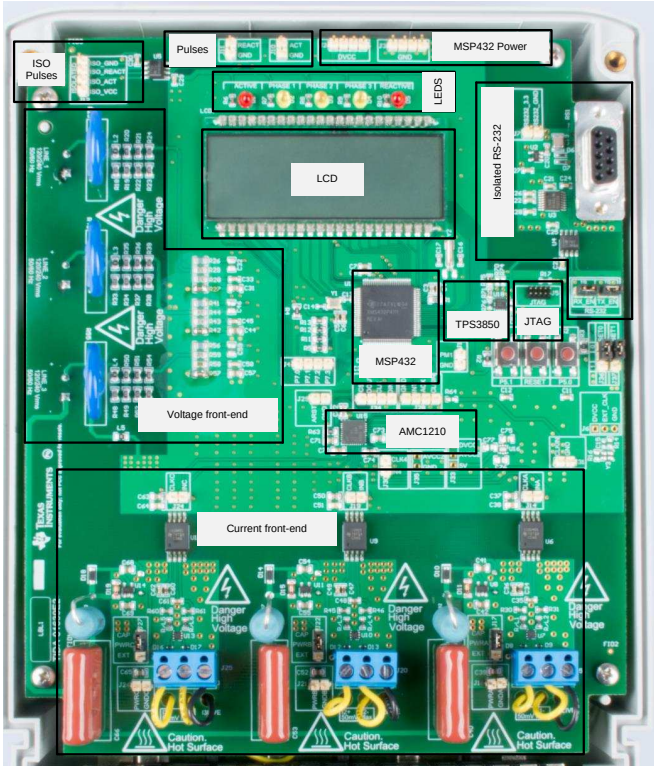


図 25. Top View of TIDA-01639 Design With Components Highlighted

3.1.2.1 Connections to the Test Setup for AC Voltages

AC voltages can be applied to the board for testing purposes at these points:

- Pad "LINE1 +" corresponds to the line connection for phase A.
- Pad "LINE2 +" corresponds to the line connection for phase B.
- Pad "LINE3 +" corresponds to the line connection for phase C.
- Pads "LINE 1 -", "LINE 2 -", "LINE 3 -" correspond to the neutral voltage. These pads are internally tied together on the PCB. The voltage between any of the three line connections to the neutral must not exceed 240-V AC at 50 and 60 Hz.
- I1+, I1−, and I1Live are connected to the output terminals of the shunt that is used for measuring the current for Phase A. When a shunt is selected, the differential voltage that is output across I1+ and I1− must not exceed 50 mV.
- I2+, I2−, and I2Live are connected to the output terminals of the shunt that is used for measuring the current for Phase B. When a shunt is selected, the differential voltage that is output across I2+ and I2− must not exceed 50 mV.
- I3+, I3−, and I3Live are connected to the output terminals of the shunt that is used for measuring the current for Phase C. When a shunt is selected, the differential voltage that is output across I3+ and I3−

must not exceed 50 mV.

図 26 shows a mapping between shunt terminals and I3 (Phase C) current pads. A similar mapping is done between the other shunts and corresponding phases.

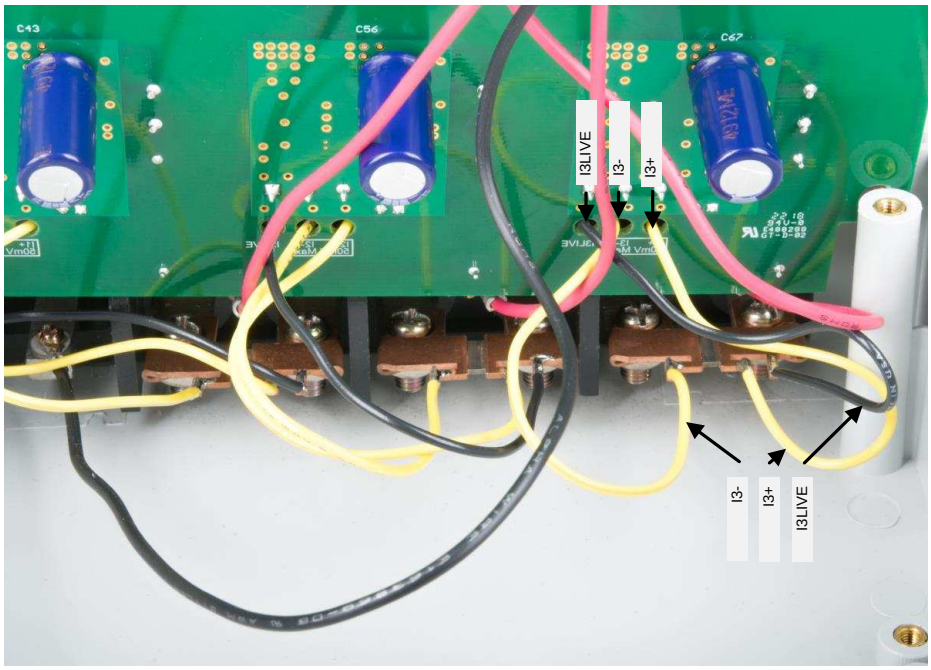


図 26. Mapping Between Shunt Terminals and Ix Current Pads

図 27 and 図 28 show the various test setup connections required for the reference design to function properly. When a test AC source must be connected, the links on the board must be connected as 図 27 shows.

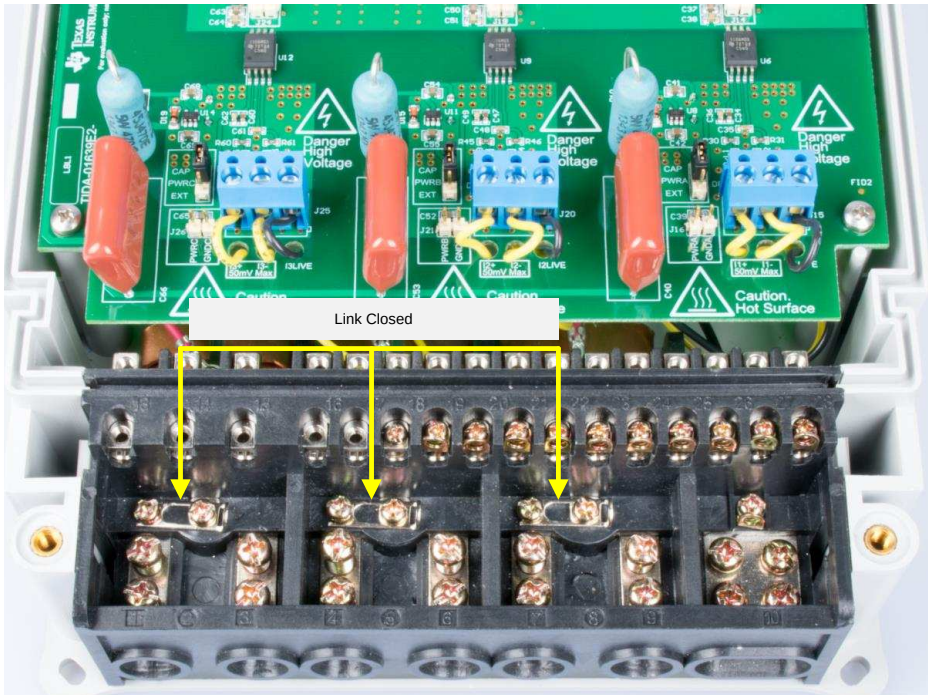


図 27. Top View of Reference Design with Links Closed

図 28 shows the connections from the front view. V_A+, V_B+, and V_C+ correspond to the lines for phases A, B, and C, respectively. V_N corresponds to the neutral voltage from the test AC source. I_A+ and I_A− correspond to the current inputs for phase A, I_B+, and I_B− correspond to the current inputs for phase B; I_C+ and I_C− correspond to the current inputs for phase C.

図 28. Front View of Reference Design with Test Setup Connections

3.1.2.2 Power Supply Options and Jumper Settings

The high-side of each AMC1106 is powered from mains. The controller side of the board is powered by a single 3.3-V DC voltage rail (DVCC), which must be derived from external power. Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. 表 2 indicates the functionality of each jumper on the board.

表 2. Header Names and Jumper Settings

NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J1	2-pin header	P2.7 GPIO pin/ADC14 Triggering Timer Output(WARNING)	Probe at this header to view the ADC14 triggering timer output.	This header has two pins: GND and PM1, where PM1 is the P2.7 GPIO pin.This header is not isolated from AC mains, so do not connect measuring equipment unless isolators external to the reference design are available.
J2	4-pin header	DVCC voltage header (WARNING)	Probe here for DVCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated. To power the controller side of this board, 3.3 V must be applied between this header and J3.
J3	4-pin header	Ground voltage header (WARNING)	Probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated. To power the controller side of this board, 3.3 V must be applied between J2 and this header.
J4	4-pin header	Header containing MSP432 P7.0, 7.1, P7.2, and P7.3 pins(WARNING)	Probe here for P7.0, P7.1, P7.2, and P7.3 GPIO pins.	The P7.0, P7.1, and P7.2 pins are used for adjusting contrast of the LCD. P7.3 is not used in this design. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J5	10-pin 2-row connector	JTAG: MSP432 programming header (WARNING)	Connect the MSP-FET- 432ADPTR adapter to this connector to power the MSP432 MCU.	The MSP-FET-432ADPTR is used to allow the MSP-FET tool to program the MSP432 device. One connector of the MSP-FET-432ADPTR adapter connects to the FET tool and the other connector connects to the JTAG connector of the MSP432. Note that the MSP432 has to be powered externally to program the MSP432 MCU. The external power can be provided between J2 and J3 on the board or a cable can be connected from the J2 header on the board to the "VCC Output" header option of the MSP-FET-432ADPTR adapter. To program the MSP432, the disable the watchdog timer functionality of the TPS3850H01 by connecting J36 to the "1" header pin option and J37 to the "0" header pin option. Since this header and the FET tool is not isolated, do not connect to this header when running off Mains and Mains is not isolated.
J7	2-pin header	Header containing RS232_3.3, which is the voltage source harvested from RS-232 line, and RS232_GND, which is the ground connection for the isolated RS-232	Probe here for the isolated 3.3-V supply generated on the RS-232's side of the isolation barrier.	
J8	2-pin jumper header	TX_EN: RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions.	—
J9	2-pin jumper header	RX_EN: RS-232 receive enable	Place a jumper here to enable receiving characters using RS-232.	—
J10	2-pin header	Active energy pulses (WARNING)	Probe here for cumulative three-phase active energy pulses. This header has two pins: GND and ACT, which is where the active energy pulses is actually output.	This header is not isolated from AC mains, so do not connect measuring equipment unless isolators external to the reference design are available. See the "ISO_ACT" pin of J12 instead, which is isolated.

表 2. Header Names and Jumper Settings (continued)

NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J11	2-pin header	Reactive energy pulses (WARNING)	Probe here for cumulative three-phase reactive energy pulses. This header has two pins: GND and REACT, which is where the reactive energy pulses is actually output.	This header is not isolated from AC mains, so do not connect measuring equipment unless isolators external to the reference design are available. See the "ISO_REACT" pin of J12 instead, which is isolated.
J12	4-pin header	Isolated pulses header	Probe here for the isolated cumulative three-phase active energy pulses and the isolated cumulative three-phase reactive energy pulses.	This header has four pins: ISO_GND, ISO_REACT, ISO_ACT, and ISO_VCC. ISO_GND is the isolated ground for the energy pulses. ISO_VCC is the VCC connection for the isolated active and reactive energy pulses. ISO_ACT is where the isolated active energy pulses are output. ISO_REACT is where the isolated active energy pulses are output. This header is isolated from AC mains so it is safe to connect to scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce the active energy pulses and reactive energy pulses at this header. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
J13	2-pin terminal block	Phase A voltage(WARNING)	Phase A line connection	This terminal block is connected to the Neutral voltage and phase A line voltage connections on the reference design case using wires. The pin on the terminal block that should be connected to neutral is denoted by a "-" on the PCB silk screen. The pin on the terminal block that should be connected to the line of Phase A is denoted by a "+" on the PCB silk screen. The neutral connection on J13, J18, and J23 are all connected to each other on the PCB. This is the Phase A line voltage connection so only probe here if using equipment that could measure the Mains voltage.
J14	2-pin header	Header with bit-stream output and modulator clock input for the AMC1106 for phase A(WARNING)	Probe between here and ground for the bit-stream output from the AMC1106 chip associated with Phase A.	This header has two pins: INA and CLKA. INA is Phase A's AMC1106's bitstream output. CLKA is Phase A's AMC1106's modulated clock input. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J15	3-pin terminal block	Shunt connections for the shunt(WARNING) of Phase A	Phase A shunt connection	This terminal block is connected to the Phase A shunt installed in the case of this reference design. Wires from the shunt are connected to this terminal block. The shunts are referenced with respect to the corresponding line of that phase so do not connect measuring equipment when running from Mains. This terminal block has the following 3 pins: I1+, I1-, and I1Live. I1Live is the line for that phase, which is used for the ground of the AMC1106 device for Phase A. The output voltage from the shunt current sensor is between I1+ and I1-. 3.1.2.1 shows the mapping between the shunts and the three pins of this terminal block.
J16	3-pin jumper header	Selection for the AMC1106 high-side power supply for Phase A(WARNING)	This header is used to select the power source for the AMC1106 associated with Phase A.	To enable powering the high-side using the onboard cap-drop supply, place a jumper from the center pin of this header to the pin labeled "CAP" on this header. To enable powering the high side by external power, apply voltage directly to the J17 header and place a jumper from the center pin of this header to the pin labeled "EXT" on this header. The applied voltage on J17 should be 3.3 or 5 V to properly power the AMC1106 when using this external power option. Since this header is close in voltage to the line A phase voltage, do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J17	2-pin header	External power header for the AMC1106 device(WARNING) of Phase A	This header is used to power the AMC1106 device for Phase A when a jumper is placed on the "EXT" option of J16.	This header contains two pins: PWRA and GNDA. GNDA is where the negative terminal of the external power supply's output should be connected. Please note that this GNDA pin is referenced with respect to the line for Phase A. PWRA is where the positive terminal of the external power supply's output should be connected. To enable powering the AMC1106's high side by external power, first apply a jumper from the center pin of J16 to the pin labeled "EXT" on this header. The applied voltage on this header should be 3.3 V or 5 V to properly power the AMC1106 when using this external power option. Since this header is close in voltage to the line A phase voltage, do not connect measuring equipment when running from Mains unless it is isolated from Mains. Also, do not connect a power supply here unless the power supply is able to have the negative terminal of its output connected to the phase A line.

表 2. Header Names and Jumper Settings (continued)

NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J18	2-pin terminal block	Phase B voltage(WARNING)	Phase B line connection	This terminal block is connected to the Neutral voltage and phase B line voltage connections on the reference design case using wires. The pin on the terminal block that should be connected to neutral is denoted by a "-" on the PCB silk screen. The pin on the terminal block that should be connected to the line of Phase B is denoted by a "+" on the PCB silk screen. The neutral connection on J13, J18, and J23 are all connected to each other on the PCB. This is the Phase B line connection so only probe here if using equipment that could measure the Mains voltage.
J19	2-pin header	Header with bit-stream output and modulator clock input for the AMC1106 for phase B(WARNING)	Probe between here and ground for the bit-stream output from the AMC1106 chip associated with Phase B.	This header has two pins: INB and CLKB. INB is Phase B's AMC1106's bitstream output. CLKB is Phase B's AMC1106's modulated clock input. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J20	3-pin terminal block	Shunt connections for Phase B's shunt(WARNING)	Phase B shunt connection	This terminal block is connected to the Phase B shunt installed in this reference design's case. Wires from the shunt are connected to this terminal block. The shunts are referenced with respect to the corresponding line of that phase so do not connect measuring equipment when running from Mains. This terminal block has the following 3 pins: I2+, I2-, and I2Live. I2Live is the line for that phase, which is used for the ground of the AMC1106 device for Phase B. The output voltage from the shunt current sensor is between I2+ and I2-. 3.1.2.1 shows the mapping between the shunts and the three pins of this terminal block.
J21	3-pin jumper header	Selection for the AMC1106 high-side power supply for Phase B(WARNING)	This header is used to select the power source for the AMC1106 associated with Phase B.	To enable powering the high-side using the onboard cap-drop supply, place a jumper from the center pin of this header to the pin labeled "CAP" on this header. To enable powering the high side by external power, apply voltage directly to the J22 header and place a jumper from the center pin of this header to the pin labeled "EXT" on this header. The applied voltage on J22 should be 3.3 or 5 V to properly power the AMC1106 when using this external power option. Since this header is close in voltage to the line B phase voltage, do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J22	2-pin header	External power header for Phase B's AMC1106 device(WARNING)	This header is used to power the AMC1106 device for Phase B when a jumper is placed on the "EXT" option of J21.	This header contains two pins: PWRB and GNDB. GNDB is where the negative terminal of the external power supply's output should be connected. Please note that this GNDB pin is referenced with respect to the line for Phase B. PWRB is where the positive terminal of the external power supply's output should be connected. To enable powering the AMC1106's high side by external power, first apply a jumper from the center pin of J21 to the pin labeled "EXT" on this header. The applied voltage on this header should be 3.3 or 5 V to properly power the AMC1106 when using this external power option. Since this header is close in voltage to the line B phase voltage, do not connect measuring equipment when running from Mains unless it is isolated from Mains. Also, do not connect a power supply here unless the power supply is able to have the negative terminal of its output connected to the phase B line.
J23	2-pin terminal block	Phase C voltage(WARNING)	Phase C line connection	This terminal block is connected to the Neutral voltage and phase C line connections on the reference design case using wires. The pin on the terminal block that should be connected to neutral is denoted by a "-" on the PCB silk screen. The pin on the terminal block that should be connected to the line of Phase C is denoted by a "+" on the PCB silk screen. The neutral connection on J13, J18, and J23 are all connected to each other on the PCB. This is the Phase C line connection so only probe here if using equipment that could measure the Mains voltage.
J24	2-pin header	Header with bit-stream output and modulator clock input for the AMC1106 for phase C(WARNING)	Probe between here and ground for the bit-stream output from the AMC1106 chip associated with Phase C.	This header has two pins: INC and CLKC. INC is Phase C's AMC1106's bitstream output. CLKC is Phase C's AMC1106's modulated clock input. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J25	3-pin terminal block	Shunt connections for Phase C's shunt(WARNING)	Phase C shunt connection	This terminal block is connected to the Phase C shunt installed in this reference design's case. Wires from the shunt are connected to this terminal block. The shunts are referenced with respect to the corresponding line of that phase so do not connect measuring equipment when running from Mains. This terminal block has the following 3 pins: I3+, I3-, and I3Live. I3Live is the line for that phase, which is used for the ground of the AMC1106 device for Phase C. The output voltage from the shunt current sensor is between I3+ and I3-. 3.1.2.1 shows the mapping between the shunts and the three pins of this terminal block.

表 2. Header Names and Jumper Settings (continued)

NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J26	3-pin jumper header	Selection for the AMC1106 high-side power supply for Phase C(WARNING)	This header is used to select the power source for the AMC1106 associated with Phase C.	To enable powering the high-side using the onboard cap-drop supply, place a jumper from the center pin of this header to the pin labeled "CAP" on this header. To enable powering the high side by external power, apply voltage directly to the J27 header and place a jumper from the center pin of this header to the pin labeled "EXT" on this header. The applied voltage on J27 should be 3.3 or 5 V to properly power the AMC1106 when using this external power option. Since this header is close in voltage to the line C phase voltage, do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J27	2-pin header	External power header for Phase C's AMC1106 device(WARNING)	This header is used to power the AMC1106 device for Phase C when a jumper is placed on the "EXT" option of J26.	This header contains two pins: PWRC and GNDC. GNDC is where the negative terminal of the external power supply's output should be connected. Please note that this GNDC pin is referenced with respect to the line for Phase C. PWRC is where the positive terminal of the external power supply's output should be connected. To enable powering the AMC1106's high side by external power, first apply a jumper from the center pin of J26 to the pin labeled "EXT" on this header. The applied voltage on this header should be 3.3 or 5 V to properly power the AMC1106 when using this external power option. Since this header is close in voltage to the line C phase voltage, do not connect measuring equipment when running from Mains unless it is isolated from Mains. Also, do not connect a power supply here unless the power supply is able to have the negative terminal of its output connected to the phase C line.
J28	4-pin header	Header containing GND and connections to the AMC1210's INT, ACK, and CLK pins (WARNING)	Probe here for the AMC1210's INT, ACK, and CLK pins.	The AMC1210's ACK pin is used to alert the MSP432 that new current samples are available. The CLK pin is the system clock of the AMC1210. The modulator clock is connected to this CLK pin so the modulator clock can be viewed by probing this CLK pin of this header. The INT pin is not used in this design. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J29	2-pin header	Header containing GND and a connection to the AMC1210's RST pin(WARNING)	Probe here for the AMC1210's RST pin.	The AMC1210's RST pin is used to reset the AMC1210. When initializing the AMC1210, the MSP432 drives this pin to reset the AMC1210. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J30	2-pin header	Header containing connections to the AMC1210's IN4 and CLK4 pins(WARNING)	Probe here for the AMC1210's IN4 and CLK4 pin.	The AMC1210's IN4 pin is the bitstream input for the fourth digital filter module on the AMC1210. The CLK4 pin is the modulator clock input/output for the fourth digital filter module on the AMC1210. The fourth digital filter module is not used in the test software and hardware of this design; however, the necessary pins for this forth digital filter module are brought out to this header in case it is desired to measure a fourth current such as the neutral current using a modulator external to this board in the future. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J34	4-pin header	Header containing the AMC1210's chip select and SPI pins	Probe here for connections to the AMC1210's chip select and SPI signals	This header contains connections to the following pins on the AMC1210: CS, RD, WR, and AD0. The CS pin is the AMC1210's chip select, which is driven manually by the AMC1210. The RD pin is configured as the AMC1210's SPI Data In or the SPI data out (SIMO) of the MSP432. The WR pin is configured as the SPI clock. The AD0 pin is configured as the AMC1210's SPI Data Out or the SPI data in (SOMI) of the MSP432. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available.
J36	3-pin jumper header	Connection to the TPS3850H01's SET0 pin	This header is used to connect the TPS3850H01's SET0 pin to either 0 or 1.	To program the MSP432, disable the watchdog timer functionality of the TPS3850H01 by connecting J36 to the "1" header pin option and J37 to the "0" header pin option. 2.3.1.1 provides more details on the associated functionality for the other states of SET0 and SET1.
J37	3-pin jumper header	Connection to the TPS3850H01's SET1 pin	This header is used to connect the TPS3850H01's SET1 pin to either 0 or 1.	To program the MSP432, disable the watchdog timer functionality of the TPS3850H01 by connecting J36 to the "1" header pin option and J37 to the "0" header pin option. 2.3.1.1 provides more details on the associated functionality for the other states of SET0 and SET1.

3.1.3 Software

The MSP432 software used for evaluating this design is test software. 2.3.2 and 3.1.4.1.1 discuss the features of the test software, which should provide insights on how to implement custom software for metrology testing.

3.1.4 Testing and Results

3.1.4.1 Test Setup

3.1.4.1.1 Voltage DC Offset and Settle Time Testing

When testing this design, two voltage front-end implementations were tested and compared to each other. Specifically, the V_{REF} voltage divider and op-amp implementation that 図 7 shows is compared to the AVCC-based voltage divider and no op-amp implementation as 図 10 shows. In this design, the V_{REF} voltage divider and op-amp implementation is actually what is used as the voltage front-end implementation. The AVCC-based voltage divider and no-amp implementation is an alternative voltage front-end circuit that is not used in this design. This alternative voltage front-end circuit is used instead in an older revision of this design. The two voltage front-end implementations are tested by comparing the performance of this design to the performance of an older revision of this design that used the AVCC-based voltage divider and no op-amp implementation.

To test the performance of the two voltage front-end implementations, DC offset and settle time testing is performed on the circuits in 図 7 and 図 10. 図 7 shows the V_{REF} voltage divider and op-amp implementation can work with either the 1.2-, 1.45-, or 2.5-V reference options that are available from the REF_A module of the MSP432; however, the AVCC-based voltage divider and no op-amp implementation shown in 図 10 can only work with the 2.5-V reference option. To better compare the results from the two implementations, a 2.5-V reference is used for the two designs with the different voltage front-end circuits. This 2.5-V reference is used in this design only for this voltage DC offset and settle time testing. For all other tests on this design, the 1.2-V reference is used instead.

When the voltage waveforms are fed to the SAR ADC of the MSP432, the average DC value of the waveforms is constantly being measured by a dc filter so that it could be subtracted from each voltage sample. For each phase, there is a separate dc filter estimate because the dc content of each phase will vary based on the individual ADC offsets and the variations in the actual resistance values within the level shifting circuit. In this design, the ADC14 is configured to represent its 14-bit ADC results as a signed binary (2's complement) 16-bit integer. By representing the 14-bit ADC results as a signed binary number, the normal 0 to 16,383 range for a 14-bit ADC is mapped to fit a range from –32,768 to 32,767. By configuring the ADC to use this signed binary representation for the ADC data, the test software of the design sees 16-bit ADC sample data instead of 14-bit ADC sample data. As a result, the measured average DC value of a voltage channel is based on an average of the signed 16-bit representation of the 14-bit ADC results instead of the average of the unsigned 14-bit representation of ADC results.

In the GUI of the design, the average DC value for the voltage channel of each phase is displayed in the "Voltage DC offset" field, as 図 29 shows.

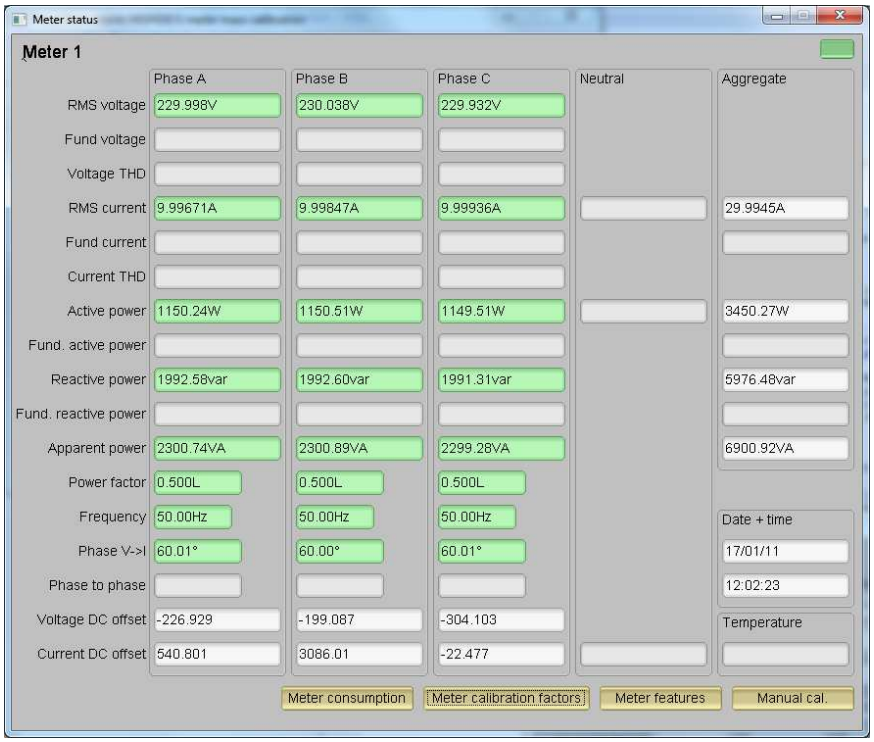


図 29. GUI Results Window That Displays Average Voltage DC Value

In testing the voltage DC offsets for both voltage front-end implementations, 3.3 V is applied as the AVCC, DVCC voltage and 230 V_{RMS} is the nominal voltage applied to the voltage front-end circuits. After applying these conditions, the values for the voltage dc offset for both voltage front-end implementations of each phase are obtained from the GUI.

For testing the settle time of both voltage front-end circuits, 230 V_{RMS} is first applied to meter to ensure that the AMC1106 devices are powered first and that the V_{RMS} waveforms are ready and stable before starting any delay measurements. After applying the V_{RMS} waveform to the meter, the MSP432 device is then powered. The time between when the MSP432 is first powered to when the V_{RMS} reading of the GUI settles between 229 V and 231 V is measured. For this measurement, please note that the readings measured on the GUI is internally averaged by the GUI and is updated at a relatively slower rate than the readings measured by the MSP432 itself. As a result, the settle time is a little longer with these GUI results than the direct metrology results on the MSP432 itself.

Another test that was performed was a cumulative active energy settle time test. In this test, the same conditions as the V_{RMS} settle time test was used except the delay from when the MSP432 is powered to when the cumulative active energy pulses settle is now measured instead of the time it takes for V_{RMS} to settle. The cumulative active energy pulse settle time was determined by connecting the cumulative active energy pulse output from the design to a reference meter and measuring the time it takes for the cumulative active energy error readings measured by the reference meter to stabilize to their final value. For this test, 10 Amps is applied on each phase of the design and a metering constant of 6400 impulses/kWh is used to map the pulse frequency to the associated energy consumption. The reference meter is set to average 10 pulses to produce one active energy error reading.

3.1.4.1.2 Metrology Accuracy Testing

To test for metrology accuracy, a source generator was used to provide the voltages and currents to the system at the proper locations mentioned in 3.1.2.1. Additionally, a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz are used for each phase.

When the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the system's active and reactive energy output pulse. In this reference design, cumulative active energy error testing, cumulative reactive energy error testing, voltage variation testing, and frequency variation testing are performed after performing energy gain calibration, phase compensation, and energy offset calibration as described in 3.1.4.2.2.2.

For cumulative active energy error and cumulative reactive energy error testing, current is varied from 100 mA to 80 A simultaneously at each phase. For cumulative active energy error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current waveforms fed to the reference design. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts. For cumulative reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used and cumulative reactive energy error is plotted instead of cumulative active energy error.

In performing metrology tests, two sets of voltage tests were also performed. In the first test, the 230-V nominal voltage was varied by ±10% at different currents and power factors. The resulting active energy error at each test point was then logged. For the second test, the active energy error was plotted when voltage was varied over a larger voltage range at unity power factor. Specifically, voltage was varied from 80 to 270 V. Testing beyond 270 V can also be done; however, this requires the 275-V varistors to be removed from the design and replaced with varistors that are rated for a higher voltage.

Another set of tests performed are frequency variation tests. For this test, the frequency is varied by ±2 Hz from its 50-Hz nominal frequency. This test is conducted at 0.5 A and 10 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error under these conditions are logged.

3.1.4.2 Viewing Metrology Readings and Calibration

This section describes the methods used to verify the results of this design with the test software.

3.1.4.2.1 Viewing Results from LCD

The LCD scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. 図 30, 図 31, and 図 32 show the mapping between the different orientations of the triangle and the phase descriptor:

図 30. Symbol for Phase A

図 31. Symbol for Phase B

図 32. Symbol for Phase C

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. 表 3 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

表 3. Displayed Parameters

PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power	AcPo	Watt (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power	rEPo	Volt-Ampere Reactive (var)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power	APPo	Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor	PF	Constant between 0 and 1	This parameter is displayed for each phase.
Voltage	Vrms	Volts (V)	This parameter is displayed for each phase.
Current	Irms	Amps (A)	This parameter is displayed for each phase.
Frequency	Fr89	Hertz (Hz)	This parameter is displayed for each phase.
Total consumed active energy	AcEn	kWh	This parameter is displayed for each phase.
Total consumed reactive energy	rEEn	kVarh	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time	t inE	Hour:minute:second	This parameter is only displayed when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date	dAtE	Year:month:day	This parameter is only displayed when the aggregate readings are displayed. This parameter is not displayed once per phase.

図 33 shows an example of the measured frequency of phase B of 49.99 Hz, displayed on the LCD.

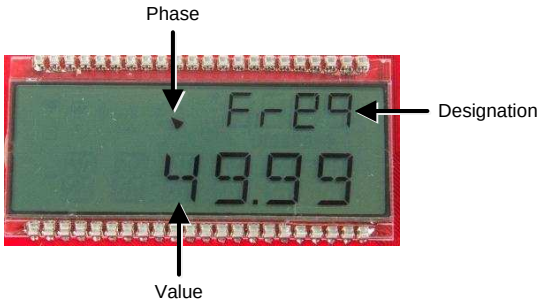


図 33. LCD

3.1.4.2.2 Calibrating and Viewing Results From PC

3.1.4.2.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the reference design to a PC using an RS-232 cable.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As 図 34 shows, this field is changed to *COM7*.

```
260       </correction>
261     </phase>
262     <temperature/>
263     <rtc/>
264   </cal-defaults>
265   <meter position="1">
266     <port name="com7" speed="9600"/>
267   </meter>
268   <reference-meter>
269     <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270     <type id="chroma-66202"/>
271     <log requests="on" responses="on"/>
272     <scaling voltage="1.0" current="1.0"/>
273   </reference-meter>
```

図 34. GUI Configuration File Changed to Communicate With Energy Measurement System

4. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the reference design, the GUI opens (see 図 35). If the GUI connects properly to the design, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

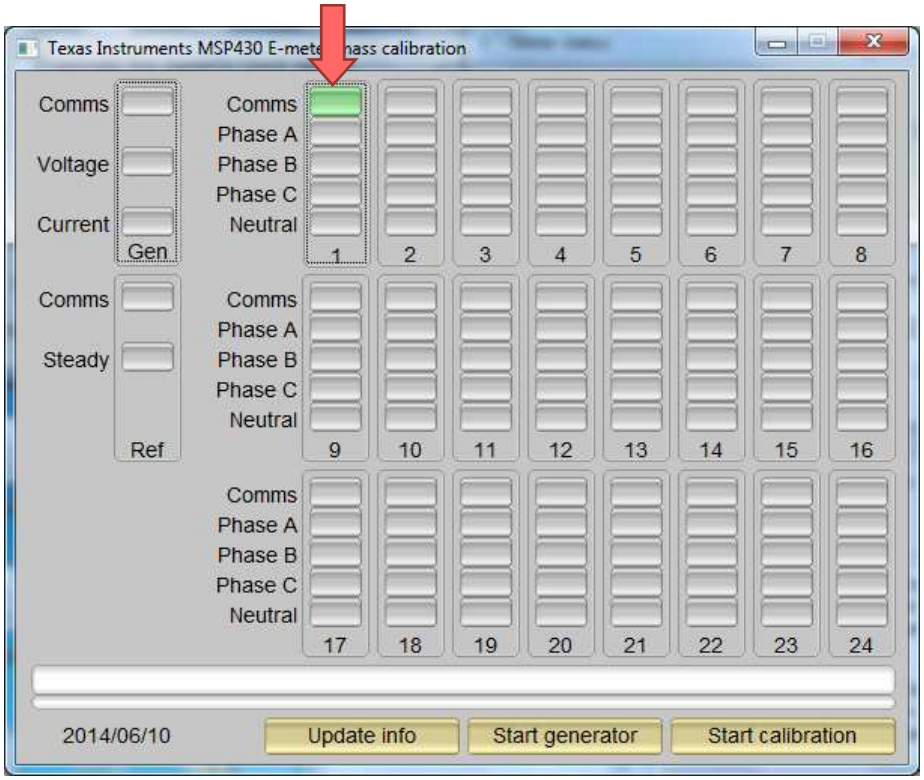


図 35. GUI Startup Window

Upon clicking on the green button, the results window opens (see 図 36). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

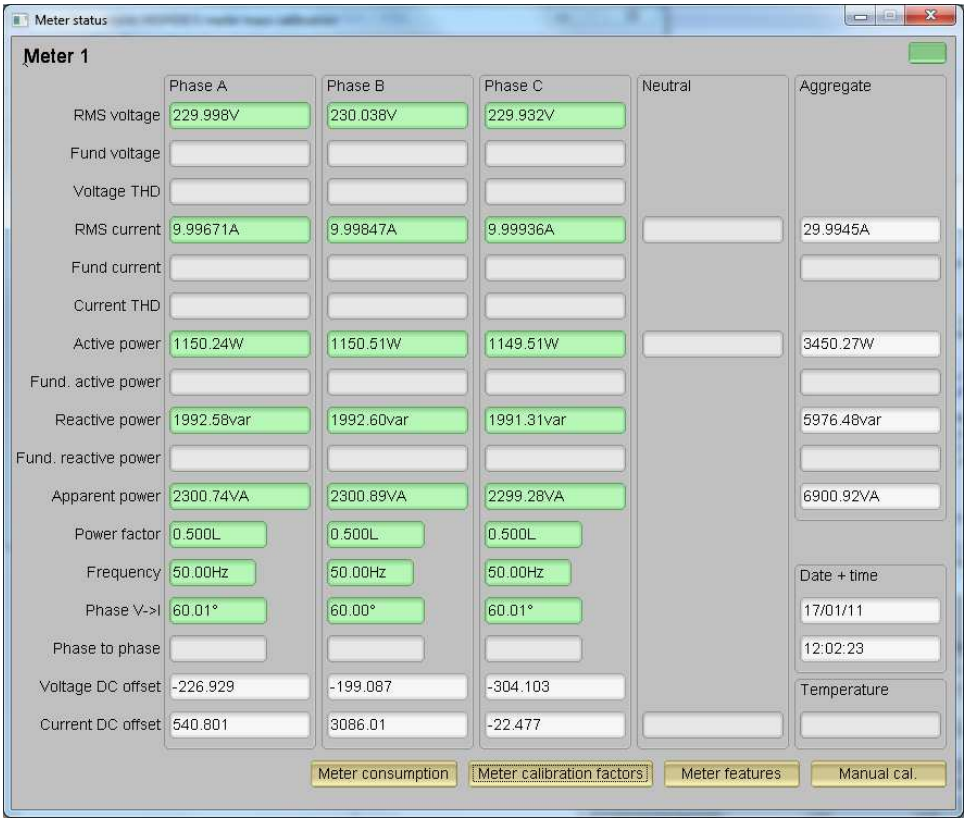


図 36. GUI Results Window

From the results window, the total-energy consumption readings can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as 図 37 shows.

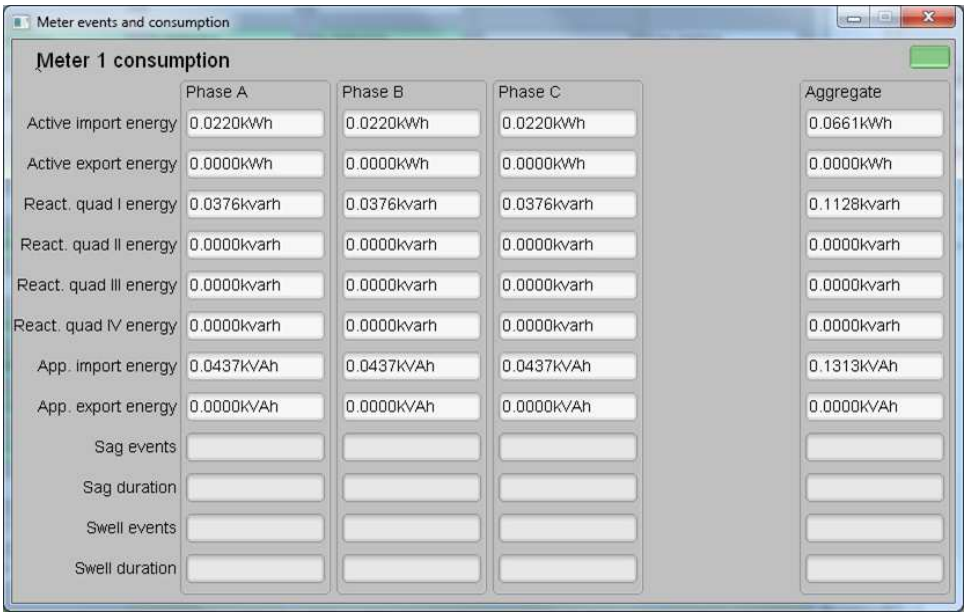


図 37. Meter Events and Consumption Window

From the results window, the user can also view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

3.1.4.2.2.2 Calibration

Calibration is key to any meter performance, and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase design.

The GUI used for viewing results can easily be used to calibrate the design. During calibration, parameters called calibration factors are modified in the test software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, active power offset (erroneously called voltage AC offset in the GUI), current scaling factor, reactive power offset (erroneously called current AC offset in the GUI), power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The power offset is used to subtract voltage to current crosstalk, which appears as a constant power offset and causes greater inaccuracies at lower currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter SW is flashed on the MSP432 devices for the first time default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted.

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with 3.1.2.1, and the energy pulses connected to the reference meter.

3.1.4.2.2.2.1 Gain Calibration

Usually, gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other two phases must be turned OFF by turning off the current but leaving the other voltages still enabled.

3.1.4.2.2.2.2 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply desired voltage and current for all phases. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 230 V, 10 A, 0º (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button that 図 36 shows. The following screen pops up from 図 38:

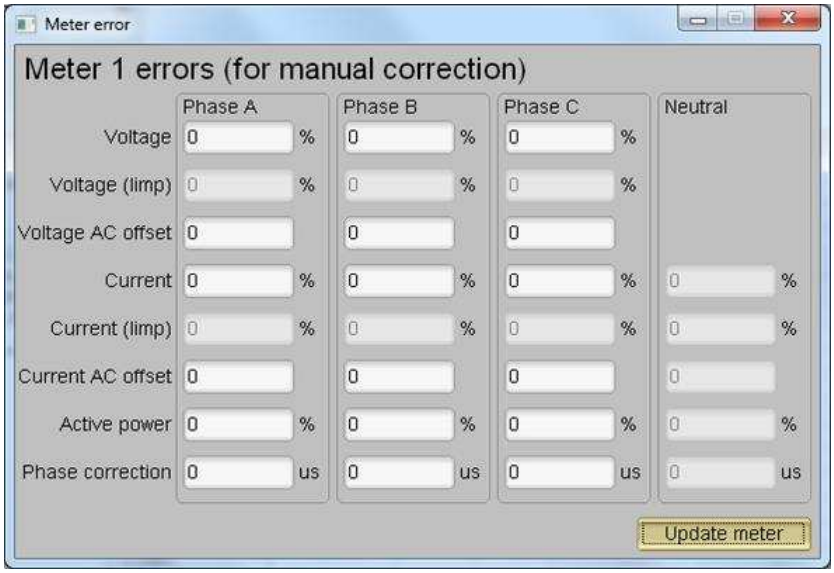


図 38. Manual Calibration Window

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated using 式 24:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (24)$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

3.1.4.2.2.2.3 Active Power Gain Calibration

注: This section is an example for one phase. Repeat these steps for other phases.

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating the active energy % error as is done with voltage and power can be done, this method is not the most accurate and should be avoided.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, perform the following steps:

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source.
3. Repeat Step 1 to Step 3 from 3.1.4.2.2.2.2 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
5. Enter the error obtained in Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

3.1.4.2.2.2.4 Offset Calibration

After performing gain calibration, if the accuracy at low currents is not acceptable, offset calibration could be performed. Offset calibration removes any crosstalk, such as the crosstalk to the current channels of a phase from the line voltages and neutral.

To perform active power offset calibration for a phase, simply add the offset to be subtracted from the active power reading (in units of mW) to the current value of the active power offset (labeled "voltage AC off" in the meter calibration factors window) and then enter this new value in the *Voltage AC offset* field in the Manual Calibration window. As an example, if the "voltage AC off" has a value of 200 (0.2 W) in the meter calibration window, and it is desired to subtract an additional 0.300 mW, then enter a value of 500 in the *Voltage AC offset* field in the Manual Calibration window. After entering the value in the *Voltage AC offset* field in the Manual Calibration window, press "Update meter".

To perform reactive power offset calibration for a phase, a similar process is followed as the process used to perform active power offset calibration. Add the offset to be subtracted from the reactive power reading (in units of mvar) to the current value of the reactive power offset (labeled "Current AC offset" in the meter calibration factors window) and then enter the value in the *Current AC offset* field in the Manual Calibration window. After entering the value in the *Current AC offset* field in the Manual Calibration window, press "Update meter".

3.1.4.2.2.5 Phase Calibration

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 1 through Step 3 from 3.1.4.2.2.2.2 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If the error from Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   a. Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error requires a positive (negative) number as correction.
   b. Click on the *Update meter* button and monitor the error values on the reference meter.
   c. If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   d. Change the phase now to −60° and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

After performing phase calibration, calibration is complete for one phase. Gain calibration, offset calibration, and phase calibration must be performed for the other phases.

This completes calibration of voltage, current, and power for all three phases. View the new calibration factors (see 図 39) by clicking the *Meter calibration factors* button of the GUI metering results window in 図 36. For these displayed calibration factors, note that the "Voltage AC off" parameter actually represents the active power offset (in units of mW) subtracted from each measurement and the "Current AC offset" parameter actually represents the reactive power offset subtracted (in units of mvar) from reactive power readings.

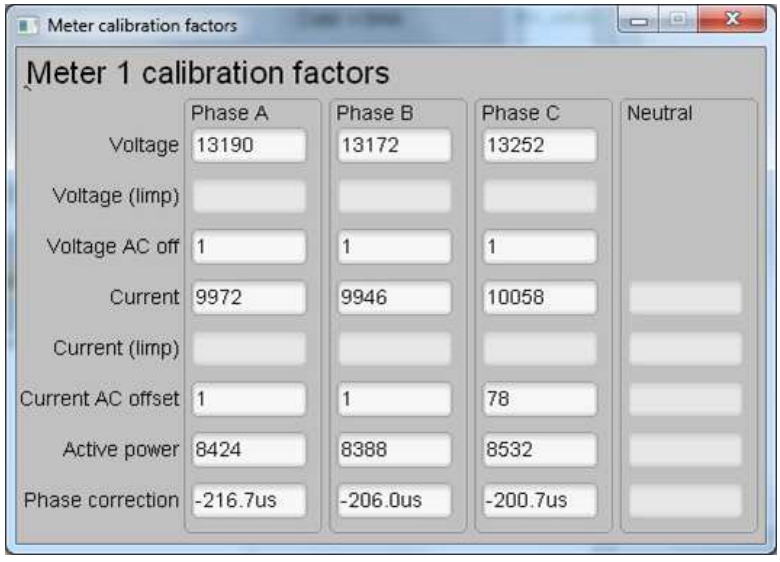


図 39. Calibration Factors Window

Also view the configuration of the system by clicking on the *Meter features* button in 図 36 to get to the window that 図 40 shows.

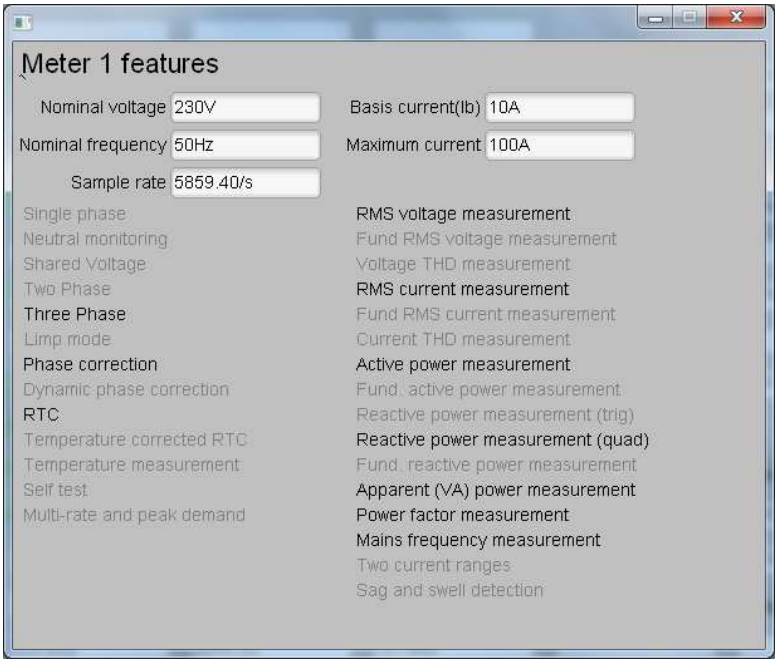


図 40. Meter Features Window

3.1.4.3 Test Results

表 4 shows the results of the DC offset testing. From these results, the V_{REF} voltage divider and op-amp implementation has a much smaller DC offset value than the AVCC voltage divider and no op-amp implementation, which is because the V_{REF} voltage divider and op-amp implementation is able to more accurately generate the ideal V_{REF} / 2 offset than the AVCC voltage divider and no op-amp implementation. As a result, the V_{REF} voltage divider and op-amp implementation is able to use more of the ADC range of the MSP432 than the AVCC voltage divider and no op-amp implementation.

表 4. DC Offset Test Results

VOLTAGE FRONT-END IMPLEMENTATION	DC OFFSET IN PHASE A VOLTAGE ADC SAMPLES	DC OFFSET IN PHASE B VOLTAGE ADC SAMPLES	DC OFFSET IN PHASE C VOLTAGE ADC SAMPLES
TIDA-01639 V_{REF} voltage divider and op-amp implementation (as 図 7 shows)	–210.871	–175.172	–300.288
AVCC voltage divider and no op-amp implementation (as 図 10 shows)	–4014.805	–3989.785	–4039.859

表 5 and 表 6 show the V_{RMS} and active energy settle time results. From these results, the V_{REF} voltage divider and op-amp implementation settles more quickly than the AVCC voltage divider and no op-amp implementation. The quicker settling time of the V_{REF} voltage divider and op-amp implementation is because the dc filter settles more quickly when initialized to 0 with this implementation since this implementation has a smaller DC offset than the AVCC voltage divider and no op-amp implementation.

表 5. V_{RMS} Settle Time Test Results

VOLTAGE FRONT-END IMPLEMENTATION	V_{RMS} SETTLING TIME
TIDA-01639 V_{REF} voltage divider and op-amp implementation (as 図 7 shows)	4 seconds
AVCC voltage divider and no-op amp implementation (as 図 10 shows)	12-13 seconds

表 6. Active Energy Settle Time Test Results

VOLTAGE FRONT-END IMPLEMENTATION	ACTIVE ENERGY SETTLING TIME
TIDA-01639 V_{REF} voltage divider and op-amp implementation (as 図 7 shows)	3 seconds
AVCC voltage divider and no-op amp implementation (as 図 10 shows)	7 seconds

3.1.4.3.1 Voltage DC Offset and Settle Time Results

3.1.4.3.1.1 Metrology Accuracy Results

For the following test results, gain, phase, and offset calibration are applied to the meter. At higher currents, the % error shown is dominated by shunt resistance drift caused by the increased heat generated at high currents.

表 7. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.10	–0.046	–0.004	–0.067
0.25	–0.018	0.043	–0.059
0.50	–0.023	0.019	–0.054
1.00	–0.001	0.026	–0.046
2.00	–0.022	0.022	–0.062
5.00	–0.019	0.013	–0.052
10.00	–0.011	0.013	–0.049
20.00	–0.029	0.011	–0.07
30.00	–0.032	–0.008	–0.083
40.00	–0.048	–0.034	–0.109
50.00	–0.086	–0.084	–0.144
60.00	–0.123	–0.136	–0.188
70.00	–0.178	–0.187	–0.241
80.00.	–0.235	–0.249	–0.307

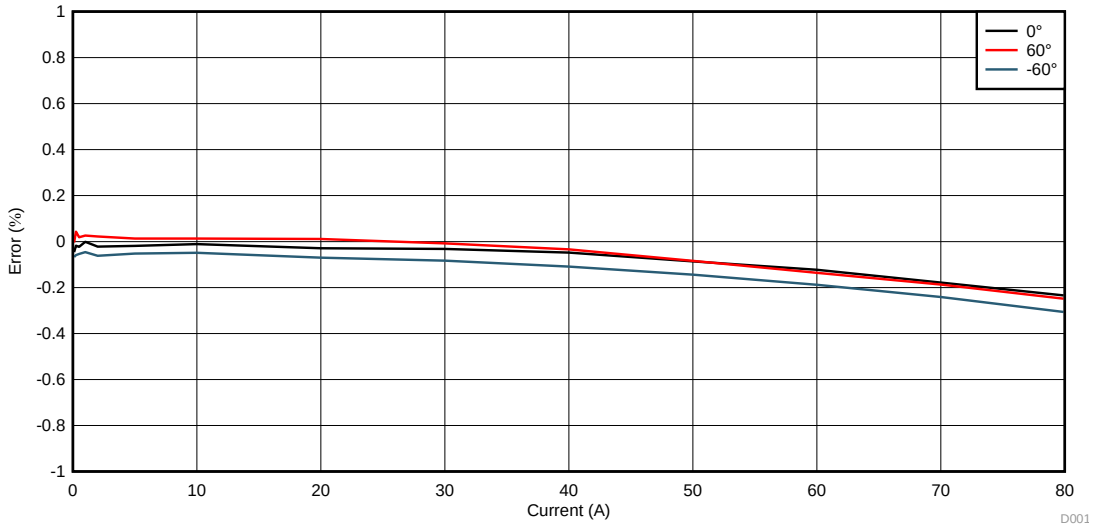


図 41. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

表 8. Cumulative Active Energy % Error Versus Current, 220-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.10	–0.016	0.043	0.03
0.25	0.014	0.011	0.034
0.50	0.013	–0.017	0.033
1.00	0.007	–0.002	0.032
2.00	0.0047	–0.016	0.013
5.00	–0.0033	–0.03	0.028
10.00	–0.003	–0.031	0.024
20.00	–0.012	–0.031	0.005
30.00	–0.011	–0.021	–0.013
40.00	–0.024	–0.058	–0.031
50.00	–0.043	–0.096	–0.047
60.00	–0.072	–0.125	–0.083
70.00	–0.1013	–0.181	–0.146
80.00	–0.181	–0.249	–0.226

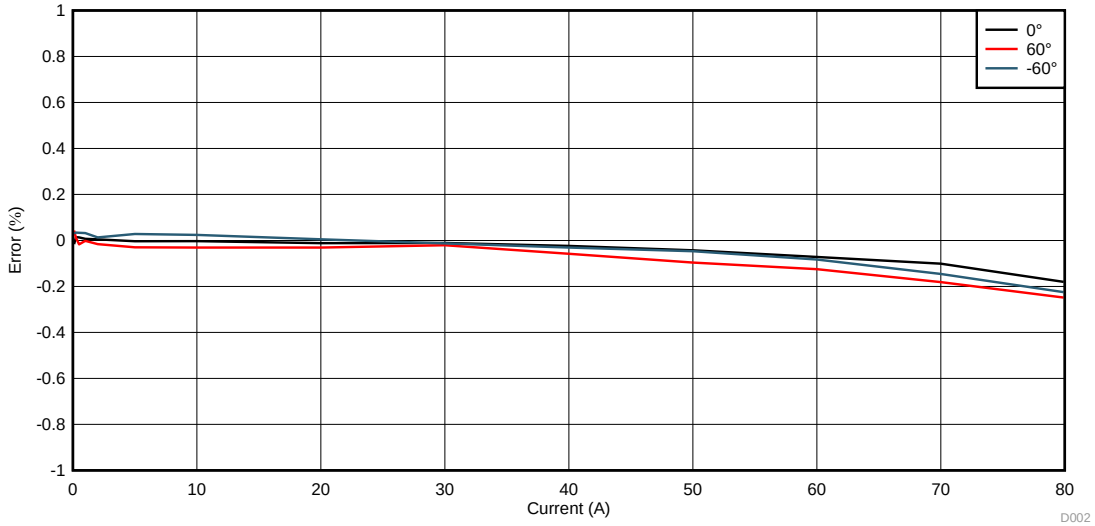


図 42. Cumulative Active Energy % Error Versus Current, 220-µΩ Shunts

表 9. Cumulative Reactive Energy % Error Versus Current

CURRENT (A)	30°	60°	–30°	–60°
0.10	–0.01	–0.014	0	–0.016
0.25	–0.168	–0.099	0.168	0.082
1.00	–0.027	–0.018	0.034	0.0265
5.00	–0.004	0.0055	–0.019	–0.007
10.00	0.022	0.006	–0.013	–0.008
20.00	–0.002	–0.007	–0.016	–0.015
40.00	–0.019	–0.0355	–0.056	–0.051
60.00	–0.055	–0.1	–0.15	–0.1498
80.00	–0.127	–0.201	–0.26	–0.259

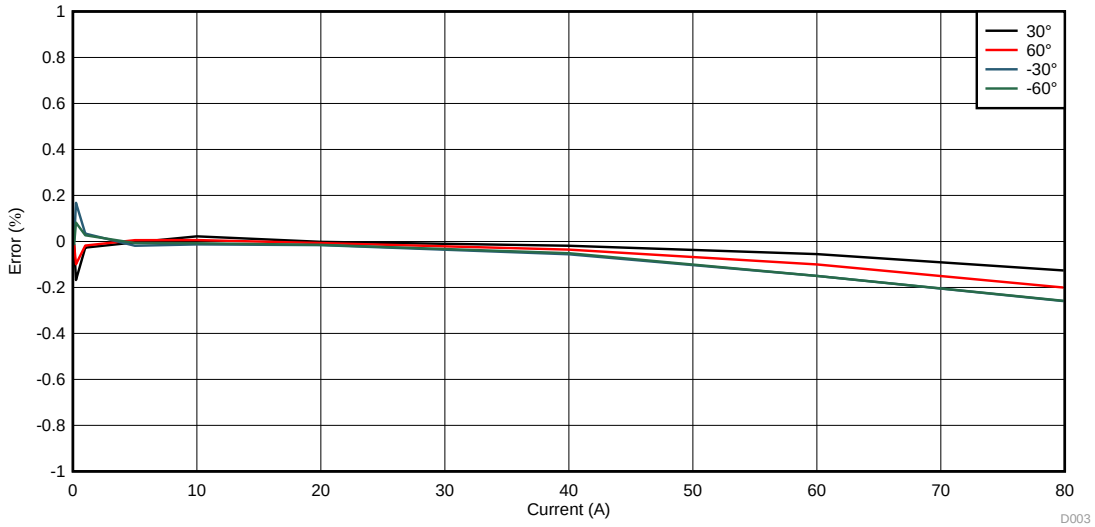


図 43. Cumulative Reactive Energy % Error Versus Current

表 10. Cumulative Active Energy Measurement Error Versus Voltage, 80 to 270 V

VOLTAGE (V)	%ERROR
80	–0.018
100	–0.026
110	–0.03
120	–0.041
150	–0.04
180	0.004
210	–0.009
220	–0.0117
230	–0.016
240	–0.018
250	–0.0193
260	–0.021
265	–0.025
270	–0.0253

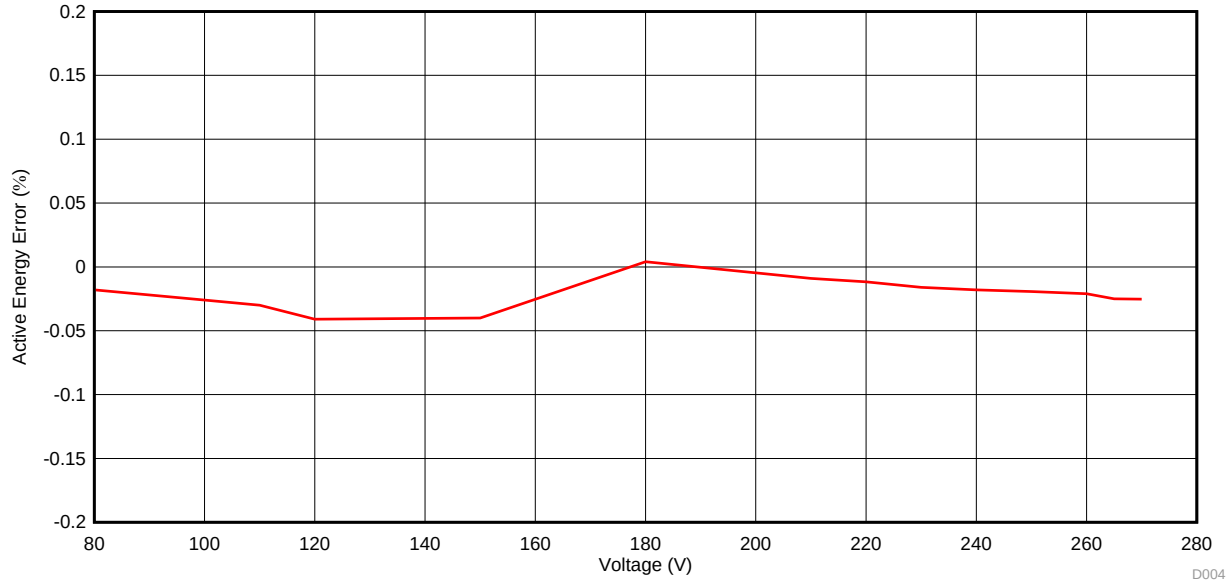


図 44. Cumulative Active Energy Measurement Error Versus Voltage, 80 to 270 V

表 11. Cumulative Active Energy Measurement Error Versus Voltage, ±10% Nominal Voltage

VOLTAGE (V)	0°, 10 A	60°, 10 A	300°, 10 A	0°, 0.5 A	60°, 0.5 A	300°, 0.5 A
207	0.0267	0.011	0.0345	0.024	0.009	0.019
230	0.023	0.012	0.023	0.0095	0.013	0.009
253	0.0125	0.027	–0.002	0.011	0.017	–0.0157

表 12. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency

CONDITIONS	48 Hz	50 Hz	52 Hz
0.5 A, 0	0.022	0.0167	0.007
0.5 A, 60	0.005	0.018	0.006
0.5 A, 300	0.006	0.014	0.008
10 A, 0	0.023	0.018	0.014
10 A, 60	0.021	0.017	0.0067
10 A, 300	0.018	0.02	0.018

3.2 Design Files

3.2.1 Schematics

To download the schematics, see the design files at TIDA-01639.

3.2.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01639.

3.2.3 PCB Layout Recommendations

For this design, the following general guidelines must be followed:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially for the ground planes of the high side of each AMC1106. In this design, there is a ground plane on both the top and bottom layer; for this situation, ensure that there is good stitching between the planes through the liberal use of vias.
- Give each AMC1106 its own set of ground planes that are used for the high side of each AMC1106. Each of these ground planes is actually referenced from a different line because each AMC1106 must be connected to the line for that particular phase.
- Use a different ground plane for the isolated RS-232. This other ground plane is at the potential of the RS-232 ground and not DGND.
- Be careful to avoid crosstalk from the delta-sigma modulation clock traces or the AMC1106 bit-stream traces.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and placing any traces underneath the crystal must be avoided. Also, keep high frequency signals away from the crystal.
- Use wide traces for power supply connections.
- Maintain at least an 8.1-mm spacing between the ground planes of the high side of each AMC1106 device and the ground plane on the controller side. This spacing maintains the recommended clearance for the AMC isolation rating. In addition, ensure that the recommended clearance and creepage spacing for other isolation devices (such as the ISO7720 and ISO7721) is also followed.
- Keep the traces of the analog input pins symmetrical and as close as possible to each other.
- To reduce parasitic coupling, run the input traces of the op amp as far away as possible from the supply or output traces of the op amp. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.

3.2.4 Layout Prints

To download the layer plots, see the design files at TIDA-01639.

3.2.5 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01639.

3.2.6 Gerber Files

To download the Gerber files, see the design files at TIDA-01639.

3.2.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01639.

3.3 Related Documentation

1. Texas Instruments, *Magnetically Immune Transformerless Power Supply for Isolated Shunt Current Measurement*

3.3.1 商標

3.4 About the Author

MEKRE MESGANAW is a systems engineer in the Grid Infrastructure group at Texas Instruments, where he primarily works on grid monitoring and electricity metering customer support and reference design development. Mekre received his bachelor of science and master of science in computer engineering from the Georgia Institute of Technology.

ALESSIO COLBACCHINI is an Analogue Field Application Engineer at Texas Instruments UK, where he supports customers in the audio and medical space. Alessio graduated from Politecnico di Milano (Italy) with a Bachelor of Science in Electrical Engineering and received his Master of Science in Electronic and Electrical Engineering from the University of Sheffield (UK).

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。