参考資料

設計ガイド

C2000™ マイクロコントローラを使用する 2 相インターリーブ LLC 共振コンバータのデザイン

概要

このリファレンス・デザインは、デジタル制御 500W 2 相インターリーブ LLC 共振コンバータを実装するものです。このシステムは、単一の C2000 マイクロコントローラ (MCU) TMS320F280025 により制御され、あらゆる動作モードで、パワー・エレクトロニクス・スイッチング・デバイスのパルス幅変調 (PWM) 波形を生成します。このデザインは、革新的なカレント・シェア技術を使用して、複数の相間における電流バランスを高精度で実現しています。

リソース

TIDM-1001	デザイン・フォルダ
Digital Power SDK	ツール・フォルダ
TMS320F280025C	プロダクト・フォルダ
UCC27524	プロダクト・フォルダ
OPA365	プロダクト・フォルダ
UCD7138	プロダクト・フォルダ

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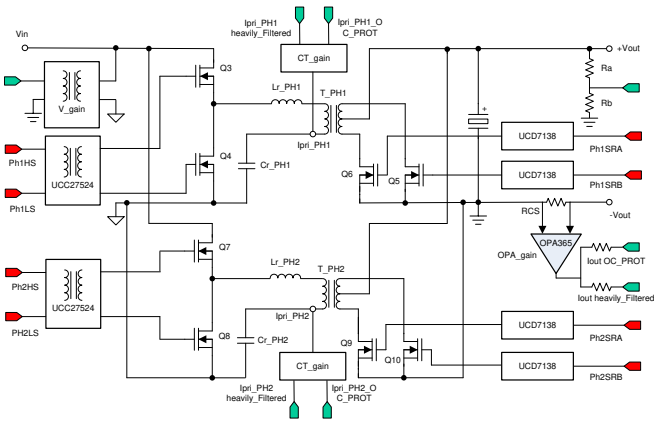
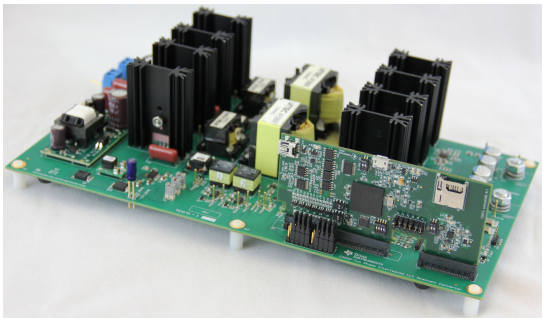
特長

- デジタル制御式の 2 相インターリーブ LLC 共振 DC/DC コンバータ
- 500W (1 相あたり 250W) の全負荷電力または 42.5A の全負荷電流
- Vin：370V～410V DC
- Vout：12V DC
- 共振周波数：250kHz、スイッチング周波数範囲：200kHz～350kHz
- ピーク効率：94.5%、負荷が定格の 10% を上回っている場合に 90% 超の効率
- 追加ハードウェアなしで、複数の相間で優れたカレント・シェアを実現
- プログラマブル制限付きフェーズ・シェディング
- 故障保護：相 / 出力過電流および出力過電圧
- 各種 C2000 powerSUITE ツールでサポート

アプリケーション

- サーバー電源
- テレコム整流器
- 自動車充電
- 産業用電源





1 System Overview

1.1 System Description

Resonant converters are popular DC-DC converters frequently used in server, telecom, automotive, industrial, and other power supply applications. The converters are a good choice for medium- to high-power applications because of their adherence to improving industry standards, ever-increasing power-density goals, and high-performance (efficiency, power density, and so forth) standards.

These are variable-frequency converters where the PWM-switching frequency of operation frequently changes during runtime. For reliable operation the changing frequencies must not produce any glitches or irregular PWM behavior. For applications with high-output currents that require input-output isolation, it is a common practice to use synchronous rectification (SR) on the secondary of the isolation transformer. SR uses additional power electronic devices switching with changing frequencies. High-power applications may require use of multiphase interleaved converters. These interleaved converters have even more devices switching with variable frequencies and additionally require fixed-phase relationships between various phases under all operating frequencies. Guaranteeing correct PWM waveform generation with changing frequencies under all operating conditions is a big challenge for the controller. Furthermore, interleaving multiple phases of resonant converters presents current sharing challenges between phases. Inadequate or improperly implemented current sharing or incorrect PWM waveform generation can lead to converter failure, significant system or component damage, and, in the worst case, significant property damage or resultant bodily injury or loss of life.

In server and telecom power supply applications, these converters are used to work as the isolated DC-DC converter stage in the rectifier system. These converters provide high efficiency and power density through soft-switching, SR, and other techniques.

These converters are gaining popularity in automotive on-board charging applications. Additionally, these devices may be used as isolated, bi-directional converters in electric vehicles (EVs) and hybrid electric vehicle (HEVs).

This design implements a 500-W, two-phase, interleaved half-bridge (HB) LLC resonant converter with SR on the secondary. The system is controlled by a single C2000 MCU, TMS320F280025C, which also generates correct PWM waveforms for all power electronic switching devices (MOSFETs) using the latest features on C2000 MCUs. An innovative current sharing technique is implemented by the C2000 MCU to accurately achieve current and phase balancing for multiphase interleaved converters.

The accompanying software allows programming the controller and experimenting with different control parameters to tune the control loop for good system performance. This design supports the use of C2000 powerSUITE tools like the compensation designer, the software frequency response analyzer, and the solution adapter. The software project allows users to evaluate the complete system with the help of these supported tools. This document provides the hardware and software design details along with the test results. This document also describes a structured step-by-step method to evaluate this solution by starting with a simple open-loop excitation and then working towards a complete well-tuned closed-loop system.

1.2 Key System Specifications

表 1. TIDM-1001 Performance Specifications

PARAMETER	TEST CONDITIONS	MINIMUM	TYP	MAXIMUM	UNITS
INPUT CHARACTERISTICS					
Voltage range	—	370	390	410	V_{DC}
Input current	Vin = 370 V_{DC}, full load = 42.5 A	—	—	1.55	A
Input current	Vin = 390 V_{DC}, full load = 42.5 A	—	—	1.5	A
Input current	Vin = 410 V_{DC}, full load = 42.5 A	—	—	1.5	A
Phase overcurrent threshold(1)	—	—	3.2	—	A
OUTPUT CHARACTERISTICS					
Output voltage, V_{out}	No load to full load	—	12	—	V_{DC}
Output overvoltage threshold	—	—	13.5	—	V_{DC}
Load regulation	V_{in} = 410 V_{DC}, I_{out} =2.5A to 42.5 A	—	50	—	mV
Line regulation	V_{in} = 370 V_{DC} to 410 V_{DC}, I_{out} = 10 A	—	< 5	—	mV
Output load current, I_{out}(2)	V_{in} = 370 V_{DC} to 410 V_{DC}	—	—	42.5	A
Output over-current threshold(1)	—	—	55	—	A
Output power(2)	—	—	—	500	W
Output power per phase	—	—	—	250	W
SYSTEM FEATURES					
Peak efficiency	V_{in} = 390 V_{DC}, I_{out}= 10 A	—	94.5%	—	—
Efficiency	V_{in} = 370 V_{DC} to 410 V_{DC}, 4.2 A <I_{out} < 42.5 A	—	> 90%	—	—
Full-load efficiency	V_{in} = 370 V_{DC}, I_{out} = 42.5 A	—	92%	—	—
Resonant frequency	—	—	250	—	kHz
Switching frequency	—	200	—	350	kHz

(1) These default overcurrent limits are programmable and may be adjusted to allow high-load operation under noisy test conditions or to limit these currents to lower levels.

(2) Note that the resonant tank inductors are the hottest components on the board. Use an external air cooling fan (CFM rating > 50) directed at the board when operating with loads (I_{out}) of 30 A or higher.

1.3 Block Diagram

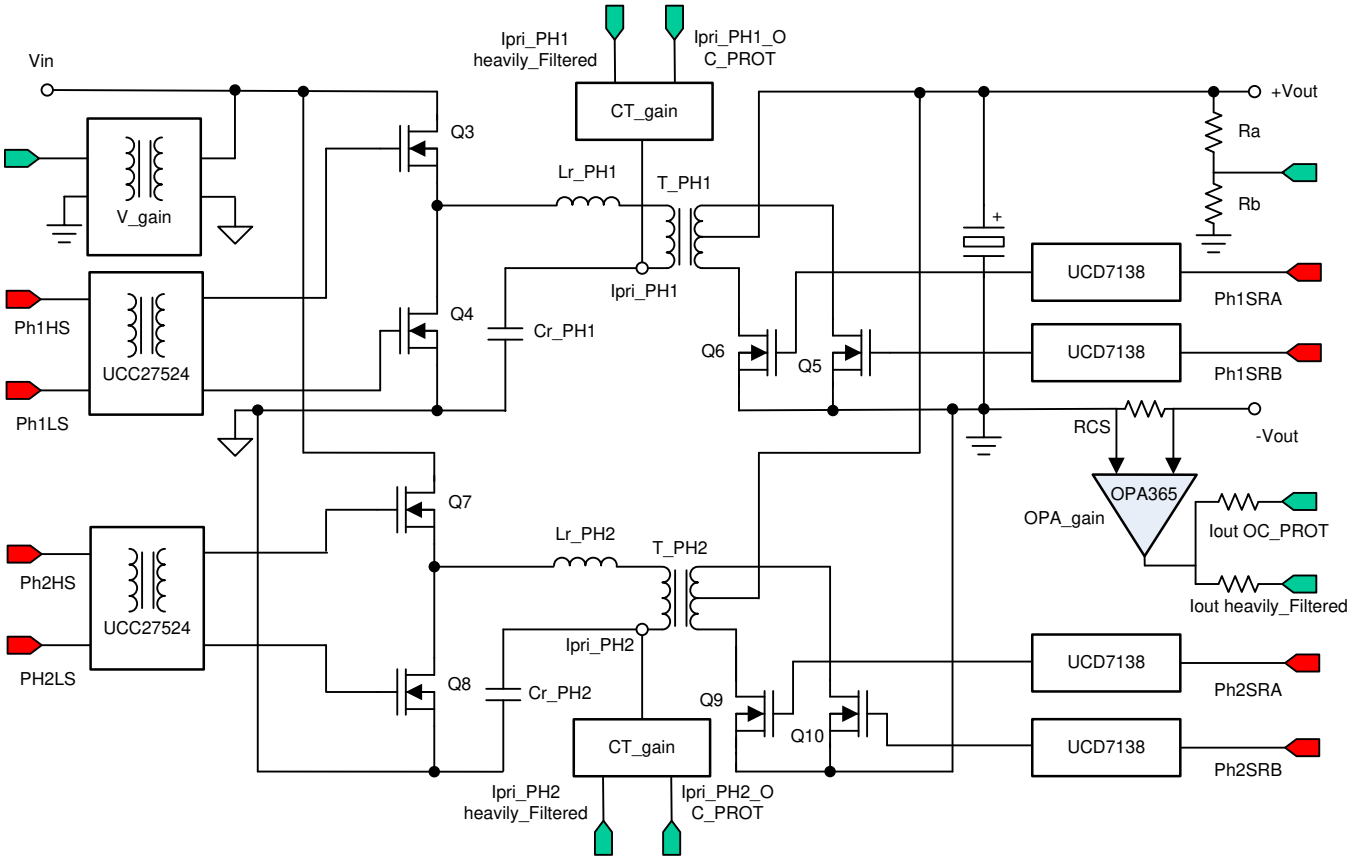


図 1. TIDM-1001 System Block Diagram

1.4 Highlighted Products

1.4.1 TMS320F280025C

The 3rd Generation TMS320F280025C is a powerful, 32-bit, floating-point MCU designed for advanced closed-loop control applications, such as industrial drives and servo motor control, solar inverters and converters, digital power, transportation, and power line communications.

These devices feature integrated performance analog and control peripherals along with various communication peripherals to enable system consolidation. Two independent 12-bit analog-to-digital converters (ADCs) provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The comparator subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals. Latest features on the PWM, CMPSS, and ADC peripherals are extensively used in this TI Design.

1.4.2 UCD7138

The UCD7138 device is a high-performance, 4-A and 6-A, single-channel MOSFET driver with body-diode conduction sensing and reporting. In this design the device is used to achieve advanced SR control without a need for typically lossy and expensive current sensing circuit. The device contains a high-speed gate driver, a body-diode conduction-sensing circuit, and a turnon delay optimization circuit. The device is suitable for high-power, high-efficiency isolated converter applications where SR dead-time optimization is desired. The benefits of the chipset include maximizing system efficiency by minimizing body-diode conduction time, robust and fast negative-current protection, and a simple interface.

The UCD7138 device offers asymmetrical rail-to-rail, 4-A source and 6-A sink peak-current drive capability. The short propagation delay and fast rise and fall time allows efficient operation at high frequencies. The UCD7138 device is capable of sensing body-diode conduction time as low as 10 ns.

1.4.3 UCC27524

The UCC2752x family of devices are dual-channel, high-speed, low-side gate-driver devices capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC2752x can deliver high-peak current pulses of up to 5-A source and 5-A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay (typically 13 ns). In addition, the drivers feature matched internal propagation delays between the two channels. These delays are very well suited for applications requiring dual-gate drives with critical timing, such as the high-side and low-side switches of a HB in this design. This delay also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with one input signal. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

1.5 Functional Description

Resonant power converters contain resonant L-C networks whose voltage and current waveforms vary in a sinusoidal pattern during one or more sub-intervals of each switching period. 図 2 shows a generic block diagram of a HB LLC resonant converter system. The resonant tank circuit is formed by external inductor L_r, transformer leakage inductance L_k, transformer magnetizing inductance L_m, and capacitor C_r. In some cases it is possible to integrate L_r into the transformer design.

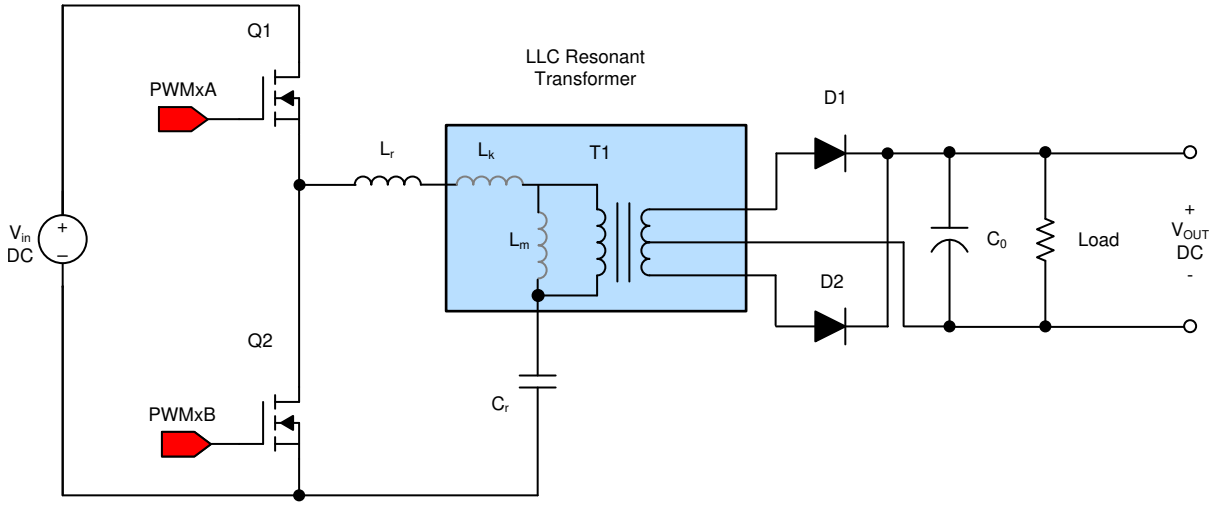


図 2. Block Diagram of HB LLC Converter

HB switches Q1 and Q2 are driven with 50% (typical) duty cycle signals that are frequency modulated. As a result the voltage at Q2 drain is a square wave voltage with changing fundamental frequency. The tank circuit acts as a band-pass filter that filters out the high-frequency and low-frequency components from this voltage and leaves the dominant fundamental frequency component. This component is then rectified on the secondary with either diode rectification or SR. A higher tank circuit current at the fundamental frequency implies higher energy that is transferred to the secondary or load. Frequency modulation of the PWM signals driving the HB switches consequently changes the tank network impedance resulting in a higher or lower tank circuit current depending on the fundamental frequency. This allows output voltage to be regulated by simply modulating the PWM frequency. [1]

1.5.1 The Resonant Tank

There are two resonant frequencies associated with this converter. The lower frequency, f_{r1}, can be calculated as 式 1.

$$f_{r1} = \frac{1}{2\pi\sqrt{(L_r + L_k + L_m)C_r}} \quad (1)$$

The second frequency, f_{r2}, can be calculated as 式 2.

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_k)C_r}} \quad (2)$$

This frequency, f_{r2}, is often referred to as the resonant frequency of the converter. The ratio $(L_r+L_k)/L_m$ is an important parameter for the designer.[2]

As mentioned above, frequency modulation changes the tank network input impedance. For frequencies above f_{r2} this impedance is inductive, while for frequencies below f_{r1} it is capacitive. For frequencies between these two resonant frequencies the impedance is inductive above a critical frequency based on the load resistance.

The LLC resonant converter is normally operated in the region where the tank impedance is inductive. This means that the impedance increases with frequency. As a result a properly regulated converter operates at low frequencies under high loads and at higher frequencies under low loads.

A typical gain vs frequency curve for the LLC HB converter is shown in 図 3. For the purposes of this discussion the combined inductance (L_r+L_k) will be referred to as L_r. As seen in 図 4, 図 5, 図 6, and 図 7, the Lr/Lm ratio plays an important role in deciding the range of frequencies over which the converter should operate.[3]

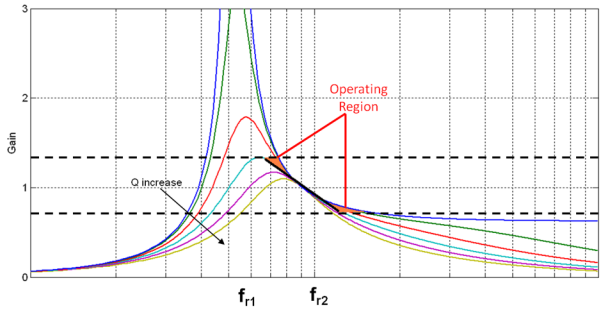


図 3. Typical Gain Versus Frequency

With a smaller L_r /$L_m$ratio, this range is larger. However, the converter may operate at frequencies relatively farther away from the resonant frequency f_{r2}. Designs with a higher L_r /L_m ratio provide a larger change in gain for a small change in frequency. As a result the converter operates over a relatively smaller range of frequencies and fairly close to the resonant frequency f_{r2} under all operating conditions.

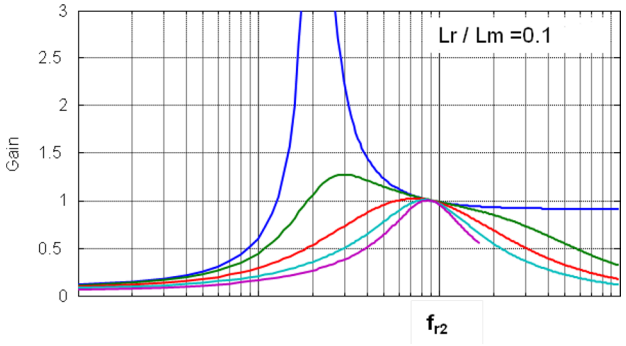


図 4. L_r/L_m = 0.1

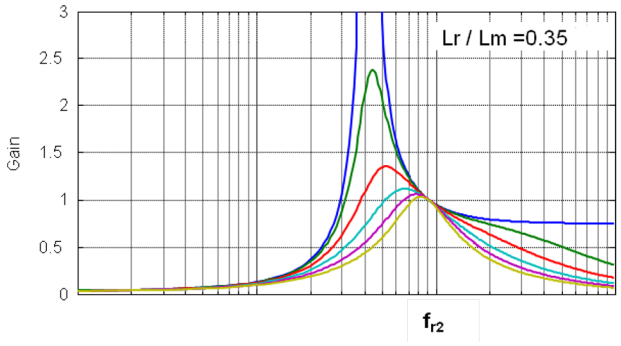


図 5. L_r/L_m = 0.35

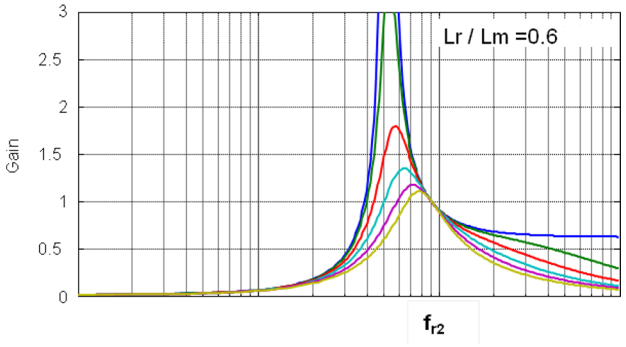


図 6. L_r/L_m = 0.6

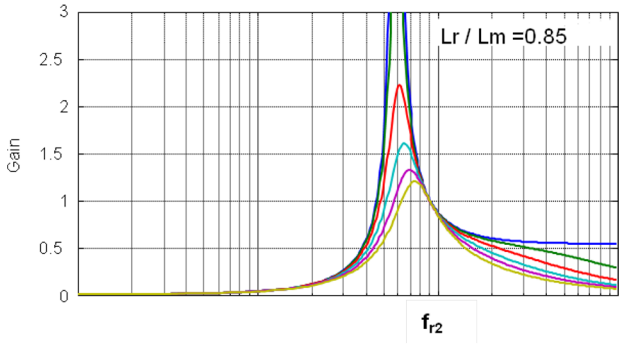


図 7. L_r/L_m = 0.85

1.5.2 Interleaving Phases

図 8 shows a generic block diagram of a two-phase interleaved HB LLC resonant converter system. Complementary PWM signals drive the high-side and low-side switches for each HB. All PWM signals shown in 図 8 operate at 50% duty cycle with some dead-time between the turn ON and turn OFF of PWM signals driving switches in the same HB.

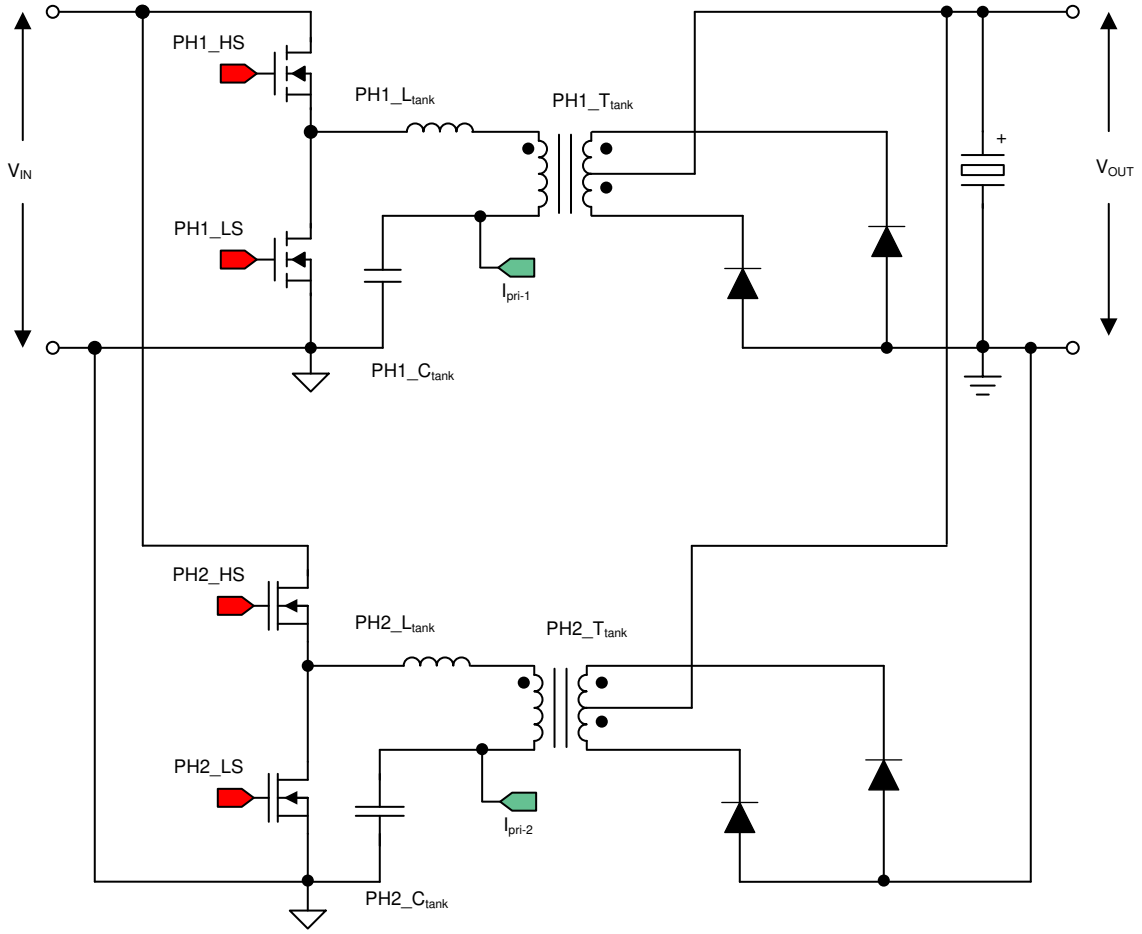


図 8. Block Diagram of Two-Phase Interleaved HB LLC Converter

1.5.2.1 Current Sharing

When two or more identical HB LLC converters are interleaved, any differences in their tank circuits lead to unequal sharing of the load current between individual phases. Unequal load sharing is a major problem in interleaving resonant converters as it decreases system efficiency, reliability, and thermal stability and can lead to high-circulating currents and even converter failure with significant system damage. As even small differences due to component tolerances may lead to considerable imbalances between phases, all interleaved resonant converters must have a way of sharing and balancing current between individual phases to allow safe, reliable, and efficient operation.

One solution is to design the tank circuit with extremely tight tolerances; however, this design ends up increasing the system cost considerably. Moreover, as mentioned above, even the slightest of differences due to tolerances may still lead to imbalances between phases. Although this solution may work for some applications, the solution is impractical on its own for most systems.

Some solutions try to match the tank circuits in different phases by adding more reactive components to the tank circuits in all or some of the phases[4]. In addition to increasing system cost and size, this solution may also increase manufacturing costs if further trimming is required on the assembly line.

More recent proposals take this approach a step further by trying to match the tank circuits during operation. Matching circuits is done by adding more power electronic switches to switch additional inductance or capacitance in and out of the tank circuit for some or all of the phases[5], which provides a good way of precisely adjusting the tank circuits at the expense of increased system cost, size, complexity, and a possible reduction in system efficiency.

There are other proposals that add extra converters based on an additional secondary winding on some or all of the LLC transformers. The operation of this additional converter is then controlled in a way to compensate for extra current being carried by the other phases[6]. This method suffers the same drawbacks as those discussed above and additionally increases complexity in the transformer design.

This design uses a new current-sharing technique that is implemented in software without a need for any additional external components or circuits. This new design is made possible by the C2000 MCU's highly-configurable PWM modules. In this implementation the PWM duty cycle for switches in the phase carrying a higher load current is decreased appropriately by a current-balancing loop in the software. The controller also adjusts PWM timing for corresponding synchronous rectifier (SR) switches in that phase.

1.5.2.2 Phase Shift Between Phases

When two identical converter stages are interleaved, the PWM signals driving switches in the second phase are phase shifted by 180° with respect to the signals driving the corresponding switches in the first phase. For a three-phase, interleaved converter the phase shift between signals driving corresponding switches in the three phases is 120°. For a four-phase interleaved converter this phase shift is 90° and so on. Phase shifting is a well-known method that provides reduced input and output current ripples, reduced bus capacitances, and better EMI and EMC performance. For two-phase, interleaved resonant converters, maintaining this phase shift between phases under all operational frequencies possesses a big challenge for the PWM controller.

When the duty cycle of PWM signals driving the switches in the two phases is identical, a 180° phase shift between the two phases can be achieved by maintaining 180° phase shift between any similar points in the PWM cycle of corresponding switches in the two phases, for example the low-to-high PWM transitions, high-to-low PWM transitions, the mid-point of the ON time, and so forth. Typically this shift is done between the mid-points of the ON time of corresponding switches in the two phases, which is shown in 図 9. A PWM period of 4 µs with a 50% duty cycle is assumed. Although dead-time is ignored here (for simplicity), this discussion is valid for the practical case of non-zero dead-time.

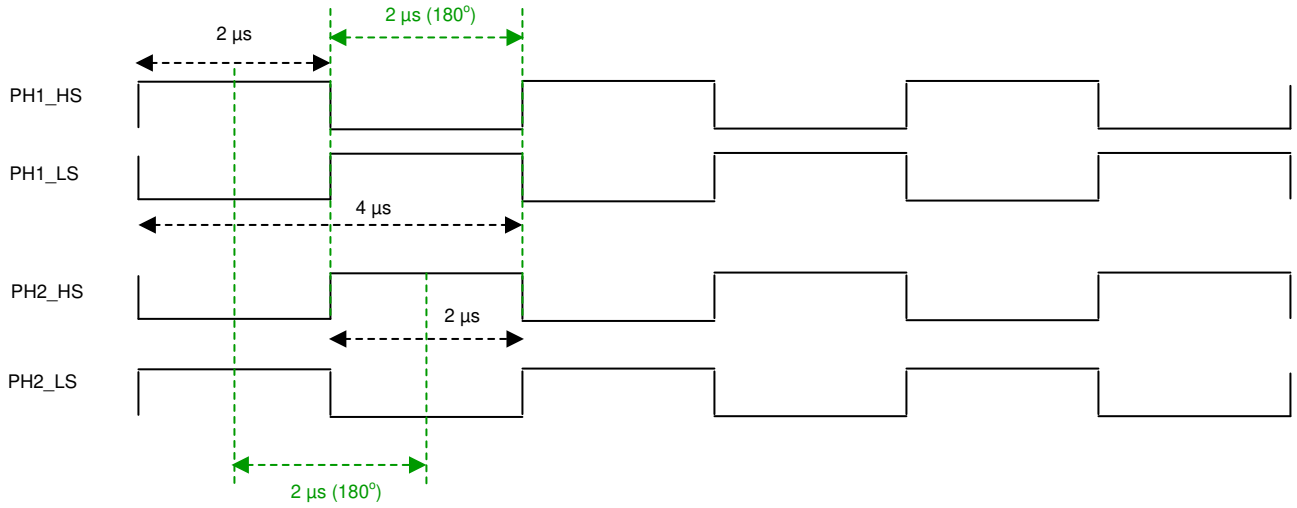


図 9. Identical Duty Cycles for Two Phases

With the current sharing technique employed here, one of the two phases, such as phase two, operates at a lower duty cycle than the other. As a result of a lower duty cycle, maintaining a 180° phase shift between the mid-point of the ON time of corresponding switches does not provide a 180° phase shift between high-to-low PWM transitions, which is shown in 図 10.

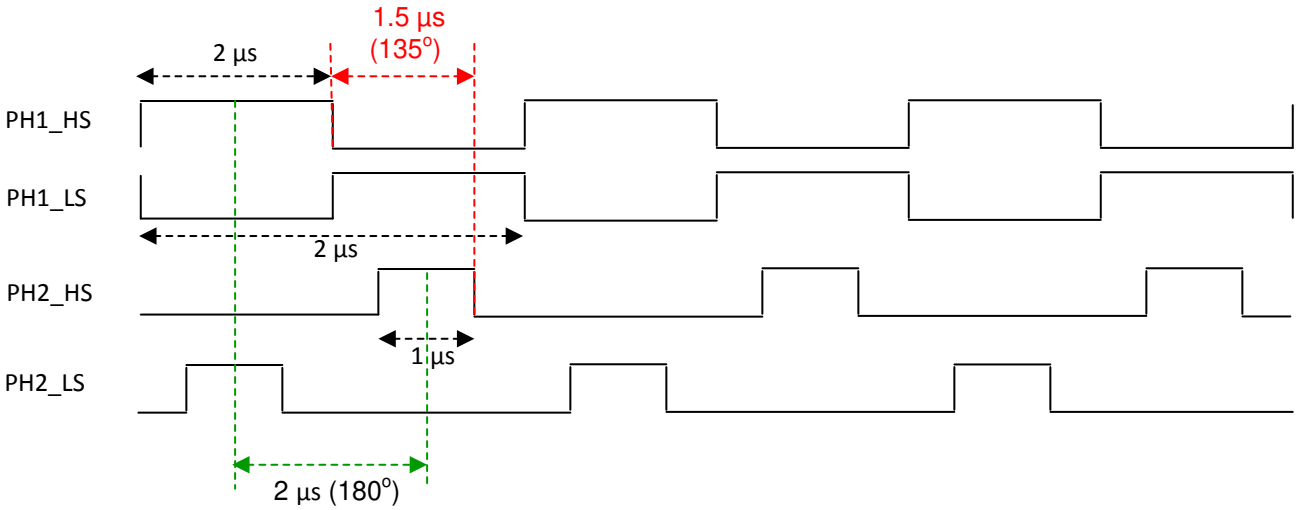


図 10. Different Duty Cycles for Two Phases

LLC resonant converters are operated in the inductive region of the gain versus frequency curve of the tank circuit. As a result to maintain correct interleaving between phases with unequal duty cycles, a 180° phase shift should be maintained between the trailing edges (high-to-low transitions) of the PWM signals driving corresponding switches in the two phases. This phase shifting scheme is used in this design, which is shown in 図 11. It is easy to infer that 図 11 will look identical to 図 9 when the same duty value is used for both phases.

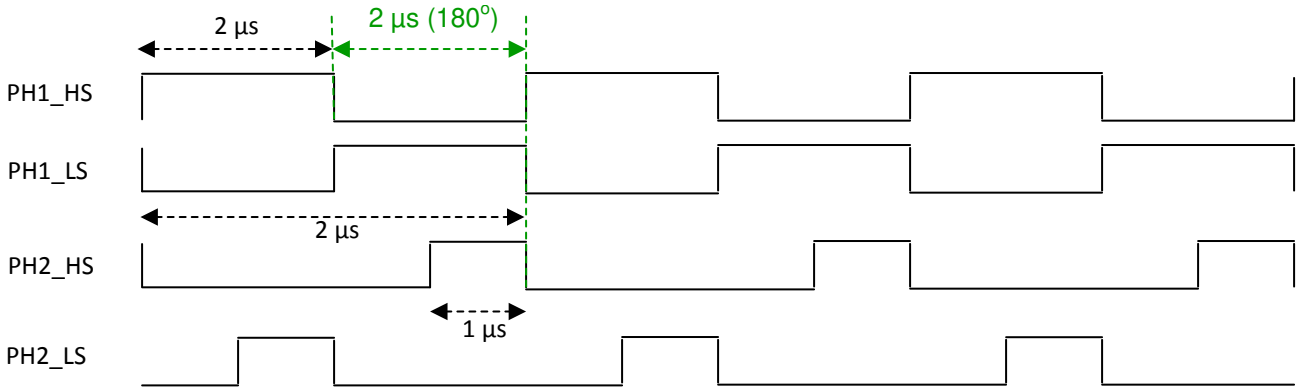


図 11. Correct PWM Waveforms for Two Phases Regardless of Individual Duty Cycles

1.6 TIDM-1001 Implementation

図 12 shows a simplified block diagram of the circuit implemented on the TIDM-1001 two-phase, interleaved LLC resonant converter design. Components L1, T1, and C21 form the resonant tank in the first phase while L2, T3, and C38 form the resonant tank in the second phase. MOSFET switches Q3 and Q4 form the HB for the first phase. Q5 and Q6 are used as SR switches for this phase. MOSFET switches Q7 and Q8 form the HB for the second phase. Q9 and Q10 are used as SR switches for this phase.

Controlling this system in different operation modes requires generating complex PWM drive waveforms along with fast and efficient control-loop calculations. This is made possible on C2000 MCUs by advanced on-chip control peripherals like PWM modules, analog comparators with on-chip 12-bit DACs, and 12-bit high-speed ADCs coupled with an efficient 32-bit CPU.

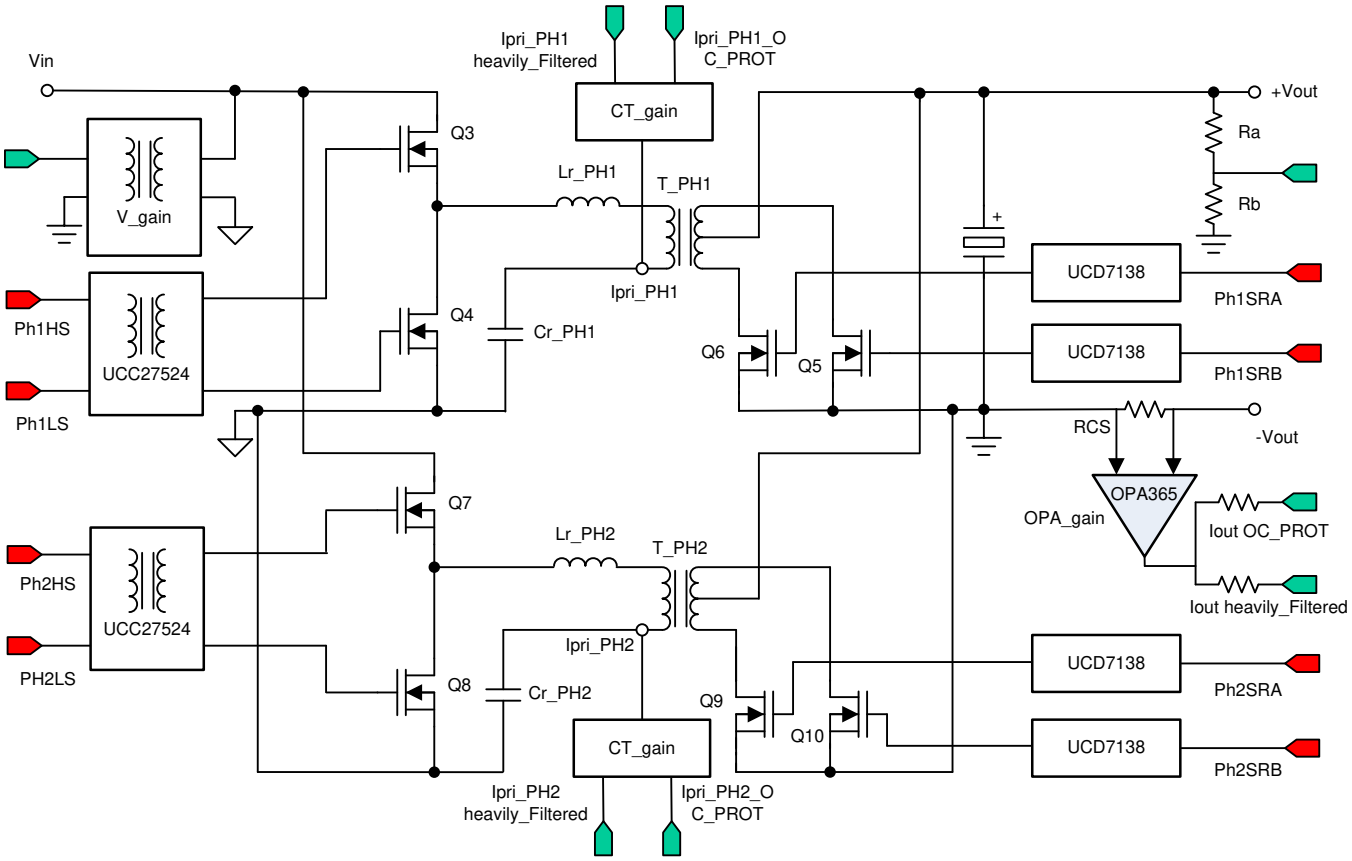


図 12. TIDM-1001 System Block Diagram

1.6.1 Controller

This converter is controlled by a single C2000 MCU from Texas Instruments, TMS320F280025C. The controller is referenced to the low voltage ground. Placing the controller on the output side of the isolation avoids any requirement for isolation in the output voltage feedback path and also possibly in the downstream communication (PMBUS, CAN, SPI, and so forth) with other modules or subsystems in the application. However, this choice necessitates isolation for the PWM signals driving the HB MOSFET switches on the high voltage side of the isolation. On this design, dual MOSFET drivers, UCC27524, from Texas Instruments along with gate drive transformers, 56PR3362, from Vitec are used for this purpose.

1.6.2 Hybrid Duty Control Mode

As this is a frequency controlled converter, the control algorithm controls the PWM switching frequency to regulate the output voltage. However, under certain operating conditions, the controller enters a new hybrid duty control mode where the duty cycle is also modulated. In this mode the switching frequency is still the controlled parameter for the voltage loop. The system enters this operating mode when it can no longer adequately regulate the output voltage with frequency control alone. This mode change is initiated when the software evaluates that the output voltage is higher than the desired voltage by a set limit, while operating at the maximum possible operating frequency. The duty can be reduced all the way to 0% if necessary, putting the PWM module into a burst mode.

1.6.3 Resonant Tank

The resonant tank is designed for a resonant frequency of 250 kHz. The external inductors L1 and L2 are 62.1 µH inductors, 75PR8126, from Vitec. Vitec transformers 75PR8125 are used as the resonant tank transformers T1 and T3. A 6.2 nF capacitor is used as the resonant tank capacitor. The transformer has a turns ratio, n, of 17 and is designed with a magnetizing inductance, L_m, of 149.2 µH and a leakage inductance, L_k, of 3.2 µH. These values provide a $(L_r + L_k)/L_m$ ratio of approximately 0.44 and a resonant frequency, f_{r2}, of approximately 250.13 kHz.

1.6.4 HB PWM Drivers

The C2000 MCU generates PWM waveforms for all four HB switches and the four SR switches. Complementary PWM signals drive the high-side and low-side switches for each HB. As explained in the previous section, when two phases are interleaved, PWM signals in the two phases operate 180° out of phase with respect to each other. All PWM signals operate at 50% duty cycle with some dead-time between the turn ON and turn OFF of PWM signals driving switches in the same HB. The only exceptions to this rule of 50% duty cycle operation are either when the current sharing algorithm forces one of the phases to operate at lower duty cycles or when the converter operates in hybrid duty control mode.

1.6.5 SR PWM Drivers

For reliable and efficient operation of this power converter, the SR turn-on and turn-off instants have to be accurately controlled relative to the PWM switching cycle and current in the transformer secondary winding. The C2000 MCU generates PWM signals for the SR switches relative to the signals driving the HB switches. A single-channel SR driver, UCD7138, from Texas Instruments detects body-diode conduction of the SR switch and uses this to turn the switch ON at the optimum point in time. The UCD7138 driver achieves this by accurately delaying the rising edge (turn ON) of the PWM signal, which comes from the C2000 MCU, to a point in time where the body-diode starts conducting.

Four of these drivers are used to drive the four SR switches. This approach brings a huge performance or cost benefit to the system as no other type of additional, and usually dissipative, current or voltage sensing is required to determine this accurate turn-on instant for the SR switches. The SR turn-off instant is controlled by the C2000 MCU.

1.6.6 Phase Shedding and Disabling SR Under Low-Load Operation

Multiphase converters use multiple identical converter phases to achieve a higher power rating. The resultant system has a significantly larger number of switching devices, which switch at high frequencies than a single converter phase. As a result the switching power losses for these converters are the sum total of switching losses in each of the converter phases. While all phases must contribute and share the load to support operations at high load, it may be possible for a few phases to handle operations at lower loads if the other converter phases are disabled. Disabling some of the converter phases is quite advantageous for improving converter efficiency as this eliminates switching losses in those disabled converter phases. As the system is operating under lower loads, any savings in power losses contributes considerably in increasing the overall system efficiency.

This design implements phase shedding by disabling one of the converter phases when the output current (I_{out}) falls below a programmable threshold (default approximately 10 A). This phase is re-enabled once the output current goes back up above a higher programmable threshold (default approximately 12 A). These two output current thresholds must provide some hysteresis (here 2 A) to avoid the system from constantly going in and out of phase shedding mode. When both phases are active and the controller software determines that the current has fallen down below the phase shedding threshold, it initiates a gradual shut-down of one of the two phases. The system continues to operate normally during this time. As soon as the controller software determines that the output current has risen above the higher phase shedding threshold, it quickly re-enables the phase that is currently disabled. Unlike disabling of the converter phase when phase shedding mode is entered, the re-enabling of a phase when phase shedding mode is exited is not gradual. Both phases are active once the system exits phase shedding mode. The phase that was active during the previous phase shedding operation is marked to be shed (disabled) when the system enters phase shedding mode again. The phase that was shed during the previous phase shedding operation is active during the next phase shedding mode operation.

Under very low load operation SR switching losses can be greater than the power savings obtained by SR. In this case the SRs may be disabled and only their body diodes used for rectification. This mode is used when the output current falls below approximately 2 A. The system exits this mode when the output current increases above approximately 3 A.

1.6.7 Feedback Signals

For proper control of the power stage under all operating conditions, the controller needs feedback information about the output voltage (V_{out}), the resonant tank currents (I_{pri-1}, I_{pri-2}), and the output current (I_{out}).

V_{out}, used for the voltage control loop, is fed back to the on-chip 12-bit ADC on the MCU by way of simple resistive voltage dividers.

A 0.5 mΩ equivalent shunt resistor is used to sense I_{out}. This signal is amplified by a low-noise, high CMRR, op-amp, OPA365, from Texas Instruments and sent to the ADC and an on-chip comparator on the MCU. I_{out} information is used for determining different operating modes and for output over-current protection.

The resonant tank currents, which are also the transformer primary currents, are each sensed using a 25 turn current sense transformer, WCM 603-7, from West Coast Magnetics and sent to the ADC and on-chip comparators. The difference between the two resonant tank currents is compared against a programmable set threshold that determines how well the currents in the two phases are shared. This threshold is user programmable. I_{pri-1} and I_{pri-2} are also used for overcurrent protection.

1.6.8 Fault Protection

At this stage, it is appropriate to introduce the shutdown mechanism used with this project. Here overcurrent protection is implemented for the transformer high voltage winding current for each phase using on-chip analog comparator subsystems CMPSS1 and CMPSS4. Output overcurrent protection is implemented using on-chip analog comparator sub-system CMPSS2. Output overvoltage protection is implemented using on-chip analog comparator 3. The reference trip levels are set using the corresponding internal 12-bit DACs, which are fed to the inverting terminals of these comparators. The comparator outputs are configured to generate a one-shot trip action on ePWM1, ePWM2, ePWM4, and ePWM5 whenever the sensed current or voltage is greater than the set limit.

The flexibility of the trip mechanism on C2000 devices provides the possibilities for taking different actions on different trip events. In this project ePWM1A, ePWM1B, ePWM2A, ePWM2B, ePWM4A, ePWM4B, ePWM5A, and ePWM5B outputs are driven low immediately to protect the power stage. These outputs are held in this state until a device reset is executed.

2 Getting Started Hardware and Software

2.1 Hardware and Resources Guide

図 13 shows some of the key components on the actual hardware.

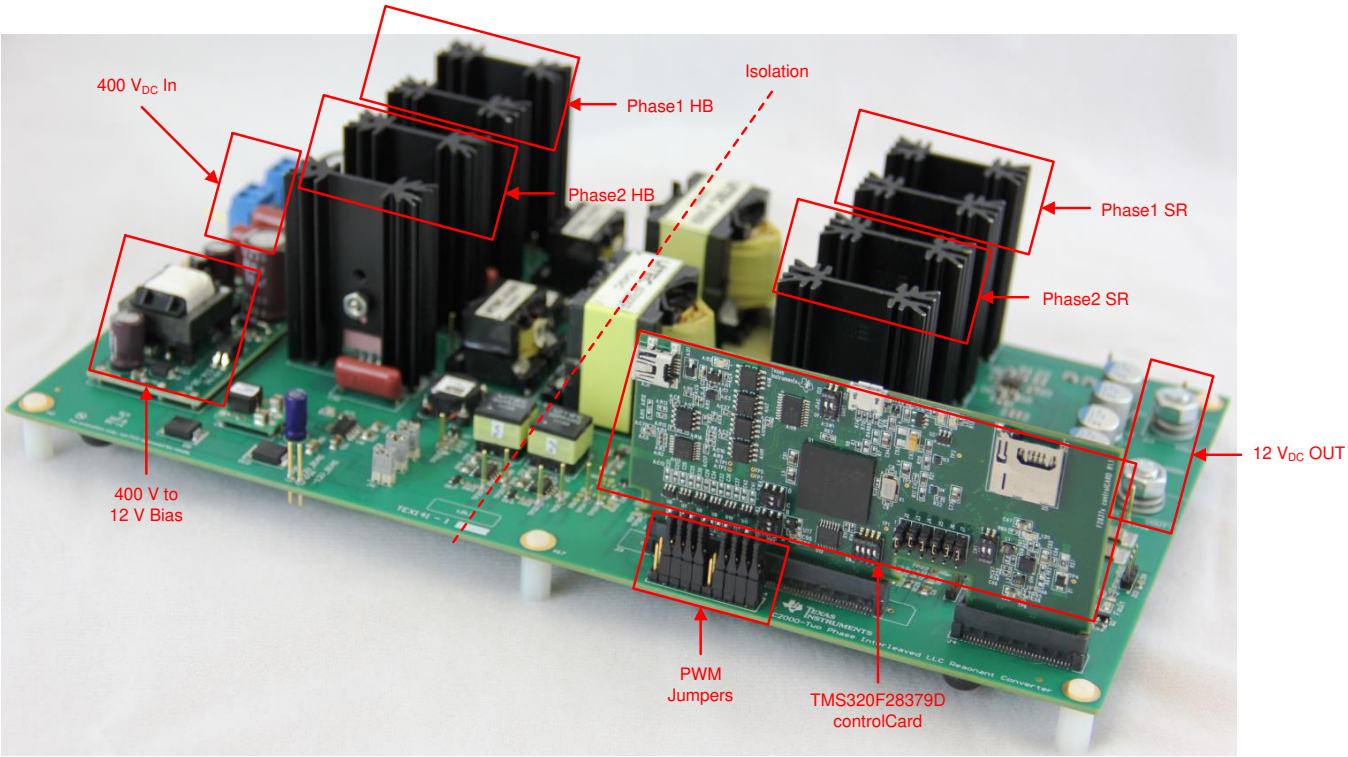


図 13. TIDM-1001 – Two-Phase Interleaved LLC Resonant Converter Board

表 2 shows the key signal connections between the TMS320F280025C controlCARD and the TIDM-1001 base board. For reference relevant portions of the schematic are also provided in 図 14 to 図 18.

表 2. Key Signal Connections

SIGNAL NAME	DESCRIPTION	CONNECTION TO controlCARD
EPWM-1A	High-side drive signal for phase one HB (Ph1_PWMHS)	GPIO-00
EPWM-1B	Low-side drive signal for phase one HB (Ph1_PWMLS)	GPIO-01
EPWM-2A	Drive signal for phase one SRA (Ph1_PWMSRA)	GPIO-02
EPWM-2B	Drive signal for phase one SRB (Ph1_PWMSRB)	GPIO-03
EPWM-4A	High-side drive signal for phase two HB (Ph2_PWMHS)	GPIO-06
EPWM-4B	Low-side drive signal for phase two HB (Ph2_PWMLS)	GPIO-07
EPWM-5A	Drive signal for phase two SRA (Ph2_PWMSRA)	GPIO-08
EPWM-5B	Drive signal for phase two SRB (Ph2_PWMSRB)	GPIO-09
Fault	Drive signal for system fault LED	GPIO-16
System_Good	Drive signal for system good LED	GPIO-17
V_{out}_fb	Output voltage feedback	CMPSS3
V_{out}_filt	Heavily filtered output voltage feedback	ADC-A8
I_{out}_fb	Output current feedback	CMPSS2
I_{out}_filt	Heavily filtered output current feedback	ADC-C0
I_{pri1}_fb	Phase one primary and resonant current feedback	CMPSS1
I_{pri1}_filt	Heavily filtered phase one primary and resonant current feedback	ADC-A3
I_{pri2}_fb	Phase two primary and resonant current feedback	CMPSS4
I_{pri2}_filt	Heavily filtered phase two primary and resonant current feedback	ADC-A5
V_{in}	Input voltage feedback	ADC-C8

This design uses a lot of jumper options for experimentation but there are some jumpers that must be populated for proper operation of the board. The jumpers that must be populated are listed below:

- J6
- J7
- J8
- J14 (positions 1 to 2, 3 to 4, 5 to 6, 7 to 8, 11 to 12, 13 to 14, 15 to 16, 17 to 18)
- J15 (for stand-alone or DEMO operation)

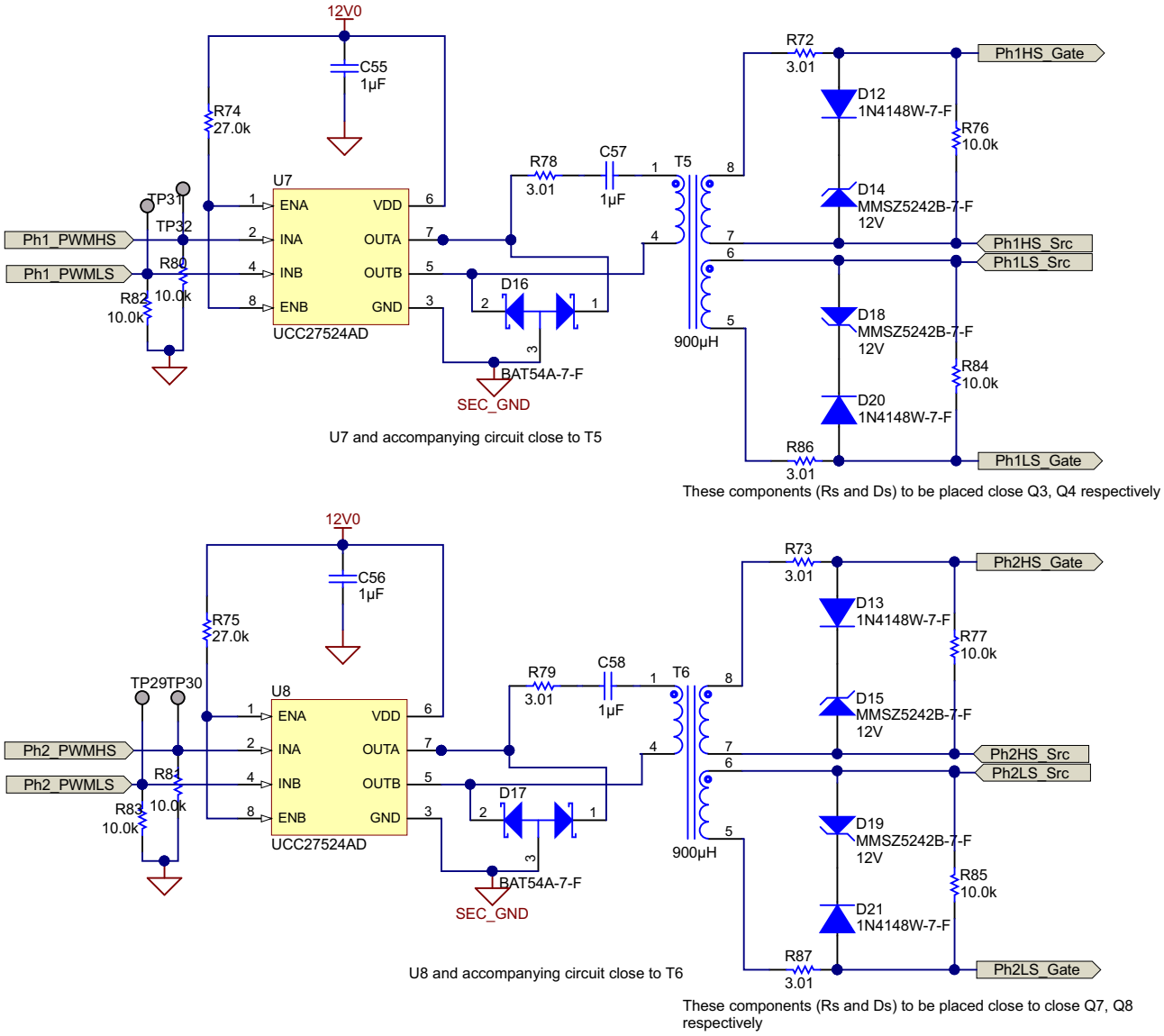


図 14. TIDM-1001 – HB PWM Drive Circuit

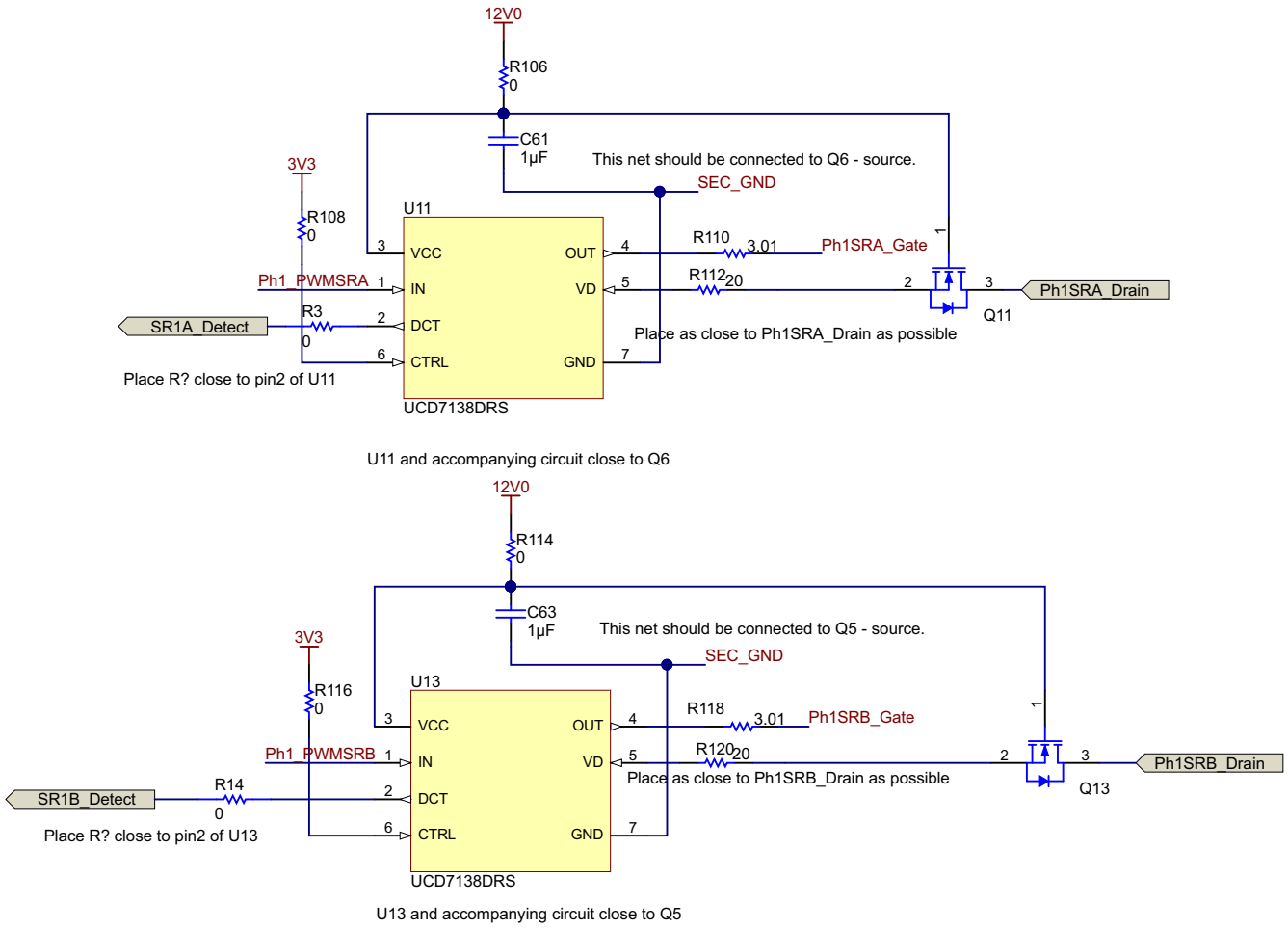


図 15. TIDM-1001 – Phase-One SR PWM Driver Circuit

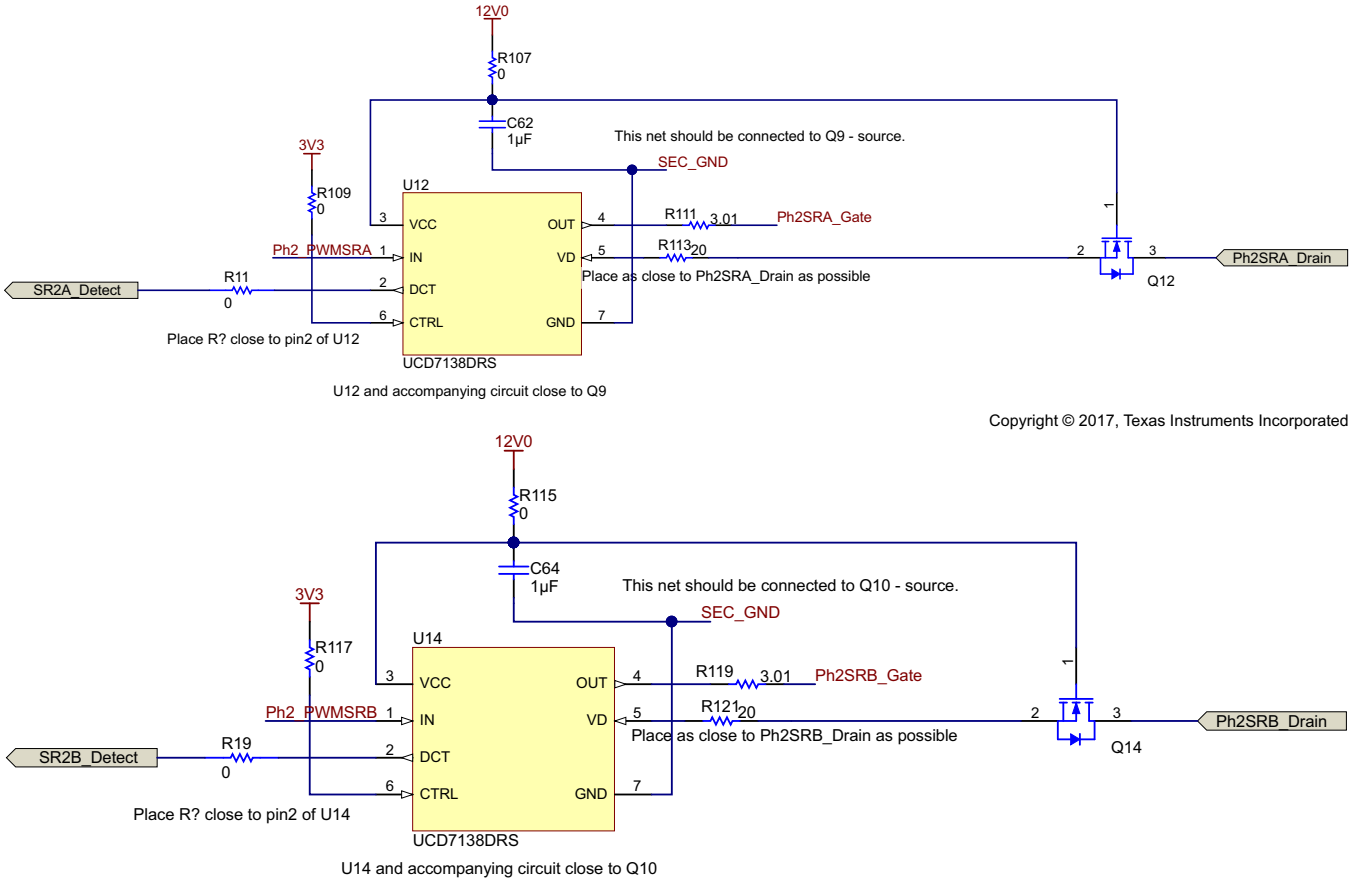


図 16. TIDM-1001 – Phase-Two SR PWM Driver Circuit

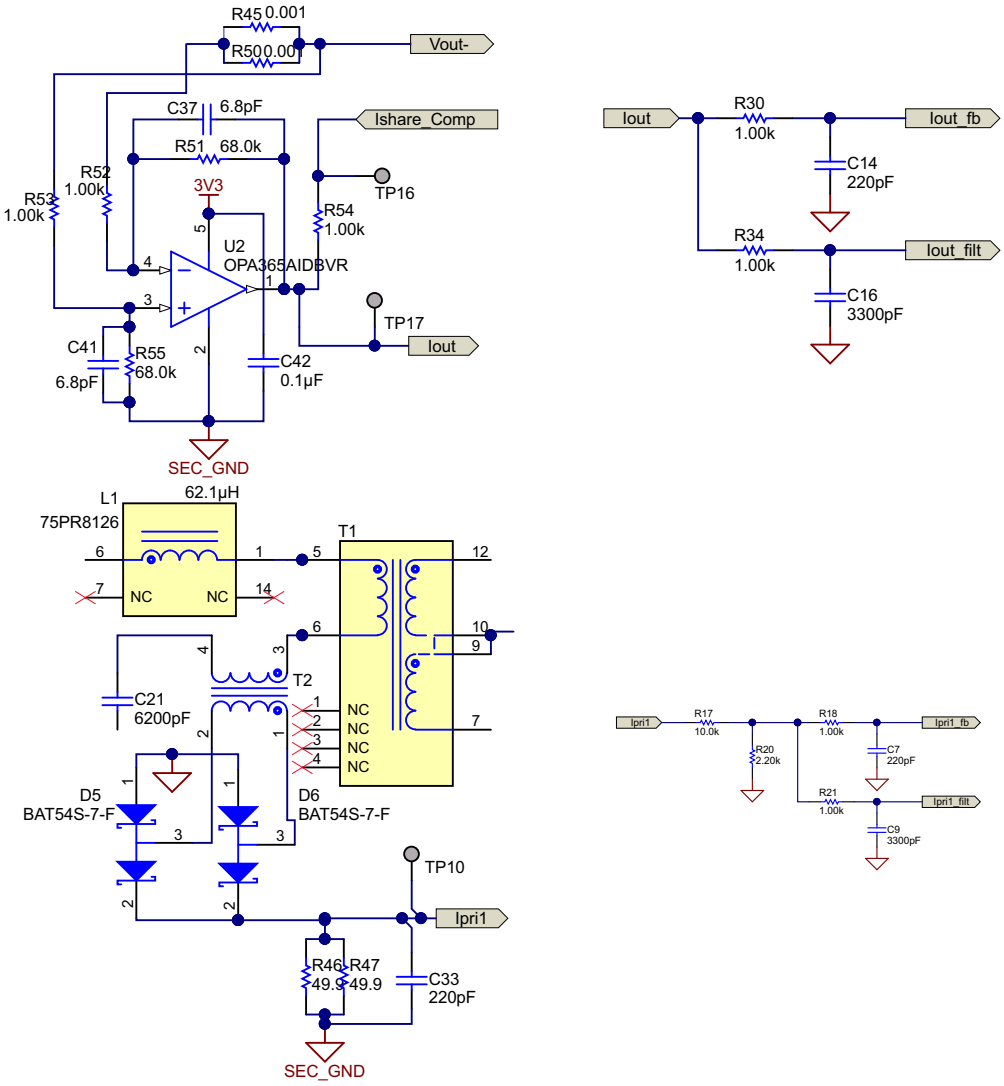


図 17. TIDM-1001 – I_{out} and I_{pri1} Feedback Circuit

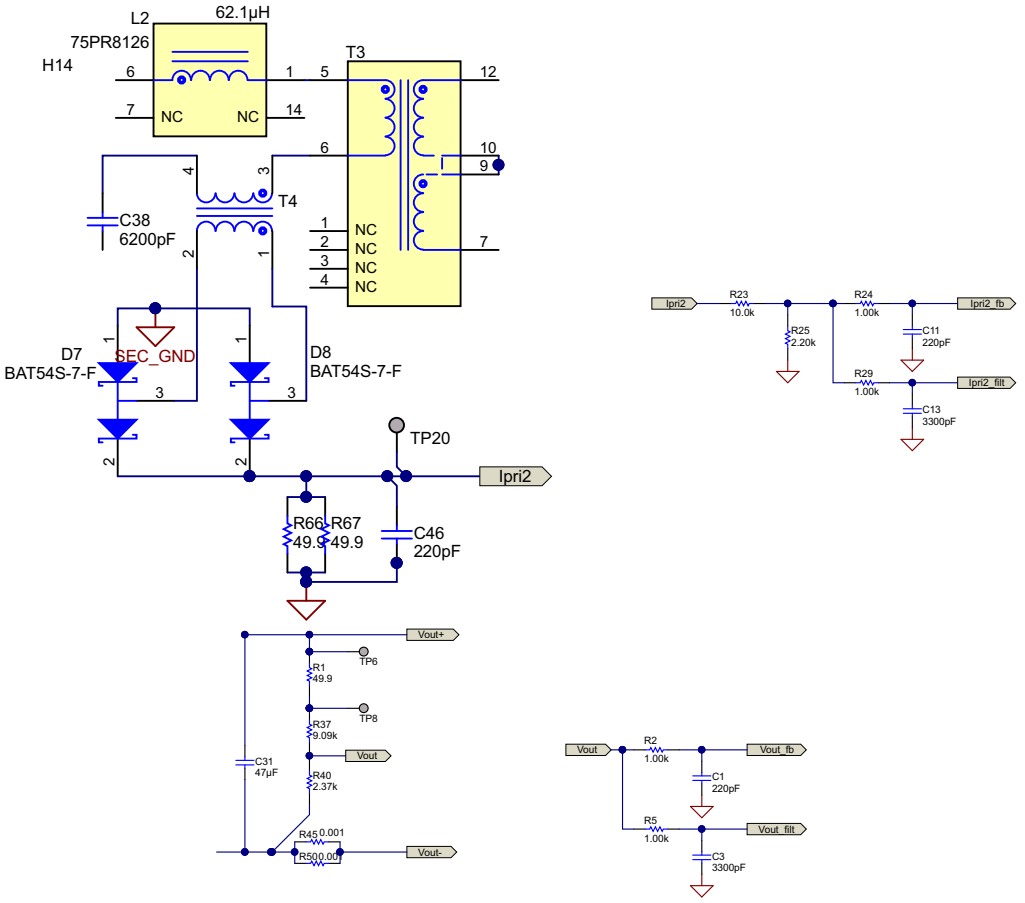


図 18. TIDM-1001 – I_{pri2} and V_{out} Feedback Circuit

2.2 Software Overview

2.2.1 Software Flow

The software project makes use of the C-background and C-ISR framework. The project uses C-background code as the main supporting program for the application, which is responsible for all system management tasks, decision making, intelligence, and host interaction. The C-ISR code is executed inside a time critical interrupt service routine (ISR), and runs all the critical control code. This code includes ADC reading, control calculations, and PWM updates. The *Control ISR* portion of the C-ISR is executed at a fixed rate of 50 kHz using a spare PWM module timer. 図 19 shows the general software flow for this project. Note the references to software frequency response analyzer (SFRA) library functions.

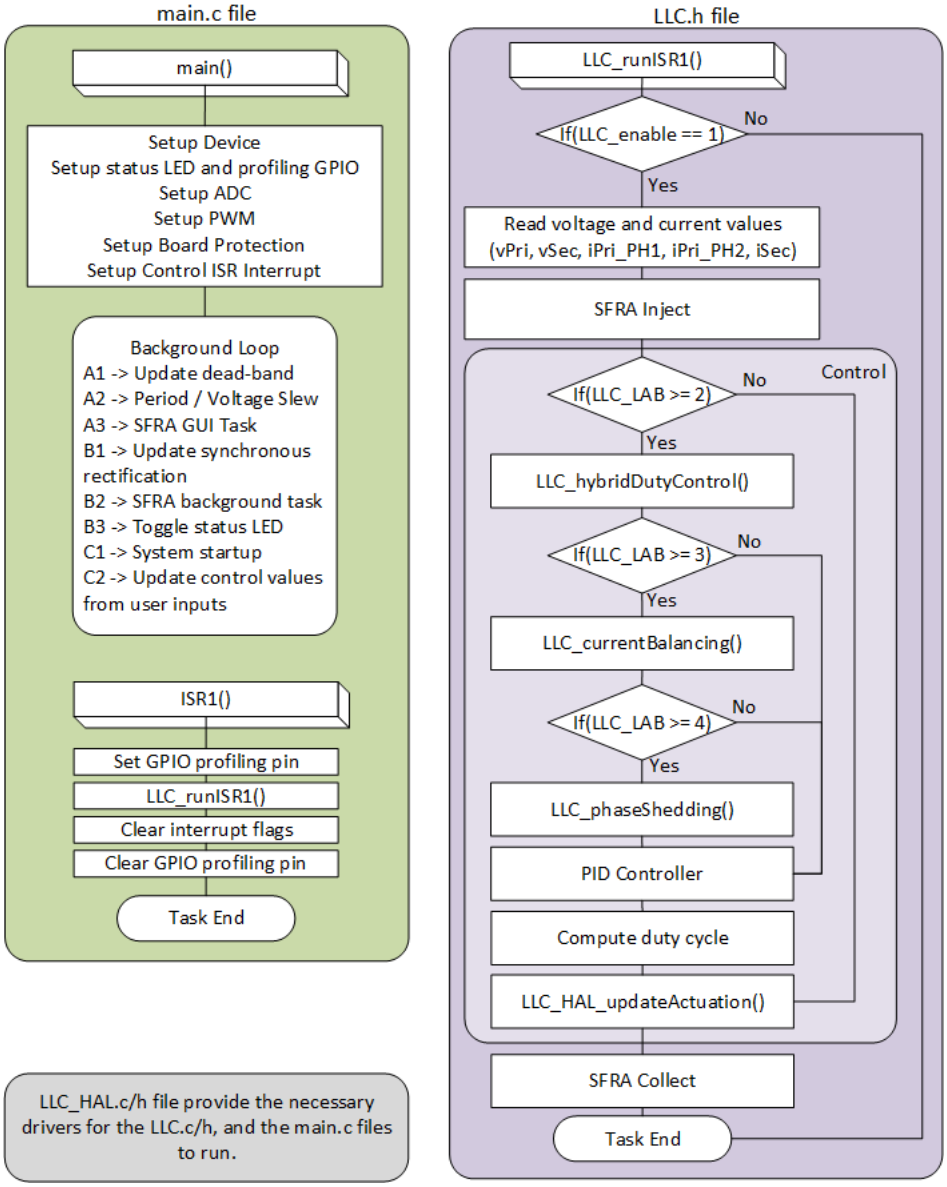


図 19. TIDM-1001 - Software Flow

Texas Instruments' SFRA library is designed to enable frequency response analysis on digitally controlled power converters using software alone, which enables performing frequency response analysis of the power converter with relative ease as no external connections or equipment is required. The optimized library can be used in high-frequency power conversion applications to identify the plant and the open-loop characteristics of a closed-loop power converter, which can be used to get stability information such as bandwidth, gain margin, and phase margin to evaluate the control loop performance. For more information, refer to the SFRA library documentation.

In addition to SFRA, this kit supports the use of other powerSUITE tools including the Compensation Designer and the Solution Adapter. These tools help users evaluate the complete system, adapt it for their end application, and tune it for improved performance. 図 20 shows the typical process flow for designing and tuning such a system using the powerSUITE tools.

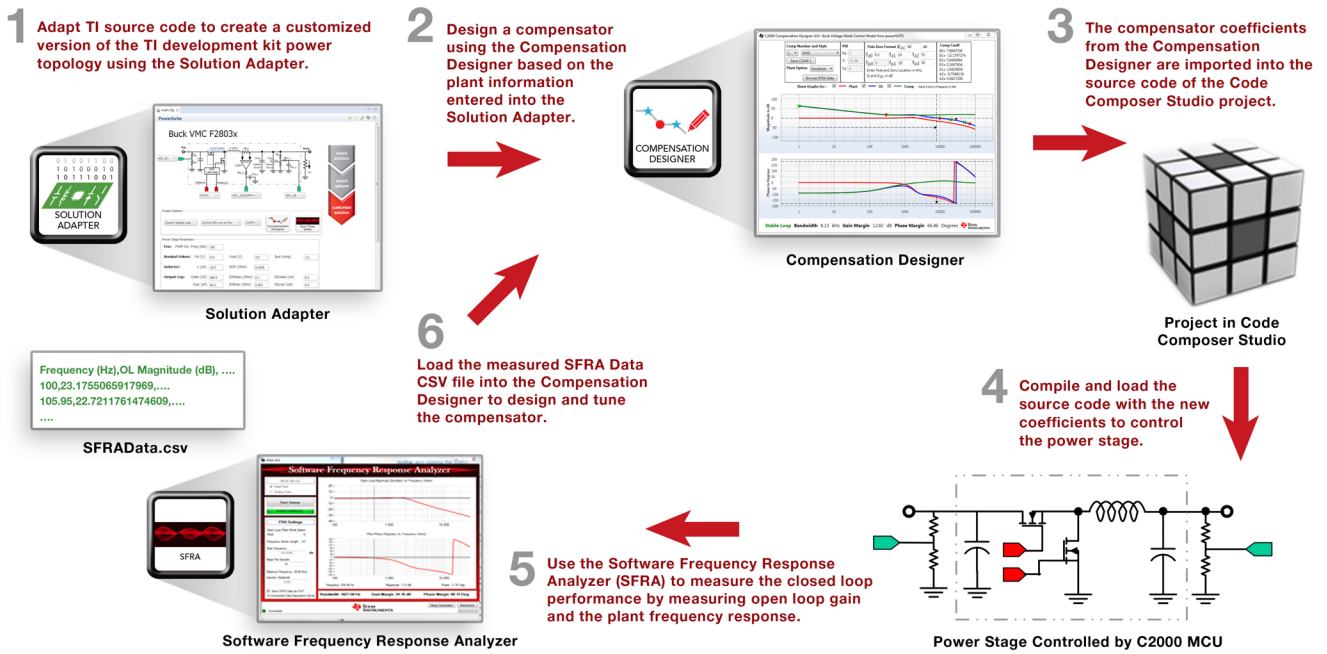


図 20. Design Flow With powerSUITE

The Solution Adapter tool allows users to adapt existing code examples from TI digital power application library and configure them to run on their custom digital power supply board that uses the same topology and similar resources. The GUI steps the user through the process of selecting the solution to adapt, selecting the relevant options for that solution, and customizing those options to adapt the software solution to the user's custom hardware design.

The Compensation Designer tool allows the design of different styles of compensators to achieve the desired closed loop performance, which can be done using the measured power stage or plant data from the SFRA Tool. The coefficients that must be programmed on the device are generated by the Compensation Designer and can be copied into the code directly. Note that the default software project uses a two-pole, two-zero control law and does not support three-pole, three-zero compensators. A PID controller is included as an option. Only the PI coefficients can be designed with Compensation Designer, but a user defined set of coefficients is defined in llc_user_settings.h and can be used to define a manually tuned PID controller. The *PID Controller Tuning Guide* provided in the documentation for the *Digital Control Library* provides guidance that can be used for this process.

The key framework C file used in this project is llc_main.c. This file is used to initialize, run, and manage the application. Driver code for the TMS320F280025C device is in llc_hal.c / llc_hal.h files. The llc.c / llc.h files have all the time-critical control code found in the ISR, as well as the other code specific to the power stage including phase shedding, current balancing, and SR enable / disable threshold. User configurable settings for the project are included in the llc_user_settings.h file. The llc_settings.h file is automatically generated by the powerSUITE GUI and if developing with powerSUITE enabled, any modifications to llc_settings.h will be overwritten when the project is built.

The modular structure makes it convenient to visualize and understand the complete system software flow. The structure also allows for easy use and for additions and deletions of various functionalities. This fact is amply demonstrated in this project by implementing an incremental lab approach, which is discussed in more detail in the 2.2.2.

2.2.2 Incremental Labs

This project is divided into four incremental labs, which makes learning and getting familiar with the board and software easier. This approach is also good for debugging and testing boards.

表 3 shows the lab options. To select a particular lab, select the corresponding project option in *main.syscfg* as shown in 表 3. When the lab option is selected, compile the complete project by selecting *rebuild-all compiler* option. 2.2.3 provides more details to run each of the lab options.

表 3. Incremental Lab Options

INCREMENTAL LAB OPTIONS	
LLC_LAB = 1	Open-loop check with SFRA (check PWM drive circuit and sensing circuit)
LLC_LAB = 2	Closed voltage loop with SFRA (check full system functionality with feedback)
LLC_LAB = 3	Current balancing with SFRA (check closed loop operation with current balancing)
LLC_LAB = 4	Efficiency improvements with SFRA (check closed loop operation with current balancing, phase shedding, and synchronous rectification threshold)

2.2.3 Procedure for Running the Incremental Labs

The main source files and the project file for C framework to bring up the system are located in the project directory. The software project included with this software is targeted for Code Composer Studio™ (CCS) version 9.3 and higher.

Follow the steps in the following subsections to build and run the example software.

注: External Power Supply Required

Nominal Output Voltage: 370-410 VDC

Max Output Current: 1.5 A

Efficiency Level V

NOTE: TI recommends using an external power supply or power accessory which that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, etc.

WARNING

TI intends this design to be operated in a lab environment only and does not consider it to be a finished product for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures. TI intends this design to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems. There area accessible high voltages present on the board. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

WARNING

High voltage! There are accessible high voltages present on the board. Electric shock is possible. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled..Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with over-voltage and over-current protection is highly recommended. TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. When energized, do not touch the design or components connected to the design.

WARNING

Hot surface! Contact may cause burns. Do not touch! Some components may reach high temperatures >55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

WARNING

Do not leave the design powered when unattended.

2.2.3.1 Lab One: Open-Loop Control With SFRA

The objective of this lab is to get familiar with the TIDM-1001 hardware and control the output voltage using direct PWM period adjustments without feedback. Because this system is running open loop, the ADC measured values are only used for instrumentation purposes in this lab. The PWM period is adjusted using the Expressions Window. Optionally, SFRA GUI can be used during run time to get frequency response of the plant.

図 21 shows the software block diagram for lab 1.

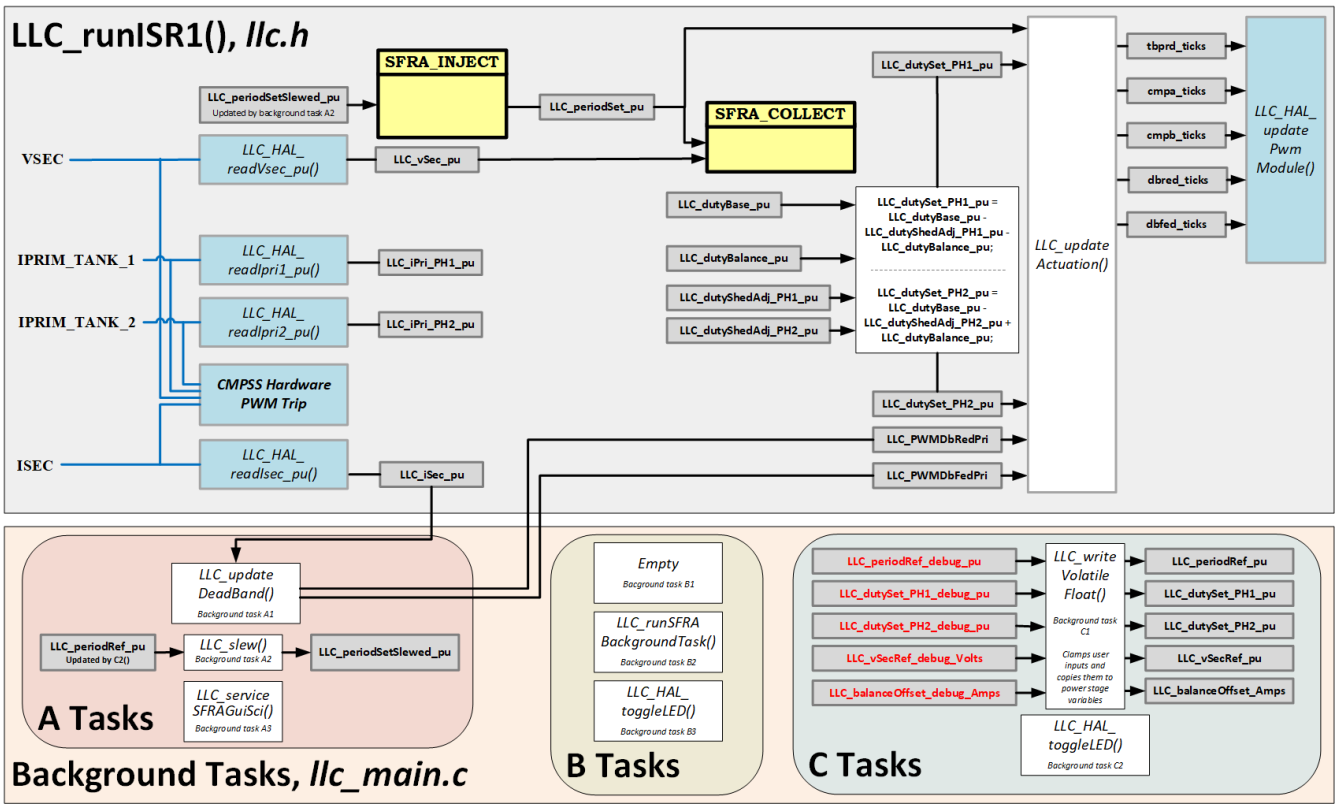


図 21. TIDM-1001 - Lab 1 software diagram

2.2.3.1.1 Overview

The software has been configured to adjust the period of the PWM outputs for the modules selected in *llc_user_settings.h* (for the TIDM-1001 board these are PWMs 1, 2 , 4, and 5). Variable *LLC_periodRef_debug_pu* is used to correctly update PWM registers inside the ISR function *LLC_runISR1()*. The PWM period command can be adjusted from the Expressions Window.

On-chip analog comparators (selected in llc_user_settings.h file) and corresponding DAC mechanisms are used to provide overcurrent protection (for the TIDM-1001 board these are CMPSSs 1, 2, 3 and 4). The reference trip levels for the comparators are defined in the llc_settings.h file: LLC_IPRI1_TRIP_AMPS, LLC_IPRI2_TRIP_AMPS, LLC_ISEC_TRIP_AMPS, LLC_VSEC_TRIP_VOLTS. These define statements set the trip configurations for phase 1 primary current, phase 2 primary current, secondary (output) current, and secondary voltage respectively. The values can be adjusted in the powerSUITE GUI.The comparator output is configured to generate a one-shot trip action on the PWM modules, selected in llc_user_settings.h, whenever the sensed current or voltage is greater than the set limit. The flexibility of the trip mechanism on C2000 devices provides the possibility for taking different actions on different trip events. In this project all PWM outputs are driven low immediately on a comparator event to protect the power stage.

The converter is driven at a PWM switching frequency between 200 kHz and 350 kHz according to the *LLC_periodSet_pu* command. The control ISR is triggered by a spare PWM module at a rate of 50 KHz, but the project supports increasing the control frequency up to 100 KHz.

A task state-machine has been implemented as part of the background code. Tasks are arranged in groups (A1, A2, A3…, B1, B2, B3…, C1, C2, C3…). Each group is executed according to three CPU timers, which are configured with periods of 1 ms, 20 ms, and 50 ms respectively. Within each group (for example, *B*) each task is run in a *round-robin* manner. For example, group B executes every 20 ms, and there are three tasks in group B. Therefore, B1, B2, and B3 execute once every 60 ms.

2.2.3.1.2 Procedure

2.2.3.1.2.1 Hardware Setup

1. To get started with the TIDM-1001 board, the user must have a TMS320F280025C controlCARD with a mini-USB cable, a 12-V DC bench power supply, and a computer with CCS version 9.3 or newer, the latest version of Digital Power SDK, and CCS SysConfig utility installed.
2. Make sure that all jumpers on the TIDM-1001 board are correctly installed as listed in the 2.1.
3. Insert the controlCARD in the 120-pin connector J3. Connect a current limited 12-V DC bench power supply between TP25 and TP26 with correct polarity. Connect an isolated, 400-V programmable DC power source to the 400-V input connector (J9 to J12) and 12-V load to the 12-V output connector (J10 and J11). Make sure that this load does not exceed the board ratings. Connect a USB B-to-A cable between the PC and the controlCARD. Do not turn ON any of the power supplies at this time.

   注: While this system can operate under *No Load* condition, it is recommended to use a load (I_{out}) of at least 5 A for the open-loop tests.

   Use an external air cooling fan (CFM rating > 50) directed at the board when operating with loads (I_{out}) of 30 A and higher
4. Make sure position two of the controlCARD switch *A:SW1* is in ON position in the SFRA setup step.

2.2.3.1.2.2 Software Setup

1. Open CCS (version 9.3 or newer). Maximize CCS to fill the screen. Close the welcome screen if it opens up.
2. On the menu bar click **Project** >**Import CCS Project**. Below the root directory, navigate to and select *..\C2000Ware_DigitalPower_SDK_X_XX_XX_XX\solutions\tidm_1001\f28002x\llc* directory. Make sure that below the **Projects** tab, 2PH_IL_LLC_F28002x is selected. Click **Finish**.
3. 2PH_IL_LLC_F28002x project should now appear in the CCS Project Explorer window. This project will invoke all the necessary tools (compiler, assembler, and linker) to build the project. A project contains all the files and build options required to develop an executable output file (.out), which can be run on the MCU hardware.
4. In the project window on the left, click the arrow sign to the left of the project name.The project window will look like 図 22.

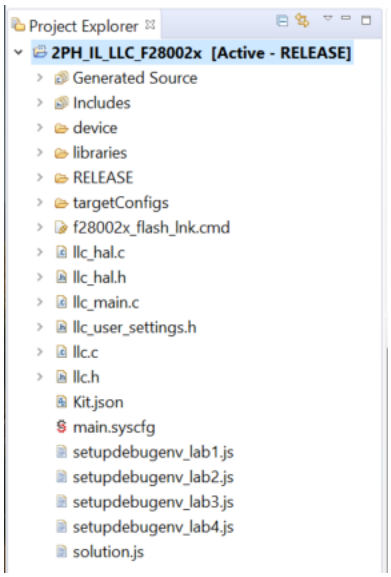


図 22. Project Window

5. If not already open, double click the main.sysconfig file name in the project window.

6. Under *Project Options* select *Open Loop* as shown in 図 23. Save *main.syscfg* file.

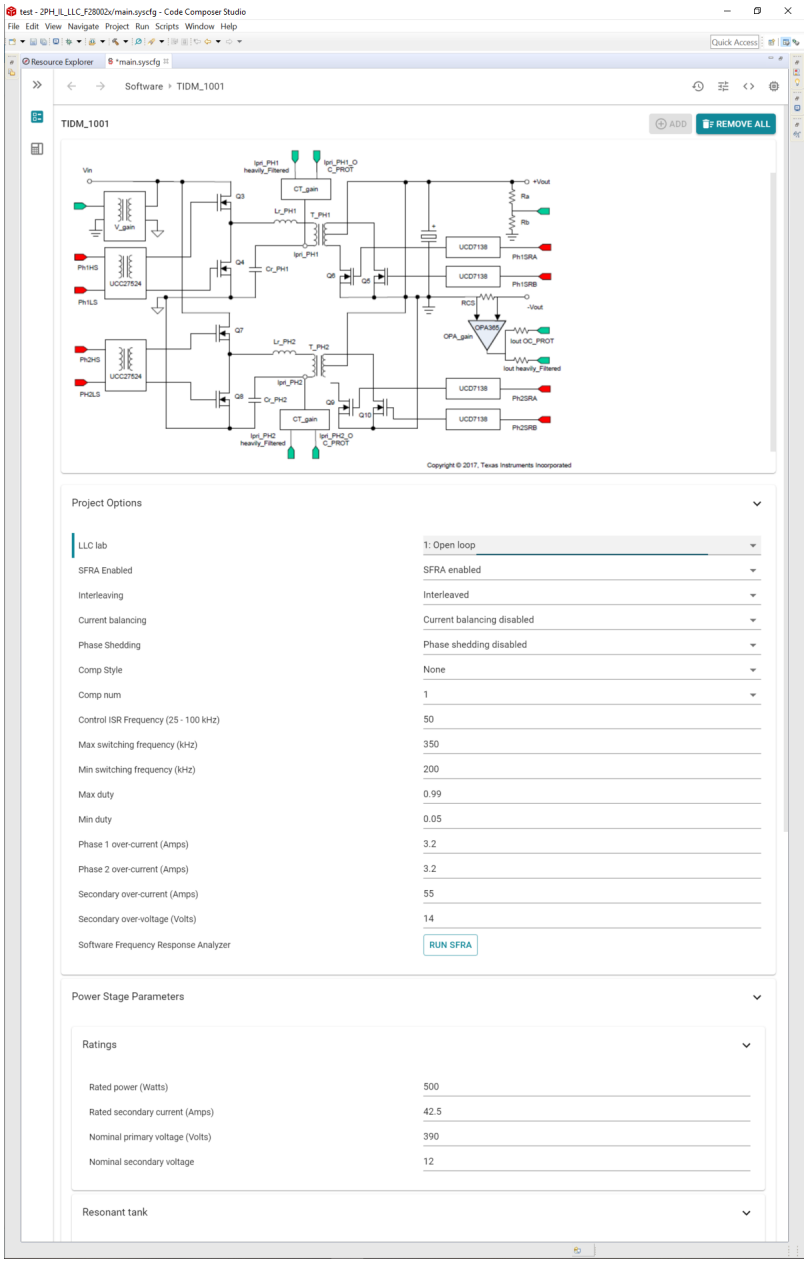


図 23. Lab One: main.syscfg

2.2.3.1.2.3 Build and Load the Project

1. Turn ON the 12-V auxiliary supply.
2. If another lab option was built previously, right-click on the project name, and click on **Clean Project**. Click **Project** > **Build All** button, and watch the tools run in the build window.
3. Click the **Debug** button () or click **Run** > **Debug**. The code should compile and load.
4. Notice the **CCS Debug** icon in the upper corner, which indicates the **Debug Perspective** view. The program should be stopped at the start of **main()**.

2.2.3.1.2.4 Debug Environment Windows

It is standard debug practice to watch local and global variables while debugging code. There are various methods for doing this in CCS, such as memory windows and watch windows. Additionally, CCS has the ability to make time (and frequency) domain plots, which allows the user to view waveforms using graph windows.

1. Populate the Expressions Window entries by clicking **View** > **Scripting console** on the menu bar and then opening the *setupdebugenv_lab1.js* file from the project directory using the scripting console **Open File** ( ) command. The Expressions Window should look like 図 24.

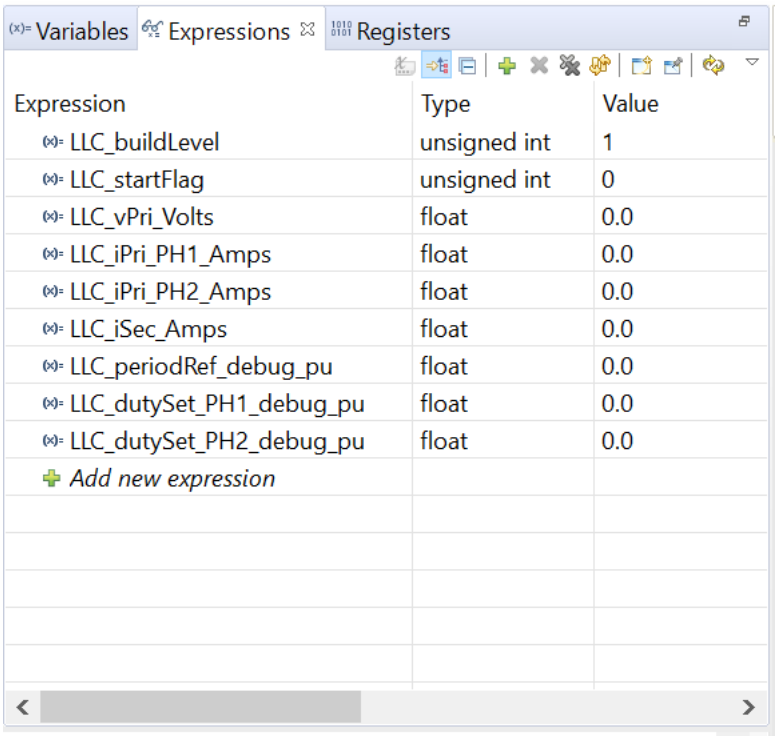


図 24. Lab One: Expressions Window at Reset

表 4. Lab 1 Description of Expressions Window Entries

VARIABLE	DESCRIPTION
LLC_buildLevel	Shows which lab is loaded.
LLC_startFlag	Set this variable to 1 to start the powerstage.
LLC_vPri_Volts	Input voltage in Volts. Only valid if jumper J15 is populated on the TIDM-1001 board.
LLC_iPri_PH1_Amps	The primary tank current in phase 1 in Amps.
LLC_iPri_PH2_Amps	The primary tank current in phase 2 in Amps.
LLC_iSec_Amps	Secondary (output) current in Amps.
LLC_periodRef_debug_pu	The variable used to control the switching period in lab 1. It is in per unit format.
LLC_dutySet_PH1_debug_pu	The variable used to control the switching duty for phase 1. It is in per unit format.
LLC_dutySet_PH2_debug_pu	The variable used to control the switching duty for phase 2. It is in per unit format.

2.2.3.1.2.5 Using Real-Time Emulation

Real-time emulation is a special emulation feature that allows windows within CCS to be updated *while the MCU is running*. This feature not only allows graphs and watch windows to update, but also allows the user to change variables or memory location values and have those changes affect the MCU behavior. This feature is very useful when tuning control law parameters on-the-fly, for example.

1. Enable real-time mode by hovering your mouse on the buttons on the horizontal toolbar and clicking 

button.
2. A message box may appear. If so, select *YES* to enable debug events. This will set bit one (DGBM bit) of status register one (ST1) to *0*. The DGBM is the debug enable mask bit. When the DGBM bit is set to *0*, memory and register values can be passed to the host processor for updating the debugger windows.
3. When a large number of windows are open, as bandwidth over the emulation link is limited, updating too many windows and variables in continuous refresh can cause the refresh frequency to slow down. Right-click on the button in the Expressions Window and select *Continuous Refresh Interval…*. The refresh rate can be slowed for the Expressions Window variables by changing the *Continuous refresh interval (milliseconds)* value. A rate of 1000 ms is usually enough for these exercises. Click on *Continuous Refresh* buttons () for the watch view.

2.2.3.1.2.6 Run the Code

1. Run the code by using the <F8> key or the *Run* button on the toolbar.
2. As this is an open-loop test (no voltage loop), care must be taken not to use too small a load to avoid accidental high output voltages. Use a load of 5A at the 12-V output.
3. Set the 400-V DC supply to output 300 V (this value is lower than the 370-V, low-end limit for the reason mentioned in the previous step). Set the power supply current limit to an appropriate level for this test. Now turn ON this 300-V power supply.
4. In the Expressions Window set *LLC_startFlag = 1.* The converter operation should start with the default LLC_periodSet_pu value resulting in approximately 350-kHz switching frequency..
5. Verify that all of the sensed values are updating in the expressions window: *LLC_vPri_Volts*, *LLC_iPri_PH1_Amps*, *LLC_iPri_PH2_Amps*, *LLC_iSec_Amps*.
6. The *LLC_periodRef_debug_pu* value may be changed between 0.57 and 1.00. As this value is increased the switching frequency decreases, which results in a higher energy delivered to the load. In open loop this results in an increase in output voltage, which should not be allowed to exceed board capabilities.
7. Verify that as the *LLC_periodRef_debug_pu* value is changed, the sense values reflect those changes. The secondary voltage should increase / decrease, and the primary and secondary currents should change accordingly.
8. The LLC_dutySet_PH1_debug_pu, and LLC_dutySet_PH2_debug_pu variables are initialized to 0.99, but they may be set to values between 0.05 and 0.99. An oscilloscope may be used to observe the changing duty cycle for the switch waveforms.
9. If desired, the SFRA tool may now be used to look at the frequency response of the plant.
10. To do this click on main.syscfg file and open SFRA. Click on setup connection and select the appropriate COM port. Make sure that the baud rate is set to *57600* and that *Boot on Connect* is unchecked. Click *OK*.

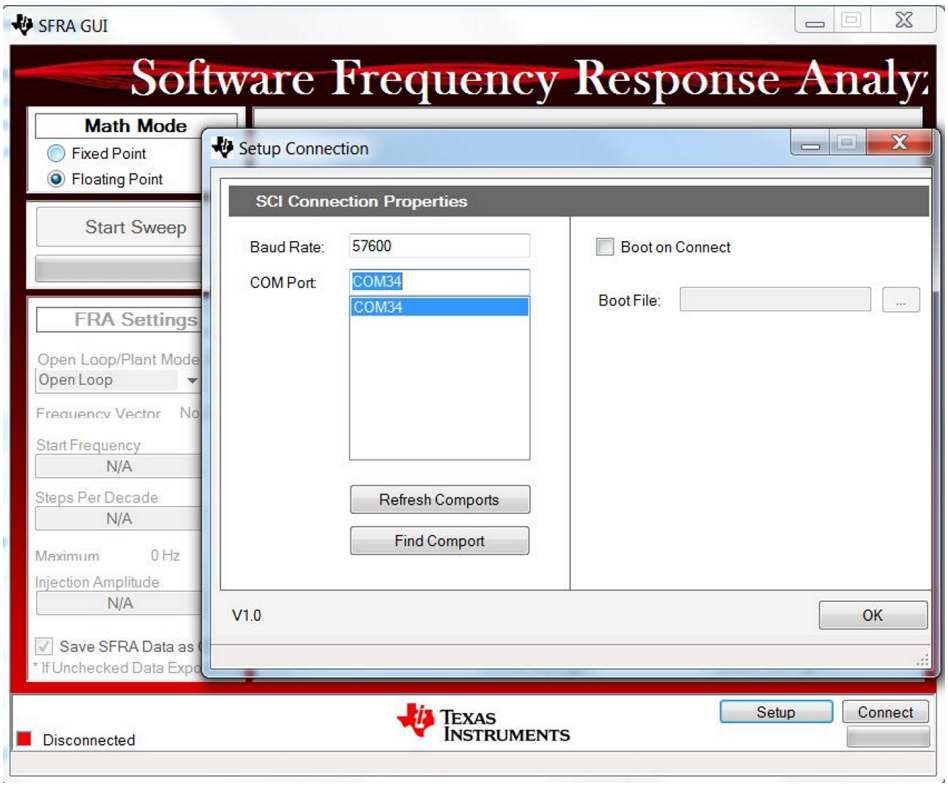


図 25. Lab One: SFRA Connections Setup

11. Select *Floating Point* math.
12. Click *Connect* on the SFRA GUI. Once the GUI is connected, click on *Start Sweep*. SFRA will start applying different frequencies and collecting the response for frequency analysis.
13. Once the frequency sweep is complete, the response will be displayed on the SFRA GUI, as shown in 図 26.

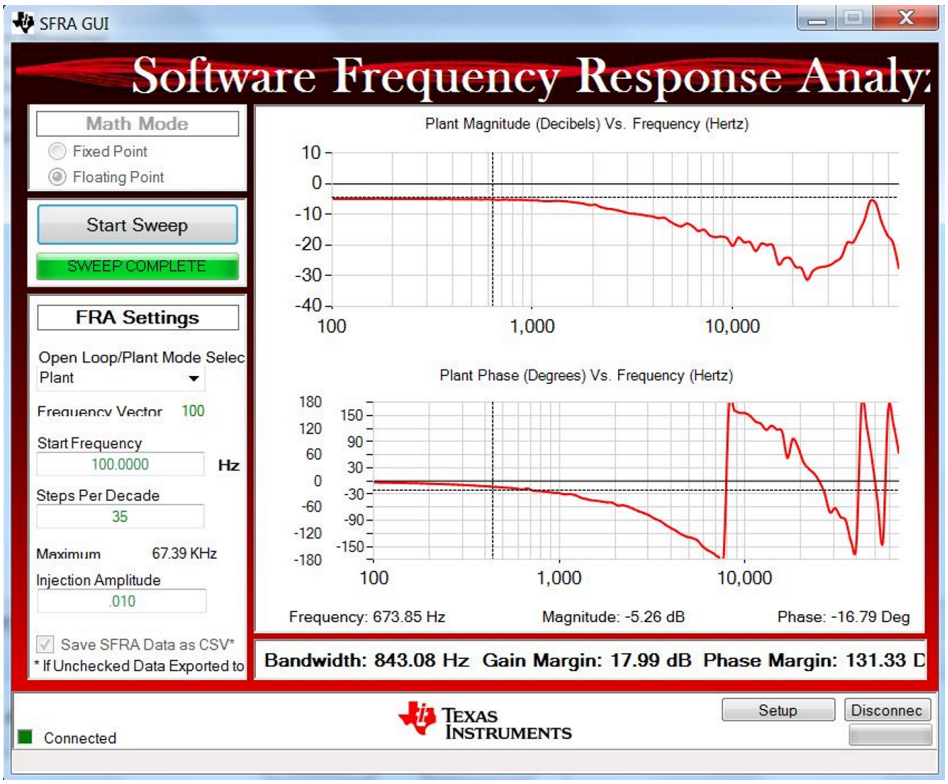


図 26. Lab One: SFRA Results

14. Close the SFRA GUI.
15. Turn OFF the 300-V DC power supply.
16. Fully halting the MCU when in real-time mode is a two-step process. First, halt the processor by using the *Suspend* button ( ) on the toolbar or by using *Run* → *Suspend*. Click button again to take the MCU out of real-time mode and then reset the MCU (*Run* → *Reset* → *CPU Reset*).
17. CCS may be left running for the next lab or optionally close CCS.

End of exercise.

2.2.3.2 Lab Two: Closed-Loop Control With SFRA

The objective of this lab is to regulate the output voltage of the converter using closed-loop feedback control realized in the form of a software-coded control loop. A compensator designed using the Compensation Designer GUI is used to achieve desired closed loop-performance. SFRA GUI can be used during run time to capture the frequency response of the system.

2.2.3.2.1 Overview

The software has been configured to provide closed loop voltage control for the two-phase, interleaved LLC resonant converter power stage. A two-pole, two-zero controller module (DCL_runDF22_C1) is used to implement the control law. The option for a PID controller module (DCL_runPID_C1) is also provided and can be selected from the powerSUITE GUI. The output voltage feedback *LLC_vSec_pu* is an input to the controller block. The reference input to the controller block comes from the slewed output voltage command *LLC_vSecSet_pu*. If used, the SFRA signal is applied to the voltage reference. The controller output *LLC_periodSet_pu* is used by the driver to update PWM registers similar to lab one. The output voltage command can be adjusted from the Expressions Window using the variable *LLC_vSecRef_debug_Volts*. The software block diagram is shown in 図 27

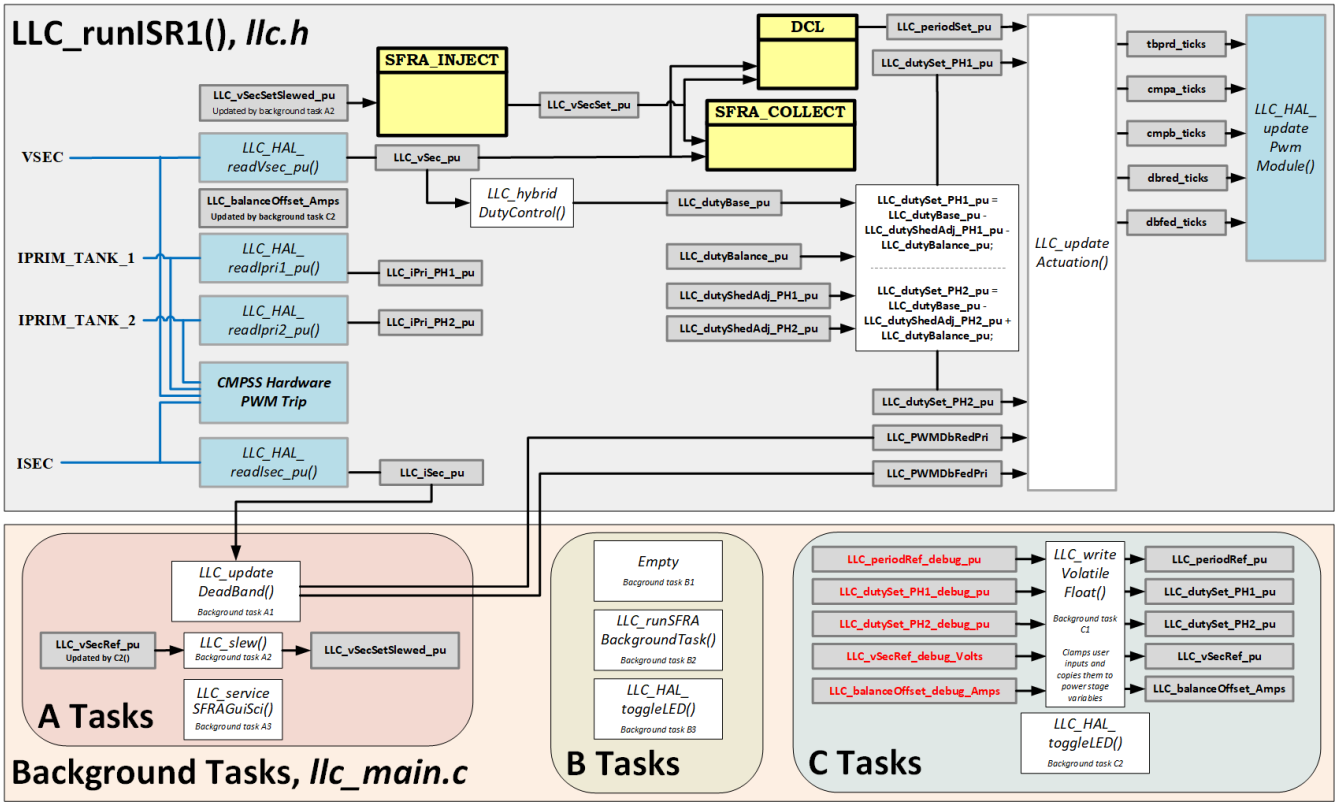


図 27. TIDM-1001 - Lab 2 Software Diagram

Similar to lab one, on-chip analog comparators (selected in llc_user_settings.h file) and corresponding DAC mechanisms are used to provide overcurrent and overvoltage protection (for the TIDM-1001 board these are CMPSSs 1, 2, 3, and 4). The reference trip level for the comparators can be set using the powerSUITE GUI, which updates the LLC_IPRI1_TRIP_AMPS, LLC_IPRI2_TRIP_AMPS, LLC_ISEC_TRIP_AMPS, LLC_VSEC_TRIP_VOLTS defines in the LLC_settings.h file. The comparator output is configured to generate a one-shot trip action on the PWM modules, selected in llc_user_settings.h, whenever the sensed current or voltage is greater than the set limit. The flexibility of the trip mechanism on C2000 devices provides the possibility for taking different actions on different trip events. In this project all PWM outputs are driven low immediately on a comparator event to protect the power stage.

The converter is driven at a PWM switching frequency between 200 kHz and 350 kHz. The ISR is triggered by a spare PWM module (PWM3). This ISR is where the control code is executed.

Similar to lab one, a task state-machine has been implemented as part of the background code. Tasks are arranged in groups (A1, A2, A3…, B1, B2, B3…, C1, C2, C3…). Each group is executed according to three CPU timers, which are configured with periods of 1 ms, 20 ms, and 50 ms respectively. Within each group (for example, *B*) each task is run in a *round-robin* manner. For example, group B executes every 20 ms, and there are three tasks in group B. Therefore, B1, B2, and B3 execute once every 60 ms.

2.2.3.2.2 Procedure

2.2.3.2.2.1 Hardware Setup

1. Follow the steps in 2.2.3.1.2.1 for lab one procedure.

注: While this system can operate under *No Load* condition, it is recommended to use a load (I_{out}) of at least 2 A for the closed-loop tests.

Use an external air cooling fan (CFM rating > 50) directed at the board when operating with loads (I_{out}) of 30 A and higher.

2.2.3.2.2.2 Software Setup

1. Follow the steps in the software setup section for lab 1 to open the powerSUITE GUI. (2.2.3.1.2.2)
2. Below **Project Options** in the powerSUITE GUI select **Closed Loop.** This will set the project to the default configurations for closed loop operation of the power stage.
3. Without changing any of the default parameters, click on *Compensation Designer*.
4. The Compensation Designer GUI shown in 図 28 uses the SFRA data from the previous run of SFRA on this system (default data for this design is in the project folder) to plot the expected frequency response for the set of compensator coefficients selected in the main.syscfg file (COMP1). The Compensation Designer GUI allows the design of different compensators to achieve desired closed-loop performance. Compensation Designer GUI can also use power stage model data, if it exists, based on the data entered in the main.syscfg file. For this project the modelled plant option is not available.

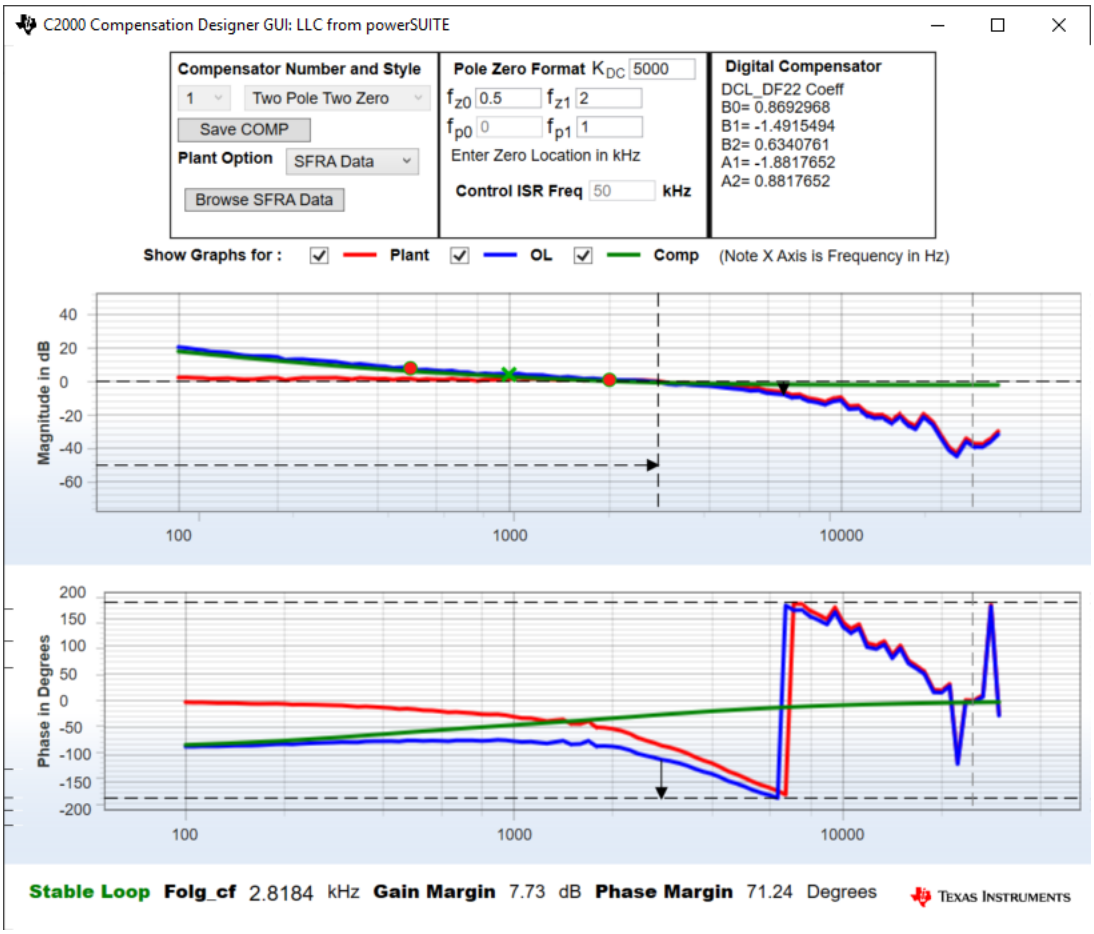


図 28. Compensation Designer GUI

5. The default compensator (COMP1) is a two-pole, two-zero compensator, which has been provided by TI. Notice that the magnitude and phase plots, for the plant, open loop, and the compensator update whenever a new compensator is selected from the list of possible compensators in main.syscfg. These plots also update when the selected compensator's parameters (pole and zero locations and gains) are changed in the Compensation Designer GUI. When any changes are made in Compensation Designer the "Save COMP" button will write the updated coefficients into the project. Note that the default software supports two-pole, two-zero, and PID compensators. The Compensation Designer GUI supports tuning only the PI coefficients of the PID controller, so if derivative action is desired the PID controller will have to be tuned manually. Guidance for manual tuning can be found in the *PID Controller Tuning Guide* provided with the *Digital Control Library* documentation.
6. Do not change any of the parameters in the Compensation Designer GUI, and leave the default set of compensator coefficients (COMP1) in main.cfg. These parameters can be changed and experimented with at a later time. Close the Compensation Designer GUI.
7. The default project options will be used. Save the main.syscfg file. This project is ready to be built and loaded.

2.2.3.2.2.3 Build and Load the Project

1. Follow the steps in 2.2.3.1.2.4 for lab one procedure.

2.2.3.2.2.4 Debug Environment Windows

It is standard debug practice to watch local and global variables while debugging code. There are various methods for doing this in CCs, such as memory windows and watch windows. Additionally, CCS has the ability to make time (and frequency) domain plots, which allows the user to view waveforms using graph windows.

1. Populate the Expressions Window entries by clicking on *View* → *Scripting console* on the menu bar and then opening the *setupdebugenv_lab2.js* file from the project directory using the scripting console *Open File* ( ) command. The Expressions Window should look like 図 29.

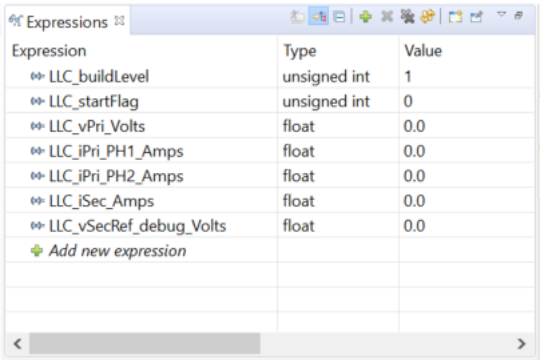


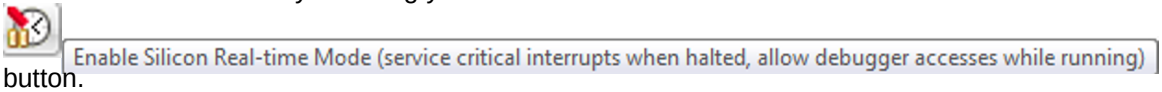
図 29. Lab Two: Expressions Window at Reset

表 5. Lab 2 Description of Expressions Window Entries

VARIABLE	DESCRIPTION
LLC_buildLevel	Shows which lab is loaded.
LLC_startFlag	Set this variable to 1 to start the power stage.
LLC_vPri_Volts	Input voltage in Volts. Only valid if jumper J15 is populated on the TIDM-1001 board.
LLC_iPri_PH1_Amps	The primary tank current in phase 1 in Amps.
LLC_iPri_PH2_Amps	The primary tank current in phase 2 in Amps.
LLC_iSec_Amps	Secondary (output) current in Amps.
LLC_vSecRef_debug_Volts	This variable allows the user to set the desired regulation voltage.

2.2.3.2.2.5 Using Real-Time Emulation

Real-time emulation is a special emulation feature that allows windows within CCS to be updated *while the MCU is running*. This feature not only allows graphs and watch windows to update, but also allows the user to change variables or memory location values and have those changes affect the MCU behavior. This feature is very useful when tuning control law parameters on-the-fly, for example.

1. Enable real-time mode by hovering your mouse on the buttons on the horizontal toolbar and clicking 

button.
2. A message box may appear. If so, select *YES* to enable debug events. This will set bit one (DGBM bit) of status register one (ST1) to *0*. The DGBM is the debug enable mask bit. When the DGBM bit is set to *0*, memory and register values can be passed to the host processor for updating the debugger windows.
3. When a large number of windows are open, as bandwidth over the emulation link is limited, updating too many windows and variables in continuous refresh can cause the refresh frequency to slow down. Right-click on the button in the Expressions Window, and select *Continuous Refresh Interval…*.

The refresh rate can be slowed for the Expressions Window variables by changing the *Continuous refresh interval (milliseconds)* value. A rate of 1000 ms is usually enough for these exercises. Click on *Continuous Refresh* buttons ( ) for the Expressions Window.

2.2.3.2.2.6 Run the Code

1. Run the code by using the <F8> key or the *Run* button on the toolbar.
2. Please use a load of at least 2 A or higher (within board specifications) at the 12-V output. If this is the first time of running closed loop test on this board, select a load between 5 A and 15 A.
3. Set the 400-V DC supply to output 390 V. Set the power supply current limit to an appropriate level for this test. Now turn ON this 390-V power supply.
4. At this point the output voltage should still be zero as the converter start command has not been initiated.
5. Now set the *LLC_startFlag* to 1 in the Expressions Window.
6. The converter operation should start and the output should ramp-up to approximately 12 V.

注: If output voltage does not ramp up to approximately 12 V, turn OFF the 390-V DC supply immediately. Verify build one operation first as described in 2.2.3.1. The user may also be required to re-verify the board components and debug hardware issues (components do not match the bill of materials (BOM), PCB fabrication issue, and so forth) before this board can be tested again.

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7. Observe the effect of varying load on the output voltage and input current. There should be virtually no effect on the output voltage. Similarly observe the effect of varying the input voltage. Again there should be virtually no effect on the output voltage. (1)
8. Different waveforms, like the PWM gate drive signals, input voltage, and current and output voltage may also be probed using an oscilloscope. Appropriate safety precautions should be taken and appropriate grounding requirements should be considered while probing these high voltages and high currents for this isolated DC-DC converter.
9. Now click on main.syscfg file and open SFRA. Click on setup connection, and select the appropriate COM port. Make sure that the baud rate is set to *57600* and that *Boot on Connect* is unchecked. Click *OK*.

(1) Make sure that these changes are made within the abilities of the board as listed in 表 1.

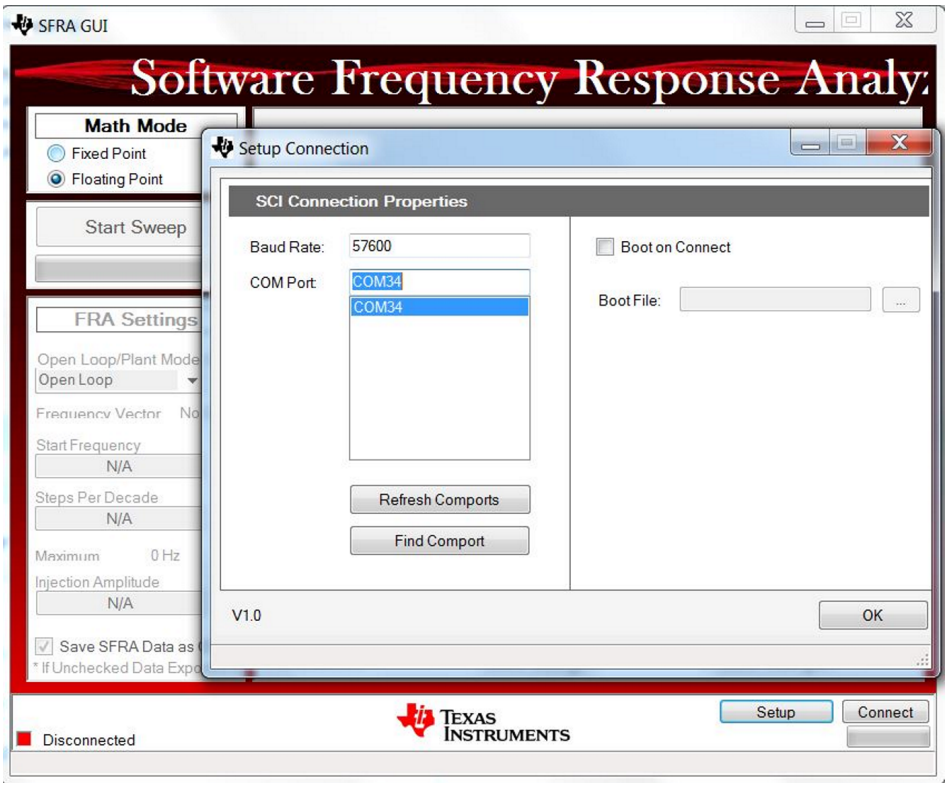

図 30. Lab Two: SFRA Connections Setup

10. Select *Floating Point* math.
11. Click *Connect* on the SFRA GUI. Once the GUI is connected, click on *Start Sweep*. SFRA will start applying different frequencies and collecting the response for frequency analysis. The effect of this process may be seen on the output voltage as observed on an oscilloscope. The high-frequency signals riding on the output voltage indicate an active SFRA run.
12. Once the frequency sweep is complete, the response will be displayed on the SFRA GUI. The bandwidth, gain margin, and phase margin should be similar to the values noted on the Compensation Designer GUI. These values may differ to varying degrees based on how closely the parameters match the actual power stage values. The input voltage and output load will also affect the power stage dynamics, and the values reported by the SFRA GUI.

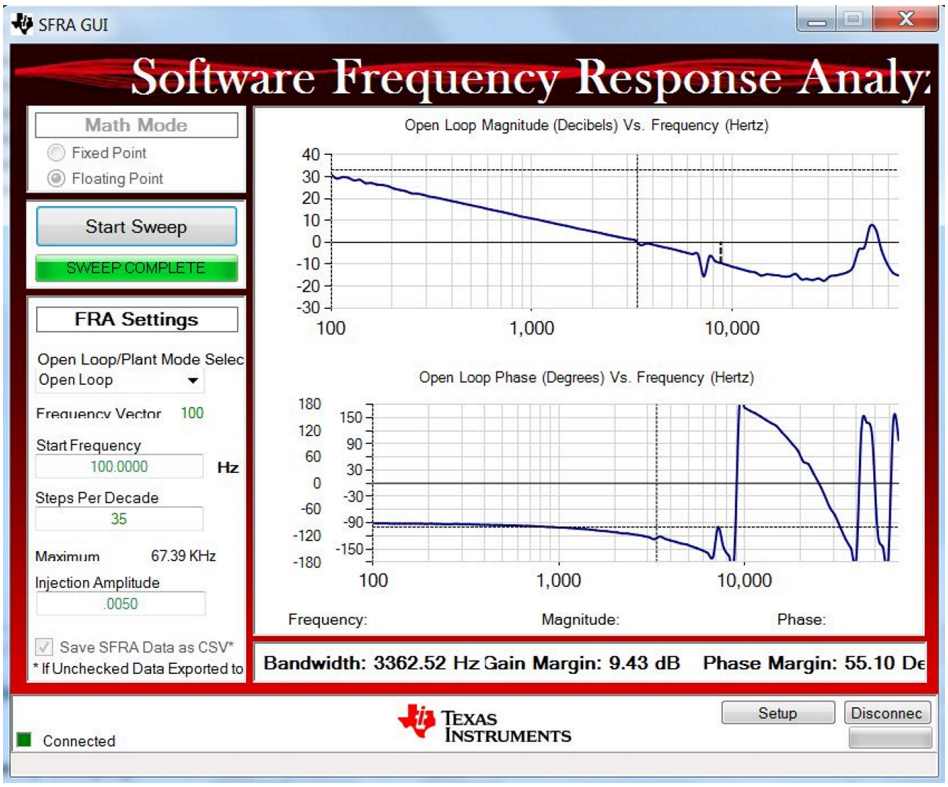

図 31. Build Two: SFRA Results

13. Close the SFRA GUI.
14. Turn OFF the 390-V DC power supply.
15. Fully halting the MCU when in real-time mode is a two-step process. First, halt the processor by using the *Suspend* button ( ) on the toolbar or *Run* → *Suspend*. Click button again to take the MCU out of real-time mode and then reset the MCU (*Run* → *Reset* → *CPU Reset*).
16. Close CCS.

End of exercise.

2.2.3.3 Lab Three: Closed-Loop Control With Current Balancing and SFRA

The objective of this lab is to show closed-loop voltage regulation with an innovative software based current balancing technique. The powerstage is operated under load and the primary tank currents are observed. A variable is given to allow the user to create an artificial current imbalance, or to offset any difference that may exist in the sensing circuitry and achieve better balancing.

2.2.3.3.1 Overview

The software for this lab is mostly identical to lab two, but additional current balancing logic has been added in this lab. The reference voltage can be set to adjust the regulation of the powerstage using the *LLC_vSecRef_debug_Volts* variable. The tank current in each phase, as well as the balancing effort can be read from the Expressions Window variables *LLC_iPri_PH1_Amps, LLC_iPri_PH2_Amps, LLC_dutyBalance_pu.* The balance variable reflects a difference in duty between the switching waveforms for the two phases, as the difference increases the phases will tend to balance. The *LLC_balanceOffset_Amps* variable can be used to fine tune the balancing by adding a positive or negative constant to the phase 1 current reading.

The software block diagram is shown in 図 32

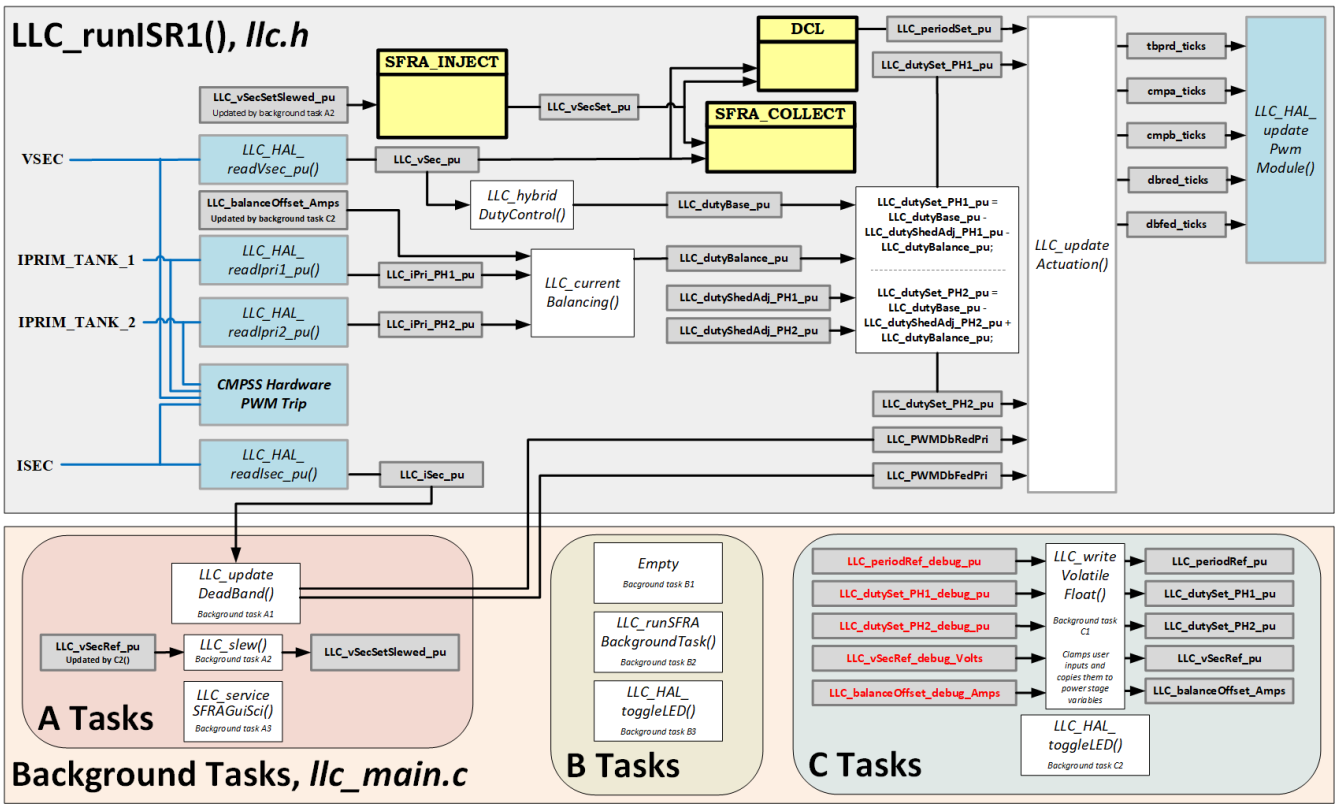

図 32. TIDM-1001 - Lab 3 software diagram

2.2.3.3.2 Procedure

The setup for this lab closely follows the setup for the previous labs.

2.2.3.3.2.1 Hardware Setup

1. Follow the steps in 2.2.3.1.2.1 for lab one procedure.

2.2.3.3.2.2 Software Setup

1. Follow steps 1-5 in 2.2.3.1.2.2 for lab one procedure to load the project and open the powerSUITE GUI.
2. Under *Project Options* select "Closed loop + current balancing".

3. Save *main.syscfg* file.

2.2.3.3.2.3 Build and Load the Project

1. Follow the steps in 2.2.3.1.2.4 for lab one procedure.

2.2.3.3.2.4 Debug Environment Windows

It is standard debug practice to watch local and global variables while debugging code. There are various methods for doing this in CCS, such as memory windows and watch windows. Additionally, CCS has the ability to make time (and frequency) domain plots, which allows the user to view waveforms using graph windows.

1. Populate the Expressions Window entries by clicking on *View* → *Scripting console* on the menu bar and then opening the *setupdebugenv_lab3.js* file from the project directory using the scripting console *Open File* ( ) command. The Expressions Window should look like 図 33.

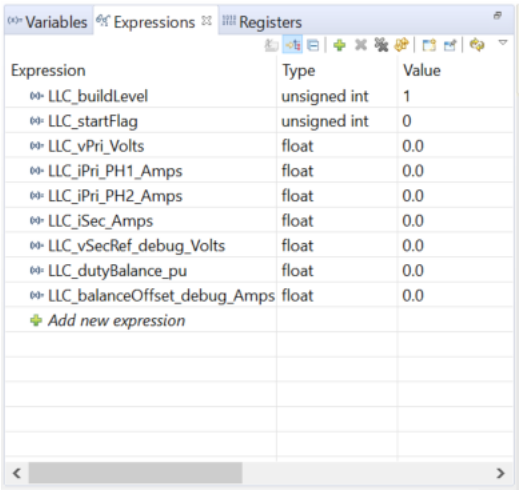

図 33. Lab Three: Expressions Window at Reset

表 6. Lab 3 Description of Expressions Window Entries

VARIABLE	DESCRIPTION
LLC_buildLevel	Shows which lab is loaded.
LLC_startFlag	Set this variable to 1 to start the powerstage.
LLC_vPri_Volts	Input voltage in Volts. Only valid if jumper J15 is populated on the TIDM-1001 board.
LLC_iPri_PH1_Amps	The primary tank current in phase 1 in Amps.
LLC_iPri_PH2_Amps	The primary tank current in phase 2 in Amps.
LLC_iSec_Amps	Secondary (output) current in Amps.
LLC_vSecRef_debug_Volts	This variable allows the user to set the desired regulation voltage.
LLC_dutyBalance_pu	This variable reflects the balancing effort that the controller is using to balance the phases.
LLC_balanceOffset_debug_Amps	This variable can be used to fine tune the current balancing.

2.2.3.3.2.5 Using Realtime Emulation

1. Follow the steps in 2.2.3.1.2.5 for lab one procedure.

2.2.3.3.2.6 Run the Code

1. Refer to steps 1-6 in 2.2.3.2.2.6 from lab two to start the operation of the power stage.
2. Observe the values of *LLC_iPri_PH1_Amps* and *LLC_iPri_PH2_Amps* in the Expressions window. The sensed values here should be close to each other and should remain close to each other across loads. There will be some noise on the instantaneous values, but averaged out over time they should be nearly equal.
3. Vary the load on the power stage and observe that the tank currents remain well balanced.
4. If desired, the *LLC_balanceOffset_debug_Amps* variable can be used to either compensate for any difference between the current sense circuits allowing for fine tuning of the current balancing, or it can be used to create a small offset between the two phase currents by programming it with an arbitrary value. Creating a small offset between the phases is a good way to demonstrate the ability of the power stage to adjust the phase currents. Set *LLC_balanceOffset_debug_Amps* to a value of 0.1 and observe the offset in the sensed values of the primary tank currents.
5. Set *LLC_balanceOffset_debug_Amps* back to 0.
6. If desired, repeat lab 2, but note the imbalance between the primary tank current values in lab 2 without current balancing.
7. Turn OFF the 390-V DC power supply.
8. Fully halting the MCU when in real-time mode is a two-step process. First, halt the processor by using the *Suspend* button () on the toolbar or *Run* → *Suspend*. Click  button again to take the MCU out of real-time mode and then reset the MCU (*Run* → *Reset* → *CPU Reset*).
9. Close CCS.

End of exercise.

2.2.3.4 Lab Four: Closed-Loop Control With Current Balancing, Phase Shedding, Synchronous Rectification Threshold, and SFRA

2.2.3.4.1 Overview

The software for this lab is mostly identical to lab three, but additional phase shedding and synchronous rectification threshold logic has been added in this lab. There are no variables that need to be adjusted in the Expressions Window. The DC load is used to step through loads from 1A-15A, recording input voltage and current, as well as output voltage and current at each step. From these observations the efficiency can be computed.

The software block diagram is shown in 図 34

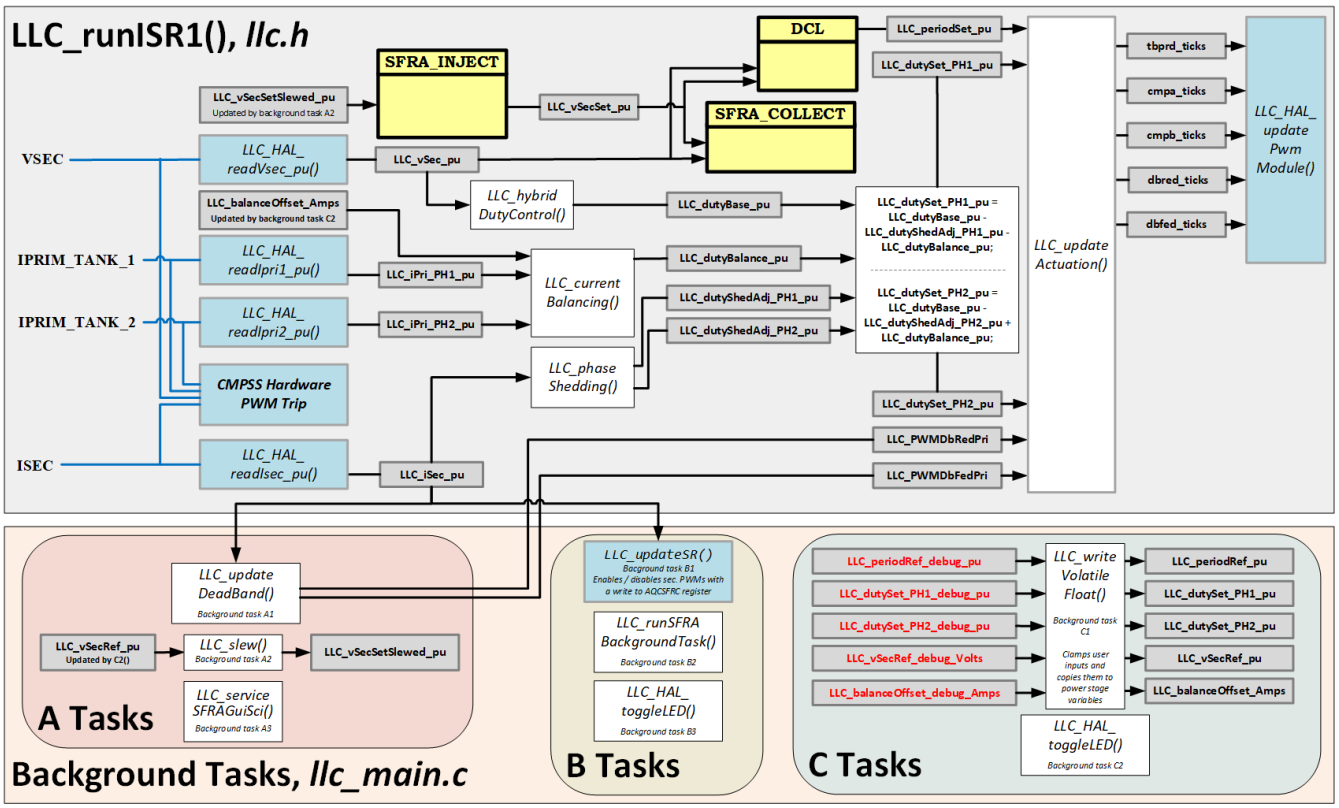

図 34. TIDM-1001 - Lab 4 software diagram

2.2.3.4.2 Procedure

The setup for this lab closely follows the setup for the previous labs.

2.2.3.4.2.1 Hardware Setup

1. Follow the steps in 2.2.3.1.2.1 for lab one procedure.

2.2.3.4.2.2 Software Setup

1. Follow steps 1-5 in 2.2.3.1.2.2 for lab one procedure to load the project and open the powerSUITE GUI.
2. Under *Project Options* select "Closed loop + current balancing + efficiency improvements".
3. Save *main.syscfg* file.

2.2.3.4.2.3 Build and Load the Project

1. Follow the steps in 2.2.3.1.2.4 for lab one procedure.

2.2.3.4.2.4 Debug Environment Windows

It is standard debug practice to watch local and global variables while debugging code. There are various methods for doing this in CCS, such as memory windows and watch windows. Additionally, CCS has the ability to make time (and frequency) domain plots, which allows the user to view waveforms using graph windows.

1. Populate the Expressions Window entries by clicking on **View → Scripting console** on the menu bar and then opening the *setupdebugenv_lab4.js* file from the project directory using the scripting console

Open File ( ) command. The Expressions Window should look like 図 35.

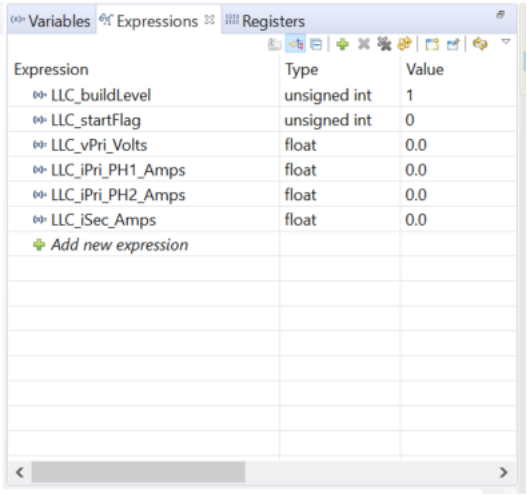

図 35. Lab Four: Expressions Window at Reset

表 7. Lab 4 Description of Expressions Window Entries

VARIABLE	DESCRIPTION
LLC_buildLevel	Shows which lab is loaded.
LLC_startFlag	Set this variable to 1 to start the power stage.
LLC_vPri_Volts	Input voltage in Volts. Only valid if jumper J15 is populated on the TIDM-1001 board.
LLC_iPri_PH1_Amps	The primary tank current in phase 1 in Amps.
LLC_iPri_PH2_Amps	The primary tank current in phase 2 in Amps.
LLC_iSec_Amps	Secondary (output) current in Amps.

2.2.3.4.2.5 Using Realtime Emulation

1. Follow the steps in 2.2.3.1.2.5 for lab one procedure.

2.2.3.4.2.6 Run the Code

1. Refer to steps 1-6 in 2.2.3.2.2.6 from lab two to start the operation of the power stage.
2. Adjust the load current to various steps in the range 1A - 15A, for each step recording the input voltage and current as well as the output current and voltage reported on the test instruments. From these measurements the efficiency can be calculated. If a power analyzer is available, the efficiency can be directly observed.
3. The efficiency will be much better for loads in the 1-10A range with the phase shedding and synchronous rectification thresholds enabled. It should be greater than 90% for all loads greater than 10% of the max load.
4. If desired, go back to lab 2 and repeat the efficiency measurements without the phase shedding and synchronous rectification thresholds enabled.
5. Turn OFF the 390-V DC power supply.
6. Fully halting the MCU when in real-time mode is a two-step process. First, halt the processor by using the *Suspend* button ( ) on the toolbar or *Run* → *Suspend*. Click button again to take the MCU out of real-time mode and then reset the MCU (*Run* → *Reset* → *CPU Reset*).
7. Close CCS.

End of exercise.

3 Testing and Results

3.1 Test Setup

図 36 shows the test setup used to validate this design. A current limited 400-V DC power supply (Agilent™ N5772A) was used to power the input. A 12-V, 600-W electronic load (Chroma 63106A) was used at the output. Simco® Aerostat XC ionizing air blower was used for air cooling when operating at loads of 30 A or higher. The following sections provide some results obtained using this board.

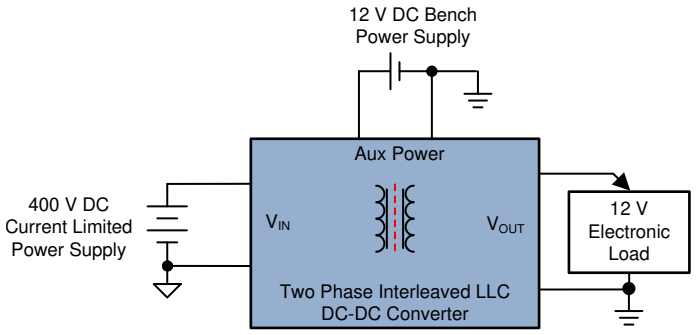

図 36. Test Setup

3.2 Test Results

3.2.1 Efficiency

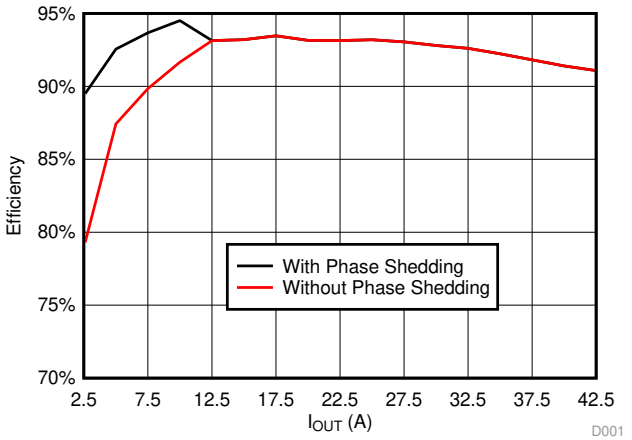

図 37. Efficiency With and Without Phase Shedding at V_{in} = 390 V_{DC}

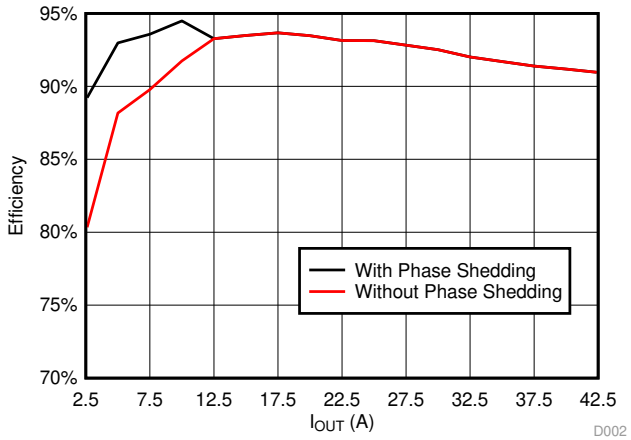

図 38. Efficiency With and Without Phase Shedding at V_{in} = 370 V_{DC}

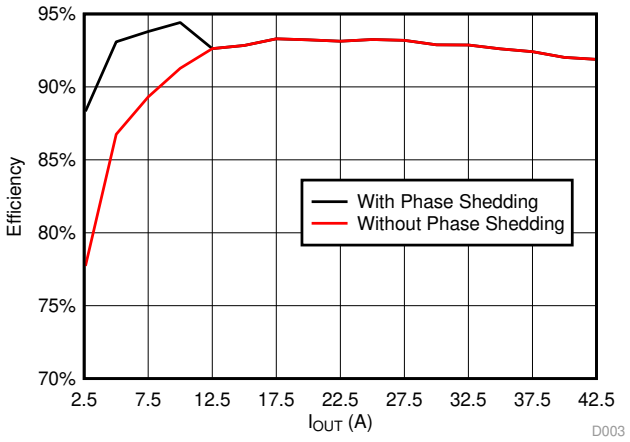

図 39. Efficiency With and Without Phase Shedding at V_{in} = 410 V_{DC}

注: For these graphs, auxiliary power is not included in efficiency calculations.

3.2.2 Load Regulation

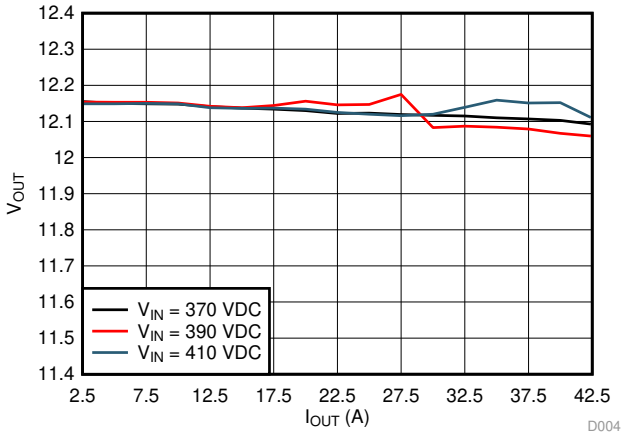

図 40. Load Regulation

3.2.3 Current Sharing

表 8 lists the average I_{tank1} and I_{tank2} values observed by the controller with and without using current sharing under different output loads. The current imbalance was calculated as the difference between resonant current in the two phases as a percentage of the resonant current in phase.

表 8. Current Sharing Between Phases(1)

Pout (W)	WITHOUT CURRENT SHARING			WITH CURRENT SHARING (DEFAULT THRESHOLDS)		
	I_{tank1} (A)	I_{tank2} (A)	Imbalance%	I_{tank1} (A)	I_{tank2} (A)	Imbalance%
26	0.61	0.63	-3.28	0.62	0.62	0.00
53	0.63	0.66	-4.76	0.646	0.651	-0.77
79	0.66	0.7	-6.06	0.67	0.67	0.00

(1) 表 8 lists the average I_{tank1} and I_{tank2} values observed by the controller with and without using current sharing under different output loads. The current imbalance was calculated as the difference between resonant current in the two phases as a percentage of the resonant current in phase one.

表 8. Current Sharing Between Phases[(1)] (continued)

105	0.69	0.72	-4.35	0.71	0.71	0.00
131	0.75	0.76	-1.33	0.76	0.76	0.00
158	0.8	0.8	0.00	0.81	0.81	0.00
184	0.87	0.85	2.30	0.87	0.87	0.00
210	0.95	0.91	4.21	0.92	0.92	0.00
236	1.01	0.94	6.93	0.98	0.98	0.00
263	1.14	0.97	14.91	1.06	1.06	0.00
289	1.22	1.02	16.39	1.14	1.14	0.00
315	1.3	1.08	16.92	1.21	1.21	0.00
341	1.41	1.15	18.44	1.28	1.28	0.00
367	1.48	1.2	18.92	1.35	1.35	0.00
394	1.54	1.27	17.53	1.41	1.41	0.00
420	1.61	1.33	17.39	1.47	1.47	0.00

図 41 and 図 42 show scope shots of current sharing between phases at I_{out} = 15 A and V_{in} = 390 V_{DC}.

- Channel one = Phase one SRA
- Channel two = Phase one I_r (I_{pri-1} or I_{tank1})
- Channel three = Phase two I_r (I_{pri-2}or I_{tank2})
- Channel four = Phase two V_r

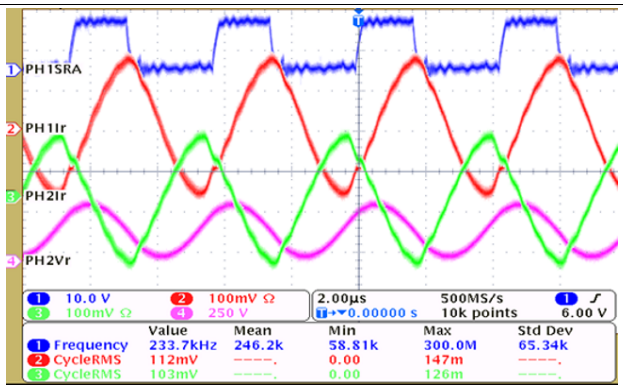

図 41. I_{tank1}(RMS) = 1.12 A, I_{tank2}(RMS) = 1.03 A (Without Current Sharing)

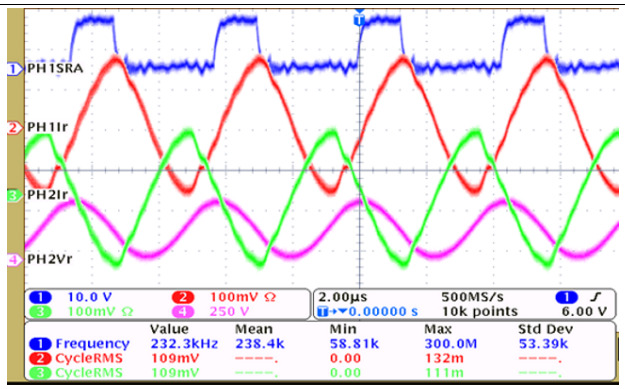

図 42. I_{tank1}(RMS) = 1.09 A, I_{tank2}(RMS) = 1.09 A (With Current Sharing)

図 43 and 図 44 show scope shots of current sharing between phases at I_{out} = 25 A and V_{in} = 390 V_{DC}.

- Channel one = Phase one SRA
- Channel two = Phase one I_r (I_{pri-1} or I_{tank1})
- Channel three = Phase two I_r (I_{pri-2}or I_{tank2})
- Channel four = Phase two V_r

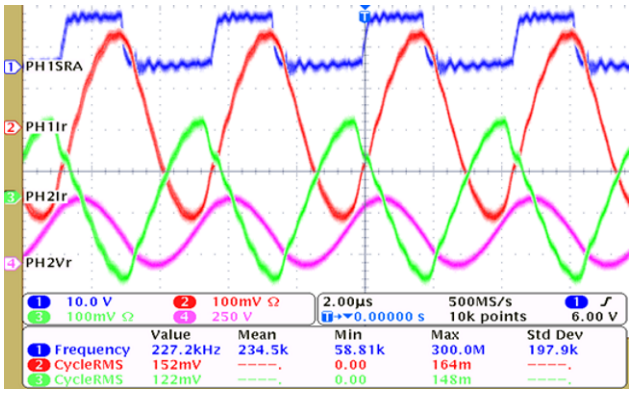

図 43. I_{tank1}(RMS) = 1.52 A, I_{tank2}(RMS) = 1.22 A (Without Current Sharing)

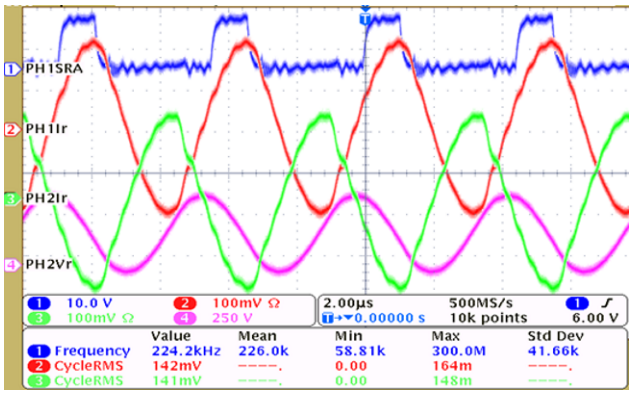

図 44. I_{tank1}(RMS) = 1.42 A, I_{tank2}(RMS) = 1.41 A (With Current Sharing)

図 45 and 図 46 show scope shots of current sharing between phases at I_{out} = 30 A and V_{in} = 390 V_{DC}.

- Channel one = Phase one SRA
- Channel two = Phase one I_r (I_{pri-1} or I_{tank1})
- Channel three = Phase two I_r (I_{pri-2} or I_{tank2})
- Channel four = Phase two V_r

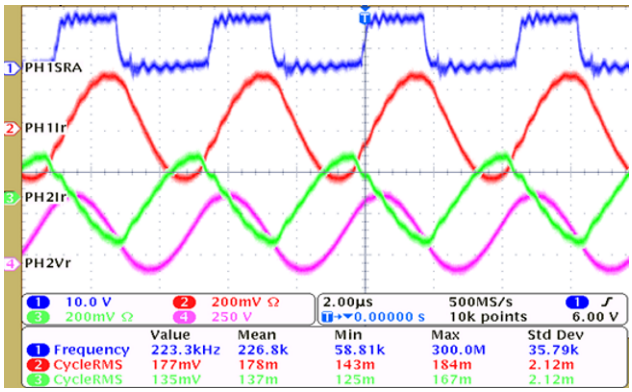

図 45. I_{tank1}(RMS) = 1.77 A, I_{tank2}(RMS) = 1.35 A (Without Current Sharing)

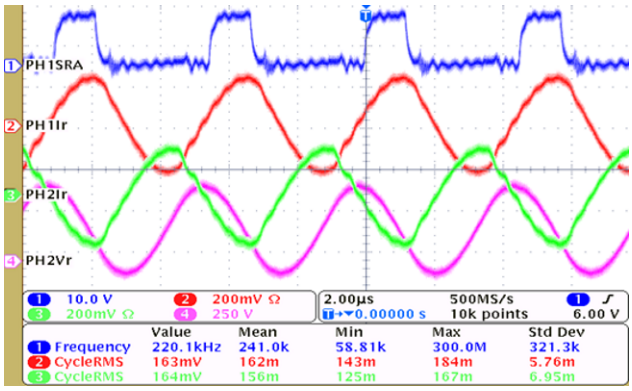

図 46. I_{tank1}(RMS) = 1.63 A, I_{tank2}(RMS) = 1.64 A (With Current Sharing)

図 47 and 図 48 show scope shots of current sharing between phases at I_{out} = 35 A and V_{in} = 390 V_{DC}.

- Channel one = Phase one SRA
- Channel two = Phase one I_r (I_{pri-1} or I_{tank1})
- Channel three = Phase two I_r (I_{pri-2} or I_{tank2})
- Channel four = Phase two V_r

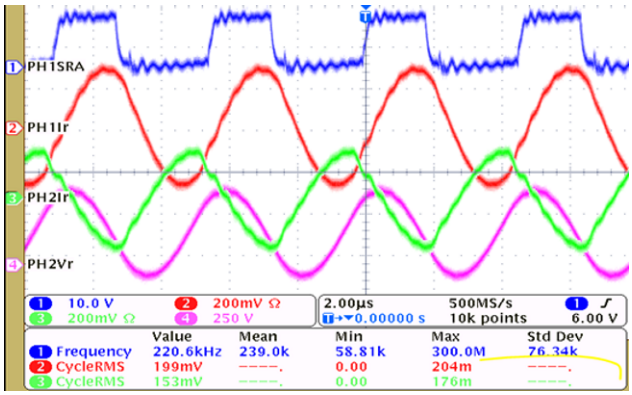

図 47. I_{tank1}(RMS) = 1.99 A, I_{tank2}(RMS) = 1.53 A (Without Current Sharing)

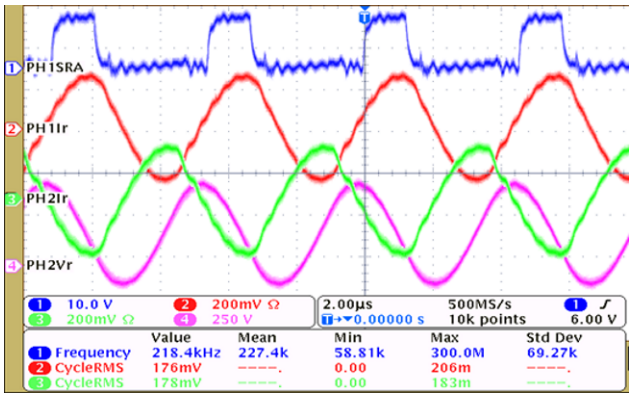

図 48. I_{tank1}(RMS) = 1.76 A, I_{tank2}(RMS) = 1.78 A (With Current Sharing)

The two resonant tank inductors (L1 and L2) are the hottest components on the board. Without any current sharing between phases, the inductor in the phase that carries more current heats up more. As a result recording thermal temperatures of these inductors under different operating conditions provides an indication of the effectiveness of the current sharing scheme. In these tests phase one seemed to contribute more to the load current than phase two. As a result phase one inductor (L1) recorded a higher temperature than L2 when current sharing was not implemented. With current sharing these inductors recorded very similar temperatures. This is clear in the following few thermal images of the board looking from the 12-V output and looking towards the 390-V input. Following thermal images were captured with the two inductors sitting on top of the corresponding transformer. No external cooling was used.

図 49 and 図 50 show thermal images at I_{out} = 25 A and V_{in} = 390 V_{DC}.

図 49. Without Current Sharing

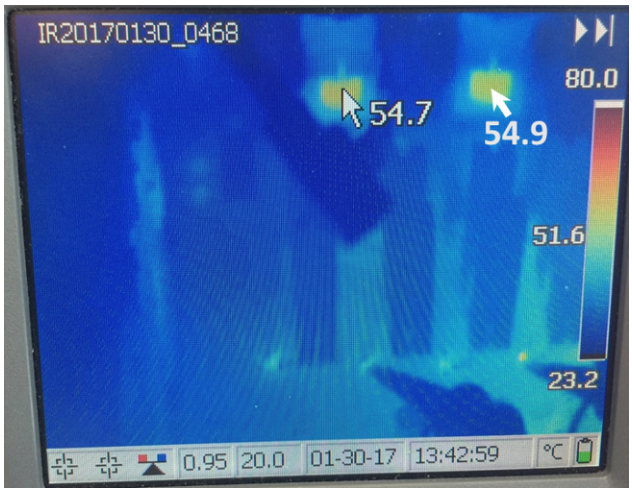

図 50. With Current Sharing

図 51 and 図 52 show thermal images at I_{out} = 30 A and V_{in} = 390 V_{DC}.

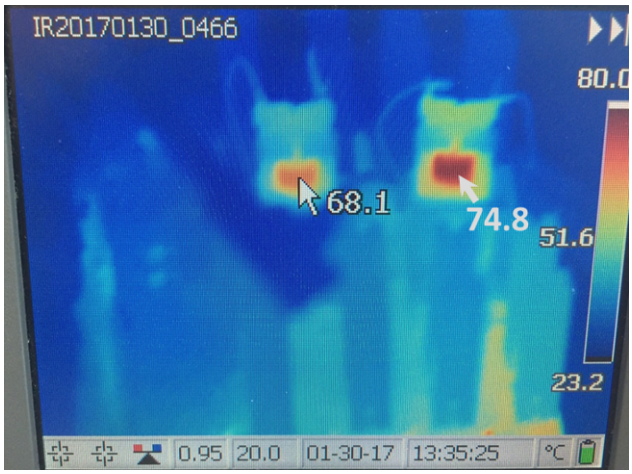

図 51. Without Current Sharing

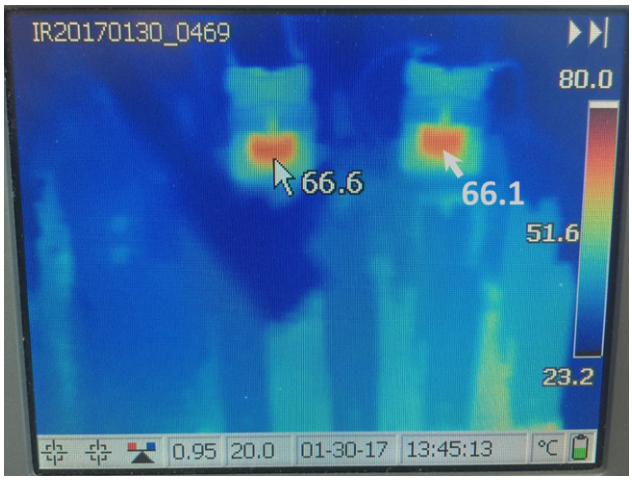

図 52. With Current Sharing

3.2.4 Output Ramp-Up (Soft-Start)

図 53 through 図 56 show the output ramp-up (soft-start) at approximately 920 ms (programmable) at V_{in} = 390 V_{DC}.

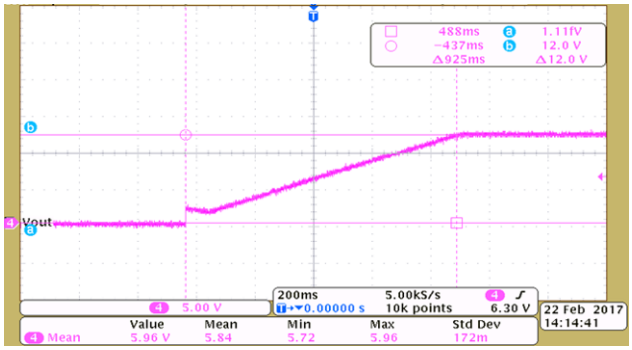

図 53. I_{out} = 0 A (No Load)

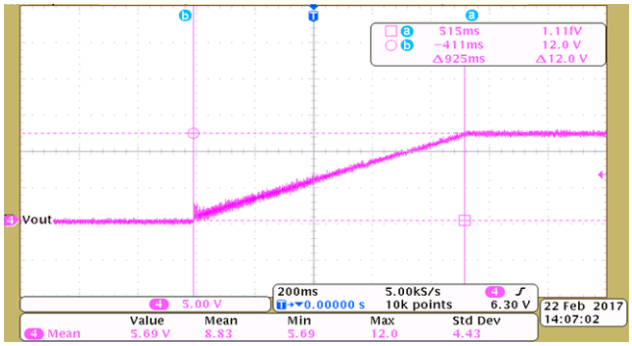

図 54. I_{out} = 10 A

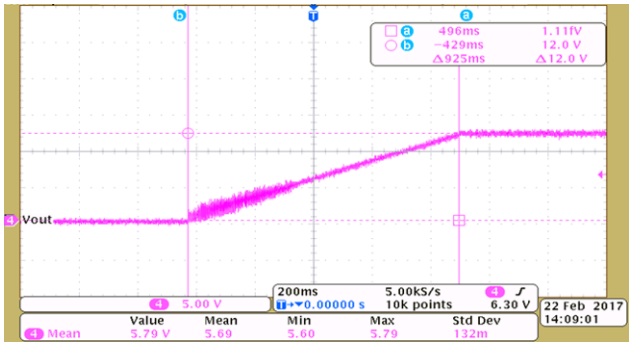

図 55. I_{out} = 25 A

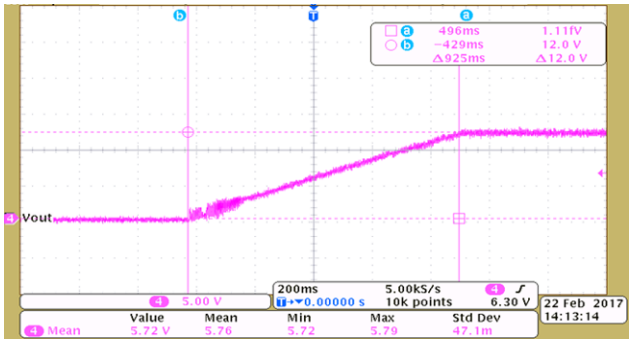

図 56. I_{out} = 42.5 A

3.2.5 Zero Voltage Switching (ZVS)

図 57 through 図 60 show ZVS on primary switches at V_{in} = 390V_{DC} where channel one = low-side switch gate to source and channel two = low-side switch drain to source.

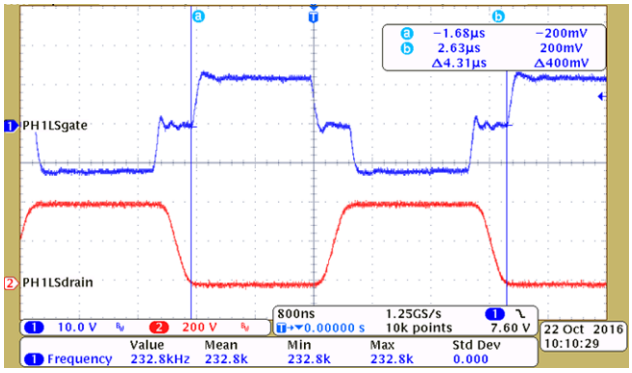

図 57. Phase One Low-Side Switch at I_{out} = 5 A

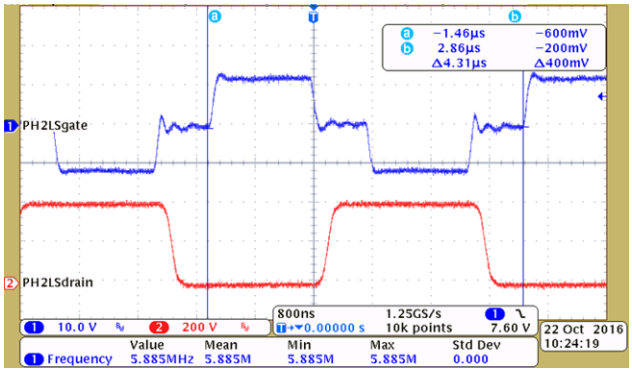

図 58. Phase Two Low-Side Switch at I_{out} = 5 A,

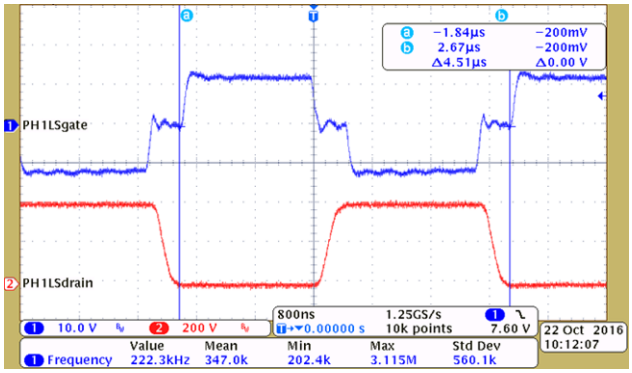

図 59. Phase One Low-Side Switch at I_{out} = 35 A

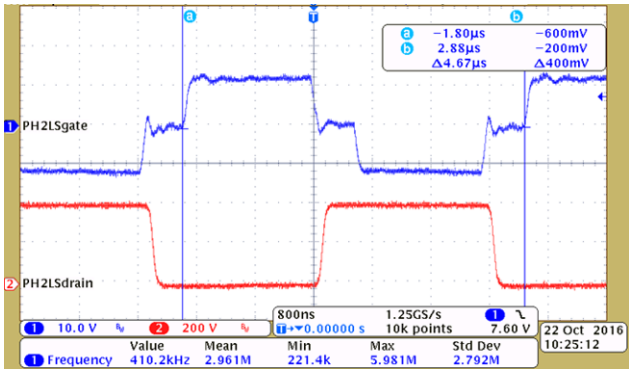

図 60. Phase Two Low-Side Switch at I_{out}= 35 A

3.2.6 Load Transients

図 61 and 図 62 show load transients at V_{in} = 390 V_{DC} with phase shedding enabled where channel four = output voltage (V_{out}) and channel three = output current (I_{out})/2.

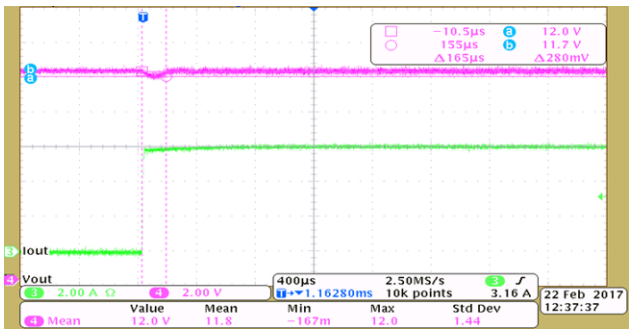

図 61. I_{out} = 0-A to 12-A Transition

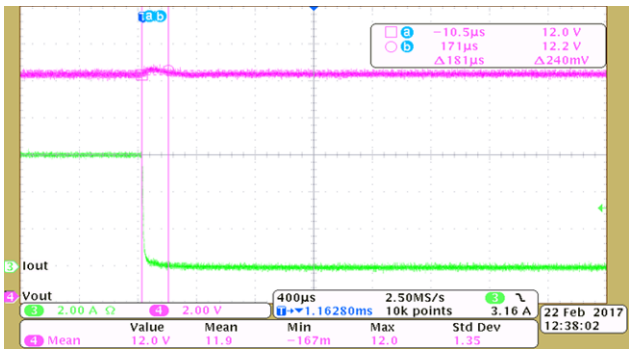

図 62. I_{out} = 12-A to 0-A Transition

図 63 and 図 64 show load transients at V_{in} = 390 V_{DC} with phase shedding enabled where channel four = output voltage (V_{out}) and channel three = output current (I_{out})/2.

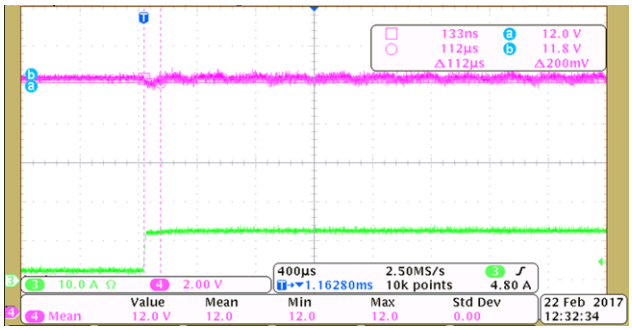

図 63. I_{out} = 5-A to 25-A Transition

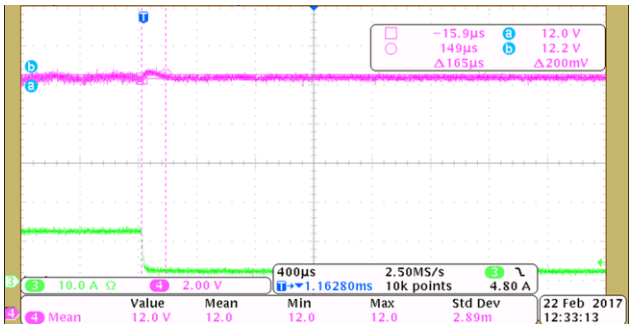

図 64. I_{out} = 25-A to 5-A Transition

図 65 and 図 66 show load transients at V_{in} = 390 V_{DC} with phase shedding enabled where channel four = output voltage (V_{out}) and channel three = output current (I_{out})/2.

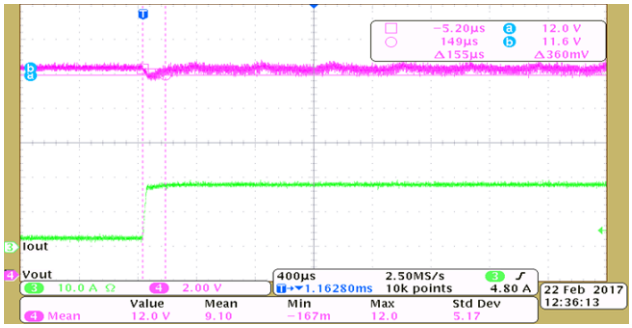

図 65. I_{out} = 5-A to 35-A Transition

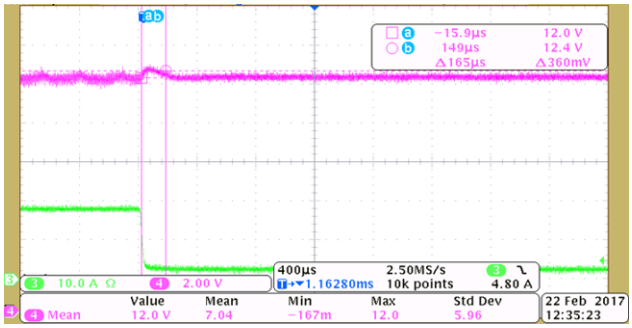

図 66. I_{out} = 35-A to 5-A Transition

3.2.7 Phase Shedding During Load Transients

図 67 and 図 68 show phase one disabled and re-enabled during load transients at V_{in} = 390 V_{DC} where channel one = phase one high-side PWM, channel two = phase two high-side PWM, channel three = output current (I_{out})/2, and channel four = output voltage (V_{out}).

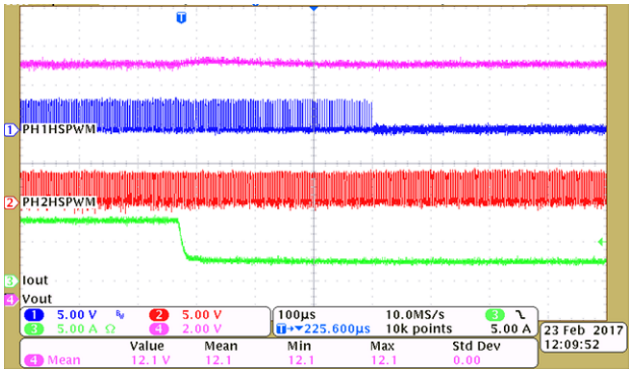

図 67. Phase One Disabled During I_{out} = 15-A to 5-A Transition

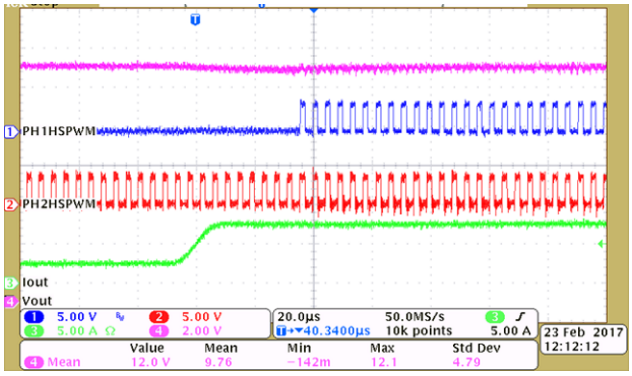

図 68. Phase One Re-enabled During I_{out} = 5-A to 15-A Transition

図 69 and 図 70 show phase two disabled and re-enabled during load transients at V_{in} = 390 V_{DC} where channel one = phase one high-side PWM, channel two = phase two high-side PWM, channel three = output current (I_{out})/2, and channel four = output voltage (V_{out}).

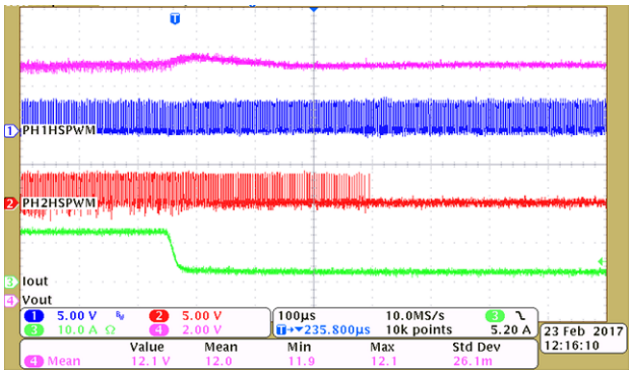

図 69. Phase Two Disabled During I_{out} = 25-A to 5-A Transition

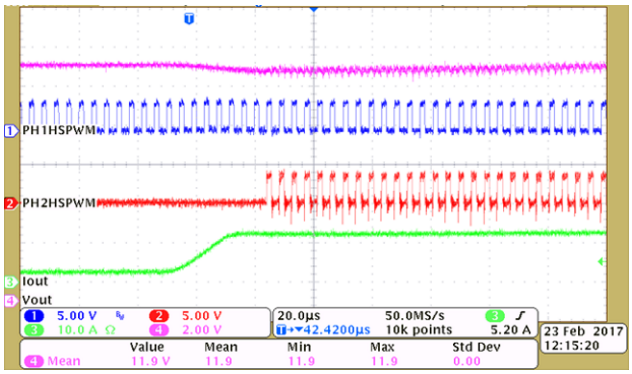

図 70. Phase Two Re-enabled During I_{out} = 5-A to 25-A Transition

3.2.8 SR Enable and Disable During Load Transients

図 71 and 図 72 show SR disabled and re-enabled during load transients at V_{in} = 390 V_{DC} where channel one = phase one SRA PWM, channel two = phase two SRA PWM, channel three = output current (I_{out})/2, and channel four = output voltage (V_{out}).

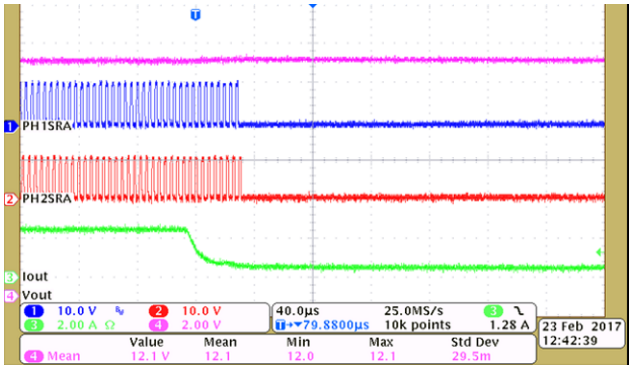

図 71. SR Disabled During I_{out} = 5-A to 1-A Transition

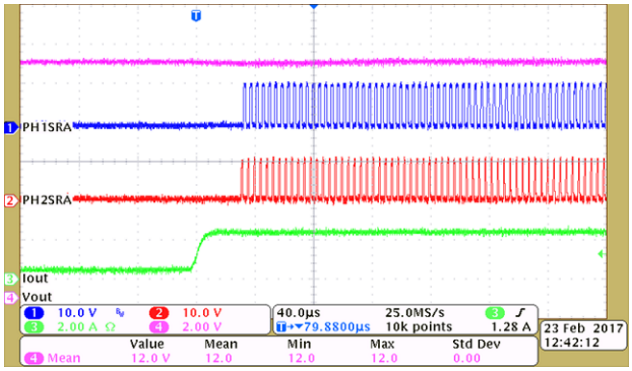

図 72. SR Re-enabled During I_{out} = 1-A to 5-A Transition

4 Adapting This Reference Design

After this reference design has been evaluated, use the Solution Adapter tool to adapt this solution to run on a custom digital power supply that uses the same topology and similar resources.

1. To do this start with a new CCS workspace. Open **Resource Explorer** and navigate to Software > **C2000Ware_DigitalPower_SDK** > **powerSUITE** > **Solution Adapter**. Click *DC-DC:* TIDM-1001.
2. On the next screen, click the **Interleaved LLC DC-DC : F280025C option.**
3. Specify a destination location for the project, and click *OK*. The *main.syscfg* file should open. The resource mapping can be changed for different ADC inputs and PWM outputs to match a custom design. These pin mappings are in the llc_user_settings.h file. The voltage and current scaling and other power stage parameters can also be changed to match a custom design from the powerSUITE GUI.
4. This allows quickly adapting the TI software without having to write code. The steps outlined in the previous sections may be used to incrementally test a custom design.
5. If further code customization is required than what is possible with main.syscfg, different source files (llc_main.c, llc_user_settings.h, and so forth) may need to be modified.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDM-1001.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-1001.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDM-1001.

5.4 Altium Project

To download the Altium project files, see the design files at TIDM-1001.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDM-1001.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-1001.

6 Software Files

To download the software files, see the design files at TIDM-1001.

7 Related Documentation

1. Texas Instruments, *LLC Converter Small Signal Modeling*, SEM2100 Technical White Paper (SLUP329)
2. STMicroelectronics,*An introduction to LLC resonant half-bridge converter*, Application Report (AN2644), 2008
3. Texas Instruments, *C2000 Resonant DC/DC Developer's Kit*, TMDSRESDCKIT Tools Folder
4. Orietti, E., P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari. *Two-phase interleaved LLC resonant converter with current-controlled inductor*. 2009 Brazilian Power Electronics Conference, 2009. doi:10.1109/cobep.2009.5347671.
5. Hu, Zhiyuan, Yajie Qiu, Laili Wang, and Yan-Fei Liu. *An Interleaved LLC Resonant Converter Operating at Constant Switching Frequency*. IEEE Transactions on Power Electronics 29, no. 6 (2014): 2931-943. doi:10.1109/tpel.2013.2273939.
6. Chen, Hui, Xinke Wu, Fangzheng Peng, Zhaoming Qian, and Changsheng Hu. *Current balance method for the two-phase interleaved LLC-RDCX with parallel PWM output regulation*. 2014 International Power Electronics and Application Conference and Exposition, 2014. doi:10.1109/peac.2014.7037843.
7. Texas Instruments, *C2000 DPSWorkshop*, Wiki Page
8. Texas Instruments, *powerSUITE - Digital Power Supply Design Software Tools for C2000™ MCUs*, powerSUITE Tools Folder
9. Texas Instruments, *C2000™ 32-bit microcontrollers*, Microcontrollers (MCU) Overview

7.1 商標

E2E is a trademark of Texas Instruments.
Code Composer Studio is a trademark of Texas Instruments, Inc..
Agilent is a trademark of Agilent Technologies, Inc..
Simco is a registered trademark of Simco Electronics.

8 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and nonconductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年3月発行のものから更新 **Page**

- ドキュメント全体で *TI Design* をリファレンス・デザインに 変更 1
- ドキュメント全体で *TMS320F28379* を *TMS320F280025C* に 変更 1
- *controlSUITE* を *Digital Power SDK* に 変更 1
- 「...および入力低電圧 / 過電圧」を 削除 1
- *Delfine* to *Third Generation* 変更 4
- *Four independent 16-bit...* to *Two independent 12-bit...* 変更 4
- The duty can be reduced all the way to 0% if necessary, putting the PWM module into a burst mode. 追加 14
- *CMPSS2* to *CMPSS4* 変更 16
- ...for the transformer high voltage winding current for each phase... 削除 16
- *CMPSS5* to *CMPSS2* 変更 16
- Output overvoltage protection is implemented using on-chip analog comparator 3. 追加 16
- ...or voltage 追加 16
- Output overvoltage protection is implemented in the software inside the state machine task A1. Whenever an output overvoltage is detected, a one-shot trip action is initiated on ePWM1, ePWM2, ePWM4, and ePWM5. 削除 16
- The software also sets the system fault LEF under these fault conditions. Input undervoltage and overvoltage protection are implemented in the software inside the slower state machine task C2. These conditions disable LLC operation and all PWMs are held in low state. LLC operation and the PWMs are re-enabled once the input comes back within programmed limits and stays good for a programmable time interval. 削除 16
- *ADC-C2* to *CMPSS3* 変更 18
- Vout, Heavily filtered output voltage feedback, ADC-A8 追加 18
- *ADC-C4/CMPSS6* to *CMPSS2* 変更 18
- *ADC-B0* to *ADC-CO* 変更 18
- *ADC-A2/CMPSS1* /to *CMPSS1* 変更 18
- *ADC-A4/CMPSS2*to *CMPSS4* 変更 18
- *ADC-C0* to *ADC-C8* 変更 18
- ...consists of two components, both... 削除 24
- The Fast Update ISR portion is triggered by the master swiitching PWM (phase one HB driver PWM) which is only executed when there is a change in frequency or when a sysem comment requires a fast update. 削除 24
- A PID controller is included as an option. Only the PI coefficients can be designed with Compensation Designer, but a user defined set of coefficients is defined in llc_user_settings.h and can be used to define a manually tuned PID controller. The *PID Controller Tuning Guide* provided in the documentation for the *Digital Control Library* provides guidance that can be used for this process. 追加 25
- *HV2PHILLLC-Main.c* to *llc_main.c* 変更 26
- Driver code for the TMS320F280025C device is in llc_hal.c / llc_hal.h files. The llc.c / llc.h files have all the... 追加 26
- This file is the brains behind the application and contains all time crtical... 削除 26
- time-critical 追加 26
- ..., as well as the other code specific to the powerstage including phase shedding, current balancing, and SR enable / disable. User configurable settings for the project are included in the llc_user_settings.h file. The llc_settings.h file is automatically generated by the powerSUITE GUI and if developing with powerSUITE enabled, any modifications to llc_settings.h will be overwritten when the project is built. 追加 26
- Table 3. Software Library Modules 削除 26
- Although a two-pole,two-zero controller is used, the controller could very well be a PI , PID, a three-pole three-zero, or any other controller that can be suitably implemented for this application. 削除 26
- *Incremental Builds* to *Incremental Labs* 変更 26
- *...two incremental builds...* to *four incremental labs...* 変更 26
- *...shows the incremental build options. To select a particular built option in main.cfg...* to *...shows the lab options. To select a particular lab, select the corresponding project option in main.syscfg* 変更 26
- *build* to *lab* 変更 26
- Table 3. *Incremental Build Options* to *Incremental Lab Options* 変更 26
- *INCR_BUILD* to *LLC_Lab* 変更 26
- LLC_LAB = 3, LLC-LAB = 4 rows to the table 追加 26

- *Procedure for Running the Incremental Builds* to *Procedure for Running the Incremental Labs* 変更 27
- *version 6.1* to *version 9.3* 変更 27
- *Build* to *Lab* 変更 28
- ...shows the software block diagram for lab 1. 追加 28
- image 変更 29
- *...main.cfg* to *...lc_user_settings.h* 変更 29
- *...Variable Period* to *LLC_periodReg_debug_pu* 変更 29
- *...ISR funtion Update Regs* to *LLC_run/SR1().* 変更 29
- ...by using the variable Period_Set. 削除 29
- *main.cfg* to *llc_user_settings_h* 変更 29
- *CMPSSs 1, 2, and 5* to *CMPSSs 1, 2, 3, and 4* 変更 29
- *...can be set using the GUI_Lpri1tripSet, Gui_lpri2tripSetvariables* to *are defined in the llc_settings.h file: LLC_IPRI1_TRIP_AMPS, LLC_IPRI2_TRIP_AMPS, LLC_ISEC_TRIP_AMPS, LLC_VSEC_TRIP_VOLTS. These define statements set the trip configurations for phase 1 primary current, phase 2 primary current, secondary (output) current, and secondary voltage respectively. The values can be adjusted in the powerSUITE GUI.* 変更 29
- *...Period_Set_pu* to *LLC_periodSet_pu* 変更 29
- *The DPL_ISR_wFRA_ISR is triggered by the master PWM module(PWM1). This ISR is where the control code and digital power library modules are executed.* to *The control ISR is triggered by a spare PWM module at a rate of 50 KHz, but the project supports increasing the control frequency up to 100 KHz.* 変更 29
- *CCS version 6.1* to *CCS version 9.3* 変更 31
- *controlSuite, and CCS GUI composer* to *Digital Power SDK, and CCS SysConfig utility* 変更 31
- *18-pin connectors J3 and J4* to *120-pin connector J3.* 変更 31
- *version 6.1* to *version 9.3* 変更 31
- *A project contains all the files and build options required to develop an executable output file (.out), which can be run on the MCR hardware. On the menu bar click Projet > Import CCS Project. Below the root directory, navigate to and select ..controlSUITE development kits directory. Make sure that below the Projects tab, HVsPHILLLC is selected...* to On the menu bar click **Project** >**Import CCS Project**. Below the root directory, navigate to and select *..\C2000Ware_DigitalPower_SDK_X_XX_XX_XX\solutions\tidm_1001\f28002x\llc* directory. Make sure that below the **Projects** tab, 2PH_IL_LLC_F28002x is selected. 変更 31
- *HV2PHILLLC project should now appear in the CCS Project Explorer window. This project will invoke all the necessary tools (compiler, assembler, and linker) to builg the project. A project contains all the files and build options required to develop an executable output file (.out), which can be run on the MCU hardware* to *2PH_IL_LLC_F28002x project should now appear in the CCS Project Explorer window. This project will invoke all the necessary tools (compiler, assembler, and linker) to build the project. A project contains all the files and build options required to develop an executable output file (.out), which can be run on the MCU hardware.* 変更 31
- *Open main.cfg file by double clicking on the...* to *If not already open, double click the main.sysconfig fi...* 変更 31
- *main.cfg* to *main.syscfg* 変更 32
- Note that the default software does not allow phase shedding in this build regardless of this selection in the main.cfg. 削除 32
- *Build One: main.cfg* to *Lab One: main.syscfg* 変更 32
- *build* to *lab* 変更 32
- ...build one 削除 32
- *AddWatchWindowVars.js* to *setupdebugenv_lab1.js* 変更 33
- *Build One* to *Lab One* 変更 33
- data in entireTable 4 変更 33
- *Period_Set* to *LLC_periodSet_pu* 変更 34
- *250_kHz* to *350-kHz* 変更 34
- (resonent frequenty) 削除 34
- Verify that all of the sensed values are updating in the expressions window: *LLC_vPri_Volts*, *LLC_iPri_PH1_Amps*, *LLC_iPri_PH2_Amps*, *LLC_iSec_Amps*. 追加 34
- Period_Set 削除 34
- *0.0* to *0.57* and *0.95* to *1.00* 変更 34
- Period_Set has been restricted to a maximum value of 0.95 in this build. 削除 34
- The LLC_dutySet_PH1_debug_pu, and LLC_dutySet_PH2_debug_pu variables are initialized to 0.99, but they may be set to values between 0.05 and 0.99. An oscilloscope may be used to observe the changing duty cycle for the switch waveforms. 追加 34
- ...shows the Expressions Window that corresponds to the operatoin of the system when Period_Set is 0.8. Period_Set -

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