Design Guide: TIDEP-01025 mmWave 診断およびモニタリング・リファレンス・デザイン

TEXAS INSTRUMENTS

概要

TIDEP-01025 は、ミリ波レーダー・センサが内蔵している 自律型の監視機能を提示します。これらの機能を活用す ると、ホスト側の処理負荷を最小化し、システムの効率を改 善することができます。このリファレンス・デザインは、プロ グラマブル・デジタル・コア、ペリフェラル、メモリの診断テ ストを実行するため、安全診断ライブラリ (SDL)を使って います。また、このリファレンス・デザインは、さまざまなハ ードウェア・コンポーネントが搭載している RF およびアナ ログ向けの監視機能を構成し、有効にします。このリファレ ンス・デザインは、さまざまな安全性リソースを活用して ASIL-B/SIL2 準拠の製品の実装を進めている開発ユー ザーを支援し、全体の開発期間および市場出荷までの期 間の短縮に貢献します。

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特長

- ミリ波レーダー・センサの内蔵診断機能と監視機能の 使用方法を提示し、システムの性能や信頼性の向上 に貢献
- 安全性リソースを使用することで、さまざまなデバイス やアプリケーションで ASIL-B/SIL2 準拠のミリ波センサ を活用でき、システムの実装効率が向上
- 実績のある EVM ハードウェア設計を基礎とし、短期間 での市場投入を実現

アプリケーション

- 長距離レーダー
- 中距離 / 短距離レーダー
- 超近距離レーダ
- 物体検出センサ
- ・ 車両の乗員検出センサ
- ドライバーのバイタルサイン監視
- 産業用および協働ロボットのレーダーによるセンシング
- 安全保護





1 System Description

The TIDEP-01025 provides a reference for creating a diagnostic and monitoring application using TI's AWR1843, AWR6843 and IWR6843 based on 77/60 GHz mmWave radio-frequency complementary metal-oxide semiconductor (RF-CMOS) technology. mmWave sensing technology detects vehicles, such as cars, motorcycles, and bicycles, at extended ranges regardless of environmental conditions, such as rain, fog, or dust. TI's mmWave sensing devices integrate a 76-81GHz/60-64GHz mmWave radar front end with ARM® microcontroller (MCU) and TI DSP cores for single-chip systems.

TI mmWave SOC has built in circuits for diagnostic and monitoring which enables the detection of both the systematic and random faults. These safety mechanisms significantly reduce system complexity and cost in safety critical applications. It is important to test these diagnostic mechanisms using SafeTI diagnostic Library (SDL).

TI's radar mmWave integrated chips (ICs) include hardware and firmware elements to enable monitoring of its mmWave analog and digital subsystems. These built-in features of RadarSS are exposed to application through firmware APIs.

This reference design demonstrates the usage of Inbuilt diagnostic and monitoring functionality of mmWave Radar Sensor. The design provides a list of required hardware, schematics, and reference software to quickly begin ASIL-B/SIL2 compliance product development. This reference design describes the example usage case as well as the design principle, implementation details, and engineering tradeoffs made in the development of this application. High-level instructions for replicating the design are provided. Here are few key diagnostic features of device:

STC, PBIST/LBIST, ECC, MPU, PARITY on miscellaneous memories and or peripheral. The details are covered in Safety Manual.

Note Further in this document *mmWave Sensor* implies to AWR1843, AWR6843, IWR6843 and *EVM* implies to AWR1843BOOST, AWR6843ISK, IWR6843ISK unless otherwise mentioned.

2 System Overview

TI's radar mmWave integrated chips (ICs) include hardware and firmware elements to enable monitoring of its mmWave, analog and digital sections. Most of digital elements of device have built in diagnostic capability.



図 2-1. mmWave Sensor Monitor & Diagnostic

Analog Subsystem contains the RF and Analog functionality of the device. It has two/three transmitters and four Receiver chains along with the Clock oscillator and FMCW signal generation circuitry (Cleanup APLL, Synthesizer, frequency multipliers etc.). Radar Subsystem is responsible for initializing and calibrating the Analog/RF modules. Also it periodically monitors the Analog/RF functionality to ensure all the Analog/RF modules work in their defined limits. This functionality can be configured through mmwavelink Monitoring APIs by MSS/DSS application with various mode and reporting options.

TOP, Master, and DSP subsystem contain various memory and digital components which have safety diagnostic features. These features can be configured and verified using Safety Diagnostic Library to manage both systematic and random faults of the device.



☑ 2-2 shows all the safety components of mmwave sensor device, which might differ for different device variants.



図 2-2. mmWave Safety Components

Note Refer to the mmWave Sensor Safety Manual for detailed information on these safety features.

2.1 Block Diagram



図 2-3. TIDEP-01025 Block Diagram

2.2 Design Considerations

This reference design showcases the usage of Diagnostic and Monitoring feature. Diagnostic tests are implemented through Safety Diagnostic Library (SDL) whereas Monitoring features are enabled on RadarSS through mmWaveLink library. Few sets of Diagnostic tests are destructive which might cause device soft and or warm reset, so within this reference design those tests are part of Secondary Bootloader (SBL). This way main application flow doesn't get hampered due to these destructive Diagnostic tests execution. Apart from these



DIAG tests, remaining DIAG are executed on MSS as well DSS core during the application initialization. Further details of implementation are available in セクション 2.4.2

2.3 Highlighted Products

2.3.1 LP8770

The LP87702-Q1 helps meet the power management requirements of the latest platforms, particularly in automotive radar and camera and industrial radar applications. The device contains two step-down DC/DC converters, and a 5-V boost converter/bypass switch. To support safety critical applications. the device integrates two voltage monitoring inputs for external power supplies, and a window watchdog.

LP8770 Features

- AEC-Q100 Qualified for Automotive Applications:
 - Device Temperature Grade 1: -40°C to +125°C, TA
- FMEDA and Functional Safety Manual available to support your ASIL compliant system designs
- Two Inputs for External Voltage Monitoring
- Two Programmable Power-Good Signals
- Dedicated Reference Voltage for Diagnostics
- Window Watchdog With Reset Output
- External Clock Input to Synchronize Switching
- Spread-Spectrum Modulation
- Programmable Start-up and Shutdown Delays and Sequencing With Enable Signal
- Two High-Efficiency Step-Down DC/DC converters:
 - Maximum Output Current 3.5 A
 - 2-MHz, 3-MHz, or 4-MHz Switching Frequency
 - Auto PWM/PFM and Forced-PWM Operations
 - Output Voltage = 0.7 V to 3.36 V
- 5-V Boost Converter With Bypass-Mode Option:
 - Maximum Output Current 600 mA
- Configurable General Purpose Outputs (GPOs)
- I2C-Compatible Interface Supporting Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes

LP87702-Q1 features include diagnostics, monitoring and protections for both device internal and system level operation:

- Soft start
- Input undervoltage lockout
- Programmable undervoltage or window (over- and undervoltage) monitoring for the input (from VANA pin)
- Programmable undervoltage or window (over- and undervoltage) monitoring for the buck and boost converter outputs
- Two inputs (VMONx) with programmable undervoltage or window (over- and undervoltage) thresholds, for monitoring external rails in the system
- One dedicated power-good output (PG0) to which selected monitoring signals can be combined
- Second programmable power-good output (PG1), multiplexed with general purpose output (GPO1)
- Power good flags with maskable interrupt
- Programmable window watchdog
- Buck and boost converter overload detection
- Thermal warning with two selectable thresholds
- Thermal shutdown

2.3.1.1 Safety Features

LP8770 supports the following safety features.

2.3.1.1.1 Window Watchdog

WDI is the watchdog function input pin and WD_RESET is the reset output. WDI pin needs to be pulsed within a certain timing window to avoid watchdog expiration. Minimum pulse width is 100 μ s. Watchdog expiration always



causes a reset pulse at WD_RESET output, otherwise device behavior after watchdog expiration is programmable.

Long open, close and open window periods are independently programmable. When long open or open window expires before WDI input is received, watchdog enters WD Reset state. Also when WDI is received during close window, watchdog enters WD Reset. Long open period can be extended by a I2C write to WD_CTRL_1 or WD_CTRL_2 register.

2.3.1.1.2 Voltage Monitoring

The LP87702-Q1 device has programmable voltage monitoring for the BUCKx and BOOST converter output voltages and for VANA, VMON1 and VMON2 inputs. Monitoring of each signal is independently enabled in PGOOD_CTRL register. Voltage monitoring can be under-voltage monitoring only (PGOOD_WINDOW = 0) or

overvoltage and undervoltage monitoring (PGOOD_WINDOW = 1). This selection is common for all enabled monitoring. Enabled monitoring signals are combined to generate power-good (PG0, PG1) and/or interrupts as described in *Power-Good Information to Interrupt and PG0 and PG1 Pins*. Monitoring comparators have a dedicated reference and bias block, which is independent of the main reference and bias block.

In the AWR1843Boost EVM, the LP87702-Q1 handles the Voltage monitoring and has capability to enable the watchdog.

- There are 2 Voltage monitors in LP8770. These are used to monitor 1.24-V rail and 1.8-V rail after the LC filter.
- The 1.0V derived from LDO (TPS7A53) whose input is 1.24-V is monitored using GPADC in AWR.
- WDI pin of the LP87702-Q1 is connected to a GPIO(x) of the AWR and this GPIO is used to feed the watchdog at appropriate intervals by the application software.
- The WD_RESET + PowerGood +GPIO0 pin of the LP87702-Q1 is connected to NRST of the AWR1843.
- The NERROR of the AWR1843 should be connected to the Reset of the CAN Transceiver.
- GPADC of the AWR1843 can be used to monitor the 1-V Power rail.

Watch needs to be enabled by writing into the WatchDog register in LP87702Q1 via I2C. For the watchdog operation the application firmware needs to generate a pulse every Window period on the GPIO(x). The recommended way to generate a pulse is to time the application and generate a pulse at appropriate points from the application in AWR1843. We do not recommend to use any timers in 1843 to generate this watchdog pulse.

2.3.2 AWR1843/xWR6843 mmWave Sensor Solution

The mmWave Sensor is an integrated single-chip, frequency modulated continuous wave (FMCW) sensor capable of operation in the 76-81GHz (AWR1843) or 60-64GHz (xWR6843) frequency band. The device is built with TI's low-power, 45-nm RFCMOS processor and enables unprecedented levels of analog and digital integration in an extremely small form factor. The device has four receivers and three transmitters with a closed-loop phase-locked loop (PLL) for precise and linear chirp synthesis. e

The sensor includes a built-in radio processor (BIST) for RF calibration and safety monitoring. Based on complex baseband architecture, the sensor device supports an IF bandwidth of 10 MHz with reconfigurable output sampling rates. The presence of ARM[®] Cortex[®] R4F and Texas Instruments C674x Digital Signal Processor (DSP) (fixed and floating point) along with 2MB (AWR1843) / 1.7MB (xWR6843) of on-chip RAM enables high-level algorithm development. This device is ASIL-B (automotive) or SIL-2 (industrial) targeted and an ideal solution for low power, self-monitored, ultra-accurate radar systems in the automotive space.

2.4 System Design

2.4.1 Hardware Block Diagram

The TIDEP-01025 is implemented for AWR1843BOOST, AWR6843ISK and IWR6843ISK EVM. The EVM needs to be connected to a host PC through universal asynchronous receiver-transmitter (UART) for MetaImage load and log collection.

The AWR1843BOOST/xWR6843ISK includes the following features:

- 1. AWR1843 Radar Device on AWR1843BOOST, IWR6843/AWR6843 Radar Device on xWR6843ISK.
- 2. Power management circuit to provide all the required supply rails from a single 5-V input
- 3. Three onboard TX antennas and four RX antennas

4. Onboard XDS110 that provides a JTAG interface, UART for sending Diagnostic test and Monitor report from mmWave device.



図 2-4. Block Diagram AWR1843BOOST



図 2-5. Block Diagram of xWR6843ISK

For more details on the hardware, see the following:

- 1. AWR1843 Evaluation Module (AWR1843BOOST) Single-Chip
- 2. AWR6843 Evaluation Module (AWR6843ISK) Single-Chip
- 3. IWR6843 Evaluation Module (IWR6843ISK) Single-Chip
- 4. mmWave Sensing Solution

The schematics and design database can be found in the following documents:

- 1. AWR1843 Evaluation Board Design Database
- 2. AWR1843BOOST Schematic, Assembly, and BOM
- 3. xWR6843BOOST Schematic, Assembly, and BOM

2.4.2 Software Components

This application showcases Diagnostic and Monitoring feature of mmWave sensor. It uses SafeTI Diagnostic Library (SDL) for diagnostic test implementation and mmWaveLink to configure monitoring on RF front end.



In this reference design application, few Diagnostic tests are done in secondary bootloader (SBL) at MSS core. At the end of these tests, SBL loads the main application to MSS & DSS RAM location reading MetaImage from sFlash.



図 2-6. Application Control Flow Diagram

☑ 2-7 shows high level of flow diagram of main application which contains MSS and DSS images. Diagnostic and Monitor test status from sensor are sent over UART to PC.



図 2-7. DIAG and Monitor App Flow Diagram



2.4.2.1 Secondary Bootloader (SBL)

The secondary bootloader primarily is responsible for updating the application meta image in the SFLASH by receiving the image over a serial interface. It then loads and runs the updated application meta image.

The ROM(primary) bootloader always loads the SBL. Application can choose to either update or load and run the application meta image.

For safety applications, the SBL may be used to perform some of destructive tests like PBIST and STC that needs to be run during boot time. These DIAG may cause core reset during the execution which is main reason to move these tests to SBL. These tests are validated before loading the main application. In-case of failure the SBL aborts and exit.



🗵 2-8. SBL Flow Diagram

2.4.2.2 mmWaveLink APIs

mmWaveLInk library provides miscllaneous APIs to communicate RadarSS over mailbox interface. In this application, monitoring features are configured by MSS/DSS application through mmWaveLink APIs. Later application receives monitoring reports through mmWaveLink callback in form of asynchronous event from RadarSS.

2.4.2.3 mmWave Safety Diagnostic Library (SDL)

The mmWave SafeTI Diagnostic Library (SDL) is a collection of functions for access to safety functions and response handlers for various safety mechanisms for TI mmWave sensors. These functions assist in the development of software applications involving functional safety.

The SDL provides a collection of diagnostic APIs and low-level driver functions to access the diagnostic features. These safety mechanisms are defined in the mmWave Device Safety Manual.

Chip Support Library (CSL) Register and Function Layer is a hardware abstraction layer that provides a low-level API for the application code to interface to the hardware.

Diagnostics Library (diag) is the Software diagnostics library that provides APIs to access Safety functions and inject/detect faults. The SDL uses CSL to interface to the hardware.



	Customer Code	Legend:
OSAL -	Diagnostic Library	Customer Code
		1
	SCL Register Layer	
	VIM ESM RCM	SPI

2-9. SDL Layer Architecture

Red blocks are Function safety quality, all relevant documents and reports are provided in SDL package.

The *Diagnostic Library* provides the implementation of the diagnostics specified in the mmWave Device Safety Manual.

Diagnostic test categories (based on time duration):

- Single-Shot Diagnostics
- Periodic Diagnostics

Diagnostic Test Tupe-

- Fault insertion diag: ECC, Parity, MPU diagnostics.
- Self test diag: LBIST, PBIST, DCC, CCM diagnostics.
- · Peripheral IO diag: peripheral loopback, Nerror In/Out diagnostics
- · Readback of static config registers: diagnostics to periodically check static configuration registers

Typical DIAG Test Flow

- Operating System Adaptation Layer OSAL layer will define the ability to add & delete hooks. Hooks can be added to ESM error and CPU exceptions.
- HW Configuration HW IP registers which need to be configured in order to execute the diagnostic.
- CPU Exception/ESM Error Diagnostic generate ESM error/CPU exceptions
- All diagnostic handler(s) are internal to the diagnostic layer.



図 2-10. DIAG Test Flow

2.4.2.4 mmWave SDK Software Block Diagram

The mmWave software development kit (SDK) enables the development of mmWave sensor applications using mmWave EVM. The SDK provides foundational components that will facilitate end users to focus on their applications. In addition, the SDK provides several demonstration applications, which will serve as a guide for integrating the SDK into end-user mmWave applications. This reference design is developed on SDK framework and uses SDL library.



図 2-11. SBL and App Block Diagram

3 Hardware, Software, Testing Requirements, and Test Results

Required Hardware and Software

The AWR1843BOOST, xWR6843ISK from Texas Instruments is an easy-to-use evaluation board for the AWR1843 and xWR6843 mmWave sensing devices.

The mmWave Diagnostic and Monitoring application runs on the AWR1843/xWR6843 EVM and sends test status to a PC connected to the EVM over USB.

Hardware

The AWR1843, xWR6843 core design includes:

- AWR1843 device: A single-chip, 77-GHz radar device with an integrated DSP
- xWR6843 device: A single-chip, 60-GHz radar device with an integrated DSP
- Power management network using a low-dropout linear regulator (LDO) and power management integrated circuit (PMIC) DC/DC supply (TPS7A88, TPS7A8101-Q1, and LP87524B-Q1)
- The EVM also hosts a device to assist with onboard emulation and UART emulation over a USB link with the PC

Software

Associated software is hosted on TI-Rex

Refer Getting Started document available in the same package for SW installation and execution steps.

3.1 Hardware Requirements

This reference design requires AWR1843BOOST, xWR6843ISK EVMs to execute the reference application. However customers can run this on their board as well.

- AWR1843 single-chip 76-GHz to 81-GHz automotive radar sensor evaluation module AWR1842BOOST
- AWR6843 single-chip 60-GHz to 64-GHz automotive radar sensor antenna plug-in module AWR6843ISK
- IWR6843 intelligent mmWave sensor standard antenna plug-in module IWR6843ISK
- Dual buck converter and 5-V boost with diagnostic functions LP87702-Q1 (component of above EVMs).

3.2 Test Setup

Test setup contains AWR1843BOOST or xWR6843ISK that is connected with PC over USB cable.





🗷 3-1. Test Setup



3-2 is the typical test flow for a reference design application.



図 3-2. Typical Test FLow

3.3 Test Results

AWR1843BOOST or xWR6843ISK is connected with the PC over USB cable. SBL image is flashed first then the main application. Refer Getting started document in the software package for exact steps to execute this application.

 \boxtimes 3-3, \boxtimes 3-4, and \boxtimes 3-5 show the test result of Diagnostic test result performed by SBL as well as Main application.



図 3-3. Diagnostic Test Results 1

🦉 COM5 - Tera Term VT	-		×
File Edit Setup Control Window Help	10	0	
y = 16	5 - 40,	. Gapa	
Debug: Loading application metaImage from Flash address: c0040000			
Debug: Parsing completed			
nnWave Safety Diagnostic Library Demo			
[SUCCESS] Diag VIM ECC 1-bit Error [SUCCESS] Diag VIM ECC 2-bit Error			
[SUCCESS] Diag Mailbox ECC 1-bit Error [MSS to BSS] [SUCCESS] Diag Mailbox ECC 2-bit Error [MSS to BSS]			
[SUCCESS] Diag Mailbox ECC 1-bit Error [BSS to MSS]			
[SUCCESS] Diag Mailbox ECC 1-bit Error [DSS to MSS]			
[SUCCESS] Diag Mailbox ECC 1-bit Error [MSS to DSS]			
[SUCCESS] Diag Mailbox ECC 2-bit Error [BSS to DSS] [SUCCESS] Diag Mailbox ECC 1-bit Error [BSS to DSS]			
[SUCCESS] Diag Mailbox ECC 2-bit Error [BSS to DSS] [SUCCESS] Diag Mailbox ECC 1-bit Error [=g=g=g=g=g=g=gs±gqS]			
[SUCCESS] Diag Mailbox ECC 2-bit Error [=g=g=g=g=g=g=g=g=g=g=g=g=g=g=g=g=g=g=g			
ISUCCESS] Diag ICMA Parity ISUCCESS] Diag ICMBA Parity			
[SUCCESS] Diag ICMB1 Parity			
[SUCCESS] Diag DMA-1 MPU			
[SUCCESS] Diag DMA-1 Parity			
[SUCCESS] MIBSPI-0 ECC Diagnostic IX RMM, Buffer Index[10] [SUCCESS] MIBSPI-0 ECC 1-Bit Diagnostic RX RAM, Buffer Index[10]			
[SUCCESS] MIBSPI-0 ECC Diagnostic TX RAM, Buffer Index[10] [SUCCESS] MIBSPI-0 ECC 2-Bit Diagnostic RX RAM, Buffer Index[10]			
[SUCCESS] MIBSPI-1 ECC Diagnostic IX RAM, Buffer Index[10] [SUCCESS] MIBSPI-1 ECC 1-Bit Diagnostic RX RAM, Buffer Index[10]			
[SUCCESS] MIBSPI-1 ECC Diagnostic IX RAM, Buffer Index[10] [SUCCESS] MIBSPI-1 ECC 2-Bit Diagnostic RX RAM, Buffer Index[10]			
[SUCCESS] Diag Watchdog Test			
[SUCCESS] Diag R4F CCH-A Test			
[SUCCESS] Diag R4F CCH-B Test			
ISUCCESS] Diag R4F CCM-A Negative lest [SUCCESS] Diag R4F CCM-A Negative Test			
[SUCCESS] Diag R4F CCM-B Negative Test [SUCCESS] Diag R4F CCM-B Negative Test			
ISUCCESS] Diag ESM Static Configuration			
[SUCCESS] Diag DMA StaticCfg Configuration			
[SUCCESS] Diag MibSPI-0 StaticCfg Configuration			
[SUCCESS] Diag DIAN StaticCfg Configuration			
[SUCCESS] Diag RCM StaticCfg Configuration			
ISUCCESS] Diag R4F StaticCfg Configuration [SUCCESS] Diag RTI Static Config			
[SUCCESS] Diag DMA Static Configuration Verify MPU [SUCCESS] Diag DMA Static Configuration Verify MPU			
[SUCCESS] Diag ESM StaticCfg Verify Violation LTC Preload [SUCCESS] Diag VIM StaticCfg Verify Violation Wakeup			
[SUCCESS] Diag VIM StaticCfg Verify Violation FallbackAddr [SUCCESS] Diag VIM StaticCfg Verify Violation FCCDiag			
[SUCCESS] Diag VIM StaticCfg Verify Violation ChanCtrl			
[SUCCESS] Diag HIBSTI-0 Static Configuration Verify Config [SUCCESS] Diag HIBSPI-0 Static Configuration Verify Config			
[SUCCESS] Diag DCAN Static Configuration Verify Config [SUCCESS] Diag MCAN Static Configuration Verify Config			
[SUCCESS] Diag RCM StaticCfg Verify Violation Mailbox ECC [SUCCESS] Diag R4F StaticCfg Verify Violation TCMB1 ext error sta	tus		
*** DSS Diagnostic Status: ***			
ISUCCESSJ DSS EDMA TPCCØ PARITY Diagnostic. [SUCCESS] DSS EDMA TPCC1 PARITY Diagnostic.			
ISUCCESSJ DSS L1P PARITY Diagnostic. ISUCCESSJ DSS L2P UMAPØ PARITY Diagnostic.			
[SUCCESS] DSS L2P UMAP1 PARITY Diagnostic.			
[SUCCESS] DSS L2 ECC 2Bit Error Diagnostic.			
ISUCCESSI DSS L3 ECC 2Bit Envon Diagnostic			





図 3-5. Diagnostic Test Results 3

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-01025

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-01025.

4.2 Tools and Software

Tools

Serial Terminal This application takes input and stream the log over the UART COM port. Serial Terminal tool is required to connect to the device over COM port.

Software

Diagnostic and Monitoring
Reference ApplicationApplication source code and binary files are available at TI-Rex below
mmWave Sensors' Platform Toolbox.

4.3 Documentation Support

1. Texas Instruments, *Enabling Functional Safety in TI mmWave Devices* presentation.

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5 About the Author

JITENDRA GUPTA is an Application engineer at Texas Instruments where he is responsible for application development and solving customer's technical problems for mmWave Sensor device. Jitendra joined TI in 2011 and has been involved in the design of various products related to WiFi and GNSS.

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