Analog Engineer's Circuit

Unipolar-to-Bipolar Level Translator Circuit, 0-V to 5-V Unipolar to ±12-V Bipolar

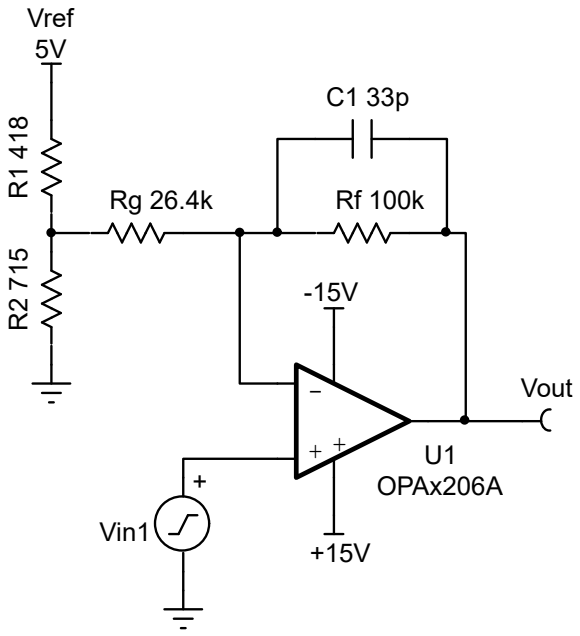
Amplifiers

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{CC}	V_{EE}	V_{ref}
0 V	5 V	–12 V	+12 V	+15 V	–15 V	5 V

Design Description

This design is intended to translate a small unipolar signal to a wide bipolar signal. A common application is to translate a 5-V DAC output to a ±12-V bipolar signal. The document provides equations needed to calculate component values for other voltage range requirements. Important error sources are covered using calculations and simulation.



Design Notes

1. The OPA206 op amp was selected for excellent DC and AC characteristics as well as built-in robustness features. This topology works well for many different op amp selections.
2. Select 0.1% 20 ppm/°C resistors for good gain, offset accuracy, and drift.
   A calibration at room temperature can be used to minimize the gain error at room temperature, but gain drift can only be reduced by minimizing the resistor drift (choosing resistors with TC ≤ 20 ppm/°C).
3. Place decoupling capacitors close to the device power supplies. The *OPAx206* data sheet provides layout suggestions, and this video on *Decoupling Capacitors* provides further details.

Specifications

Parameter	Design Goal	Simulated (Without Buffered Voltage Divider)	Simulated (With Buffered Voltage Divider)
V_{outMin}	–12 V	–11.8 V	–11.95 V
V_{outMax}	+12 V	+11.92 V	+11.99 V
Bandwidth	50 kHz	48.5 kHz	48.5 kHz
Noise	N/A	32.9 μV_{RMS}	24.2 μV_{RMS}

Design Steps

1. Define the input and output conditions.
   For this example, V_{inMin} = 0 V, V_{inMax} = 5 V, V_{outMin} = –12 V, V_{outMax} = 12 V.
2. Select a reference voltage. Generate this voltage from a precision source such as a series or shunt voltage reference (for example REF5050). Typically, a power-supply voltage developed by a low dropout regulator does not have sufficient accuracy to act as a reference. V_{ref} = 5 V in this example.
3. Choose a large resistance for R_f. Typical practical values range from 50 kΩ to 1 MΩ. R_f = 100 kΩ in this example.
4. Calculate gain based on the input range and output range.

$$G = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{12\ V\ -\ (-12\ V)}{5\ V\ -\ 0\ V} = 4.8$$

5. Calculate R_g based on R_f and signal gain.

$$R_g = \frac{R_f}{(G-1)} = \frac{100\ k\Omega}{(4.8-1)} = 26.31\ k\Omega\ \left(26.4\ k\Omega\ \text{standard value}\right)$$

6. Calculate the output of the voltage divider based on minimum signal. If this number is negative, use a different topology. Also, this number must be less than V_{ref} from step 2.

$$V_{div} = \frac{V_{outMin} - (V_{inMin} \times G)}{\left(-R_f/R_g\right)} = \frac{-12\ V - (0\ V \times 10)}{\left(-R_f/R_g\right)} = 3.168\ V$$

7. Calculate R_1 and R_2 to achieve the desired divider output. The equations used for this calculation assume that (R_1 || R_2) = R_g/100, so that R_g >> (R_1 || R_2). The reason this is done is that the voltage divider has an impact on gain. The actual gain including the voltage divider is 3.781, whereas the ideal gain was 4.8. The following equations show the algebraic rearrangement of the voltage divider equation to a ratio of R_1/R_2. This ratio is defined as α and used throughout the calculation.

$$\left(\frac{R_2}{R_1 + R_2}\right)V_{ref} = V_{div}\ \text{rearrange to}\ \frac{R_1}{R_2} = \frac{V_{ref}}{V_{div}} - 1$$

$$\alpha = \frac{R_1}{R_2} = \frac{V_{ref}}{V_{div}} - 1\ = 0.583\ \left(\text{define } \alpha \text{ as } R_1/R_2,\ \text{substitute } V_{ref} \text{ and } V_{div}\right)$$

$$R_1 = \frac{R_g}{100}(\alpha + 1) = 418\ \Omega\ \left(417\ \Omega\ \text{standard value}\right)$$

$$R_2 = R_1/\alpha = 714.9\ \Omega\ (\text{or } 715\ \Omega\ \text{standard value})$$

$$G_{loaded} = \frac{R_f}{R_g + \left(R_1 \middle|\middle| R_2\right)} + 1 = 4.75\ \left(\text{ideal gain was } 4.8\right)$$

8. As an option, a buffer can be placed between the voltage divider and R_g. Doing this improves the accuracy and also eliminates the requirement that R_g >> (R_1 || R_2). See accuracy difference in the *DC Transfer Characteristics* section. In this case, the value of R_f can be selected as a smaller value which improves noise. Also, the divider resistors are independent from the feedback, so any values can be used for R_1 and R_2 as selected and shown in step 7, provided that the ratio is correct. This allows selection of larger values of R_1 and R_2 to minimize divider current.
9. A filter capacitor can be used across R_f to limit bandwidth and minimize noise (f_c = 50 kHz in this example).

$$C_f = \frac{1}{2\pi R_f f_c} = \frac{1}{2\pi(100\ k\Omega)(50\ kHz)} = 31.8\ pF\ \left(33\ pF\ \text{standard value}\right)$$

DC Transfer Characteristics

The following images show the DC Transfer function for the standard and buffered version of the circuit. Note that the buffered version is more accurate. Also note that the values selected in the buffered version, use the same ratios, but the magnitudes are adjusted. The buffered version decreased the feedback network impedance for better noise, and increased the divider network for better power dissipation. Note that the inaccuracy in the transfer function can be accounted for with a simple calibration (see the *Calibration* video).

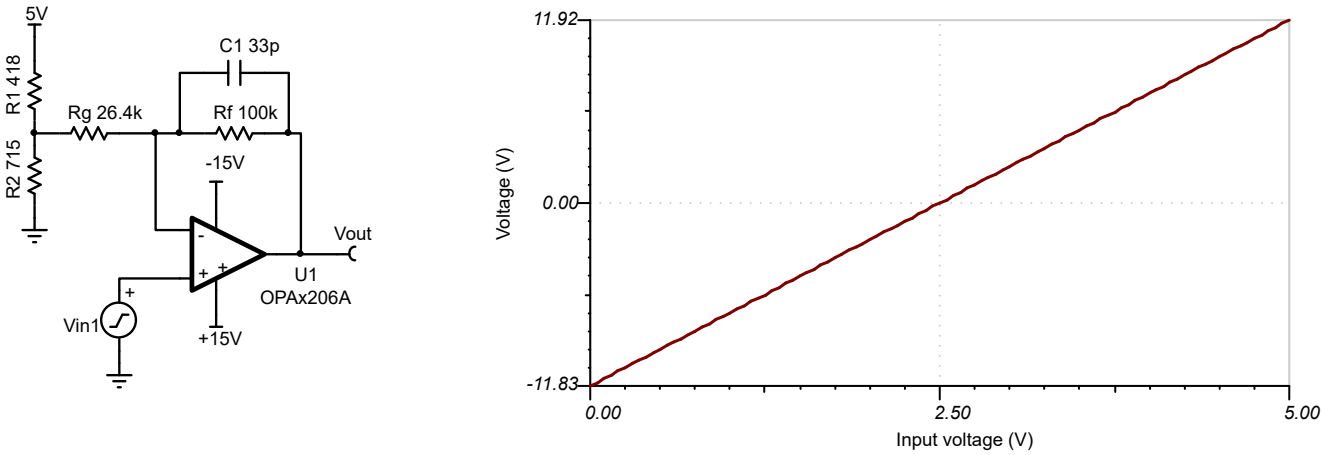


Figure 1-1. DC Transfer Characteristics for Unbuffered Circuit

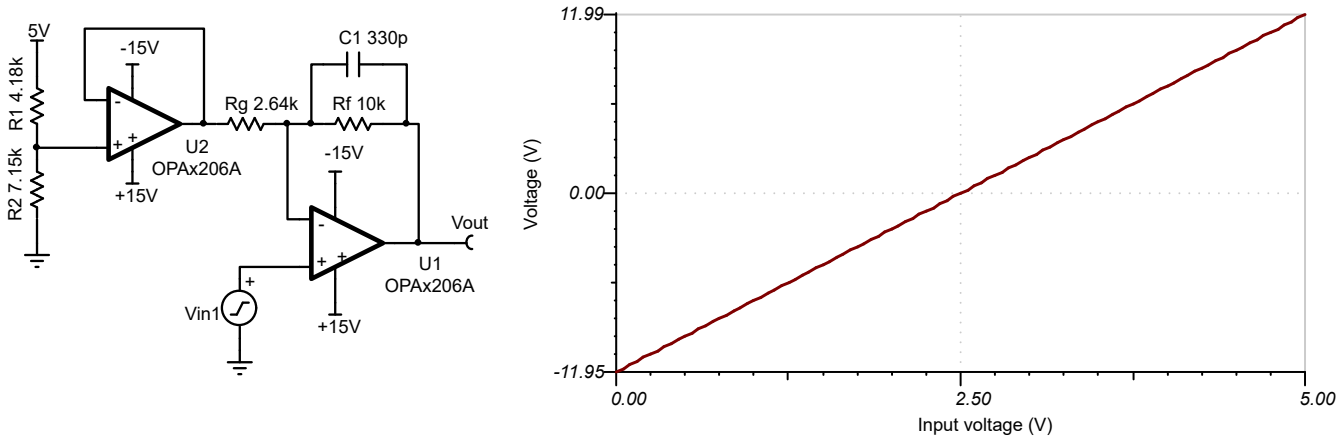


Figure 1-2. DC Transfer Characteristics for Buffered Circuit

AC Transfer Characteristics

The capacitor C_f sets the cutoff frequency to 100 kHz. This causes the gain of the amplifier to roll-off until gain is 1 V/V or 0 dB. At higher frequency the bandwidth limitations of the amplifier causes gain to roll-off again. The expected bandwidth of 50 kHz compares well to the simulated 48.5 kHz. Additional detail on bandwidth limitations are given in the *Bandwidth* video series.

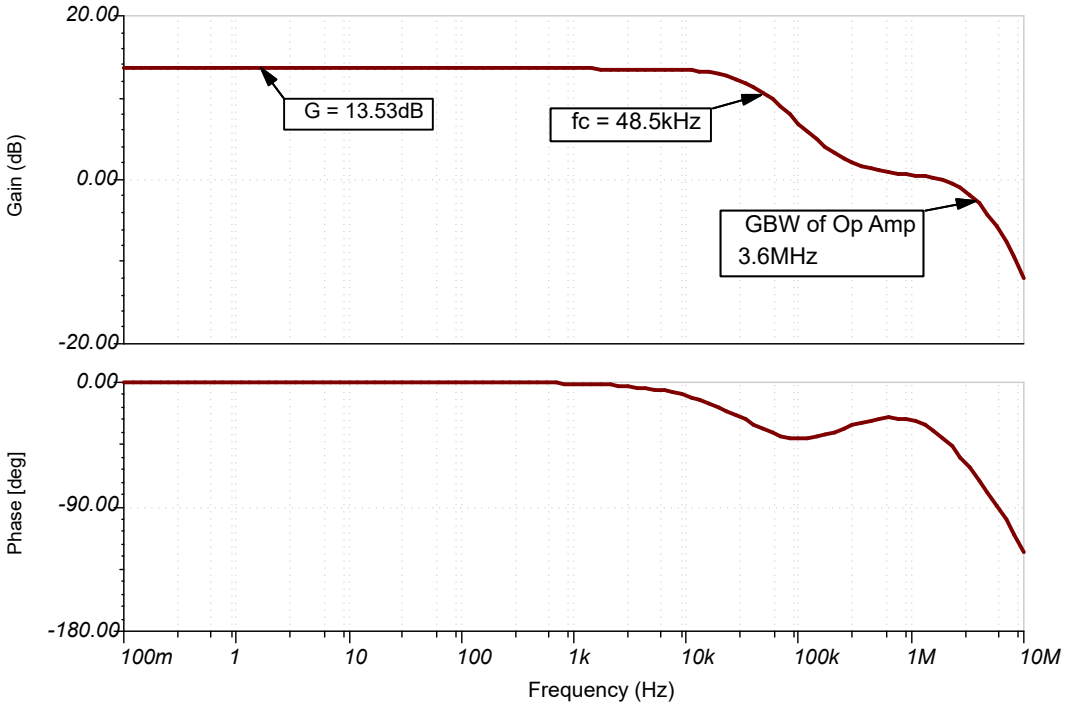


Figure 1-3. AC Transfer Characteristics for Level Translator

Noise Simulation

Total noise is approximately 32.9 μV_{RMS}. Peak-to-peak is approximately 6 × RMS = 197 µVpp. For more information on noise analysis and optimization see the *Noise* video series. Note that the noise of the buffered version is lower because the voltage divider uses lower resistor values which minimizes total noise.

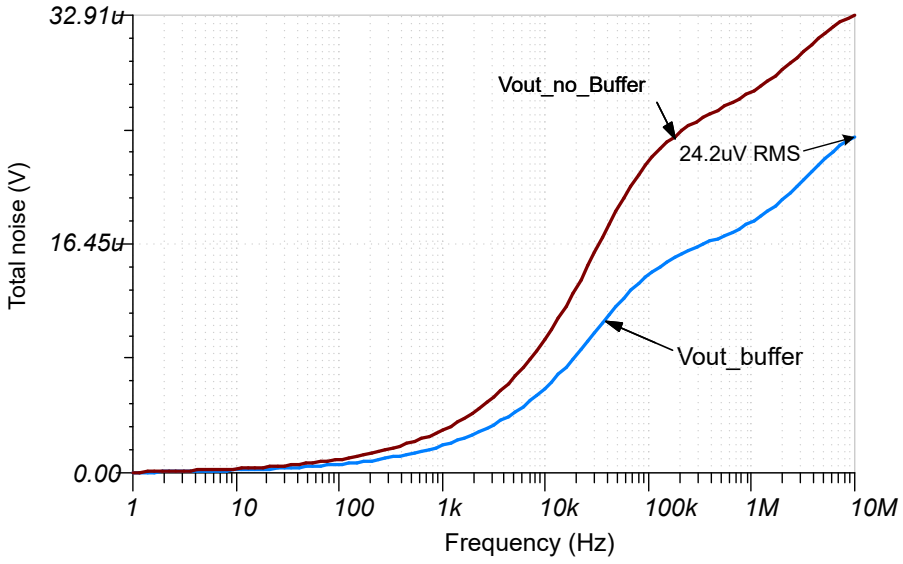


Figure 1-4. Total RMS Noise for Level Translator

Stability

This circuit is stable for capacitive loads from 0 pF to 120 pF. The analysis below shows 48.2°C of phase margin for a 120-pF load (45°C and better is considered stable). For more information on stability see the *Stability* video series.

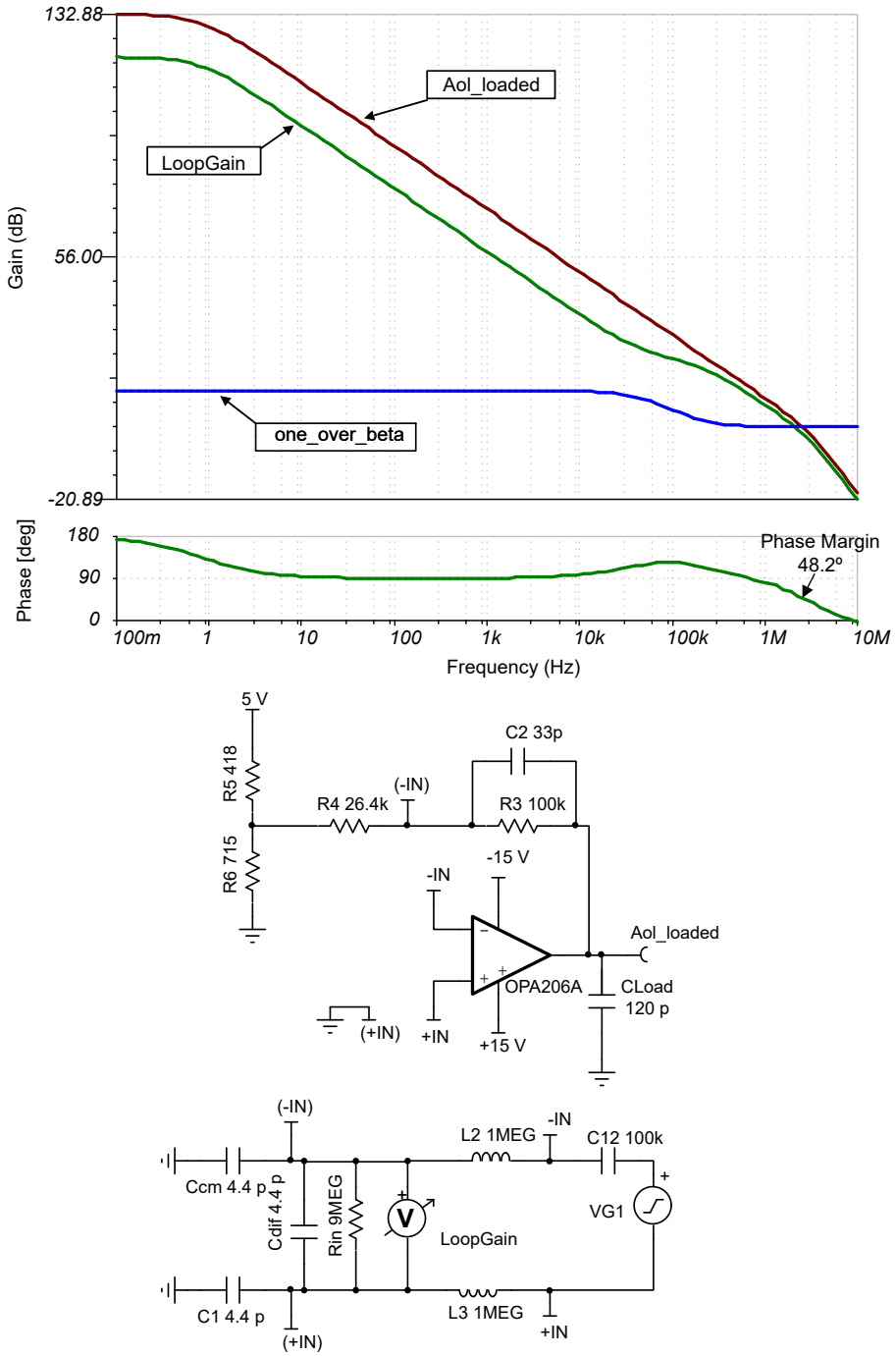


Figure 1-5. Stability of Level Translator Circuit

Design Featured Devices and Alternative Parts

This design works with most amplifiers that accept high-voltage ±15-V supplies. Depending on the application the key parameters can be different. The following table shows three different options representing different categories of devices. Package-trimmed devices have good offset and offset drift by adjusting internal device resistors, zero-drift devices use an internal calibration to reduce offset and drift, and general-purpose are optimized for best cost. When using a zero-drift option, a best practice is to keep the total feedback impedance less than 10 kΩ (R_f || (R_g + R_1 || R_2) < 10 kΩ). This is recommended to avoid translating bias current into offset voltage. Click on the *other possible devices* link for a list of other options in the same category.

Device	Key Features	Other Possible Devices
OPA206	36-V supply, 3.6-MHz bandwidth, low noise (8 nV/√Hz), rail-to-rail output, 240-µA supply current, low offset 25 µV, 0.5 µV/˚C, e-trim™ op amp,with super-beta inputs and OVP	36-V e-trim™
OPA182	36-V supply, 2-MHz bandwidth, rail-to-rail input to -V/Out, low noise (8.8 nV/√Hz), low offset 25 µV, 0.03 µV/˚C, zero-drift amplifier	36-V zero-drift
LM358B	36-V supply, 1.2-MHz bandwidth, rail-to-rail input to -V, general-purpose	36-V cost-optimized

Design References

1. See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.
2. See circuit TINA SPICE simulation file sbomcf8.
3. See circuit PSPICE simulation file sbomcf7.
4. For more information on many op-amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs.
5. See the *OPAx206 Input-Overvoltage-Protected, 4-µV, 0.08-µV/°C, Low-Power Super Beta, e-trim™ Op Amps* data sheet for layout guidelines.

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