Texas Instruments

Application Brief
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Phase-Noise Performance of the CDC7005 at UMTS and CDMA Frequencies

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ABSTRACT

This application brief presents phase-noise data taken on Texas Instruments CDC7005 jitter cleaner and synchronizer PLL. The phase noise performance of CDC7005 depends on the phase noise of the reference clock, the voltage-controlled crystal oscillator (VCXO) clock, and the CDC7005 itself. This applications brief shows the phase noise performance of the CDC7005 clock synthesizer at the most popular Universal Mobile Telecommunications System (UMTS) and Code Division Multiple Access (CDMA) frequencies. It helps the user in choosing the right clocking solution for their particular applications. The test results reveal that the CDC7005 can provide clock outputs better than −145-dBc/Hz phase noises at 1-MHz offset from the carrier frequency with proper VCXO and loop bandwidth selection. Low phase noise is required for most base station applications such as UMTS and CDMA and its derivatives as well as many other jitter stringent applications.

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1 Introduction

Phase noise (PN) is the short-term instability caused by variation of frequency (phase) of a signal referenced to the carrier level and a function of the carrier offset (i.e., relative noise level within a 1-Hz bandwidth). Integration of PN over a given frequency band yields phase jitter RMS.

The CDC7005 is a low phase noise/low jitter clock synthesizer and jitter cleaner with five programmable LVPECL outputs. It requires either an external or internal low pass loop filter in addition to an external VCXO to complete the phase locked loop. By selecting VCXO and loop bandwidth, the device achieves the best performance at its outputs. This brief includes phase noise plots of the most common frequencies used in base station applications. In addition, the phase noise of the clock source feeding the CDC7005 is included for completeness.

2 Test and Measurements Setup

The block diagrams of the test setup are shown in Figure 1. An input reference clock from the HP8664A signal generator is fed into the Agilent E5250 and the phase noise of the source is measured (indicated by the dotted line). The same signal is then fed into one leg of the VCXO_IN of the CDC7005 and the phase noise is measured through the Agilent E5250 analyzer (open-loop).

All measurements were taken at nominal 3.3-V power supply, room temperature, and open loop PLL. The HP8644 as a signal generator, the CDC7005 evaluation module (EVM) in 1x mode, and the Agilent E5250 phase noise test system were used. The test setup below was used for most the phase noise testing. The phase noise can be measured up to 40 MHz from the carrier frequency, although some measurements were taken up to 10 MHz or 1 MHz from the carrier depending upon the desired clock frequency.

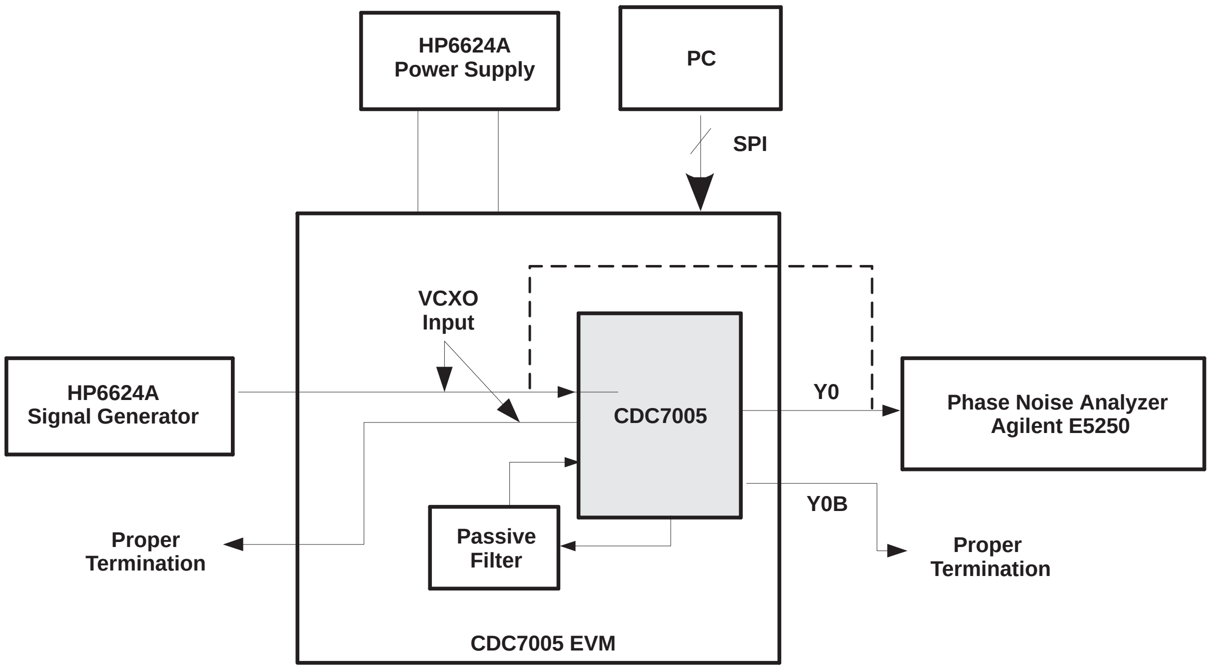

Figure 1. Test Setup of the Phase-Noise Measurements

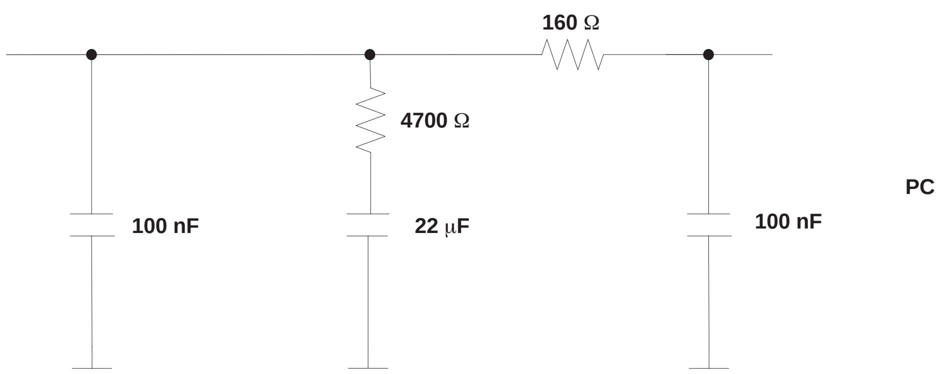

Figure 2. External Passive Loop Filter Circuit on the CDC7005 EVM

3 Summary and Conclusion

The CDC7005 PLL tracks the input reference signal up to the loop bandwidth, while it follows the VCO (here VCXO) phase noise floor at frequencies above the loop bandwidth. The VCXO phase noise performance is critical in achieving good phase noise performance and meeting stringent phase noise requirements in base station applications.

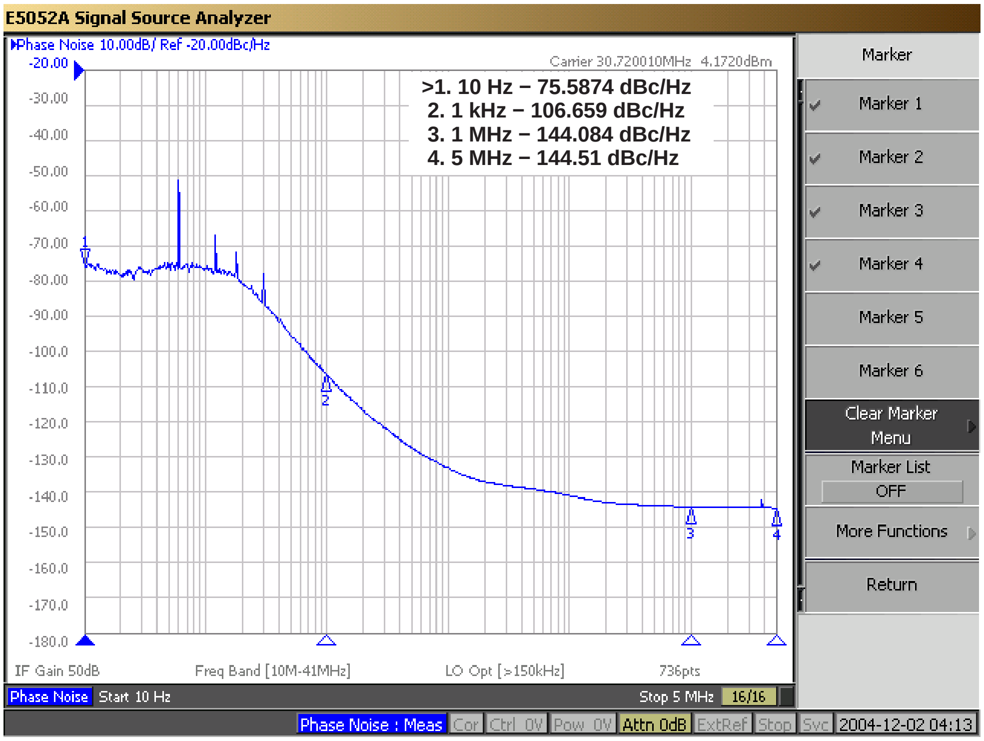

Figure 3. Phase Noise of the CDC7005 at 30.72 MHz Driven by HP8664A

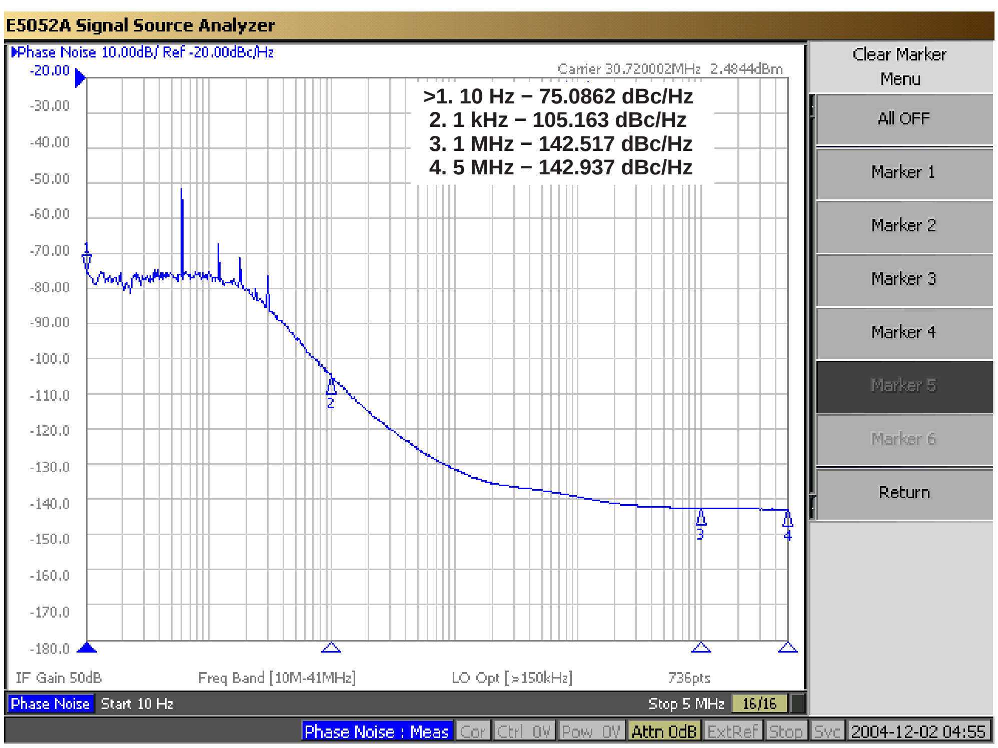

Figure 4. Phase Noise of the HP8664A at 30.72 MHz

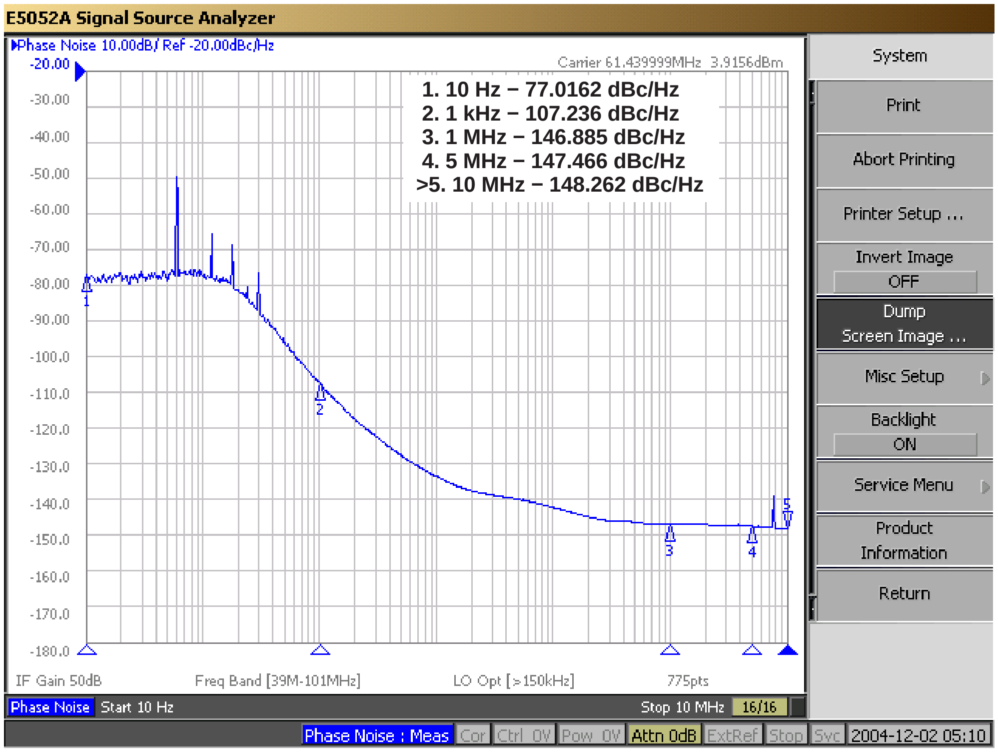

Figure 5. Phase Noise of the CDC7005 at 61.44 MHz Driven by HP8664A

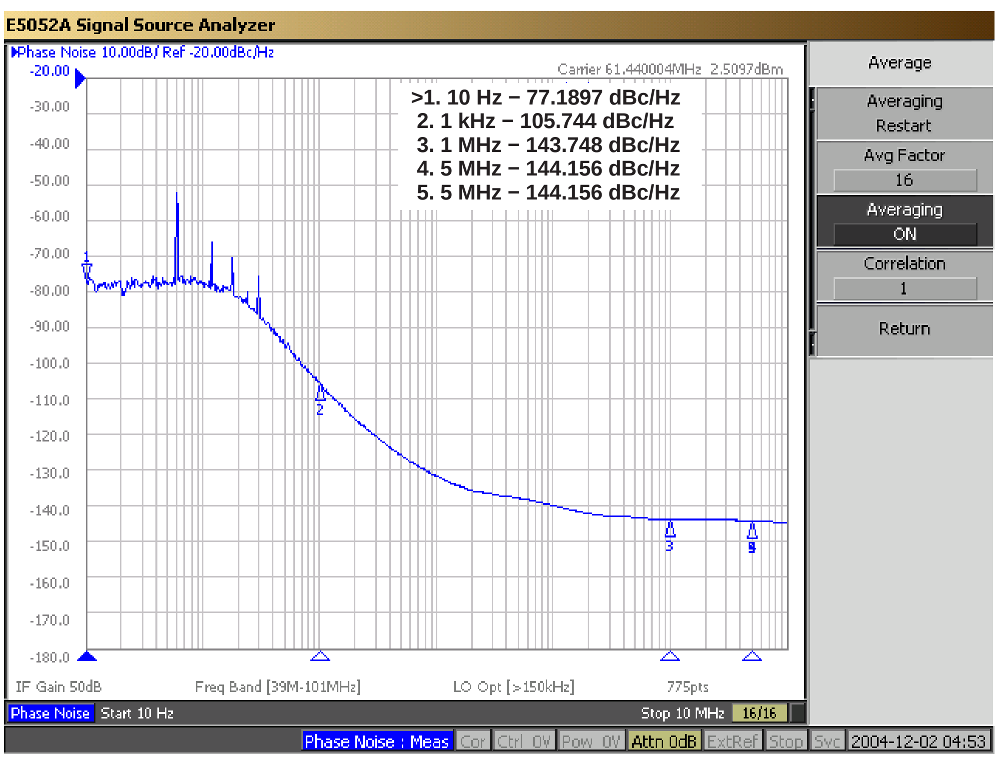

Figure 6. Phase Noise of the HP8664A at 61.44 MHz

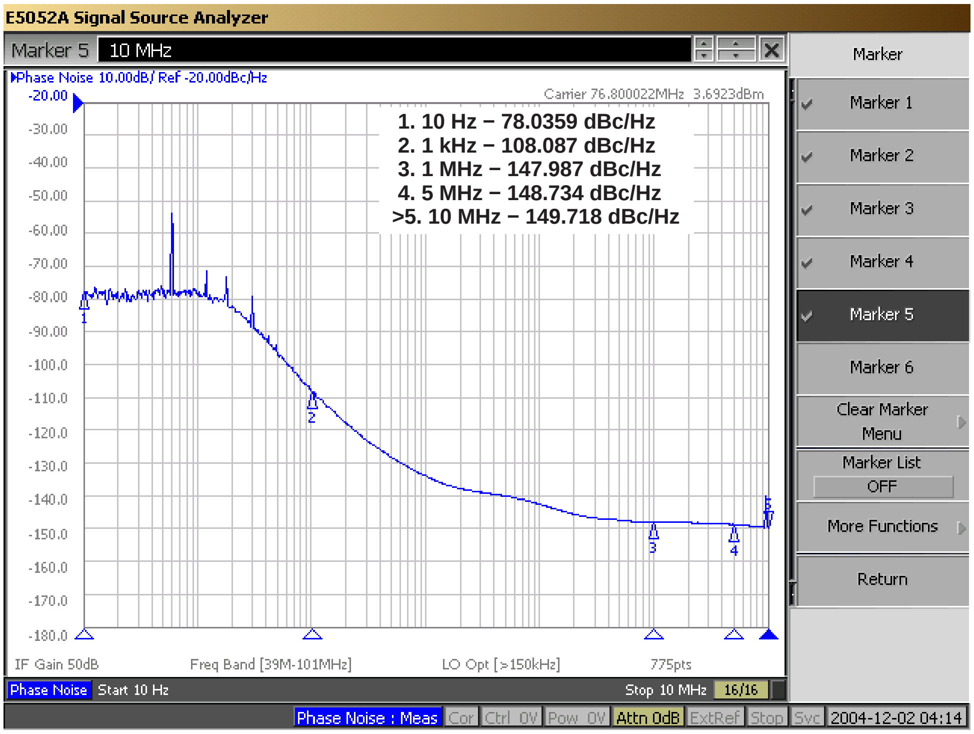

Figure 7. Phase Noise of the CDC7005 at 76.8 MHz Driven by HP8664A

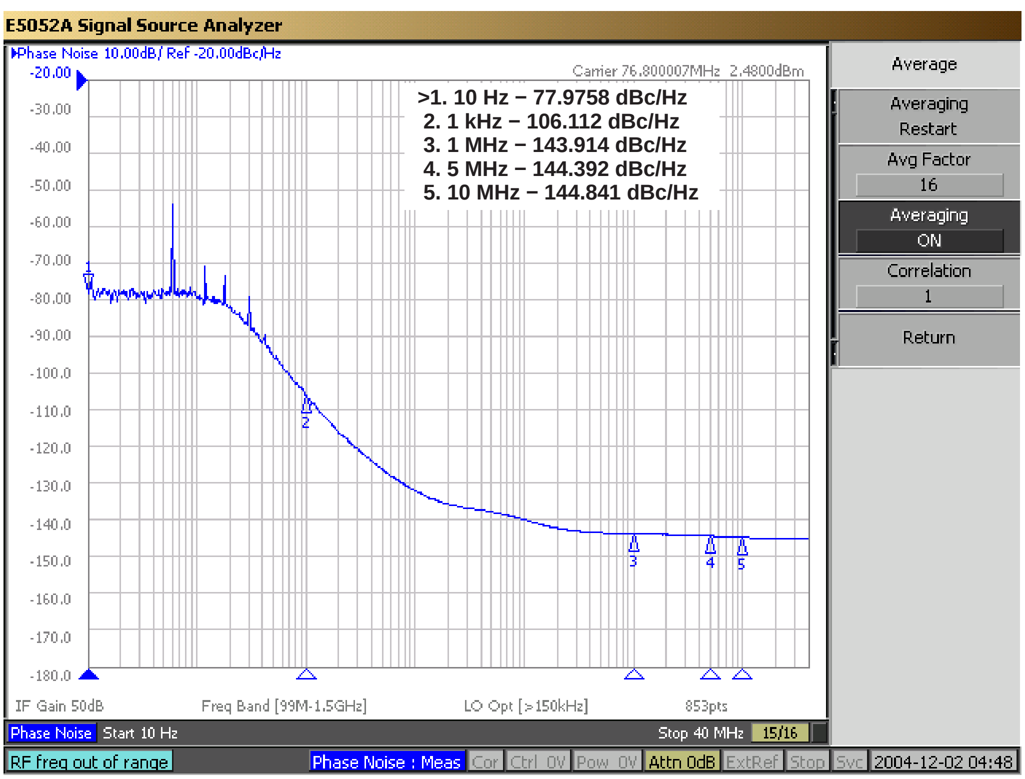

Figure 8. Phase Noise of the HP8664A at 76.8 MHz

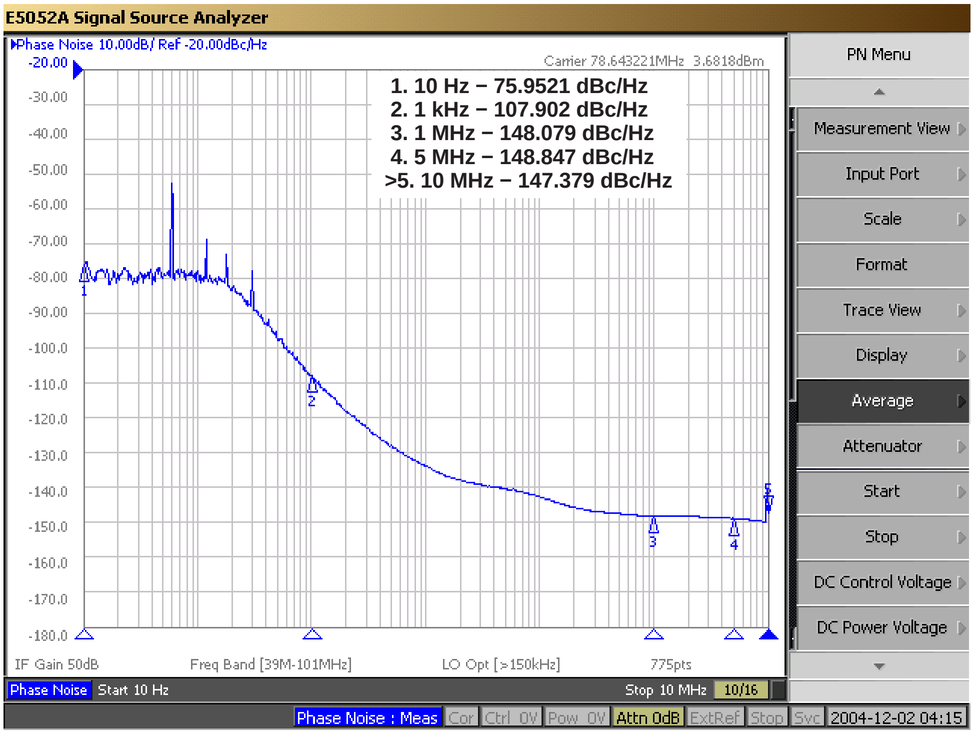

Figure 9. Phase Noise of the CDC7005 at 78.6432 MHz Driven by HP8664A

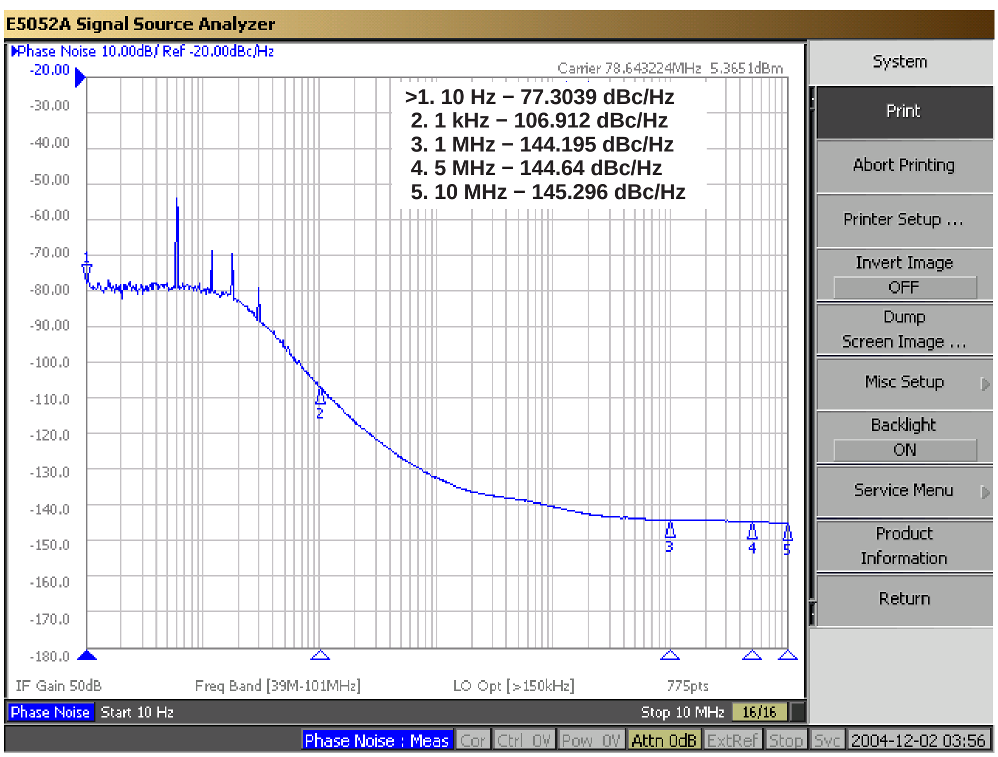

Figure 10. Phase Noise of the HP8664A at 78.6432 MHz

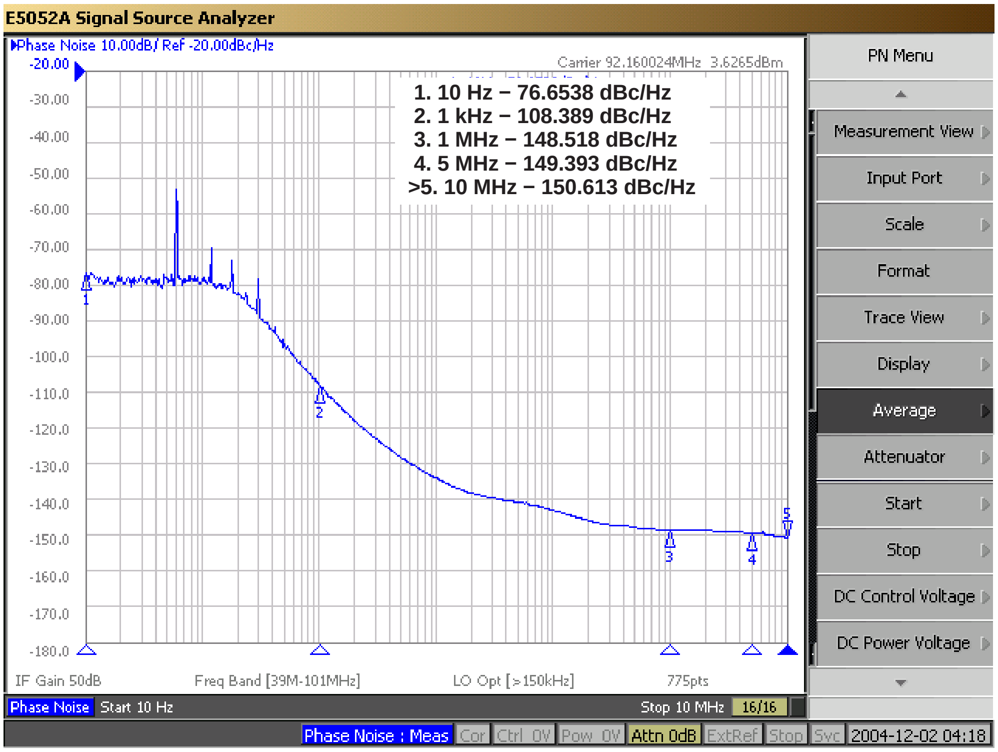

Figure 11. Phase Noise of the CDC7005 at 92.16 MHz Driven by HP8664A

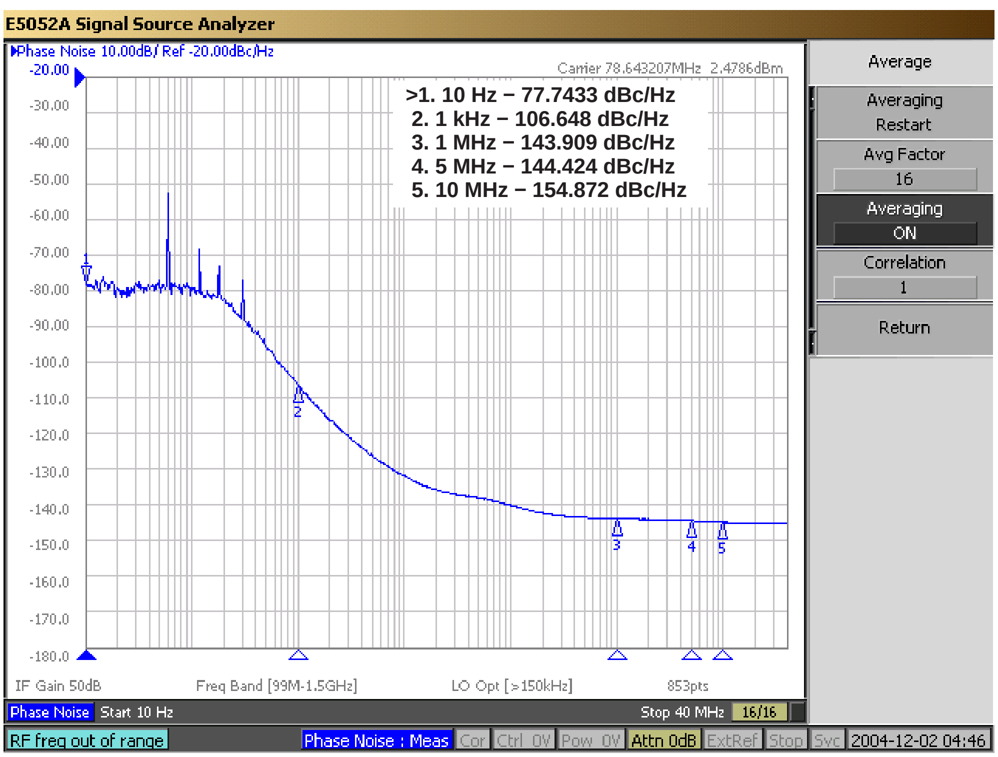

Figure 12. Phase Noise of the HP8664A at 92.16 MHz

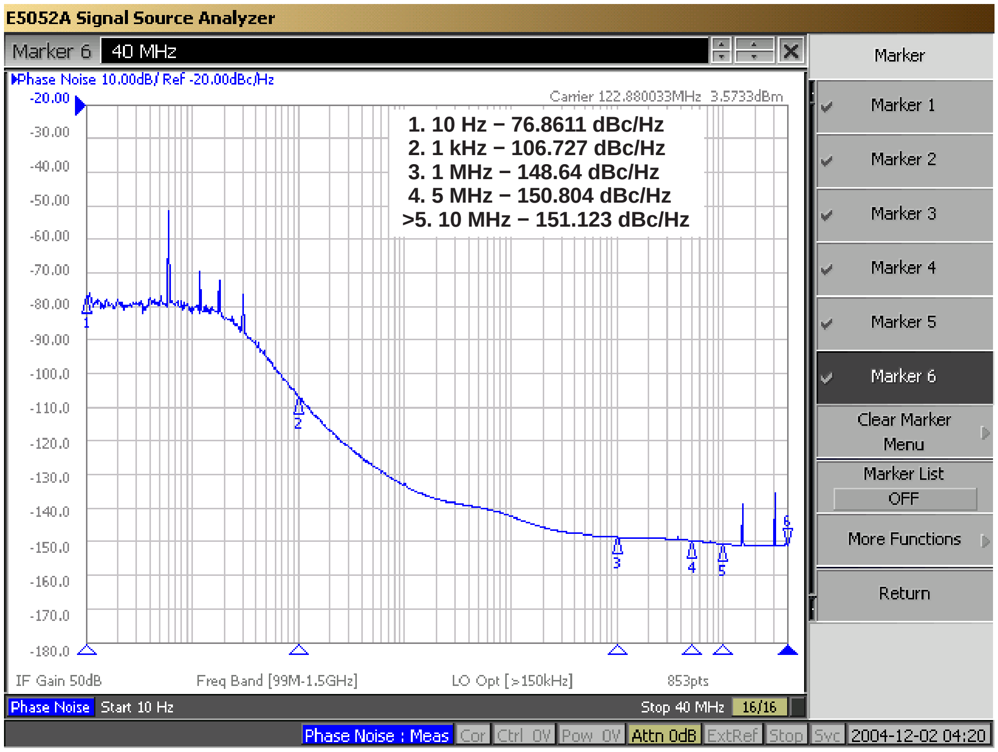

Figure 13. Phase Noise of the CDC7005 at 122.88 MHz Driven by HP8664A

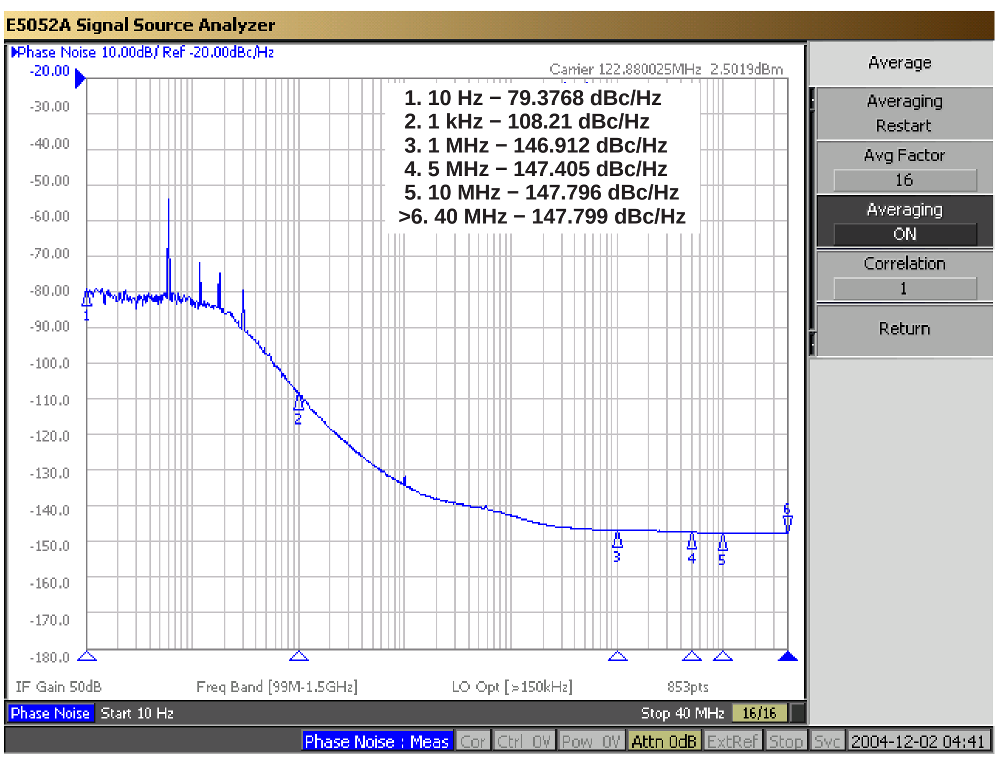

Figure 14. Phase Noise of the HP8664A at 122.88 MHz

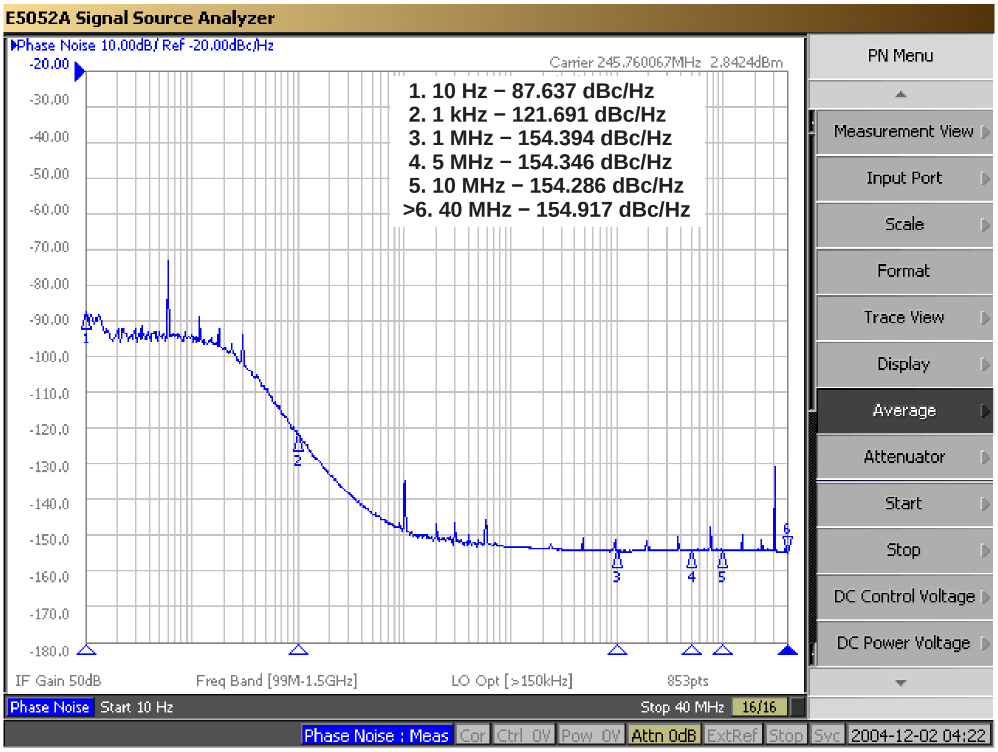

Figure 15. Phase Noise of the CDC7005 at 245.76 MHz Driven by HP8664A

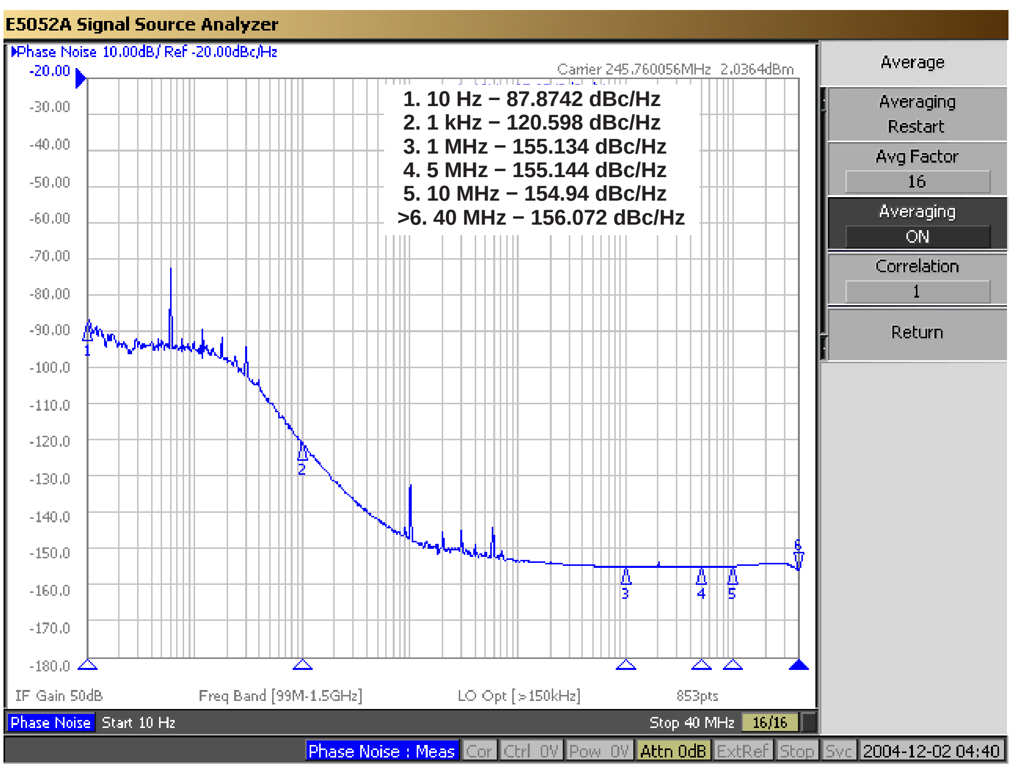

Figure 16. Phase Noise of the HP8664A at 245.76 MHz

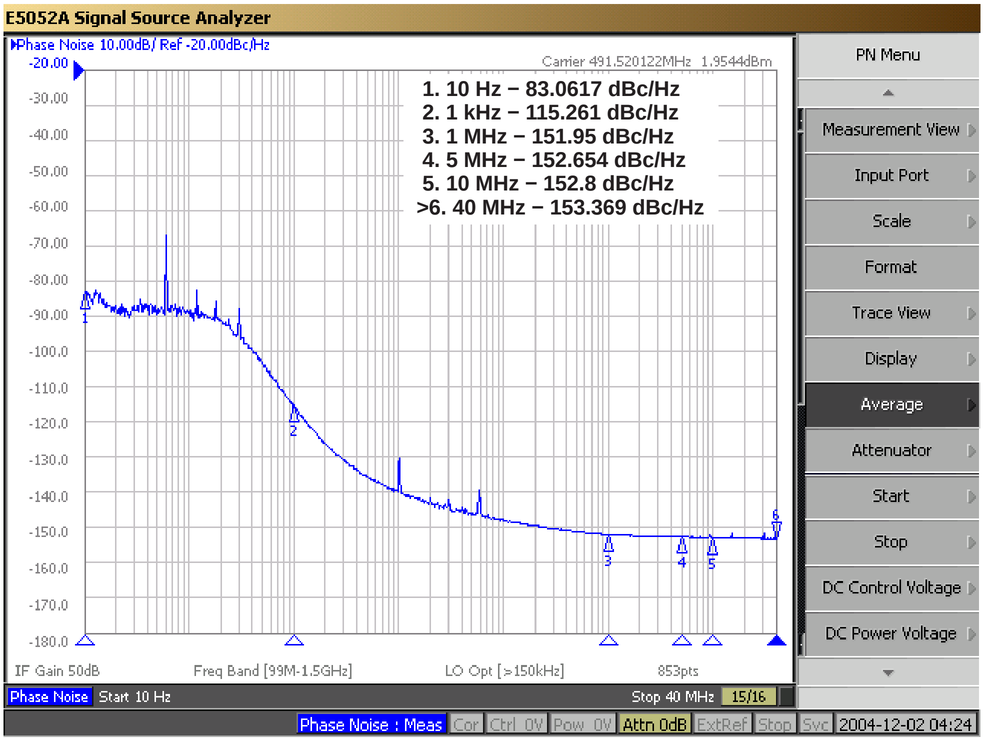

Figure 17. Phase Noise of the CDC7005 at 491.52 MHz Driven by HP8664A

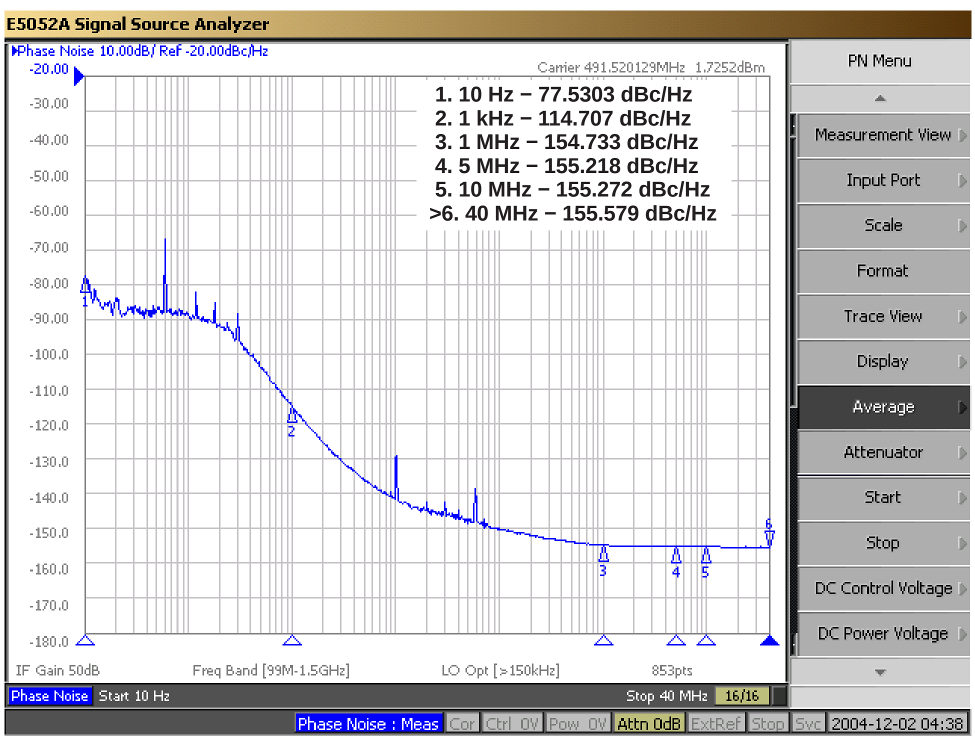

Figure 18. Phase Noise of the HP8664A at 491.52 MHz

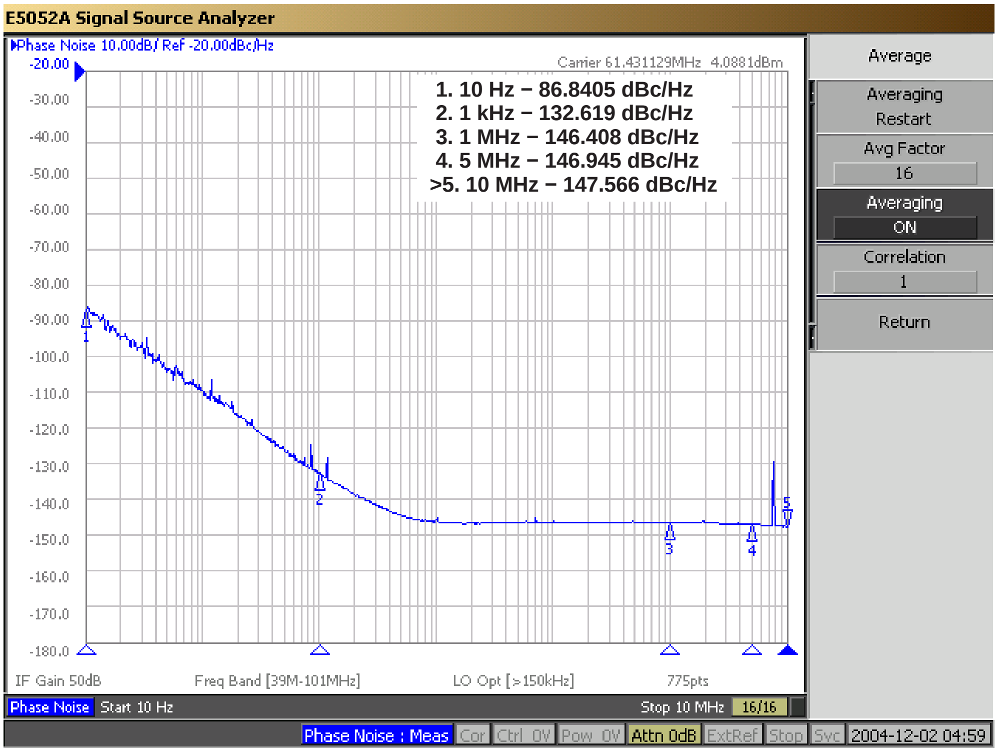

Figure 19. Closed-Loop Phase Noise of the CDC7005 at 61.44 MHz

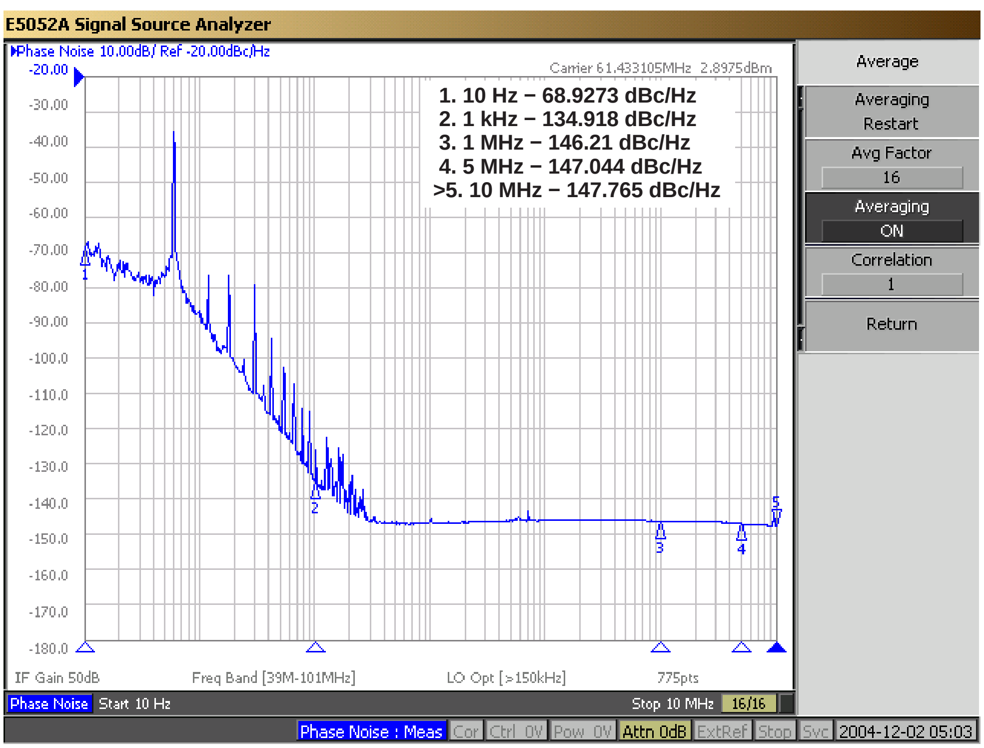

Figure 20. Phase Noise of Toyocom 61.44 MHz VCXO

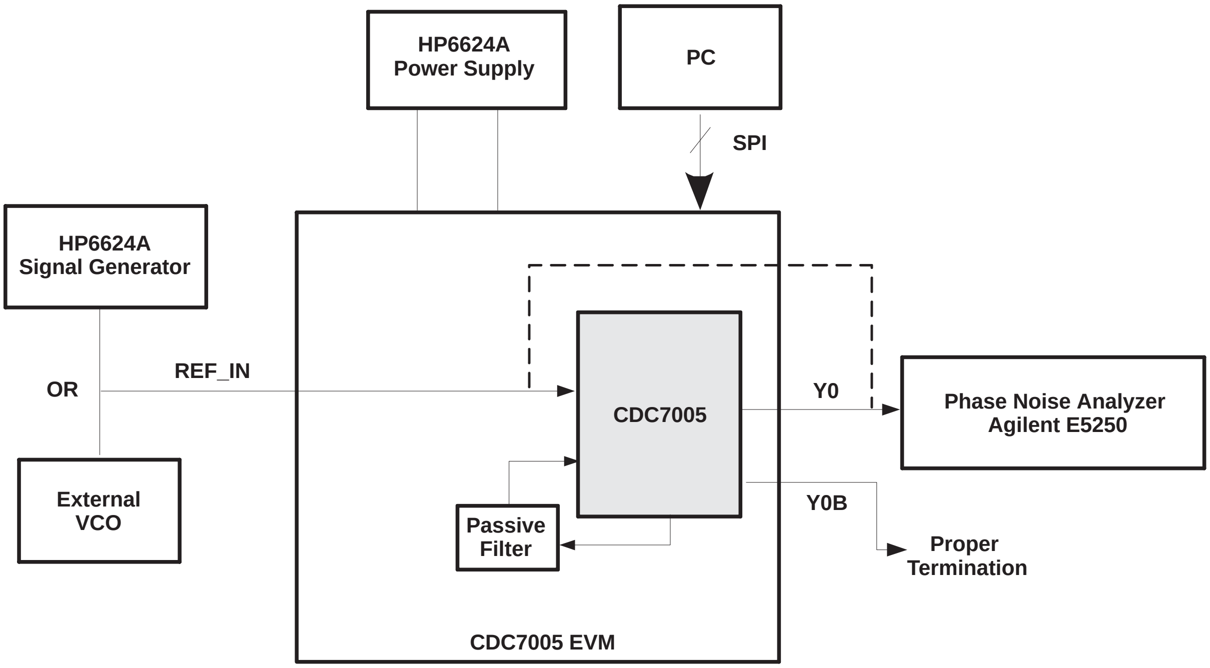

Figure 21. Close-Loop Phase Noise Performance of CDC7005 With Toyocom 61.44-MHz VCXO

From the data above, it is evident that a low phase noise clock output is easily attainable from the CDC7005, with the proper selection of differential or single-ended VCXO's.

4 Test Summary

PC

The test results reveal that the CDC7005 can provide clock outputs better than −145-dBc/Hz phase noises at 1-MHz offset from the carrier frequency. Low phase noise is required for most base station application such as UMTS and CDMA and its derivatives as well as many other jitter stringent applications.

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2. Paul Woodley, O&M Sales, Inc., Paul.Woodley@o−m−sales.com
3. Micky Kilpatrick, Agilent Technologies, micky_kilpatrick@agilent.com

6 References

4. CDC7005 data sheet, Texas Instruments, SCAS685
5. CDC7005 EVM user's guide, Texas Instruments, SCAU005
6. Using the CDC70005 as a 1:5 PECL Buffer With Programmable Divider Ratio, Texas Instruments, http://focus.ti.com/lit/an/scaa060/scaa060.pdf

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