# Functional Safety Information LM25141 Functional Safety FIT Rate, FMD and Pin FMA

# **TEXAS INSTRUMENTS**

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# 1 Overview

This document contains information for LM25141 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

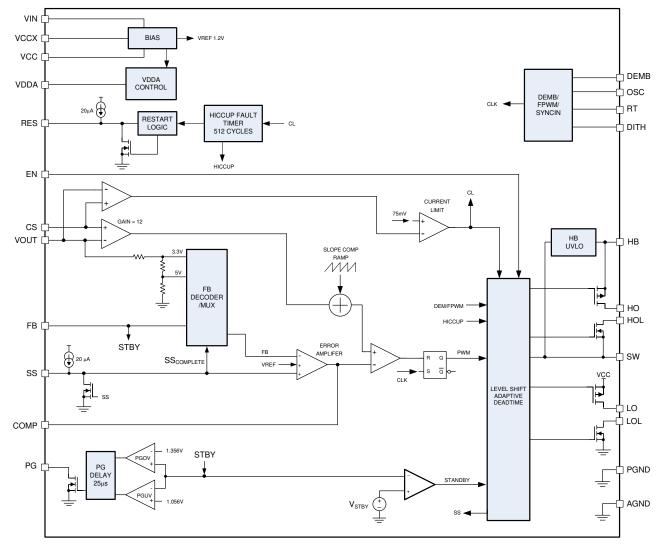


Figure 1-1. Functional Block Diagram

LM25141 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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### 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM25141 based on two different industrywide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

#### Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)			
Total Component FIT Rate	15			
Die FIT Rate	4			
Package FIT Rate	11			

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

#### Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS/BICMOS ASICs Analog & Mixed > 50V supply	32 FIT	55°C

The Reference FIT Rate and Reference Virtual  $T_J$  (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



## 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM25141 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60%
Output not in specification – voltage or timing	25%
Gate driver stuck on	5%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

### Table 3-1. Die Failure Modes and Distribution



## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM25141. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

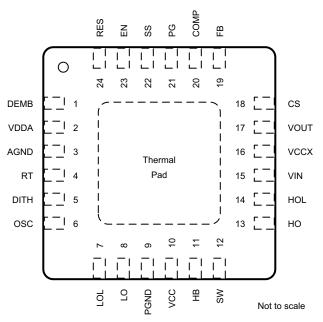
- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuit to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Class	Failure Effects
A	Potential device damage that affects functionality
В	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

### Table 4-1. TI Classification of Failure Effects

Figure 4-1 shows the LM25141 pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the LM25141 data sheet.





Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit as per LM25141 data sheet is used
- PG is pulled up to VOUT

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	V <sub>OUT</sub> = expected, DEMB mode only, and no synchronization is available.	С
DEINID	1	If DEMB = VDDA, V <sub>OUT</sub> = 0 V. Loaded VCC output	В
VDDA	2	V <sub>OUT</sub> = 0 V. No switching. Loaded VCC output	В
AGND	3	AGND is GND. V <sub>OUT</sub> = expected	D
RT	4	Normal operation. V <sub>OUT</sub> = expected. F <sub>SW</sub> defaults to 2.2 MHz or 440 kHz, depending on OSC.	С
DITH	5	Dither disabled. V <sub>OUT</sub> = expected	С
osc	6	If OSC = GND, then F <sub>SW</sub> = 440 kHz. V <sub>OUT</sub> = expected	С
030	0	If OSC = VDDA, then V <sub>OUT</sub> = 0 V. Loaded VCC output	
LOL	7	V <sub>OUT</sub> = 0 V. The VCC regulator is loaded to current limit.	В
LO	8	V <sub>OUT</sub> = 0 V. The VCC regulator is loaded to current limit.	В
PGND	9	PGND is GND. V <sub>OUT</sub> = expected	D
VCC	10	V <sub>OUT</sub> = 0 V. The VCC regulator is loaded to current limit.	В
HB	11	V <sub>OUT</sub> = 0 V. The VCC regulator is loaded to current limit.	В
SW	12	V <sub>OUT</sub> = 0 V. Excessive current from VIN	В
HO	13	V <sub>OUT</sub> = 0 V. High-side MOSFET cannot be turned on.	В
HOL	14	V <sub>OUT</sub> = 0 V. High-side MOSFET cannot be turned on.	В
VIN	15	V <sub>OUT</sub> = 0 V	В
VCCX	16	V <sub>OUT</sub> = expected. The internal VCC regulator provides bias voltage.	С
VOUT	17	V <sub>OUT</sub> = 0 V. Current limit reached and hiccup mode occurs.	В
CS	18	V <sub>OUT</sub> = 0 V	В
FB	10	If FB = VDDA, then $V_{OUT} = 0$ V.	D
	19	If FB = GND, then $V_{OUT}$ = 5 V.	В
COMP	20	V <sub>OUT</sub> = 0 V	В
PG	21	V <sub>PG</sub> = 0 V. V <sub>OUT</sub> = expected	С
SS	22	V <sub>OUT</sub> = 0 V	С
EN	23	V <sub>OUT</sub> = 0 V. The LM25141 is disabled and enters shutdown.	С
RES	24	V <sub>OUT</sub> = expected. The LM25141 cannot exit hiccup mode.	С

#### Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

### Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	Diode emulation/FPWM mode undefined. V <sub>OUT</sub> = expected, erratic switching	С
VDDA	2	V <sub>OUT</sub> = 0 V. Poor noise immunity	С
AGND	3	V <sub>OUT</sub> = 0 V	В
RT	4	Normal operation. Frequency modulation feature is disabled. V <sub>OUT</sub> = expected	С
DITH	5	V <sub>OUT</sub> = expected	С
OSC	6	F <sub>SW</sub> 440 kHz or 2.2 MHz. V <sub>OUT</sub> = expected	С
LOL	7	V <sub>OUT</sub> = 0 V. No discharge path for low-side MOSFET gate	В
LO	8	V <sub>OUT</sub> = expected. Lower efficiency	С
PGND	9	V <sub>OUT</sub> = 0 V. Uncontrolled behavior because of floating ground	В
VCC	10	V <sub>OUT</sub> = 0 V	В
HB	11	V <sub>OUT</sub> = 0 V. High-side gate drive floating	В
SW	12	V <sub>OUT</sub> = VIN. High-side FET control floating	В
НО	13	V <sub>OUT</sub> = 0 V. Will not regulate	В
HOL	14	V <sub>OUT</sub> = VIN. Will not regulate. Excessive current from VIN	В
VIN	15	V <sub>OUT</sub> = 0 V	В

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCX	16	V <sub>OUT</sub> = expected	D
VOUT	17	V <sub>OUT</sub> = oscillation. Will not regulate	В
CS	18	V <sub>OUT</sub> = oscillation. No overcurrent or current sense information for current mode control.	В
FB	19	V <sub>OUT</sub> will not regulate. The controller will be configured for adjustable output.	В
COMP	20	DUT = oscillation. Will not regulate	
PG	21	V <sub>OUT</sub> = expected. No PG information	С
SS	22	V <sub>OUT</sub> = expected	D
EN	23	V <sub>OUT</sub> = 0 V	В
RES	24	V <sub>OUT</sub> = expected. Will exit hiccup mode quickly because low parasitic capacitor value.	С

### Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

### Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	VDDA	V <sub>OUT</sub> = regulation, normal operation, and FPWM mode is enabled.	С
VDDA	2	AGND	V <sub>OUT</sub> = 0 V	В
AGND	3	RT	V <sub>OUT</sub> = regulation. Frequency modulation is disabled.	С
RT	4	DITH	V <sub>OUT</sub> = regulation. Frequency modulation is disabled.	С
DITH	5	OSC	V <sub>OUT</sub> = regulation. F <sub>SW</sub> = 440 kHz	С
OSC	6	LOL	V <sub>OUT</sub> = unregulated	В
LOL	7	LO	V <sub>OUT</sub> = expected	С
LO	8	PGND	V <sub>OUT</sub> = 0 V	В
PGND	9	VCC	V <sub>OUT</sub> = 0 V	В
VCC	10	HB	V <sub>OUT</sub> = 0 V	В
HB	11	SW	V <sub>OUT</sub> = 0 V. The VCC regulator is in current limit.	В
SW	12	НО	V <sub>OUT</sub> = 0 V	В
НО	13	HOL	V <sub>OUT</sub> = expected	В
HOL	14	VIN	V <sub>OUT</sub> = 0 V	A
VIN	15	VCCX	If $V_{VIN}$ > 6.5 V, then $V_{OUT}$ = 0 V. Exceeds the VCCX absolute maximum ratings	A
VCCX	16	VOUT	V <sub>OUT</sub> = expected	D
VUUX	10		If $V_{OUT}$ is > 6.5 V, then it exceeds the VCCX absolute maximum rating.	A
VOUT	17	CS	$V_{\text{OUT}}$ cannot regulate, current limit is disabled, and there is no current sense information.	В
CS	18	FB	If FB = VDDA, then $V_{OUT}$ = 3.3 V.	В
03	10	ГО	If FB = GND, then V <sub>OUT</sub> = 0 V. Excessive current from VIN	В
FB	19	COMP	If FB = VDDA, then V <sub>OUT</sub> = VIN.	A
ГD	19	COMP	If FB = GND, then $V_{OUT}$ = 0 V.	В
COMP	20	PG	V <sub>OUT</sub> = 0 V	В
PG	21	SS	V <sub>OUT</sub> = 0 V	В
SS	22	EN	If $V_{EN}$ > 6.5 V, then it will exceed the absolute maximum rating of the SS pin. $V_{OUT}$ = 0 V	A
EN	23	RES	If $V_{EN}$ > 6.5 V, then it will exceed the absolute maximum rating of the SS pin. $V_{OUT}$ = 0 V	A
RES	24	DEMB	If DEMB = GND, $V_{OUT}$ = regulation, then it will not restart if current limit is reached.	В
IXEO	24		If DEMB = VDDA, then $V_{OUT}$ = regulation. No hiccup mode	В

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
		If DEMB = GND, then V <sub>OUT</sub> = 0 V. Excessive current for VIN	В
DEMB	1	If DEMB = VDDA and $V_{VIN}$ < 6.5 V, then $V_{OUT}$ = expected and there is erratic switching.	В
		If $V_{VIN}$ > 6.5 V and exceeds the maximum rating of the DEMP pin, the device is damaged.	А
VDDA	2	If $V_{VIN}$ > 6.5 V, $V_{OUT}$ = 0 V, and exceeds the maximum rating of the VDDA pin, the device is damaged.	Α
	2	If $V_{VIN}$ < 6.5 V, then $V_{OUT}$ = expected.	D
AGND	3	High VIN current. V <sub>OUT</sub> = 0 V	В
RT	4	If $V_{VIN} < 6.5 \text{ V}$ , then $V_{OUT} = 0 \text{ V}$ .	В
		If $V_{VIN}$ > 6.5 V and exceeds the maximum ratings, then the device is damaged.	A
DITH	5	If V <sub>VIN</sub> > 6.5 V, the device is damaged.	A
		If $V_{VIN}$ < 6.5 V, <sub>OUT</sub> = expected. No spread spectrum	С
		If OSC = GND and high VIN current, then V <sub>OUT</sub> = 0 V.	В
OSC	6	If OSC = VDDA, VIN > 6.5 V, the device is damaged, and $V_{OUT}$ = 0 V.	A
		If OSC = VDDA, VIN < 6.5 V, $V_{OUT}$ = expected, and there is erratic switching.	С
LOL	7	If $V_{VIN}$ < 6.5 V, $V_{OUT}$ = 0 V and there is excessive current from VIN.	В
LOL	1	If $V_{VIN}$ > 6.5 V, exceeds the maximum ratings for the LO pin and the device is damaged.	A
10	8	If $V_{VIN}$ < 6.5 V, $V_{OUT}$ = 0 V and there is excessive current from VIN.	В
LO	0	If $V_{VIN}$ > 6.5 V, exceeds the maximum ratings for the LOL pin, the device is damaged	A
PGND	9	V <sub>OUT</sub> = 0 V. Excessive current from VIN	В
NCC	10	If V <sub>VIN</sub> < 6.5 V, then V <sub>OUT</sub> = expected.	D
VCC	10	If $V_{VIN}$ > 6.5 V, exceeds the maximum ratings and the device is damaged.	Α
	44	If $V_{VIN}$ < 6.5 V, then $V_{OUT}$ = expected and there is erratic switching.	В
HB	11	If $V_{VIN}$ > 6.5 V, exceeds the maximum rating the device is damaged and $V_{OUT}$ = VIN.	Α
SW	12	V <sub>OUT</sub> = VIN. Excessive current from VIN	Α
110	40	If V <sub>VIN</sub> < 6.5 V, V <sub>OUT</sub> drops lower than VIN, no switching, and excessive current from VIN.	В
НО	13	If $V_{VIN}$ > 6.5 V, exceeds maximum ratings of the HO pin, the device is damaged, and $V_{OUT}$ = VIN.	Α
		If V <sub>VIN</sub> < 6.5 V, V <sub>OUT</sub> drops lower than VIN, no switching, and excessive current from VIN.	
HOL	14	If V <sub>VIN</sub> > 6.5 V, exceeds maximum ratings of the HO pin, the device is damaged, and V <sub>OUT</sub> = VIN.	— В
VIN	15	N/A	В
	10	For VCCX = VOUT, $V_{IN}$ < 6.5 V and $V_{OUT}$ = VIN.	В
VCCX	16	If V <sub>VIN</sub> > 6.5 V, it exceeds the VCCX pin maximum rated voltage and the LM25141 is damaged.	A
VOUT	47	If $V_{VIN} < 15.5 V$ , VOUT = VIN.	В
VOUT	17	If V <sub>VIN</sub> > 15.5 V and exceeds the maximum rating, the LM25141 is damaged.	A
		$V_{VIN} < 6.5 V. V_{OUT} = VIN$	В
CS		If V <sub>VIN</sub> > 15.5 V and exceeds the maximum rating, the LM25141 is damaged.	A
		If $V_{VIN}$ < 6.5 V, FB = VDDA, then $V_{OUT}$ = expected.	В
FB	19	If V <sub>VIN</sub> < 6.5 V, FB = GND, then V <sub>OUT</sub> = 0 V. Excessive current from VIN	В
		If $V_{VIN}$ > 6.5 V and exceeds the maximum ratings, the LM25141 is damaged.	A
		If $V_{VIN} > 5 V$ and $< 6.5 V$ , $V_{OUT} = 0 V$	В
COMP	20	If $V_{VIN}$ > 6.5 V and exceeds the maximum ratings, the LM25141 is damaged.	A
	<u> </u>	If V <sub>VIN</sub> < 6.5 V, V <sub>OUT</sub> = expected and PG forced high.	В
PG	21	If $V_{VIN}$ > 6.5 V and exceeds the maximum ratings, the LM25141 is damaged.	A
		If V <sub>VIN</sub> < 6.5 V, then V <sub>OUT</sub> = expected.	D
SS	22	If $V_{VIN}$ > 6.5 V and exceeds the maximum ratings, the LM25141 is damaged.	A
EN	23	V <sub>OUT</sub> = expected	D

#### Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN



Table 4 0.1 In Third for Betrice This enout encated to Vity (continued)				
Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class	
RES	$If V_{VIN} < 6.5 V, V_{OUT} = expect$	If $V_{VIN}$ < 6.5 V, $V_{OUT}$ = expected. No hiccup mode	С	
	24	If $V_{VIN}$ > 6.5 V and exceeds the maximum ratings, the LM25141 is damaged.	А	

### Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

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