Application Note

Impact of Narrow Pulse Widths in Gate Driver Circuits

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ABSTRACT

In high power, high frequency power topologies, noise coupling from supply, gate, or input ringing can cause unpredictable gate driver behavior which sometimes lead to glitches and failure. Extreme duty cycles (either close to 0 or close to 100%), with tens of nanoseconds of ON or OFF time duration can aggravate the ringing and overshoot that harm internal gate drive circuits that can lead to electrical overstress (EOS). Engineers often overlook these severe duty cycle conditions in their designs because the stressful effects to the gate driver are not obvious. The goal of this application note is to introduce the concept of narrow input pulses, show the impact on the gate drive circuitry, and discuss system factors that influence the behavior. In the end, it is shown how the pulse width limitation in your specific system can be defined, and approaches are suggested to limit the impact on the system.

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Trademarks

1 Introduction

A typical MOSFET turn-on and turn-off periods are shown in Figure 1-1. The goal for the gate driver is to reach a given MOSFET's target gate-to-source voltage (V_{GS}) by charging up the gate of the MOSFET, through a minimum gate threshold voltage (V_{TH}) and apply the maximum drive strength during the miller plateau region to charge the gate to the maximum drive voltage. A complete transition is achieved when the target V_{GS} is met and no gate current (I_G) flows to charge the external load. This defines the minimum pulse width, PW_{min}, for an ON-transition. For an OFF-transition, the procedure goes in reverse but the defined minimum pulse width is when V_{GS} = 0V and I_G = 0A. Zero Current Switching (ZCS) is achieved when I_G = 0A and is the good target when transitioning between ON/OFF or OFF/ON transitions for the gate driver.

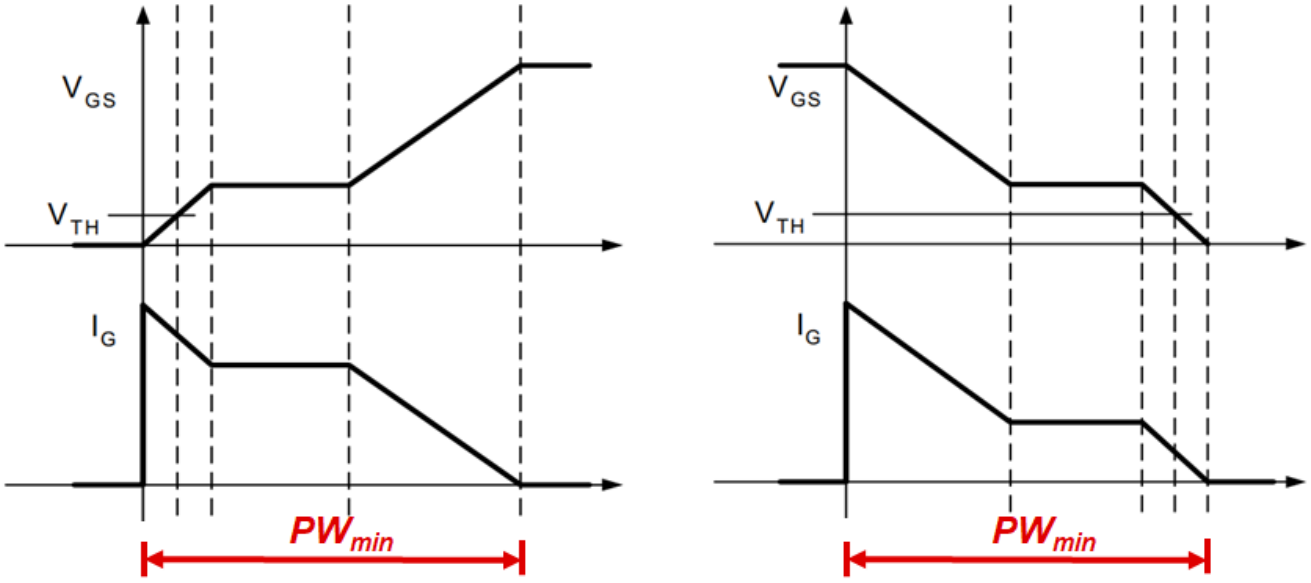

Figure 1-1. MOSFET Gate Turn ON and OFF Period

Table 1-1. Minimum Pulse Width Specification in Data Sheet

Parameter		Test Condition	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise , 20% 80% measured points	C_{out}= 1.8nF		6	16	ns
t_{FALL}	Output fall time, 90% to 10% measured points	C_{out}= 1.8nF		7	12	ns
t_{PWmin}	Minimum pulse width	Output off for less than minimum C_{out}= 0pF			20	ns

It is important to note that the minimum pulse width specification in a data sheet only describes the ability of an UNLOADED driver (C_{OUT}=0pF) to produce an output pulse from an input of at least the specified width and is not an indication of the pulse minimum width for robust, reliable operation for the gate driver.

A typical application can have a load on the gate driver and often operates at the recommended maximum VDD voltage. Under these conditions, the minimum pulse required by the driver IC can be 4 to 5 times larger than this specification defined at no load.

Each application can have a different minimum pulse width that can be reliably applied to the gate driver. There are a few variables that can impact the minimum pulse that can be applied. These factors include: the gate capacitance, VDD supply voltage, series resistance (R_G), peak current (I_{pk}), and PCB layout parasitic.

2 When Can Extreme Narrow Input Pulses Happen in a Power Stage?

AC/DC power supplies are widely used to transform grid side AC input voltage to stable DC voltage in personal electronics, industrial and automotive applications. A Power Factor Correction (PFC) stage is incorporated to reduce harmonics and protect the grid. In Totem Pole PFC configurations and three phase full bridge PFC designs, there are very short duty cycles with fast switching MOSFETs at every AC input zero crossing. Some engineers also implement a soft start at zero crossings to avoid large current spikes. In this type of design, the duty cycle of power switch can be commanded to a very low value upon restart after a zero crossing.

In hard switching DC/DC converter systems, the output voltage can fluctuate during load transients, either from no load to high load, or high load to low load. Under these conditions, primary driver can send extreme low or high duty cycles command to adjust to the outer voltage loop feedback signal.

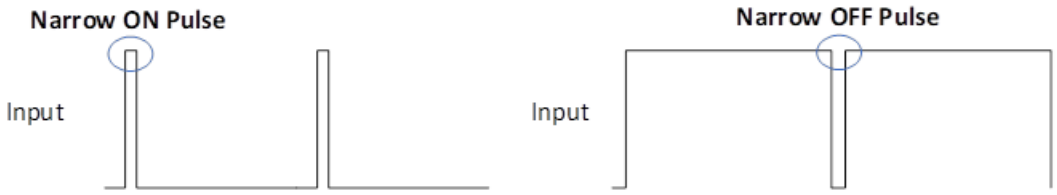

Figure 2-1. Narrow On Pulse and Narrow OFF Pulse

3 How Narrow Input Pulse Widths Threaten the Gate Driver

Gate drivers sink and source current when switching the gate of a MOSFET. There's a pull-up and pull-down structure inside the device, which buffers the input signal and provides sufficient current to charge and discharge the gate capacitance. Figure 3-1 shows an example of an output structure where a parallel combination of a PMOS and NMOS device enable the output for the gate driver.

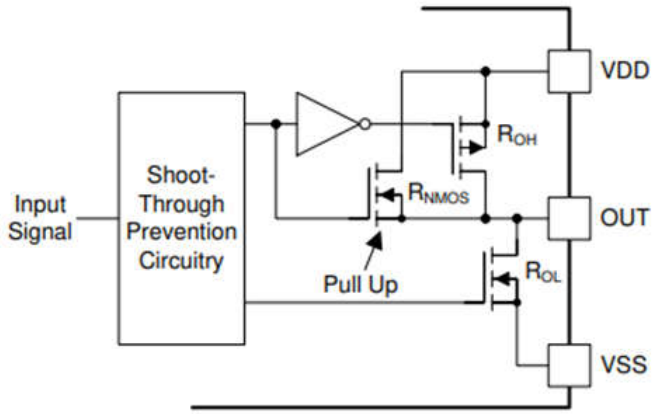

Figure 3-1. Example Gate Driver Output Stage (for one Channel)

In the narrow ON pulse scenario, the MOSFET turn-on procedure has not completed when the driver receives the OFF command, and the internal totem-pole pull-up stage is still continually conducting a very high current (I_G >> 0).

In a real-world gate drive circuit, the inductance *Lpcb* of Figure 3-2 in series with VDD can be large due to parasitic PCB trace inductance. When combined with internal driver parasitic inductance from the bond wires, the total inductance on at VDD can often be over 10nH. When the drive current suddenly gets cut off, a large parasitic inductance can cause significant voltage spikes (Vspike= L di/dt), which can lead to voltage exceeding the recommended operating conditions, even going beyond the absolute maximum rating in some cases.

Note

Voltage at pin is typically much lower than that seen at drain of internal FET.

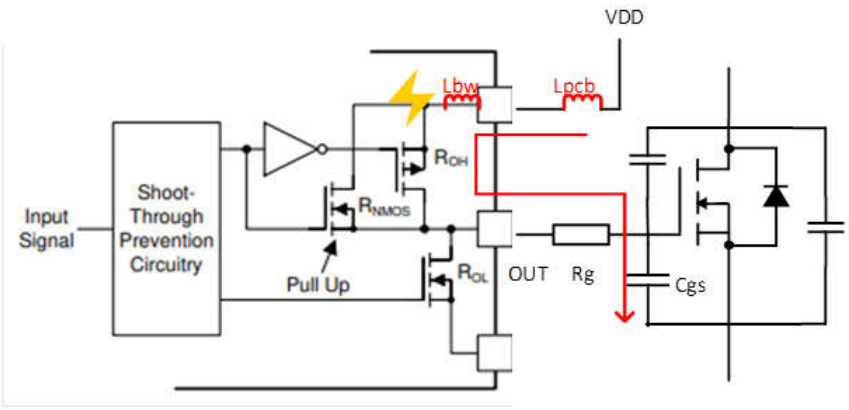

Figure 3-2. Gate Turn on Current Path and Parasitic

As discussed in the previous section, the gate driver can experience a short input pulse width at every AC zero crossing for a typical totem pole PFC circuit. In the end equipment lifetime, narrow pulse events can happen hundreds of millions of times. Therefore, narrow input pulses can become a hidden risk for a project. Exceeding the maximum VDD or VOUT voltage might not lead to a sudden failure during the project development phase, but repetitive operating outside device SOA can cause early degradation and premature damage of a gate driver.

Similarly, the narrow OFF input pulse (close to 100% duty) might also lead to overstress of OUT and VDD. In the narrow OFF pulse scenario, the MOSFET turn-off procedure has not completed when the driver receives the ON command, and the internal totem-pole pull-down stage is still continually conducting very high current (I_G >> 0). The large parasitic inductance and sudden current change can cause significant voltage spikes on output pin. When the OUT voltage is higher than VDD voltage, it can further stress the VDD pin as well.

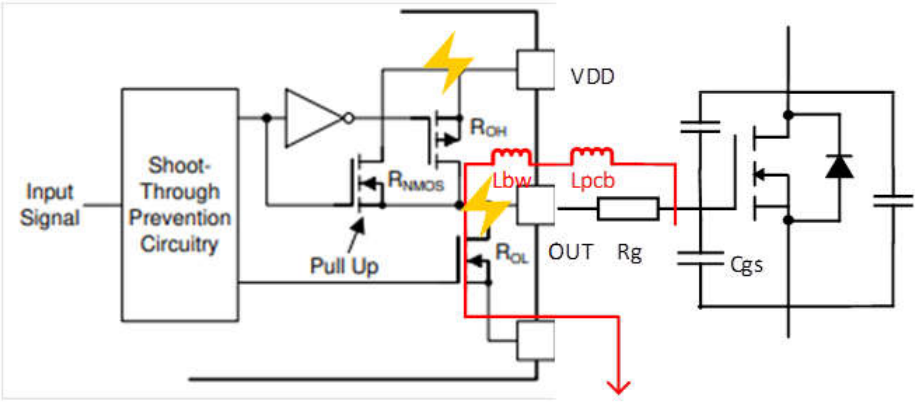

Figure 3-3. Gate Turn Off Current Path and Parasitic

4 Which System Factors Can Influence the Result

Although a narrow input pulse width scenario can be destructive from a product lifetime point of view and must be avoided, it is hard to provide an exact value of minimum input pulse width even for a known operating condition. This is because of the numerous variables like PCB layout and decoupling capacitor placement can affect the internal voltage spike significantly. However, some simple math can provide a starting point for estimating the minimum pulse width that can be applied to the gate driver input in a given system.

For the narrow on pulse scenario, internal VDD pad voltage can be assumed from Equation 1.

$$VDD_{internal} = VDD_{supply} + \left(L_{bondwire} + L_{PCB}\right)\frac{dI}{dt} \quad (1)$$

Where:

- VDD_{supply} refers to bias power voltage which is used to supply the gate drive circuit, normally from flyback for the high voltage topology.
- $L_{bondwire}$ refers to the IC internal bond wire parasitic inductance, usually around 5nH.
- L_{PCB} refers to the external PCB trace parasitic from supply to the pinout.

We can see several factors that can impact the internal overvoltage stress during narrow on pulse event, but the most important factor is the gate drive current at the switch OFF moment. Everything that increases the gate drive strength can also increase the $\frac{dI}{dt}$ which includes a larger gate voltage bias, small gate resistor (R_G), and larger gate capacitance. Most importantly, the gate current is not flat and linear during MOSFET turning on as shown in Figure 1-1, so the earlier MOSFET switches off, the larger the voltage spike that can be induced.

Narrow OFF pulse voltage spike estimation is a little bit more complicated. When the gate driver receives the turn ON command when the turn off period has not completed, the output voltage has not declined to zero. When the sinking current is interrupted, the spike seen on the Internal OUT pad is increased by the voltage drop across the PCB parasitic and bond wire inductance.

$$OUT_{internal} = max\{VDD_{internal}, V_{gate} + \left(L_{bondwire} + L_{PCB}\right)dI/dt\} \quad (2)$$

Where:

- $VDD_{internal}$ refers to the internal VDD pad voltage.
- V_{gate}t is the gate driver output, it is also the gate voltage of the MOSFET. This voltage decrease as the off pulse extends and gate discharges.
- $L_{bondwire}$ refers to the IC internal bond wire parasitic inductance, usually around 5nH.
- L_{PCB} refers to the external PCB trace parasitic from supply to the pinout.

When the off pulse is very short, $V_{gate} + \left(L_{bondwire} + L_{PCB}\right)\frac{dI}{dt}$ is higher than internal VDD pad voltage.

As the off pulse extends, $V_{gate} + \left(L_{bondwire} + L_{PCB}\right)\frac{dI}{dt}$ slowly decreases and the output follows the VDD internal voltage instead.

5 How do you Know Whether Your System Should Limit Narrow Pulses?

The table below shows some common scenarios within the gate driver that can make the system design more susceptible to narrow pulses along with some mitigation tactics to consider.

Table 5-1. Table of Scenarios Susceptible to Narrow Pulses

Gate Driver Scenarios Susceptible to Narrow Pulse		Mitigation
Gate resistance (R_G)	Having a low R_G can lead to a higher di/dt.	Size R_G to help limit the di/dt for the gate driver.
External VDD	Having a higher External VDD can leave lower margin in case of a narrow pulse that can exceed the absolute maximum rating for the device.	Consider limiting VDD range in the application.
Decoupling capacitor placement	Placing decoupling capacitors far away from the gate driver pins has a negative impact and can increase the parasitic trace inductance in the system.	Place decoupling capacitors as close the gate driver as possible to reduce parasitic inductance. Consult the TI data sheet for layout recommendations.

As discussed in the previous section, the high $\frac{dI}{dt}$ coupled with parasitic inductance is the most important and easiest factor to control to avoid voltage spikes for narrow input commands. Extending the pulse width to make sure gate drive current has dropped close to zero can effectively minimize the change in current, $\frac{dI}{dt}$.

One way to determine the minimum pulse width for your system is to monitor the MOSFET V_{GS} voltage to decide whether the turn-ON or turn-OFF transition has completed. To make sure that negative impacts of narrow pulses do not cause damage to the gate driver, the primary recommendation is to have the driver output rise to higher than 90% of VDD before changing states again to achieve a *Zero Current Switching* for the turn-on.

In the case of a turn-off pulse, have the output fall to less than 10% of VDD before turning back on. This can make sure that large voltage spikes are not generated due to non-zero current switching of a high current in the presence of inductive parasitic on the PCB and in component package connections.

Figure 5-1 shows the relationship between VOUT, IOUT, Internal VDD of the gate driver, and a range of pulse widths to show the time required for a complete transition. In this example, the minimum pulse width of 40ns has IOUT low to achieve ZCS. In the case of 10ns pulse width, IOUT is being supplied near maximum output current and VOUT has not completed a full ON transition. The parasitic inductance can cause a high voltage spike internally to the gate driver that can cause the internal VDD to exceed the absolute maximum VDD voltage that the gate driver. Damage to the gate driver might not be seen immediately, but violating the absolute maximum ratings of the device can impact the integrity of the internal circuitry and degrade to the point of failure or physical damage to the IC induced from electrical overstress.

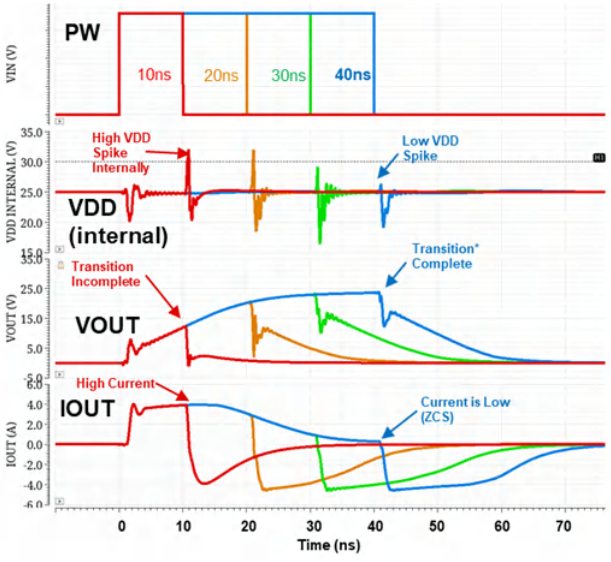

Figure 5-1. V_{out} and VDD Internal Voltage as on Pulse Extends

6 Summary

Some high voltage, high frequency applications scenarios do expose the gate driver to short input pulses and it is important for system designer to understand the impact of non-zero current switching from applying narrow pulses that can lead to internal stresses of the gate drive which can lead to damage of components inside the gate driver. To make sure safe operation, a complete transition is achieved when the V_{GS} = VDD is met and no I_G current flows to charge the external load. For the turn-ON condition, the recommendation is to have the driver output rise to higher than 90% of VDD before changing states again to achieve a *Zero Current Switching*. In the case of a turn-off pulse, have the output fall to less than 10% of VDD before turning back on. This will make sure that large voltage spikes are not generated due to non-zero current switching of a high current in the presence of inductive parasitic on the PCB and in component package connections. In addition, sizing R_G to help limit the di/dt for the gate driver, providing enough margin between VDD abs max and the operating condition, and proper decoupling capacitor placements can help mitigate issues in the driver from narrow pulses.

7 References

- Texas Instruments, UCC21520-Q1, product folder.
- Texas Instruments, UCC21530-Q1, product folder.

8 Revision History

Changes from Revision * (December 2023) to Revision A (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *Cout=9pF* to *Cout=0pF*	2

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