Application Note

Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part II: Hybrid Sense Network Design for Stability

Andrew Xiong, Miranda Gu

ABSTRACT

In power design for applications such as ADC, RF transceiver and analog front end (AFE), output voltage ripple is an important factor for power quality evaluation. In previous DC-DC power supply, two-stage power design, including buck converter and LDO, are normally used to support low output voltage ripple requirement. In recent years, a type of power design using buck converter and secondary stage passive filter attracts more attention. Compared with conventional design with LDO, reduced design size and total efficiency improvement can be achieved. But a pair of conjugate poles can be introduced by the added passive filter, which threatens the loop stability.

In *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part I: Filter Design for Output Ripple Reduction* application note, the second stage filter components selection method to achieve required output voltage ripple is introduced. In Part II, the hybrid sense network design method for stability is further studied. The loop response of peak current mode converter with second stage filter is analyzed at first. On the basis, the stability design method is proposed. Finally, an application design flow is proposed and it is verified by experiments with TPS62933F.

Table of Contents

Trademarks

1 Introduction

For the power of signal processing system design using ADCs, PLLs and RF transceivers, low output voltage ripple is an important factor for power quality evaluation. In some power design designed to achieve low output voltage ripple, normally a buck converter is used for voltage step down as first stage and an LDO is used to filter ripple as second stage. However, the BOM cost, design size and conversion efficiency can cause concern in some compact or cost-effective application.

In recent years, a new low ripple power design attracts more attention by using a secondary stage passive LC filter combined with buck converter. Compared with conventional design with LDO, reduced design size and efficiency improvement can be achieved. See *Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter* application note. But a pair of conjugate poles can be introduced by the added passive filter, which threatens the loop stability.

After adding second stage filter, different feedback sense networks can cause different impacts on loop stability. The schemes of feedback are divided into three types in this *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part I: Filter Design for Output Ripple Reduction* application note: first stage sense, second stage sense and hybrid sense. In this paper, the advantages and disadvantages of those three types of feedback sense are compared at first. And hybrid sense is selected as the recommended feedback sense network due to the good performance on load regulation and loop stability. On the basis, the loop response of peak current mode buck regulator with hybrid sense is analyzed and the stability design method is proposed. Combined with the second stage filter components selection restriction in Part I, the application design flow of PCM converter based low ripple power design is proposed. At last, the design method proposed in this application note is verified by experiments with TPS62933F, *TPS6293x 3.8-V to 30-V, 2-A, 3-A Synchronous Buck Converters in a SOT583 Package*. The *TPS62933F Low-Output-Ripple Power Supply With Second Stage Filter Reference Design* including schematic and PCB layout design based on the proposed design method.

To be noted, the method proposed in this application note can only be used as a reference material. Due to the simplification in deduction and non-designed for factors in reality, the calculated results can have difference with bench test.

2 Comparison of Feedback Sense Methods with Second Stage Filter

Figure 2-1 to Figure 2-3 show the schemes of power designs with second stage filter, correspond to the power designs with first stage sense, second stage sense and hybrid sense. The advantages and disadvantages of each design are summarized in the following:

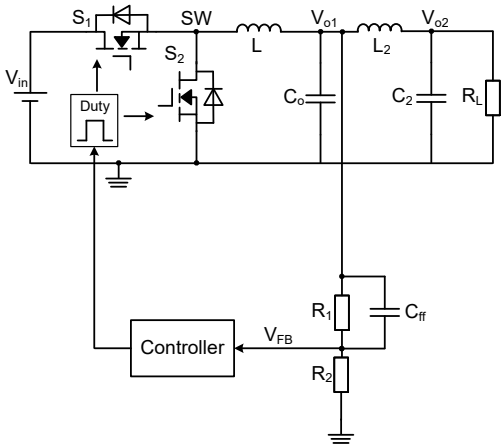

Figure 2-1. Scheme of Converter Second Stage Filter Design with First Stage Sense

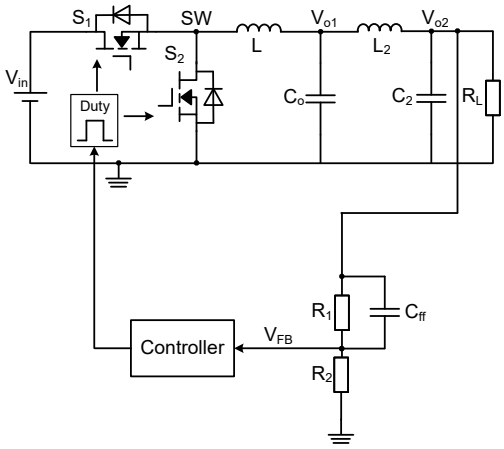

Figure 2-2. Scheme of Converter Second Stage Filter Design with Second Stage Sense

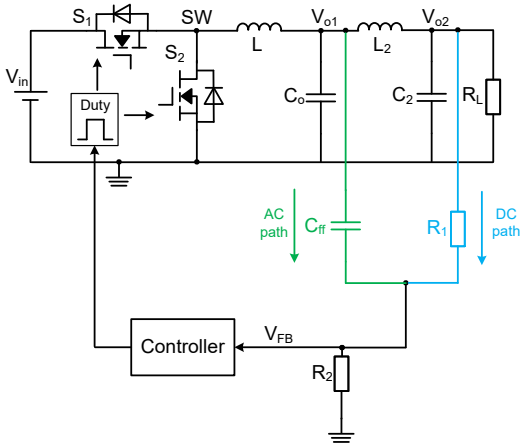

Figure 2-3. Scheme of Converter Second Stage Filter Design with Hybrid Sense

- With first stage sense, the feedback sense point is V_{o1} and the voltage drop on DCR of L_2 can't be compensated, so load regulation performance is worse. But the stability is good as the double poles of second stage filter are not included in the control loop.
- With second stage sense, the voltage drop on DCR of L_2 can be compensated. But the double poles of second stage filter can have obvious impacts on the loop response. When the values of L_2 and C_2 become larger, the double poles frequency of second stage filter reduces and can be closer to bandwidth, which can cause less phase margin and possible instability. That limits the maximum value of second stage filter components selection and the ability to reduce output ripple.
- With hybrid sense, the feed-forward capacitor C_{ff} is connected with V_{o1} and upper feedback resistor R_1 is connected with V_{o2}. The AC disturbance of V_{o1} can be coupled to V_{FB} and reduce the portion of V_{o2} AC disturbance in total feedback. That can help to reduce the effects of second stage filter on loop stability. And the load regulation performance is also good since the DC regulation is based on feedback from V_{o2}. So the loop stability and output accuracy can be made sure at the same time with the hybrid feedback sense.

Due to the obvious advantages of hybrid sense, the application design method in this application note is based on this sense approach.

3 Transfer Function Derivation of PCM Converter with Second Stage Filter and Hybrid Sense

Figure 3-1 shows the PCM buck converter including second stage filter and hybrid sense.

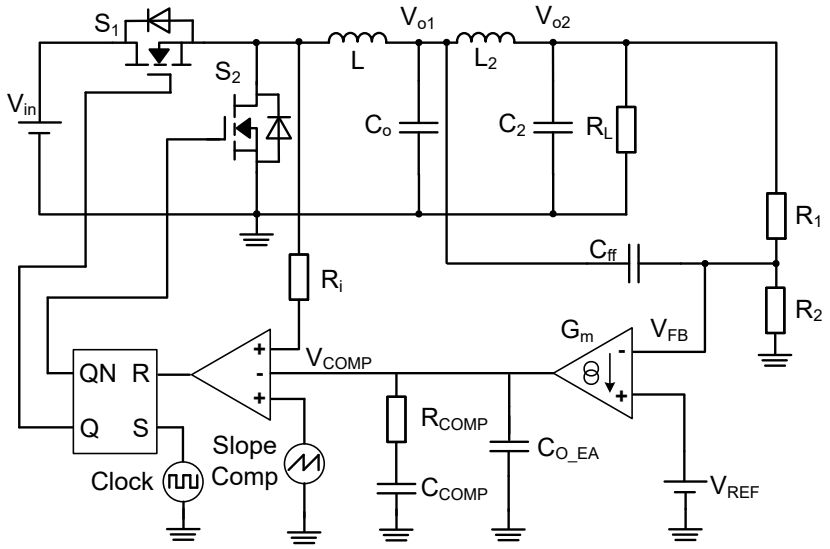

Figure 3-1. Simplified Schematic for PCM Buck Converter with Second Stage Filter and Hybrid Sense

Figure 3-2 is the overall control block diagram of PCM buck converter with second stage filter and hybrid sense. The variable notation refers to application note[5].

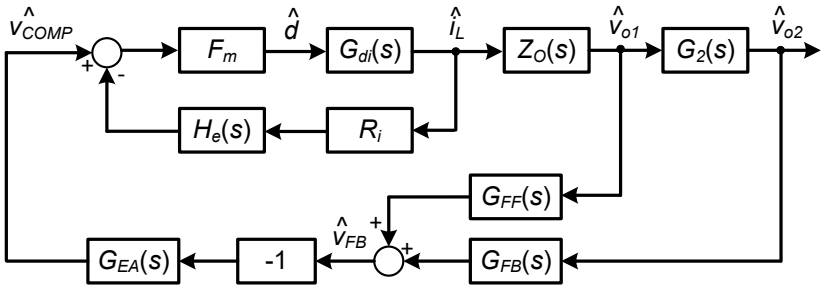

Figure 3-2. Control Implementation of PCM Buck Converter with Second Stage Filter and Hybrid Sense

Among all the variables, the meanings of below ones are same as normal PCM buck converter without second stage filter:

- G_{di} is the duty cycle to i_L transfer function.
- G_{EA} is the transfer function of the error amplifier with certain compensation.
- F_m is the gain of PCM PWM comparator.
- R_i is the current sensing resistor.
- H_e is the transfer function model of inductor current sampling-hold effect.

The following transfer functions are new added or the meanings are changed from normal buck converter without second stage filter:

- Z_O is the transfer function of output impedance (combining 1st stage and second stage filter).
- G_2 is the transfer function of second stage filter.
- G_{FF} is the transfer function of the feed-forward path for v_{o1} in feedback network.
- G_{FB} is the transfer function of the feedback path for v_{o2} in feedback network.

This application note does not introduce the derivation method of those transfer function expressions which have same meanings as normal PCM buck converter without second stage filter. The expressions are listed as Equation 1 to Equation 4.

$$G_{di}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}\approx\frac{V_{IN}}{sL} \quad (1)$$

$$G_{EA}(s)=\frac{\hat{v}_{COMP}(s)}{-\hat{v}_{FB}(s)}\approx\frac{G_m}{C_{COMP}}\frac{1+sR_{COMP}C_{COMP}}{s\left(1+sR_{COMP}C_{O\_EA}\right)} \quad (2)$$

$$F_m=\frac{f_{SW}}{S_n+S_e} \quad (3)$$

$$H_e(s)=\frac{s/f_{SW}}{e^{s/f_{SW}}-1}\approx 1-\frac{s}{2f_{SW}}+\frac{s^2}{(\pi f_{SW})^2} \quad (4)$$

where, S_n is the on-time slope of the sensed-current waveform and S_e is the external ramp slope.

$$S_n=R_i\frac{V_{IN}-V_O}{L} \quad (5)$$

$$S_e=V_{Se}\times f_{SW} \quad (6)$$

After adding second stage filter, the output impedance structure of buck converter changes from Figure 3-3 to Figure 3-4.

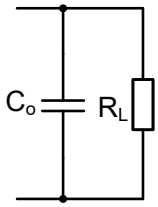

Figure 3-3. Output Impedance Structure with One Stage Filter

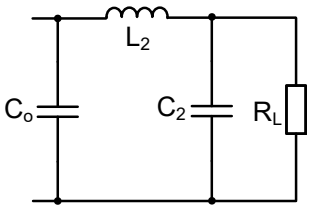

Figure 3-4. Output Impedance Structure with Two Stage Filter

Since the output capacitors used in the design of a low-ripple design is generally low-ESR MLCC, to simplify the derivation of the loop model, the capacitor ESR effect is ignored here. From Figure 3-4, we can get the expression of the output impedance Z_O of two stage filter as:

$$Z_O(s)=\frac{C_2L_2R_Ls^2+L_2s+R_L}{C_2C_OL_2R_Ls^3+C_OL_2s^2+(C_2+C_O)R_Ls+1} \quad (7)$$

G_2 reflects the low pass filter effects of second stage filter L_2 and C_2. The expression is:

$$G_2(s)=\frac{R_L}{C_2L_2R_Ls^2+L_2s+R_L} \quad (8)$$

The feedback signal V_{FB} includes V_{O1} information coupled through feed-forward path and V_{O2} information through feedback voltage divider. According to the superposition theorem, we can get:

$$G_{FF}(s)=\frac{\hat{v}_{FB}(s)}{\hat{v}_{O1}(s)}\Big|_{\hat{v}_{O2}(s)=0}=\frac{C_{ff}R_1R_2s}{C_{ff}R_1R_2s+R_1+R_2} \quad (9)$$

$$G_{FB}(s)=\frac{\hat{v}_{FB}(s)}{\hat{v}_{O2}(s)}|_{\hat{v}_{O1}(s)=0}=\frac{R_2}{C_{ff}R_1R_2s+R_1+R_2} \quad (10)$$

Based on the relation of Figure 3-2, it can be derived:

$$G_{FB\text{-}TOTAL}(s)=\frac{\hat{v}_{FB}(s)}{\hat{v}_{O1}(s)}=G_{FF}(s)+G_{FB}(s)G_2(s) \quad (11)$$

4 Overall Loop Model

After adding second stage filter, the transfer functions of the current inner loop are not changed from normal PCM buck converter. The expression of transfer function from control to inductor current G_{ci} is given in the Loop Response Considerations in Peak Current Mode Buck Converter Design application note:

$$G_{ci}(s)=\frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)}=\frac{1}{R_i}\frac{1}{1+s\times\left[\frac{V_{Se}f_{SW}L+(0.5V_{IN}-V_O)R_i}{V_{IN}R_if_{SW}}\right]} \quad (12)$$

To prevent sub-harmonic oscillation, it is necessary to avoid the existence of right-half-plane poles in the inner-loop closed-loop transfer function, so the inductance constraint range obtained according to Equation 12 is:

$$L>\frac{R_i(V_O-0.5V_{IN})}{V_{Se}f_{SW}} \quad (13)$$

Based on Figure 3-2, the open loop response of PCM buck converter with second stage filter and hybrid sense is:

$$G_{open}(s)=G_{EA}(s)\times G_{ci}(s)\times Z_O(s)\times G_{FB\text{-}TOTAL}(s) \quad (14)$$

Substituting Equation 11 to Equation 14, we can get the open loop transfer function as:

$$G_{open}(s)=G_{EA}(s)\times G_{ci}(s)\times Z_O(s)\times [G_{FF}(s)+G_{FB}(s)G_2(s)] \quad (15)$$

There is some simplification in the derivation of this small signal model, but it can mostly reflect the actual loop response, especially the response in middle frequency range near bandwidth affecting stability.

The small signal modeling accuracy is verified with TPS62933F under the operating condition: V_{in}=24V, V_{out}=1.2V, I_{out}=3A, F_{sw}=500kHz, L=2.2uH, C_o=90uF, L_2=20nH, C_2=47uF, R_1=5kohm, R_2=10kohm, C_{ff}=680pF.

The comparison of loop response between small signal model and simplis simulation for the converter with second stage filter is shown as Figure 4-1.

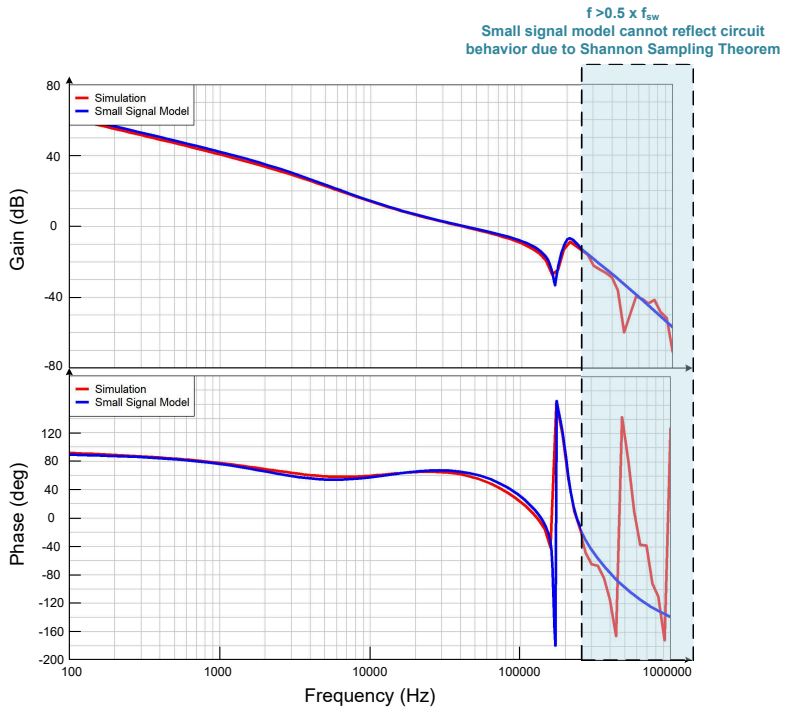

Figure 4-1. Comparison of Loop Response Between Small Signal Model and Simplis Simulation

5 Zero and Pole Analysis

The analysis about poles and zeros is introduced in the following. In the open loop transfer function Equation 15, the poles and zeros generated by $G_{EA}(s)$ and $G_{ci}(s)$ are the same as those in general purpose PCM buck converters without second stage filter.

$G_{EA}(s)$ with type II compensation consists of an initial pole with frequency close to zero $f_{P1\text{-}EA}$, a middle frequency zero $f_{Z\text{-}EA}$, and a high frequency pole $f_{P2\text{-}EA}$:

$$f_{Z\text{-}EA}=\frac{1}{2\pi R_{COMP}C_{COMP}} \tag{16}$$

$$f_{P2\text{-}EA}=\frac{1}{2\pi R_{COMP}C_{O\_EA}} \tag{17}$$

A pole is generated by $G_{ci}(s)$ and the frequency is:

$$f_{P\text{-}ci}=\frac{V_{IN}R_i f_{sw}}{2\pi[V_{Se}f_{sw}L+(0.5V_{IN}\text{-}V_O)R_i]} \tag{18}$$

For the rest of part in Equation 15, calculate $Z_O(s)$ x $G_{FB\text{-}TOTAL}(s)$ and we can get:

$$Z_O(s)\times G_{FB\text{-}TOTAL}(s)=\frac{R_2\left(R_L+C_{ff}R_1R_Ls+C_{ff}L_2R_1s^2+C_2C_{ff}L_2R_1R_Ls^3\right)}{(R_1+R_2+C_{ff}R_1R_2s)\left[C_2C_OL_2R_Ls^3+C_OL_2s^2+(C_2+C_O)R_Ls+1\right]} \tag{19}$$

As shown from the previous transfer function has four poles and three zeros. Among all the parameters, output load resistance R_L varies during operation when load current changes. Figure 5-1 reflects the frequency response with different R_L.

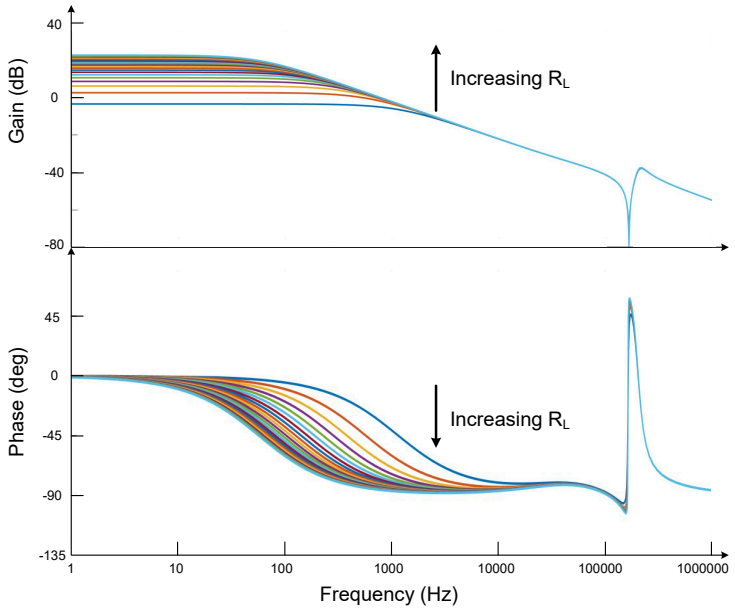

Figure 5-1. Frequency Response of Equation (19) with Different R_L

As shown in Figure 5-1, the middle frequency and high frequency responses with different R_L are almost same. While in the low frequency range, the response with larger R_L has smaller phase. For the power solution design with low bandwidth, that can cause less phase margin. Thus the larger R_L corresponds to worse case for stability.

To simplify Equation 19, consider the worst case when the output resistance is infinite R_L->+∞:

$$Z_O(s)\times G_{FB\text{-}TOTAL}(s)|_{R_L\to+\infty} \approx \frac{R_2\left(1+C_{ff}R_1s+C_2C_{ff}L_2R_1s^3\right)}{s(R_1+R_2+C_{ff}R_1R_2s)\left[C_2C_OL_2s^2+(C_2+C_O)\right]} \quad (20)$$

Figure 5-2 shows the map of zeros and poles of above transfer function.

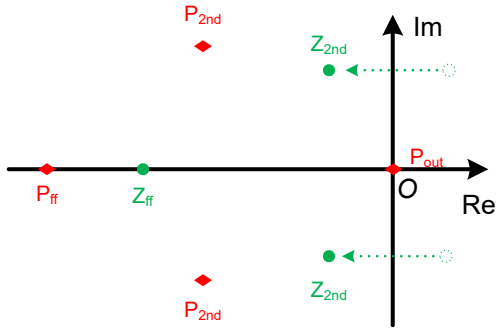

Figure 5-2. Location of Zeros and Poles in Equation (20)

The four poles in Equation 20 include an initial pole P_{out} whose frequency is 0Hz, a pole P_{ff} at frequency f_{Pff} and a pair of conjugate poles P_{2nd} at frequency $f_{P\text{-}2nd}$. Expression of f_{Pff} and $f_{P\text{-}2nd}$ are shown as Equation 21 and Equation 22:

$$f_{Pff}=\frac{1}{2\pi C_{ff}}\left(\frac{1}{R_1}+\frac{1}{R_2}\right) \quad (21)$$

$$f_{P\text{-}2nd}=\frac{1}{2\pi\sqrt{\frac{C_2C_O}{C_2+C_O}L_2}} \quad (22)$$

The three zeros in Equation 20 include a zero Z_{ff} at frequency f_{Zff} and a pair of conjugate zeros Z_{2nd} at frequency $f_{Z\text{-}2nd}$.

The expression of f_{Zff} is complicated as shown in Equation 23. And it can be proven that $f_{Zff}\le f_{Pff}$.

$$f_{Zff}=-\frac{1}{2\pi}\frac{5.67\times10^{15}\left(\sqrt{3}\sqrt{C_2^3C_{ff}^4L_2^3R_1^4\left(4C_{ff}^2R_1^2+27C_2L_2\right)}-9C_2^2C_{ff}^2L_2^2R_1^2\right)^{\frac{2}{3}}-1.3\times10^{16}C_2C_{ff}^2L_2R_1^2}{1.49\times10^{16}C_2C_{ff}L_2R_1\sqrt[3]{\sqrt{3}\sqrt{C_2^3C_{ff}^4L_2^3R_1^4\left(4C_{ff}^2R_1^2+27C_2L_2\right)}-9C_2^2C_{ff}^2L_2^2R_1^2}} \quad (23)$$

The conjugate zeros Z_{2nd} are located in the right half plane if considering L_2 as a designed for inductor with no DCR. But for the real inductor or ferrite bead with DCR of several mΩ or larger, the conjugate zeros normally move to left half plane with positive damping effects.

The expression of the conjugate zeros frequency $f_{Z\text{-}2nd}$ is too complicated. As an article to guide application design, the detailed mathematical analysis can not be applied here, since the conjugate zeros Z_{2nd} are not utilized for any important target like compensating phase margin in the following design guide.

Normally, the frequency $f_{Z\text{-}2nd}$ is smaller than $f_{P\text{-}2nd}$, and the they are close. With larger C_{ff}, the frequency $f_{Z\text{-}2nd}$ can be closer $f_{P\text{-}2nd}$. Figure 5-3 shows a typical gain response of PCM converter with second stage filter and hybrid sensing. The poles and zeros marked in red are newly introduced after adding the second stage filter.

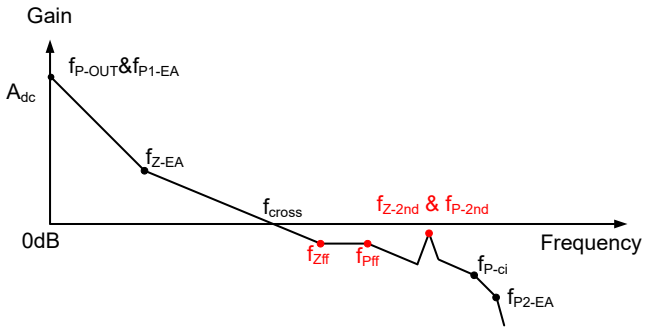

Figure 5-3. PCM Converter Loop Response with Second Stage Filter and Hybrid Sensing

6 Stability Design Method

To make sure of the system stability margin, the recommendation is that the loop gain needs to cross 0dB with -20dB/dec slope. By adjusting the frequencies of those poles and zeros shown in Figure 5-3, there can be many different approaches to achieve the target. This application note only proposes one simplified stability design method as reference.

1. $f_{Z-EA} < f_{cross}$, $f_{P-ci} > f_{cross}$ and $f_{P2-EA} > f_{cross}$

   In the stability design of normal PCM buck converter without 2nd stage filter, it's recommended to make f_{Z-EA} smaller than bandwidth f_{cross} and keep the f_{P-ci} & f_{P2-EA} larger than bandwidth, which can make loop gain cross 0dB with -20dB/dec slope [5-6]. Those design limitations are inherited in this design method.
2. Keep all the zeros and poles introduced by second stage filter out of bandwidth, including:
   - $f_{Zff} > f_{cross}$

     If the zero Z_{ff} is inside bandwidth, it can further increase converter bandwidth f_{cross} and improve dynamic response. But that would make it more difficult to estimate the bandwidth and cause more uncertainties. To simplify the stability design, $f_{Zff}>f_{cross}$ is given as a restriction. Typically, the bandwidth of PCM converter is set as $f_{cross}\leq f_{SW}/10$.

     Since the expression of f_{Zff} in Equation 23 is very complicated, an example of how to use Microsoft® Excel® or MATLAB® to calculate f_{Zff} is introduced in Appendix A.
   - $f_{P-2nd} > 2 \times f_{cross}$

     Recommend to keep $f_{P-2nd} > 2 \times f_{cross}$ to avoid effects of the conjugate poles on phase margin. Combined with Equation 22, the range of the 2nd stage filter capacitor C_2 can be derived as:

$$L_2 < \frac{\left(\frac{1}{C_2}+\frac{1}{C_O}\right)}{16\pi^2 f_{cross}^{\ 2}} \tag{24}$$

     The bandwidth f_{cross} with 2nd stage filter can be received with Equation 25.

$$f_{cross} \approx \frac{V_{ref} G_m R_{comp}}{2\pi V_{out} R_i (C_O + C_2)} \tag{25}$$

     For specific device TPS62933F, the bandwidth f_{cross} is:

$$f_{cross} \approx \frac{6.35}{V_{out}(C_O + C_2)} \tag{26}$$

3. Avoid second gain crossing through damping effects of L_2 DC resistance

   As mentioned in section 5, the conjugate zeros Z_{2nd} are located in the right half plane with negative damping, if considering L_2 as an designed for inductor with no DCR.

   The same effect for lack of damping also exists on the conjugate poles P_{2nd}. Those effects can cause resonance peak and loop gain may crosses 0dB twice, as shown in the case DCR_{L2}=0 of Figure 6-1.

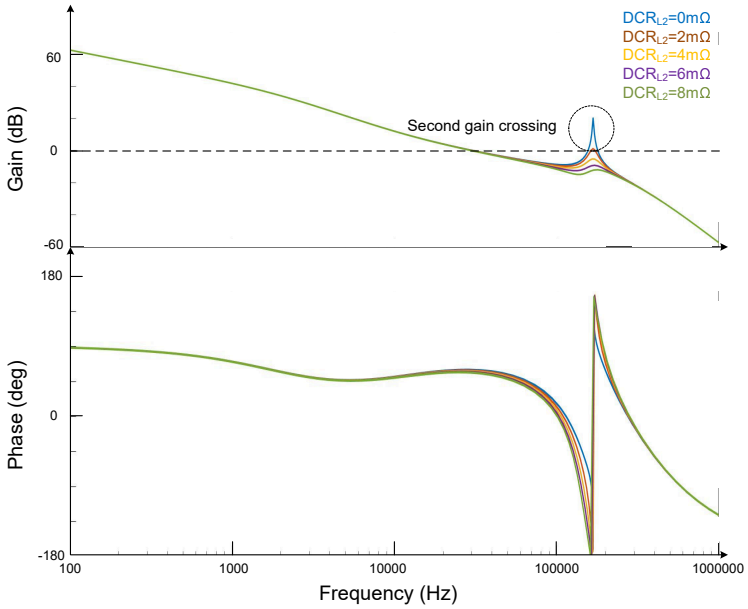

Figure 6-1. PCM Converter Loop Response with Second Stage Filter When Changing DCR_{L2}

The second gain crossing has a chance to cause system instability [7]. Like the example in Figure 6-1, increasing DCR_{L2} can effectively reduce the resonance peak amplitude and avoid second gain crossing. Increasing conjugate poles frequency f_{P-2nd} is another approach to avoid second gain crossing, like shown in Figure 6-2.

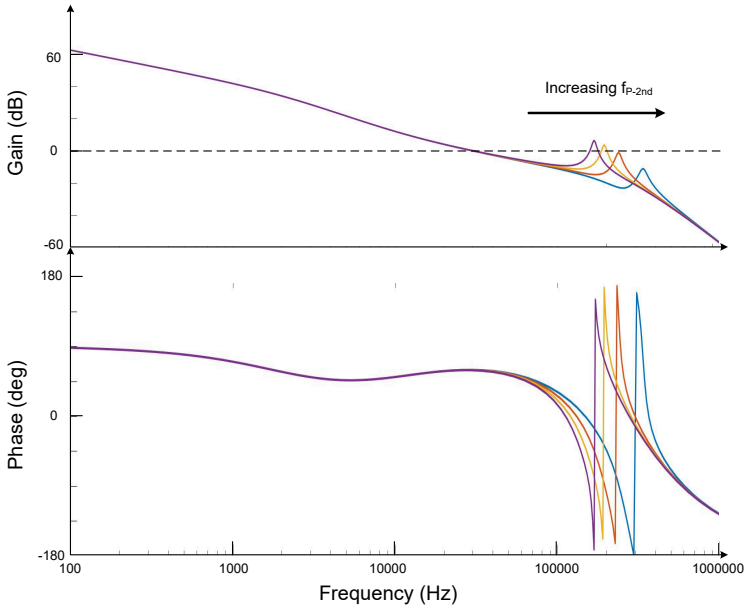

Figure 6-2. PCM Converter Loop Response with Second Stage Filter When Changing f_{P-2nd}

As second gain crossing does not normally happen with DCR_{L2} of real inductor or ferrite bead (several mΩ or larger), further mathematical analysis is not included in this application note. But the above two methods can be tried, if you already follow the design flow in next section, but there is still instability issue.

7 Design Example and Experimental Validation with TPS62933F

Figure 7-1 is a proposed design flow for PCM converter with second stage filter. All the inductance and capacitance used in calculation are effective value considering degrading.

To clarify, $f_{cross} \leq f_{SW}/10$ for (C_o+C_2) calculation in Figure 7-1 is a conservative restriction to simplify the design flow. The bandwidth can be set higher according to actual conditions.

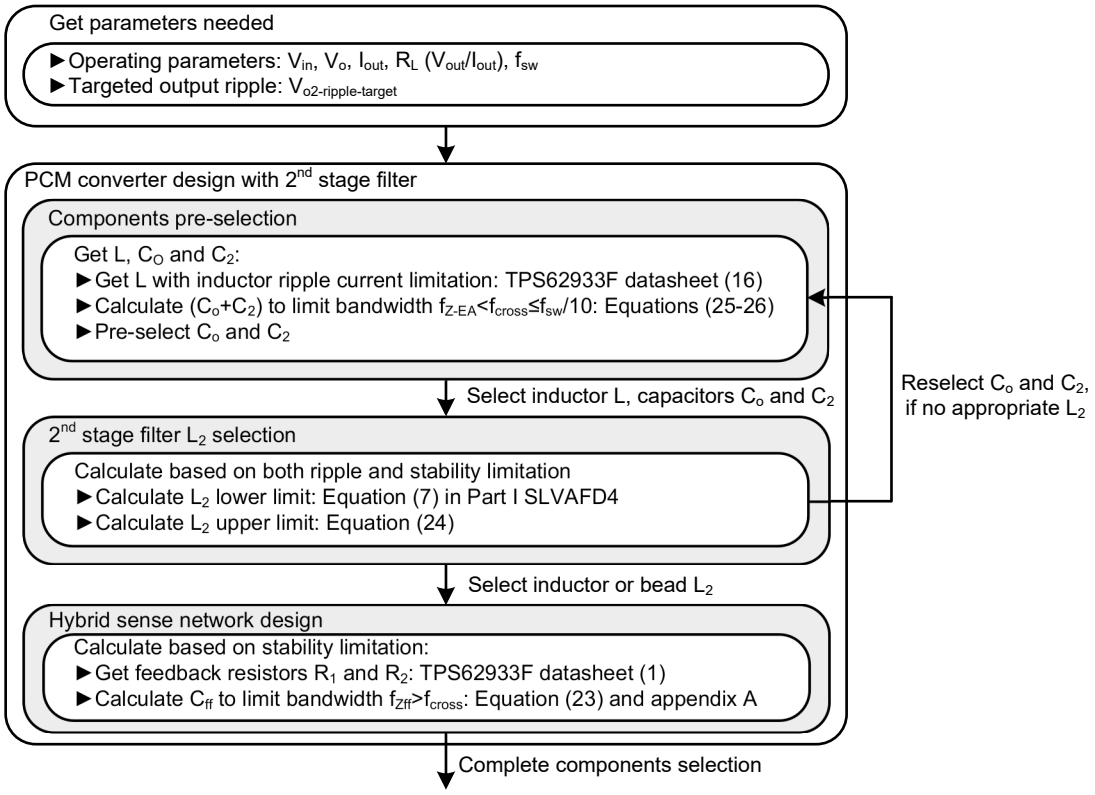

Figure 7-1. Design Flow Chart of PCM Converter with Second Stage Filter

A design example is given with operating condition as: Vin=24V, Vout=1.2V, f_{sw}=500kHz, I_{out}=3A. Targeted output ripple pk-pk amplitude $V_{o2\text{-}ripple\text{-}target}$ is smaller than 1mV.

Based on the Equation 16 in TPS62933F data sheet, L=2.2uH is selected with K=0.345 (K is the ripple ratio of the inductor current: ΔI_L / I_{OUT_MAX}).

With Equation 26 for TPS62933F, we can get the lower limitation of (C_o+C_2) as 105.8uF by setting f_{cross}=50kHz, which equals to $f_{SW}/10$. This set bandwidth is also much larger than $f_{Z\text{-}EA}$ of TPS62933F 10.6kHz[5].

Pre-select C_o=69uF (47uF+22uF) and C_2=47uF. The estimated f_{cross} is 45.6kHz with Equation 26.

Calculate L_2 lower limit with equation 7 in Part I SLVAFD4: $L_2 \geq 8.2$nH.

Calculate L_2 upper limit with Equation 24 in this application note: $L_2 < 109$nH.

Here we select two ferrite beads for verification of both limits: BLE18PS080SN1 with 15.3nH@1MHz close to lower limit and BLM18SN220TN1 with 103.4nH@1MHz close to upper limit.

For the feedback network, firstly select R_1=5kΩ and R_2=10kΩ following equation (1) in TPS62933F data sheet. Using the tool in appendix A for making $f_{Zff} > f_{cross}$, we can get C_{ff}=620pF corresponding to f_{Zff}=48.3kHz for the case with L_2=15.3nH, and C_{ff}=470pF corresponding to f_{Zff}=47.4kHz for the case with L_2=103.4nH.

Figure 7-2 to Figure 7-4 show the experimental verification results of the power design with BLE18PS080SN1. The ripple amplitude is within 1mVpp in Figure 7-3 and can satisfy the requirement. Figure 7-4 is the load transient waveform when changing output current from 0.75A (25% of 3A) to 2.25A (75% of 3A) with 2.5A/us slew rate, which shows the good loop response.

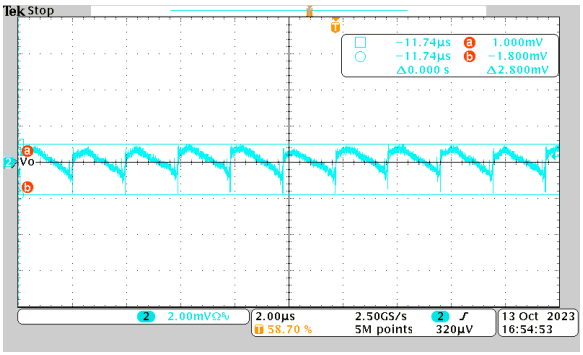

Figure 7-2. First Stage Output Voltage Ripple in the Case with BLE18PS080SN1 (L_2=15.3nH at 1MHz)

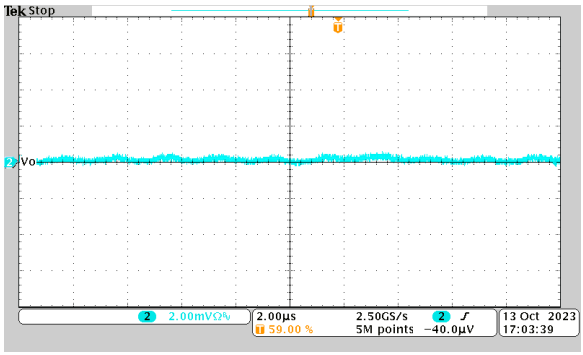

Figure 7-3. Second Stage Output Voltage Ripple in the Case with BLE18PS080SN1 (L_2=15.3nH at 1MHz)

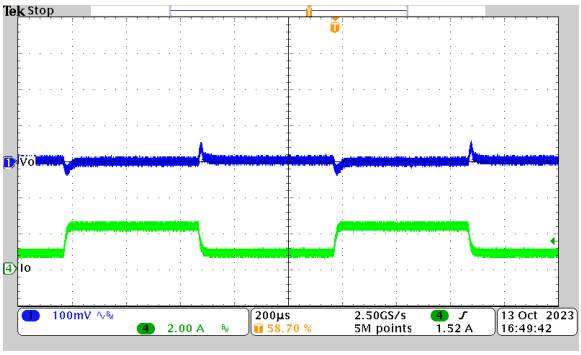

Figure 7-4. Load Transient Performance (0.75A/2.25A) in the Case with BLE18PS080SN1 (L_2=15.3nH at 1MHz)

Figure 7-5 to Figure 7-7 show the experimental verification results of the power design with BLM18SN220TN1. With larger L_2 value, the ripple amplitude is further reduced to within 1mVpp in Figure 7-6. Figure 7-7 is the load transient waveform when changing output current from 0.75A (25% of 3A) to 2.25A (75% of 3A) with 2.5A/us slew rate, which shows the good loop response. The details can be found in TI reference design 3.8V to 30V Input, 3A, 1.2V Low-Output-Ripple Power Supply With Second Stage Filter Reference Design.

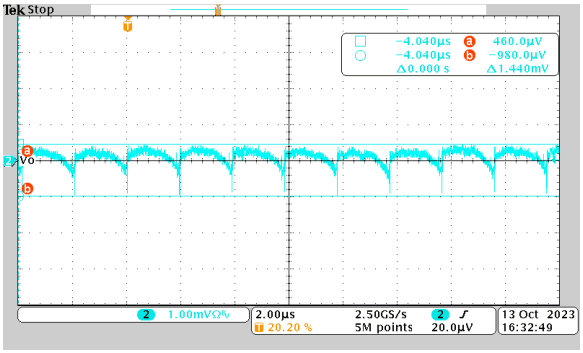

Figure 7-5. First Stage Output Voltage Ripple in the Case with BLM18SN220TN1 (L_2=103.4nH at 1MHz)

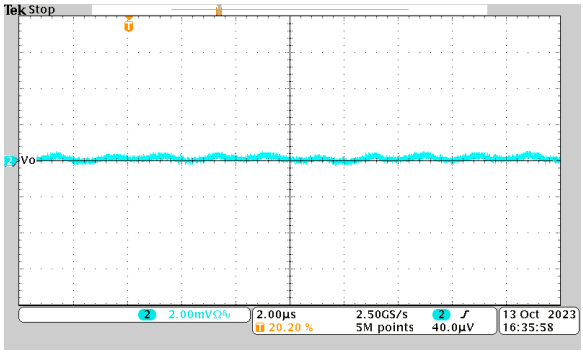

Figure 7-6. Second Stage Output Voltage Ripple in the Case with BLM18SN220TN1 (L_2=103.4nH at 1MHz)

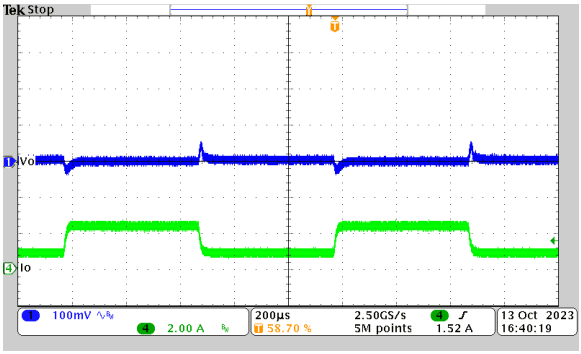

Figure 7-7. Load Transient Performance (0.75A/2.25A) in the Case with BLM18SN220TN1 (L_2=103.4nH at 1MHz)

8 Summary

A components selection method for second stage filter is proposed in this application note to make sure converter stability. Three types of feedback network design to support second stage filter are introduced at first and the advantages of hybrid sensing feedback is highlighted. On the basis, the loop response of peak current mode converter with second stage filter is analyzed at first. Then the expressions of zeros and poles introduced by second stage filter and hybrid sensing are derived through small signal analysis. The stability design method and low ripple power design flow are further proposed. Finally, the proposed method is verified by experiments.

9 References

1. Texas Instruments, *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part I: Filter Design for Output Ripple Reduction*, application note.
2. Texas Instruments, *Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter*, application note.
3. Texas Instruments, *TPS6293x 3.8-V to 30-V, 2-A, 3-A Synchronous Buck Converters in a SOT583 Package*, data sheet.
4. Texas Instruments, *TPS62933F Low-Output-Ripple Power Supply With Second Stage Filter Reference Design*.
5. Texas Instruments, *Loop Response Considerations in Peak Current Mode Buck Converter Design*, application note.
6. Texas Instruments, *Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part I: How to Select the Output Capacitor*, application note.
7. Texas Instruments, *Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part II: How to Select the Feedforward Capacitor*, application note.
8. https://www.ridleyengineering.com/hardware/ap310-analyzer/ap300-application/loop-stability-requirements.html

A Appendix

Example to use Excel or Matlab calculate f_{Zff}

If Excel is used, first input parameters following below format.

	A	B	C	D	E
1	R_1	C_2	L_2	Cff	fzff
2	5.00E+03	4.70E-05	1.53E-08	6.2E-10	

Figure A-1. Use Excel to calculate f_{Zff} Step1

Change the variable name of values A2-D2 as the values of A1-D1.

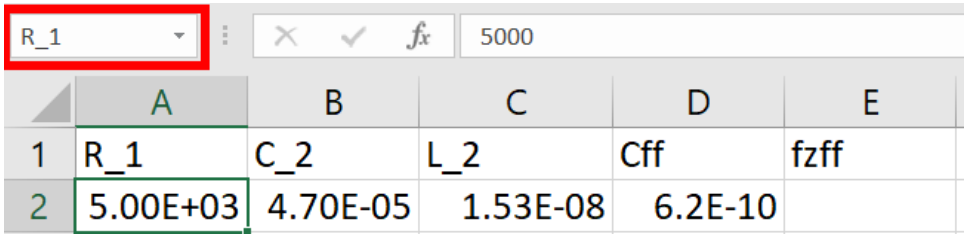

Figure A-2. Use Excel to calculate f_{Zff} Step2

Input equation in E2. Input "=" first, then copy and paste below contents:

```
-(5.67e15*(sqrt(3)*sqrt(C_2^3*Cff^4*L_2^3*R_1^4*(4*Cff^2*R_1^2+27*C_2*L_2))-9*C_2^2*Cff^2*L_2^2*R_1^2
)^(2/3)-1.3e16*C_2*Cff^2*L_2*R_1^2)/
(1.49e16*C_2*Cff*L_2*R_1*(sqrt(3)*sqrt(C_2^3*Cff^4*L_2^3*R_1^4*(4*Cff^2*R_1^2+27*C_2*L_2))-9*C_2^2*Cff
^2*L_2^2*R_1^2)^(1/3))/2/3.14
```

Then the f_{Zff} is calculated. And we can adjust C_{ff} to make $f_{Zff}>f_{cross}$.

	A	B	C	D	E
1	R_1	C_2	L_2	Cff	fzff
2	5.00E+03	4.70E-05	1.53E-08	6.2E-10	48258.1

Figure A-3. Use Excel to calculate f_{Zff} Step3

If Matlab is used, the following code can be used as an example:

```
clc
clear
R1=5e3;
C2=47e-6;
L2=15.3e-9;
Cff=620e-12;
fzff=-(5.67e15*(sqrt(3)*sqrt(C2^3*Cff^4*L2^3*R1^4*(4*Cff^2*R1^2+27*C2*L2))-9*C2^2*
Cff^2*L2^2*R1^2)^(2/3)-1.3e16*C2*Cff^2*L2*R1^2)/
(1.49e16*C2*Cff*L2*R1*(sqrt(3)*sqrt(C2^3*Cff^4*L2^3*R1^4*(4*Cff^2*R1^2+27*C2*L2))-
9*C2^2*Cff^2*L2^2*R1^2)^(1/3))/2/3.14
```

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265