TEXAS INSTRUMENTS

UCC2541 72-W Synchronous Buck Converter

User's Guide

February 2006

System Power MAN

SLUU239

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Literature Number: SLUU239
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1 Introduction

The UCC2541 is a voltage-mode synchronous-buck PWM controller for high current output converters of 30 A or higher. Higher efficiencies are achieved utilizing TI's proprietary Predictive Gate Drive™ technology. The UCC2541 is based on the parent device UCC2540 which is a secondary side post-regulator for isolated applications. This controller provides a bootstrap circuit to allow the use of an N-channel MOSFET as the topside buck switch, reducing conduction losses and increasing silicon device utilization. By controlling the turn-off and turn-on of the main and the synchronous switch, Predictive Gate Drive™ minimizes MOSFET body diode conduction and reverse recovery losses for higher efficiency, lower EMI and thermal improvements. This user's guide provides details on a single-phase synchronous-buck power converter with an input of nominal 12 V and an output of 1.8 V rated for 40-A continuous current output.

2 Applications

High Current (>30 A) Point-of-Load Converters for:

- Servers
- Telecom Equipment
- Power Supply Modules

3 Features

- V_{IN} = 9.0 V to 15 V
- V_{OUT} = 1.8 V +/–3%
- I_{OUT} = 0 A to 40 A
- Efficiency >80% at 40 A
- Output Voltage Ripple < 2%
- Power Semiconductor Devices
- Parallel MOSFETs for Higher Power
- External Synchronization Input
- Remote Shutdown Input

4 Electrical Performance Specification

Table 1. Electrical Performance Specification

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage	Over Io range	9	12	15	V
UVLO	Under-voltage lockout (mode 1)	V_{IN} increasing	8.0	8.5	9.0	
		V_{IN} decreasing	7.5	8.0	8.5	
		Hysteresis	0.3	0.5	0.8	
I_O	Output current	60°C, 200 LFM airflow 25°C, natural convection	0		40	A
f_S	Switching frequency		270	300	330	kHz
ΔREG_{LINE}	Line regulation	Over V_{IN} range			5	mV
ΔREG_{LOAD}	Load regulation	Over I_O range			5	
ΔREG_{TOT}	Total output variation	Includes set point, line, load			3	%
			1.746	1.800	1.854	V
η	Efficiency	Peak I_{OUT} = 15A, V_{IN} = 9 V		90%		
		Full-load I_{OUT} = 40 A, V_{IN} = 12 V		83%		
V_R	V_{OUT} ripple (pk-pk)	20-MHz bandwidth limited		2		$\%/V_O$
I_O	Over-current threshold	trip Reset, followed by auto-recovery		52		A
t_{TR}	Transient response	1 A/µs 10 to 90% $I_{O(max)}$		30		µs
ΔV_{TR}				120		mV

5 Schematic

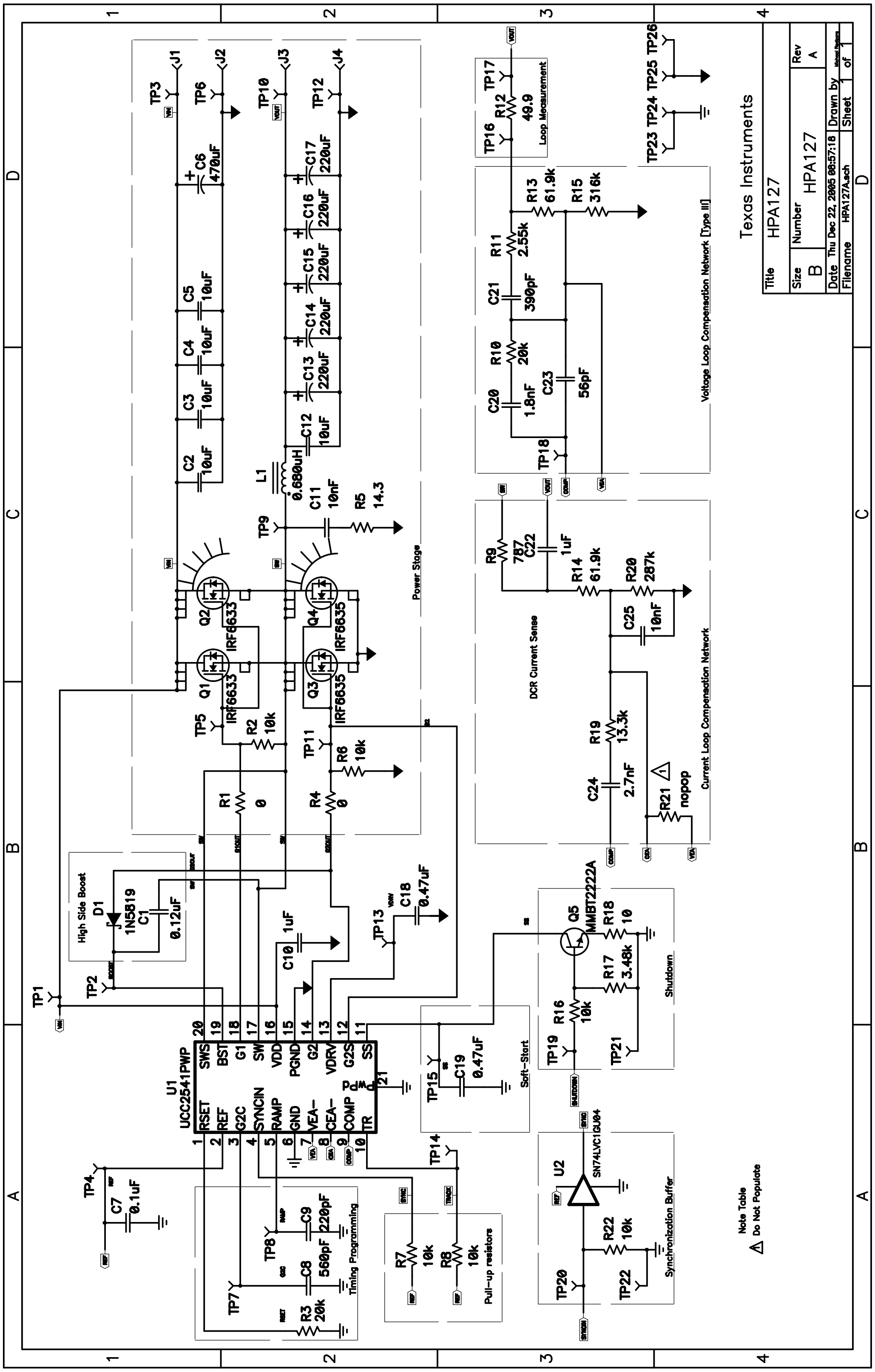

Figure 1. EVM Schematic

6 Description

The HPA127 EVM module is a high-current single-phase 300-kHz synchronous buck power converter with a nominal 12-V input between 9 V and 15 V and an output of 1.8 V rated for 40-A continuous current output.

The converter can be divided into functional blocks:

- **Device Bias:** The converter is configured for mode 1 operation where the bias voltage is 8.5 V or higher and is compatible with a 12-V_{DC} bias supply. Bias is supplied directly from the converter input voltage to VDD. The low-side drive bias, V_{DRV} = 7.2 V, is generated through a linear regulator internal to the UCC2541. The high-side gate drive, BST, is derived from V_{DRV} through two diode drops and is boosted by a flying capacitor and diode combination (D1/C1) using the synchronous rectifier drive, G2. V_{REF} is derived through a linear regulator internal to the UCC2541 from V_{DRV}.
- **Timing:** The timing section sets the oscillator capacitor charging current. Capacitors set the ramp timing and the synchronous rectifier gate cutoff time.
- **Power Train:** The power switches consists of two parallel high side control, Q1/Q2, and two parallel low-side synchronous rectifiers, Q3/Q4. The input filter is a capacitive filter with C6 as bulk capacitance and four ceramic capacitors to filter ripple current. The output filter consists of a low DCR, high current inductor and five low ESR specialty polymer (SP) aluminum electrolytic capacitors.
- **Control Loop Compensation:** A type III network compensates the voltage regulation loop. TP16/TP17 and R12 provide a point to inject a signal and make voltage control loop measurements. Overcurrent is detected by voltage across the DCR of the output inductor.
- **Auxiliary Functions (Synchronization, Tracking, Shutdown):** Synchronization and tracking inputs are pulled up to the reference voltage through R7 and R8 respectively. The Synchronization input signal is buffered by a single non-inverting gate and triggers on the falling edge. The converter can be shutdown by applying the reference voltage, V_{REF}, to the shutdown pin, pulling the soft-start pin to ground.

CAUTION

Synchronization frequency should be NO LESS than 360 kHz to avoid possible catastrophic failure of the converter.

7 Test Setup

7.1 Equipment Setup

The basic test setup recommended for evaluating the UCC2541EVM is shown below in Figure 2. The test setup consists of an input power supply, output loads, and meters to measure current and voltage on the input and output. Calibrated low-ohm resistors are recommended to measure the currents.

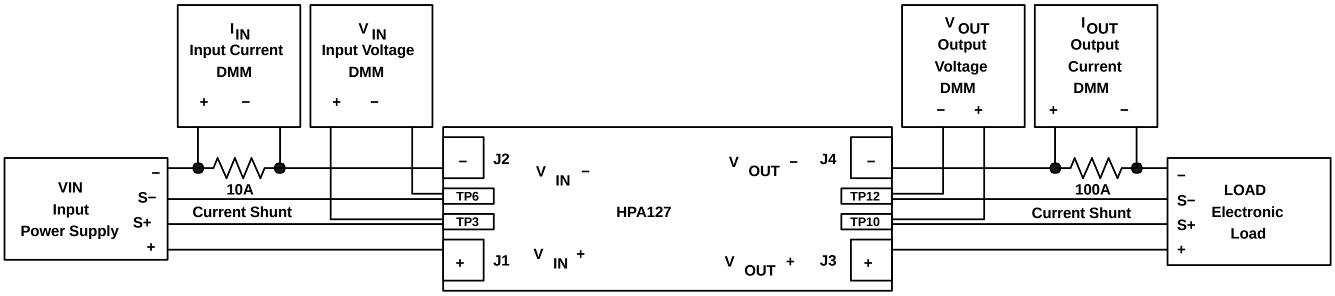

Figure 2. Recommended EVM test configuration.

7.2 Output Loads (LOAD)

For the output load, V_{OUT}, a programmable electronic load, LOAD, set to constant resistance mode and capable of sinking 60 A at 1.8 V is used. Constant resistance mode for the load requires that the output voltage is sensed at the output of the converter. Using a dc voltmeter, measure the output voltage, V_{OUT}, directly at the output test points V_{OUT+} (TP10) and V_{OUT-} (TP12). Measure the output current, I_{OUT}, with a shunt connected in series with return of the load. The LOAD shoud have leads of sufficient gauge to minimize voltage drop between device under test and LOAD. A cable length less than four feet at 4 gauge (8 gauge minimum) is recommended.

7.3 Input Power Supply (VIN)

The input voltage source shall be a variable dc source capable of supplying between 0 V_{DC} and 15.5 V_{DC}, at no less than 10 A_{DC}. Using a dc voltmeter, measure the input voltage, V_{IN}, directly at the input test points V_{IN+} (TP3) and V_{IN-} (TP6). For fault protection to the EVM, limit the source current to not more than 10 A_{DC}. Measure the input current, I_{IN}, with a shunt connected in series with the return of the source supply as shown. Use of the current shunt requires that the dc source remote sense lines be connected to the input test points for accurate voltage setting.

7.4 Network Analyzer (not shown)

To measure the closed loop response of the auxiliary output, a network analyzer can be connected directly across TP16 and TP17. The 49.9-Ω resistor (R12) between the output load and the voltage feedback allows for non-invasive measurement of the control to output loop response.

7.5 Power Up/Down Sequence

The following procedure is recommended primarily for powering up and shutting down the UCC2541 EVM. Never walk away from a powered evaluation module for extended periods of time.

7.6 Power Up Sequence

- Turn on the electronic load, LOAD. Set the electronic load to 4 A.
- Turn on the input power supply. Starting with the input dc power supply at the zero volt setting, slowly increase the voltage to the EVM operating range, 9.0 V to 15 V.
- The converter begins operating when the input voltage is at or before 9.0 V maximum, measured on the VIN DMM.

7.7 Power Down Sequence

- Decrease the input power supply to 0 V and turn it off.
- Turn off electronic load.

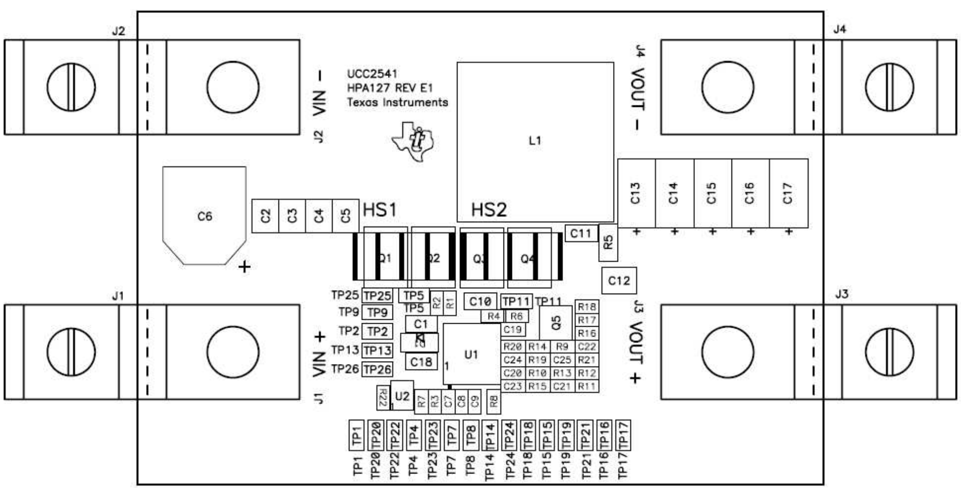

Figure 3. Test Points for HPA127 Evaluation (TOP)

Note: Input/output test points input voltage test points, TP3/TP6, and output voltage test points, TP10/TP12 are mounted on the bottom side of the PCB.

Table 2. EVM TESTPOINTS

TEST POINT	NAME	DESCRIPTION
Bias		
TP1	VIN	Power supply input voltage to the converter.
TP2	Boost	High-Side Control MOSFET driver supply pin.
TP4	Reference	3.3-V reference.
TP13	VDRV	7.2-V MOSFET driver regulated voltage
Timing		
TP7	G2C	Low-side synchronous rectifier cutoff. Discharges with G1 rising edge in normal operation. Turns off the SR after a fixed interval of 3 times the ramp time during zero duty-cycle conditions.
TP8	RAMP	Oscillator PWM ramp
TP15	SOFTSTART	Voltage output soft start ramp. Shut down is active when this pin is driven low by shutdown circuit.
Power Train		
TP3	VIN (input)	Power supply voltage to the converter. Common point for input measurement and input power supply remote sense.
TP5	G1	High-side control MOSFET gate drive.
TP6	Power ground (input)	Return for power supply voltage to the converter. Common point for input measurement and input power supply remote sense.
TP9	Switch node	Switching or phase node common between control and synchronous rectifier MOSFETs.
TP10	V_{OUT} (output)	Converter output voltage to the load. Common point for output voltage measurement and load remote sense.
TP11	G2	Low-side synchronous rectifier gate drive.
TP12	Power ground (output)	Return for converter output voltage to the load. Common point for output voltage measurement and load remote sense.
TP16	V_{OUT} sense low (loop measurement)	Low-side connection point for network analyzer.
TP17	V_{OUT} sense high (loop measurement)	High-side connection point for network analyzer.
TP18	Compensation	Voltage/current error amp compensation pin.
External Controls		
TP14	Tracking	Tracking input to the voltage error amp.
TP19	Shutdown	Shutdown input. 3.3 V applied to this point shuts the converter down.
TP20	Synchronization	Synchronization input. Synchronizes oscillator to system clock.
Grounds		
TP21, TP22, TP23, TP24	Signal ground	
TP25, TP26	Power ground	

8 Performance Data and Characteristic Curves

8.1 Characteristic Curves

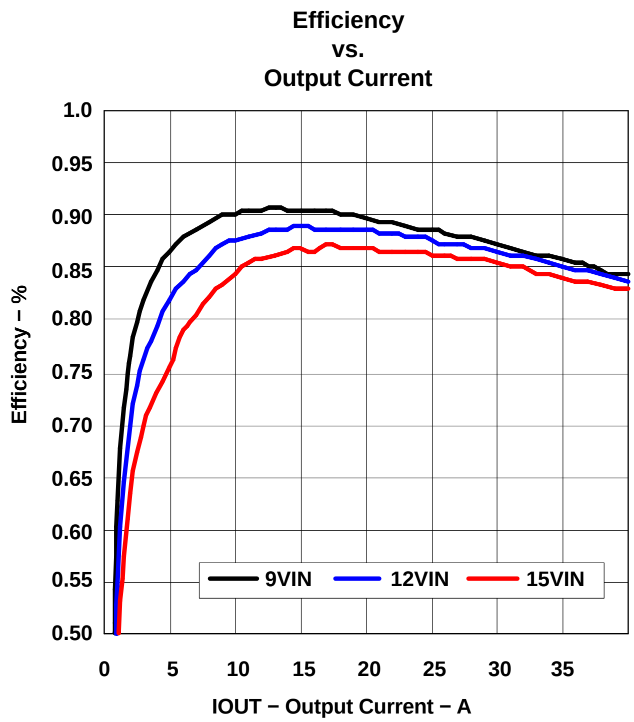

Figure 4.

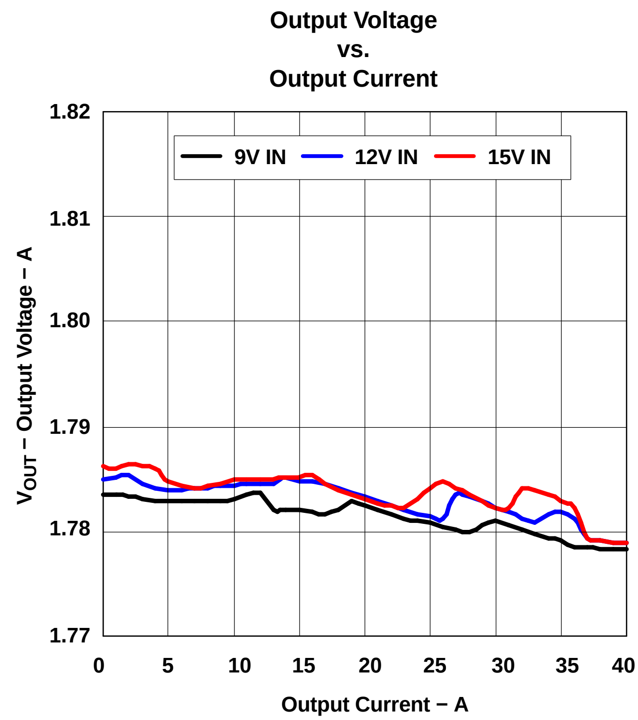

Figure 6.

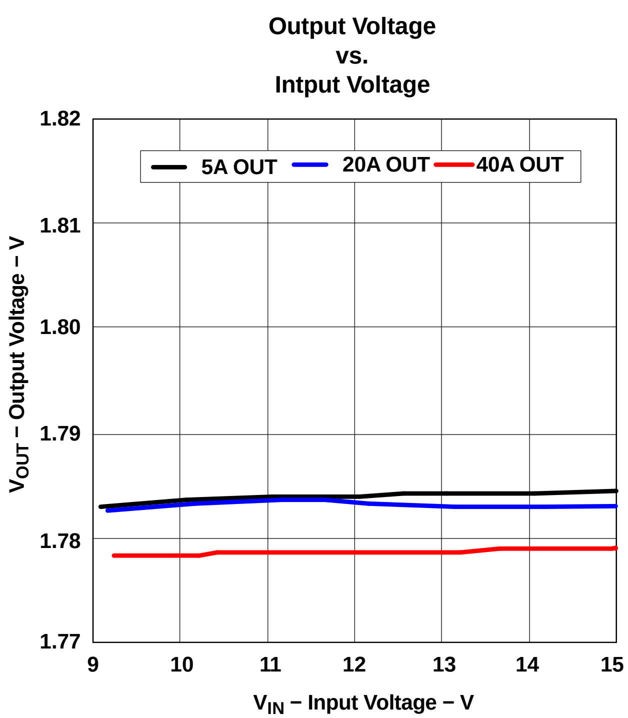

Figure 5.

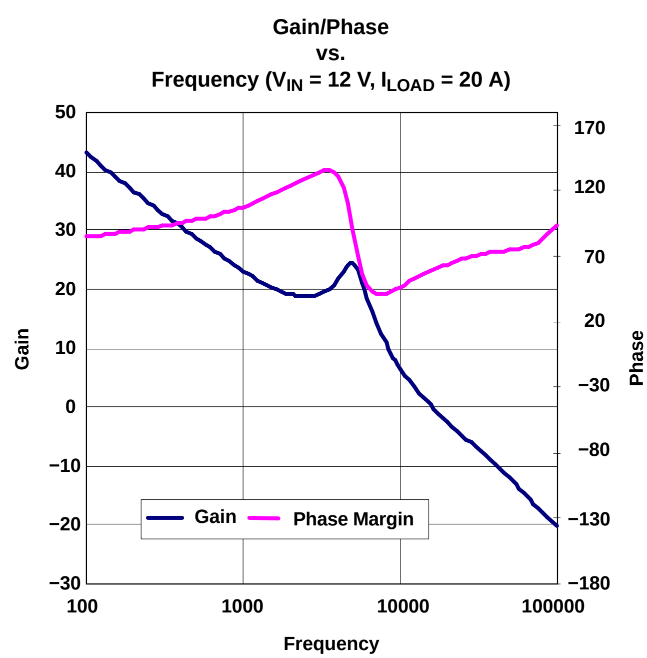

Figure 7.

8.2 Typical Waveforms

Typical Waveforms

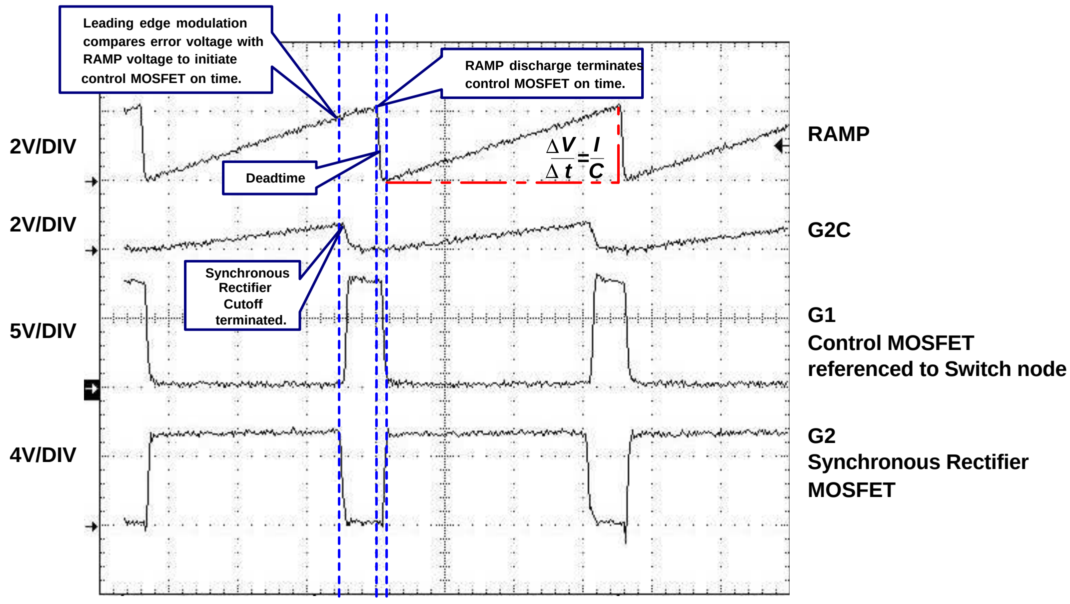

Figure 8.

Turn−On Trajectory

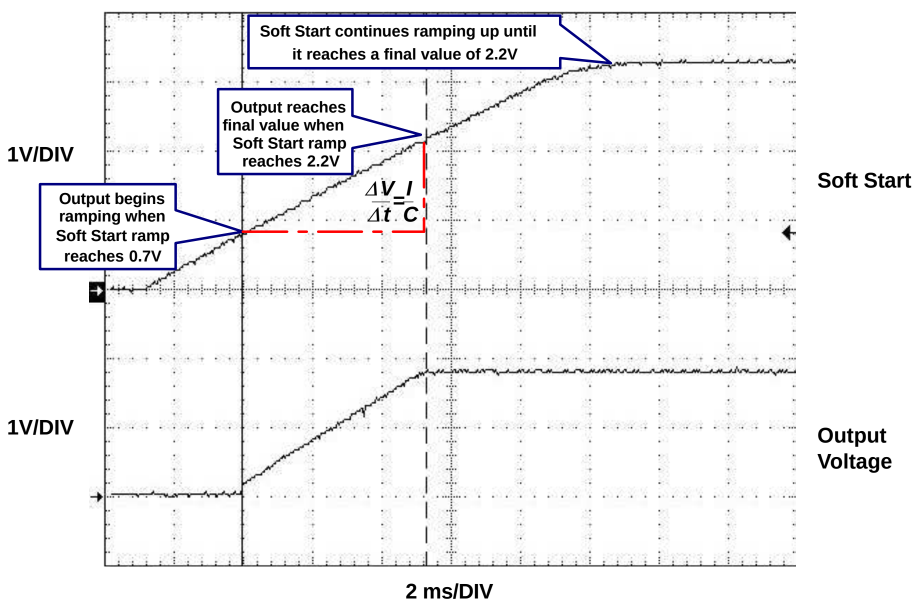

Figure 9.

Output Voltage Ripple

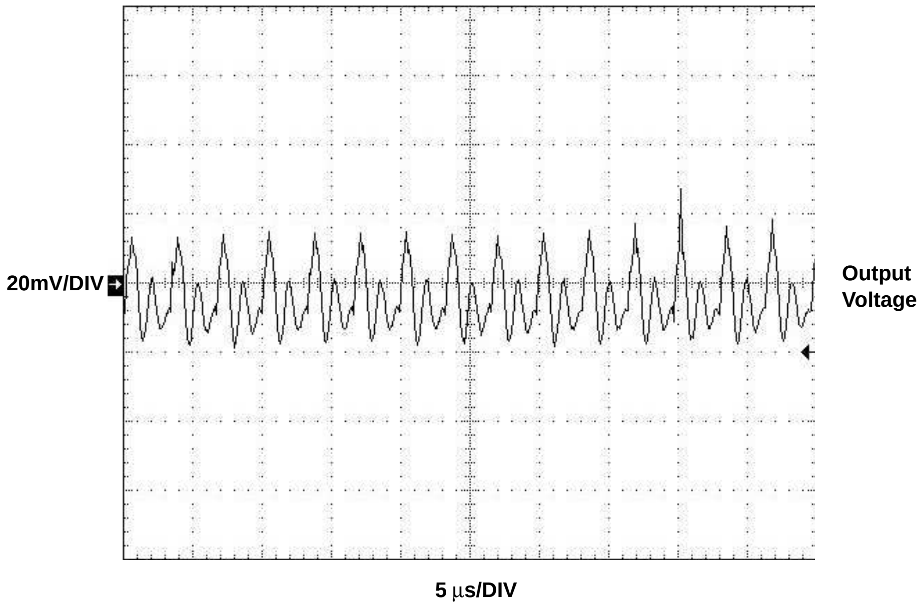

Figure 10.

Load Transient on the Output

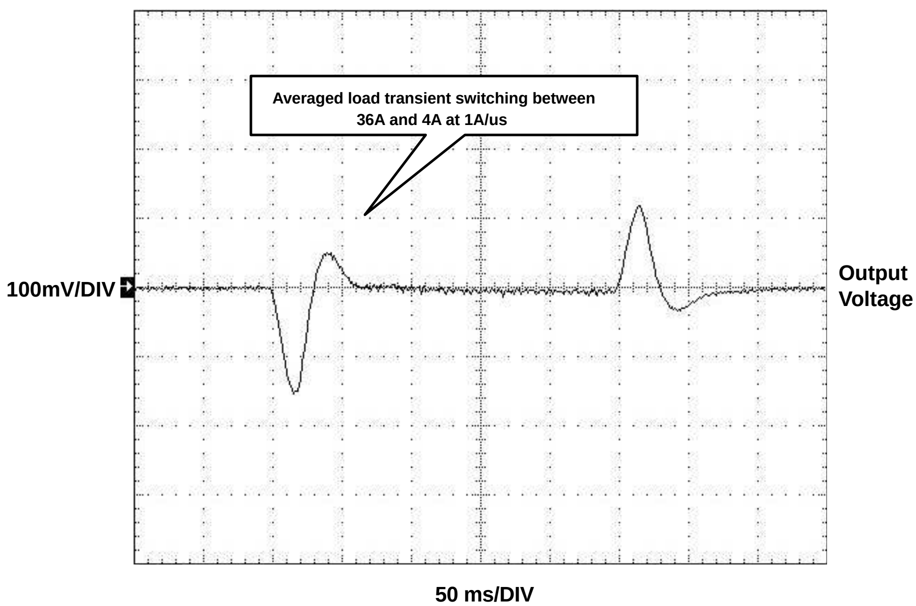

Figure 11.

Predictive Gate Drive

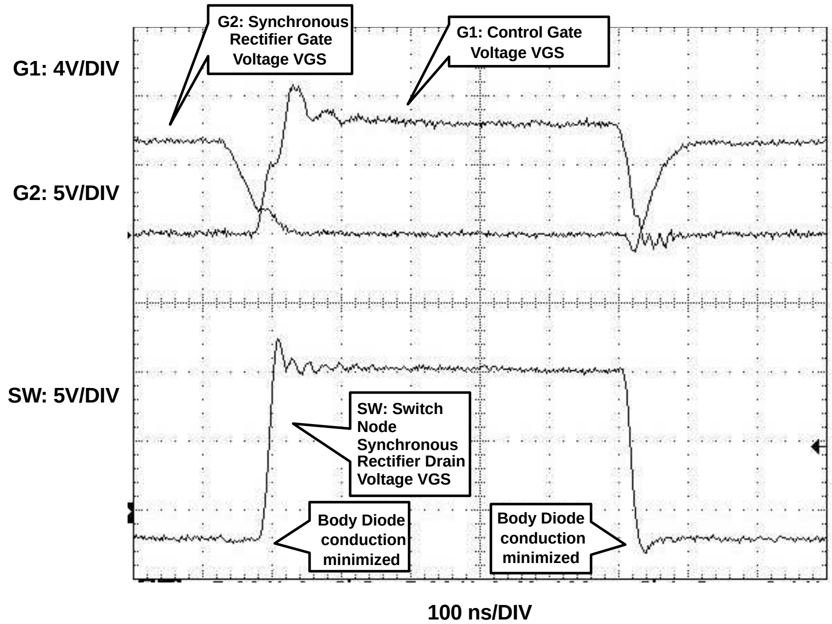

Figure 12.

Converter Shutdown

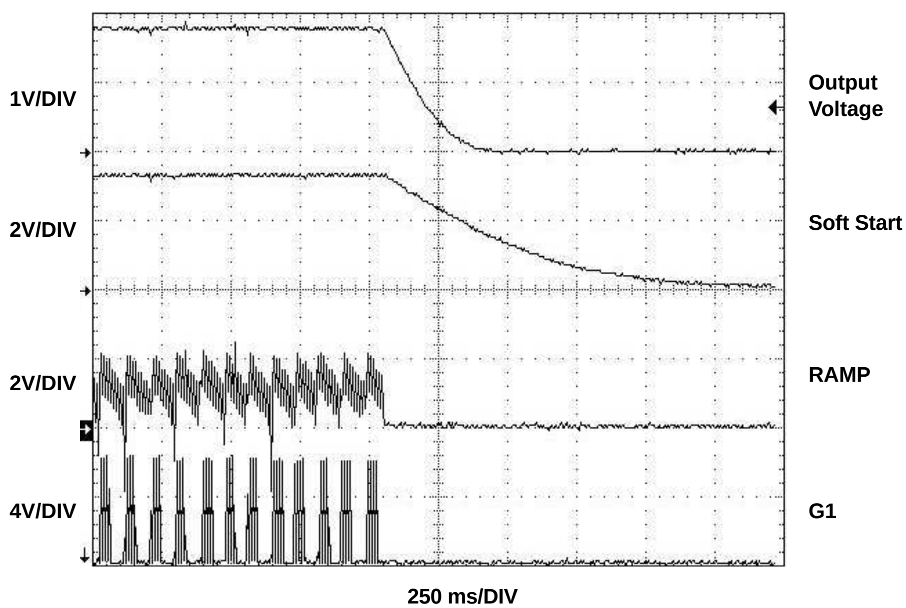

Figure 13.

Overcurrent Protection

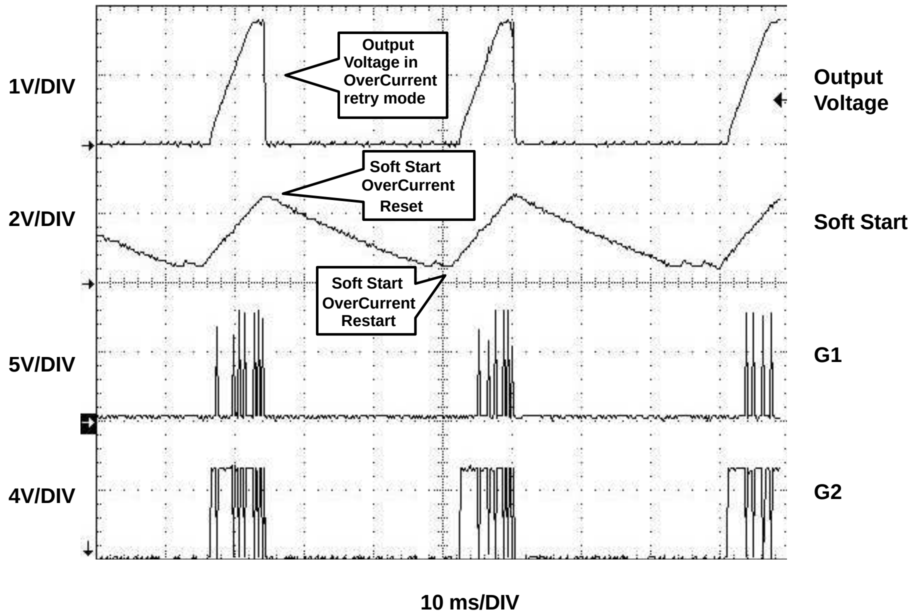

Figure 14.

9 EVM Assembly Drawing and PCB Layout.

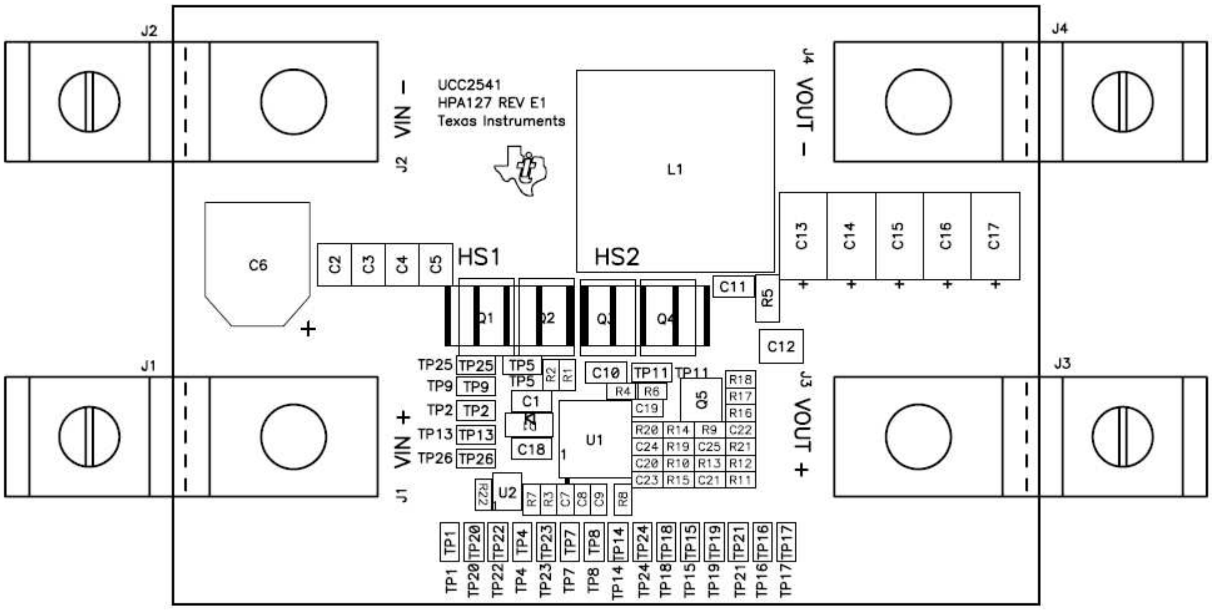

Figure 15. Top Assembly

Figure 16. Bottom Assembly

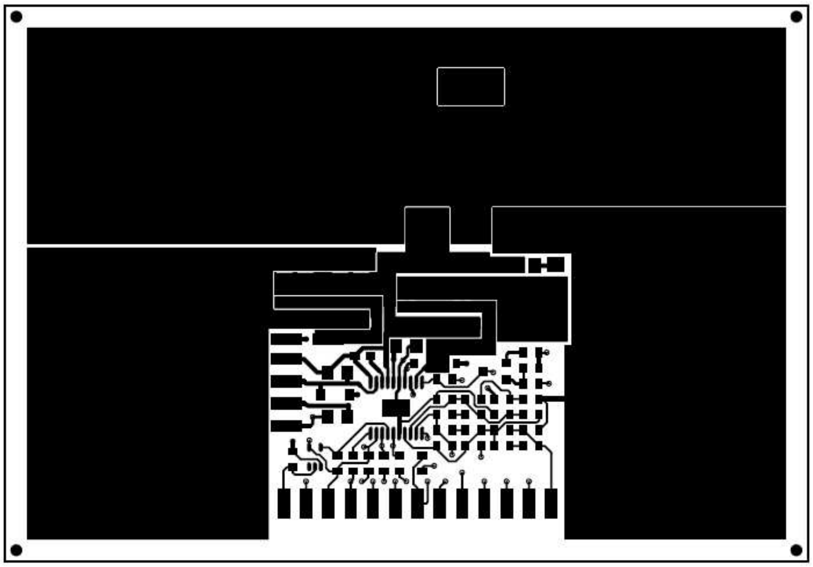

Figure 17. Layer 1 (Top)

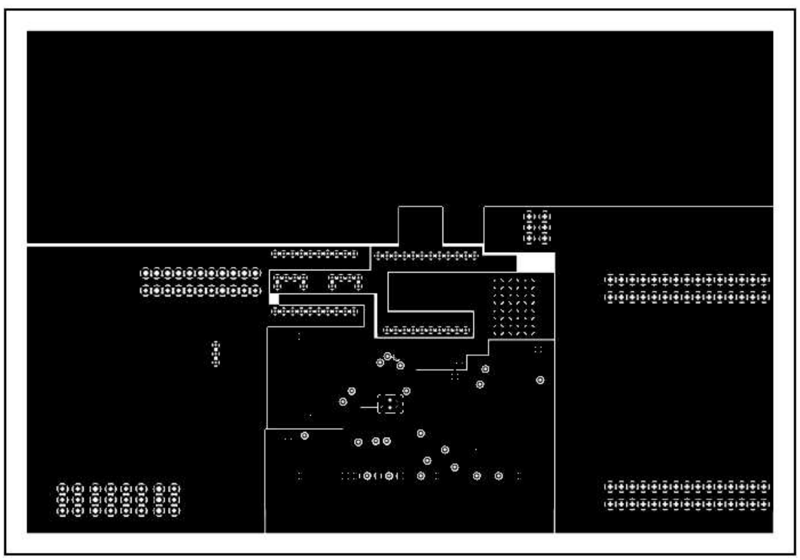

Figure 18. Layer 2 (Inner 1)

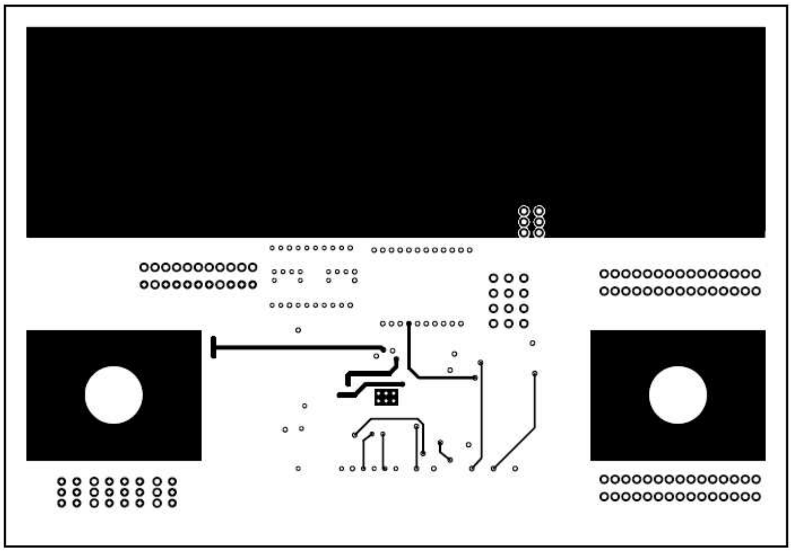

Figure 19. Layer 3 (Inner 2)

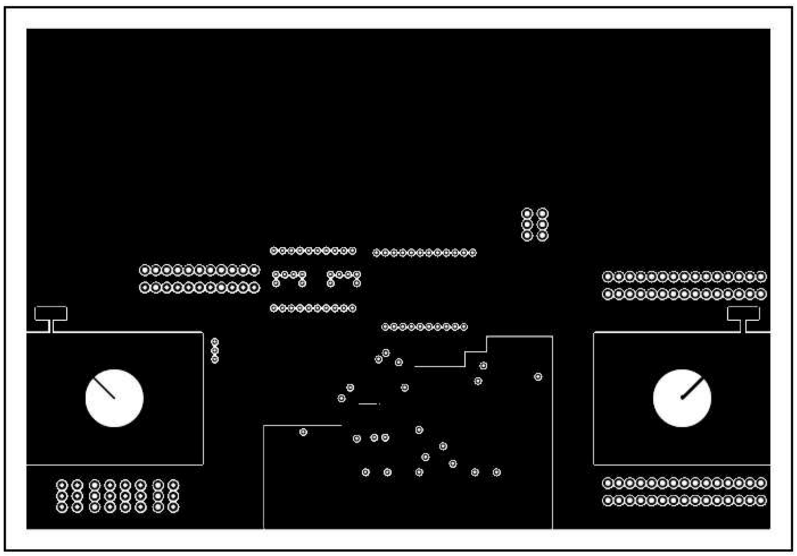

Figure 20. Layer 4 (Bottom)

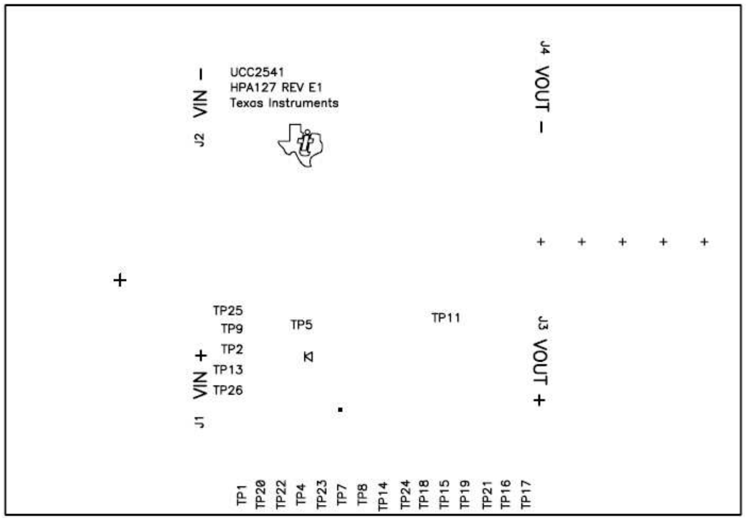

Figure 21. Top Silk Layer

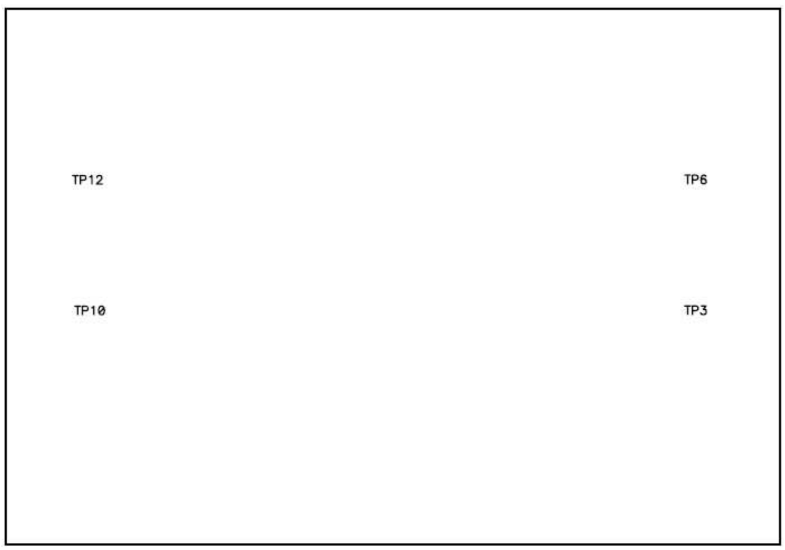

Figure 22. Bottom Silk Layer

10 List of Material

Table 3. List of Materials

REF	QTY	DESCRIPTION	PART NUMBER	MFR
C1	1	Capacitor, ceramic, 25 V, X7R, ±10%, 0.12 µF, 0805	Std.	Std.
C10	1	Capacitor, ceramic, 25 V, X7R, 10%, 1 µF, 0805	Std.	Std.
C11	1	Capacitor, ceramic, 50 V, C0G, ±5%, 10 nF, 0805	Std.	Std.
C13, C14, C15, C16, C17	5	Capacitor, aluminum, 4 V, 20% (SE series), 220 µF, 7343	EEF-SE0G221R	Panasonic
C18, C19	2	Capacitor, ceramic, 16 V, X7R, 10%, 0.47 µF, 0603	Std.	Std.
C2, C3, C4, C5, C12	5	Capacitor, ceramic, 16 V, X5R, 10%, 10 µF, 1210	Std.	Std.
C20	1	Capacitor, ceramic, 50 V, NPO, 5%, 1.8 nF, 0603	Std.	Std.
C21	1	Capacitor, ceramic, 50 V, C0G, 5%, 390 pF, 0603	Std.	Std.
C22	1	Capacitor, ceramic, 6.3 V, X5R, 10%, 1 µF, 0603	Std.	Std.
C23	1	Capacitor, ceramic, 50 V, NPO, 5%, 56 pF, 0603	Std.	Std.
C24	1	Capacitor, ceramic, 50 V, C0G, 5%, 2.7 nF, 0603	Std.	Std.
C25	1	Capacitor, ceramic, 16 V, X7R, 10%, 10 nF, 0603	Std.	Std.
C6	1	Capacitor, aluminum, SM, ±20%, 25 V, 470 µF, 0.406 x 0.457 inch	EEV-FK1E471P	Panasonic
C7	1	Capacitor, ceramic, 16 V, X7R, 10% , 0.1 µF, 0603	Std.	Std.
C8	1	Capacitor, ceramic, 50 V, NPO, 5%, 560 pF, 0603	Std.	Std.
C9	1	Capacitor, ceramic, 50 V, NPO, 5%, 220 pF, 0603	Std.	Std.
D1	1	Diode, schottky, 1 A, 40 V, SOD123	1N5819	Std.
HS1, HS2	2	Heatsink, DIP, 0.530 x 0.25 in.	619453B00250	Aavid
J1, J2, J3, J4	4	Copper, single barrel, one-hole, straight tongue (fixed) lug, #14 - #4 AWG wire, 1/4 stud hole, 1.55 x 0.50 in	CX70-14-C	Panduit
L1	1	Inductor, SMT, 62 A, 0.85 mΩ, 0.680 µH, 0.790 x 0.770 in.	SER2010-681MLB	Coilcraft
Q1, Q2	2	Transistor, MOSFET, 20 V, 59 A, 5.6mΩ, MP Can	IRF6633	IR
Q3, Q4	2	Transistor, MOSFET, 30 V, 180 A, 1.3 mΩ, MX Can	IRF6635	IR
Q5	1	Transistor, NPN, 40 V, 1 A, SOT-23	MMBT2222A	Std.
R1, R4	2	Resistor, chip, 1/16 W, 1%, 0 Ω, 0603	Std.	Std.
R11	1	Resistor, chip, 1/16 W, 1%, 2.55 kΩ, 0603	Std.	Std.
R12	1	Resistor, chip, 1/16 W, 1%, 49.9 Ω, 0603	Std.	Std.

Table 3. List of Materials (continued)

REF	QTY	DESCRIPTION	PART NUMBER	MFR
R13, R14	2	Resistor, chip, 1/16 W, 1%, 61.9 kΩ, 0603	Std.	Std.
R15	1	Resistor, chip, 1/16 W, 1%, 316 kΩ, 0603	Std.	Std.
R17	1	Resistor, chip, 1/16 W, 1%, 3.48 kΩ, 0603	Std.	Std.
R18	1	Resistor, chip, 1/16 W, 1%, 10 Ω, 0603	Std.	Std.
R19	1	Resistor, chip, 1/16 W, 1%, 13.3 kΩ, 0603	Std.	Std.
R2, R6, R7, R8, R16, R22	6	Resistor, chip, 1/16 W, 1%, 10 kΩ, 0603	Std.	Std.
R20	1	Resistor, chip, 1/16 W, 1%, 287 kΩ, 0603	Std.	Std.
R21	0	Resistor, chip, 1/16 W, yy%, nopop, 0603	Std.	Std.
R3, R10	2	Resistor, chip, 1/16 W, 1%, 20 kΩ, 0603	Std.	Std.
R5	1	Resistor, chip, 1/8 W, 1%, 14.3 Ω, 1206	Std.	Std.
R9	1	Resistor, chip, 1/16 W, yy%, 787 Ω, 0603	Std.	Std.
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	26	Test point, SMT, 0.105 x 0.040	5015	
U1	1	IC, Digital Power Controller For Power Supply Applications, PWP20	UCC2541PWP	TI
U2	1	IC, single inverter, SC-70	SN74LVC1GU04DCKx	TI
	1	PCB, 3.6 x 2.5 x 0.062 in.	HPA127	Any
	2	Machine screw, hex head, 1/4-20, 3/8 in., steel		
	2	Nut, hex, 1/4-20, steel,		
	2	Washer, flat, 1/4-20, steel,		
	1	Epoxy, thermal adhesive	3880	Loctite

11 Reference

- Data Sheet, *UCC2541 High-Efficiency Secondary-Side Synchronous Buck PWM Controller*, Texas Instruments Literature Number SLUS539

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 15 V and the output voltage range of 0 V to 1.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 50° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265