User's Guide

SLUU366A–March 2010–Revised April 2010

bq2415x RGY EVM (HPA255)

This user's guide describes the features, setup, and operation of the bq2415x RGY evaluation board. Included are the bill of materials, board layout, and schematic.

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1 Introduction

1.1 EVM Features

- Evaluation module for bq2415x
- High-efficiency, fully integrated NMOS-NMOS synchronous buck charger with 3-MHz frequency
- Integrated power FETs for up to 1.25-A charge rate
- Programmable battery voltage, charge current, and input current via I^2C™ interface
- Input operating range 4 V–6 V
- Boost mode operation for USB OTG
- LED indication for status signals
- Test points for key signals available for testing purposes. Easy probe hook-up.
- Jumpers available. Easy to change connections.

1.2 General Description

The bq2415x evaluation module is a complete charger module for evaluating compact, flexible, high-efficiency, USB-friendly switch-mode charge management solution for single-cell Li-ion and Li-polymer batteries used in a wide range of portable applications.

The bq2415x integrates a synchronous PWM controller, power MOSFETs, input current sensing, high-accuracy current and voltage regulation, and charge termination, into a small WCSP package.

The charge parameters can be programmed through an I^2C interface.

For details, see the bq2415x data sheet (SLUS942).

1.3 I/O Description

Table 1. Input/Output Jack Descriptions

Jack	Description
J1–DC+	AC adapter or USB, positive output
J1–DC–	AC adapter or USB, negative output
J2–BAT+	Charger positive output, connect to CSOUT pin
J2–AUXPWR/CD	Connect to AUXPWR/CD pin
J2–BAT–	Battery negative terminal, connect to DC-
J3–SCL	I2C clock, connect to SCL pin
J3–SDA	I2C data, connect to SDA pin
J3–DC–	AC adapter or USB, negative output
J4–STAT	Status output, can be connected to STAT pin by JMP1 set to EXT (2-3)
J4–OTG/SLRST/TS/ISEL	Connect to OTG/SLRST/TS/ISEL pin
J4–DC–	AC adapter or USB, negative output

1.4 Controls and Key Parameters Setting

Table 2. Control and Key Parameters Settings for JMP1 Through JMP5

Jack	Description	Factory Setting
JMP1	LED 1-2: Connect STAT pin to LED on EVM EXT 2-3: Connect STAT pin to J4-1	Jumper On LED (1-2)
JMP2	HI 1-2: OTG/SLRST/TS/ISEL high (input or battery voltage) LO 2-3: OTG/SLRST/TS/ISEL low (ground)	See table below
JMP3	J2-BAT+ connect to J2-AUXPWR/CD	See table below
JMP4	AUXPWR/CD pin connect to high or low or float	See table below
JMP5	OTG/SLRST/TS/ISEL pin 10k resistor to ground or float	Jumper On

Table 3. Factory Jumper Settings

Spin	JMP1	JMP2	JMP3	JMP4	JMP5
HPA255-001 (bq24150)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-002 (bq24151)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-003 (bq24152)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-004 (bq24153)	(-LED-) ON	(-LO-) ON	OFF	(-LO-) ON	ON
HPA255-005 (bq24155)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-006 (bq24156)	(-LED-) ON	(-HI-) ON	OFF	(-LO-) ON	ON
HPA255-007 (bq24159)	(-LED-) ON	OFF	OFF	(-LO-) ON	ON

1.5 Recommended Operating Conditions

Table 4. Recommended Operating Conditions

		Min	Typ	Max	Unit	Notes
Supply voltage, V_{IN}	Input voltage from ac adapter input	4	5	6	V	
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal of J8	0	3–4.2	4.44	V	
Supply current, I_{AC}	Maximum input current from ac adapter input	0	0.1–0.5	1.5	A	
Charge current, I_{chrg}	Battery charge current	0.55	0.7	1.25	A	
Operating junction temperature range, T_J		0		125	°C	

2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA255 evaluation board. On the test procedure the following naming conventions are followed. Refer to the HPA255 schematic for details.

VXXX :	External voltage supply name (VADP, VBT, VSBT)
LOADW :	External load name (LOADR, LOADI)
V(TPyyy) :	Voltage at internal test point TPyyy. For example, V(TP12) means the voltage at TP12.
V(Jxx) :	Voltage at jack terminal Jxx.
V(TP(XXX)) :	Voltage at test point “XXX”. For example, V(ACDET) means the voltage at the test point which is marked as “ACDET”.
V(XXX, YYY) :	Voltage across point XXX and YYY.
I(JXX(YYY)) :	Current going out from the YYY terminal of jack XX.
Jxx(BBB) :	Terminal or pin BBB of jack xx
Jxx ON :	Internal jumper Jxx terminals are shorted
Jxx OFF :	Internal jumper Jxx terminals are open
Jxx (-YY-) ON :	Internal jumper Jxx adjacent terminals marked as “YY” are shorted
Measure: → A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components

2.2 Equipment

2.2.1 POWER SUPPLIES

Power Supply 1 (PS1): a power supply capable of supplying 5 V at 2 A is required.

2.2.2 LOAD 1

A 10-V (or above), 2-A (or above) electronic load that can operate at constant current mode.

2.2.3 LOAD 2

A HP 6060B 3-60V/0-60A, 300-W system dc electronic load.
Or: equivalent.

2.2.4 METERS

Four Fluke 75, (equivalent or better)
Or: Two equivalent voltage meters and two equivalent current meters. The current meters must be able to measure a 2-A current.

2.2.5 COMPUTER

A computer with at least one USB port and a USB cable. The bq2415x evaluation software must be properly installed.

2.2.6 HPA172 COMMUNICATION KIT

A HPA172 USB to I2C communication kit.

2.2.7 SOFTWARE

Double click on the “SETUP.EXE” file. Follow the installation steps.

2.3 Equipment Setup

(A) Set the Power Supply 1 for 5 V ±100 mVdc, 2 ±0.1-A current limit and then turn off supply.

(B) Connect the output of Power Supply 1 in series with a current meter (multimeter) to J1 (DC+, DC–).

(C) Connect a voltage meter across J1 (DC+, DC-).

(D) Connect the Load 2 in series with a current meter (multimeter) to J2 (BAT+, BAT–). Make sure a voltage meter is connected across J2 (BAT+, BAT–). Turn on the Load 2. Use the constant voltage mode. Set the output voltage to 2.5 V.

(E) Turn off Load 2.

(F) Connect J5 to HPA172 kit by 10-pin ribbon cable. Connect the USB port of the HPA172 kit to the USB port of the computer. The connections are shown in Figure 1.

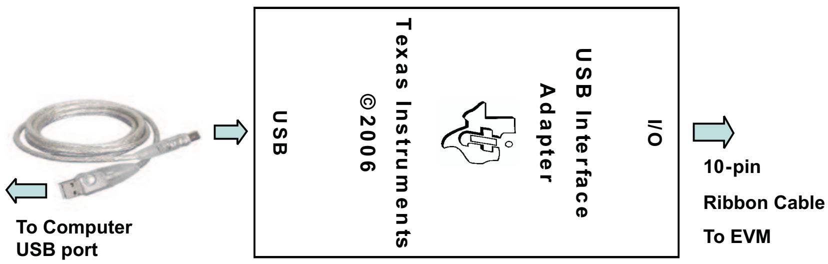


Figure 1. Connections of the HPA172 Kit

(G) Install jumpers per following table.

Table 5. JMP1 Through JMP5 Installation Settings

Spin	JMP1	JMP2	JMP3	JMP4	JMP5
HPA255-001 (bq24150)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-002 (bq24151)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-003 (bq24152)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-004 (bq24153)	(-LED-) ON	(-LO-) ON	OFF	(-LO-) ON	ON
HPA255-005 (bq24155)	(-LED-) ON	(-LO-) ON	ON	OFF	ON
HPA255-006 (bq24156)	(-LED-) ON	(-HI-) ON	OFF	(-LO-) ON	ON
HPA255-007 (bq24159)	(-LED-) ON	OFF	OFF	(-LO-) ON	ON

After completing the preceding steps, the test setup for HPA255 appears as is shown in Figure 2.

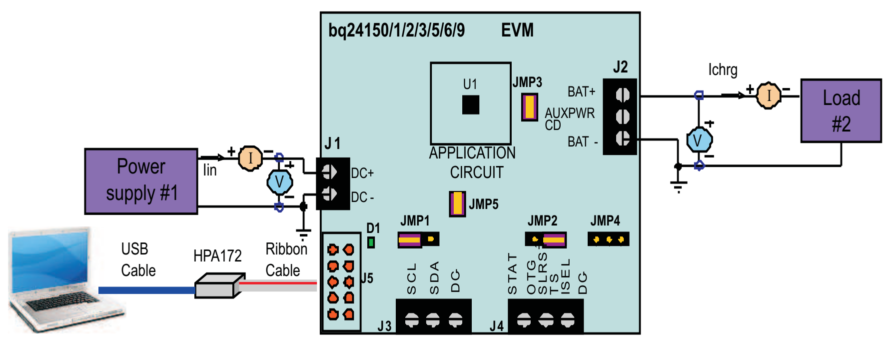


Figure 2. Original Test Setup for HPA255 (bq2415x EVM)

(H) Turn on the computer. Open the bq2415x evaluation software. The main window of the software is shown in Figure 3.

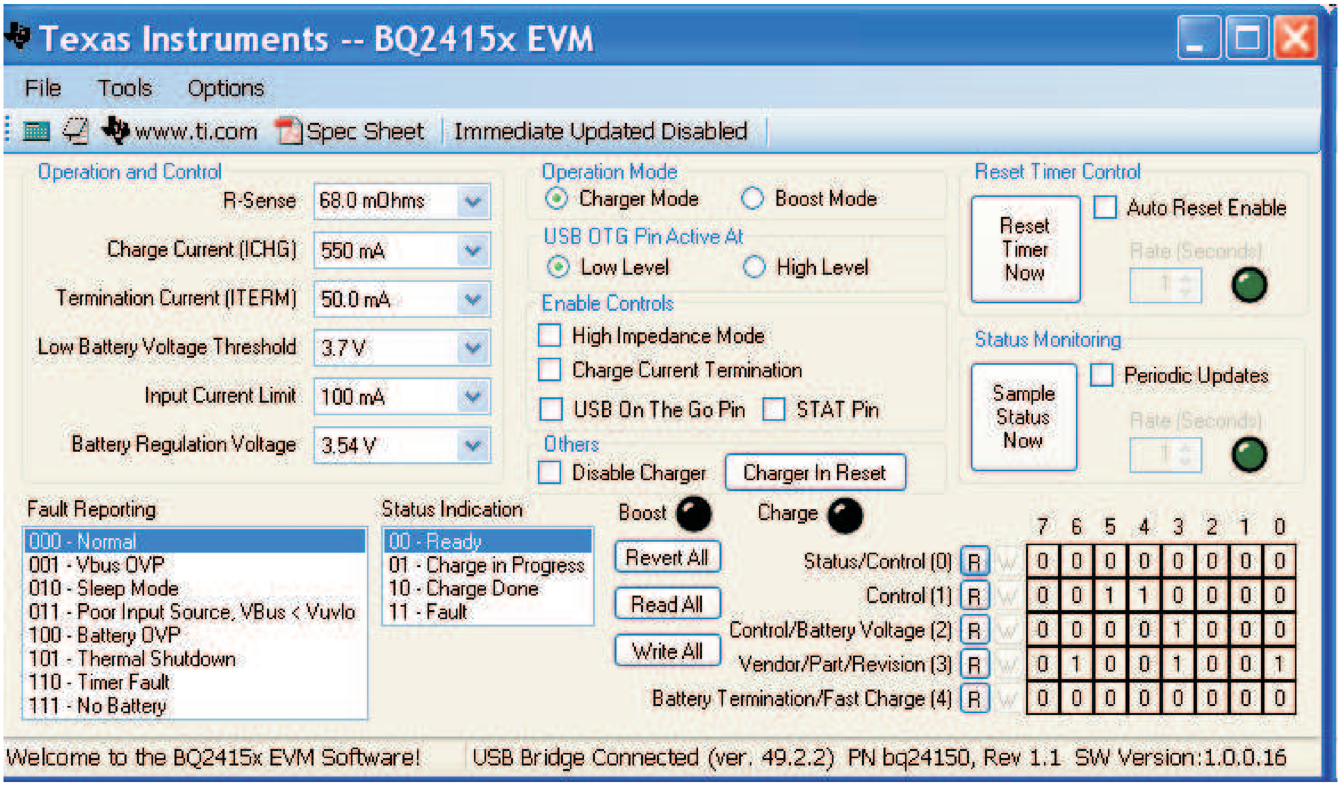


Figure 3. Main Window of the bq2415x Evaluation Software

2.4 *Procedure*

2.4.1 Charge Voltage and Current Regulation

1. Ensure that Section 2.3 steps are followed. Turn on PS1.
2. Software setup: Click Immediate Update Disabled button. It changes to Immediate Update Enabled. Check Auto Reset Enable, set Rate to 5 seconds. Check Periodic Updates, set Rate to 1 second. Ensure that Operation Mode is Charger Mode. Uncheck Charge Current Termination. Check STAT Pin. Select Battery Regulation Voltage to 4.20V.

   Measure → V(J2(VBAT+, VBAT–)) = 4.2 ±100 mV
   Observe → D1 is on.
3. Enable Load 2.

   Measure → V(J2(VBAT+, VBAT–)) = 2.5 ±100 mV
   Measure → Ichrg = 160 mA ±40 mA
   Measure → Iin = 93 mA ±5 mA
4. Select Charge Current to 1.25 A, select Input Current Limit to 500 mA.

   Measure → Ichrg = 750 mA ±100 mA
   Measure → Iin = 475 mA ±25 mA
5. Check Disable Charger. Turn off PS1, turn off Load 2, and disconnect

2.4.2 Boost Function (For –001, –002, –003, –004, –007 ONLY)

1. Adjust PS1 output to 3.7 V and disable the output. Connect the PS1 in series with a current meter (multimeter) to J2 (BAT+, BAT-). Ensure that a voltage meter is connected across J2 (BAT+, BAT-).
2. Set the Load 1 current to 200 mA ±20 mA but disable the output. Connect the output of the Load 1 in series with a current meter (multimeter) to J1 (DC+, DC-). Ensure that a voltage meter is connected across J1 (DC+, DC-). The setup is now like that shown in Figure 4 for HPA255.

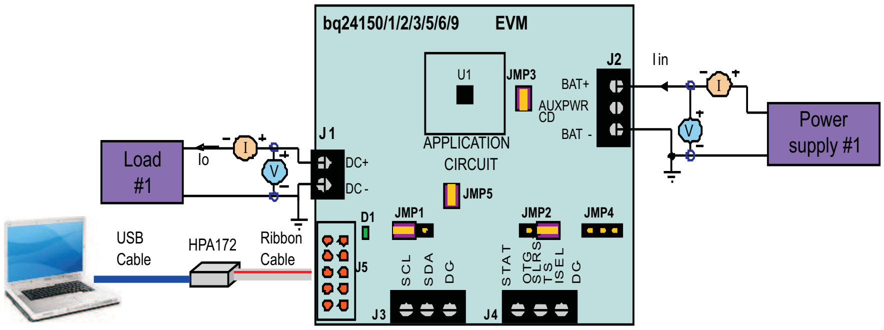


Figure 4. Test Setup for HPA255

3. Turn on PS1 output.
4. Software setup: Change Operation Mode to Boost Mode.
   Measure → V(J1(DC+, DC–)) = 5 V ±0.2 V
5. Enable Load 1.
   Measure → V(J1(DC+, DC-)) = 5 V ±0.2 V
   Measure → Iin = 330 mA ±40 mA
   Measure → Io = 200 mA ±20 mA

3 PCB Layout Guideline

1. To obtain optimal performance, the power input capacitors, connected from input to PGND, must be placed as close as possible to the integrated circuit (IC).
2. The output inductor must be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high-frequency oscillation problems, proper layout to minimize high-frequency current path loop is critical.
3. The sense resistor must be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers. (Do not route the sense leads through a high-current path.)
4. Place all decoupling capacitors close to their respective IC pin and as close as possible to PGND. (Do not place components such that routing interrupts power stage currents.) All small control signals must be routed away from the high-current paths.
5. The printed-circuit board must have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small-signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, no ground-bounce issue occurs, and having the components segregated minimizes coupling between signals.
6. The high-current charge paths into VBUS, PMID, and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins must be connected to the ground plane to return current through the internal low-side FET.

4 Board Layout, Schematic, and Bill of Materials

4.1 Board Layout

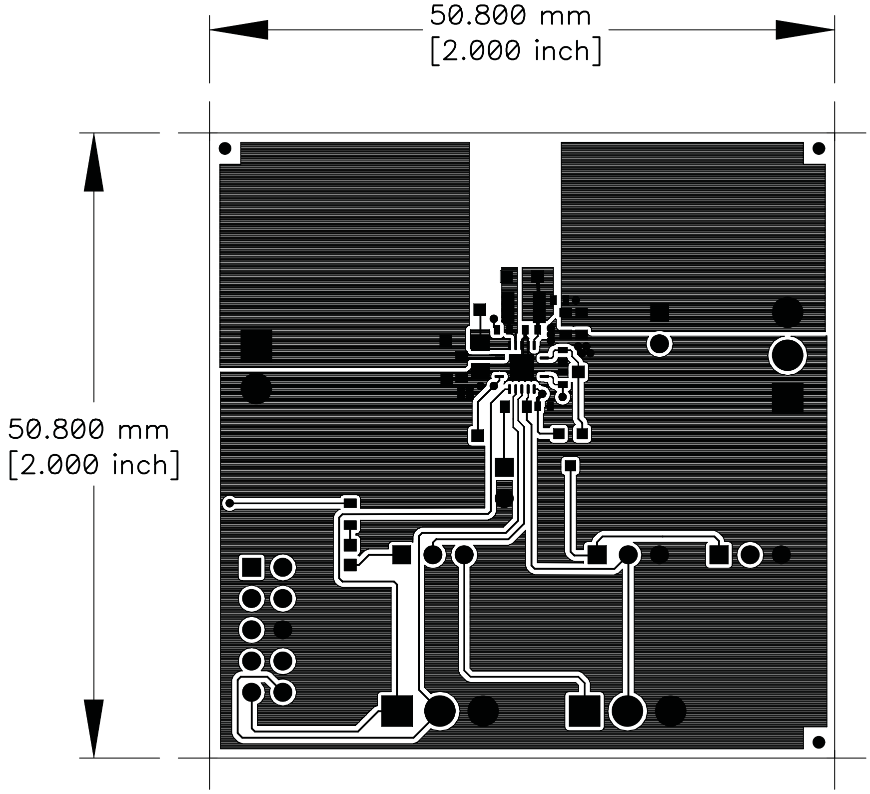


Figure 5. Top Layer

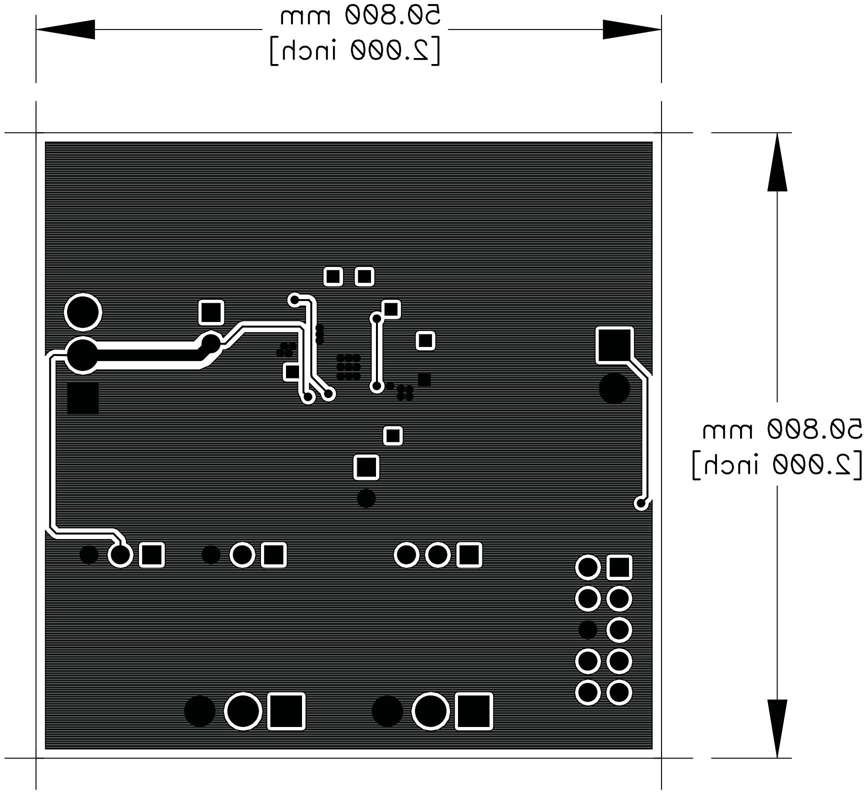


Figure 6. Bottom Layer

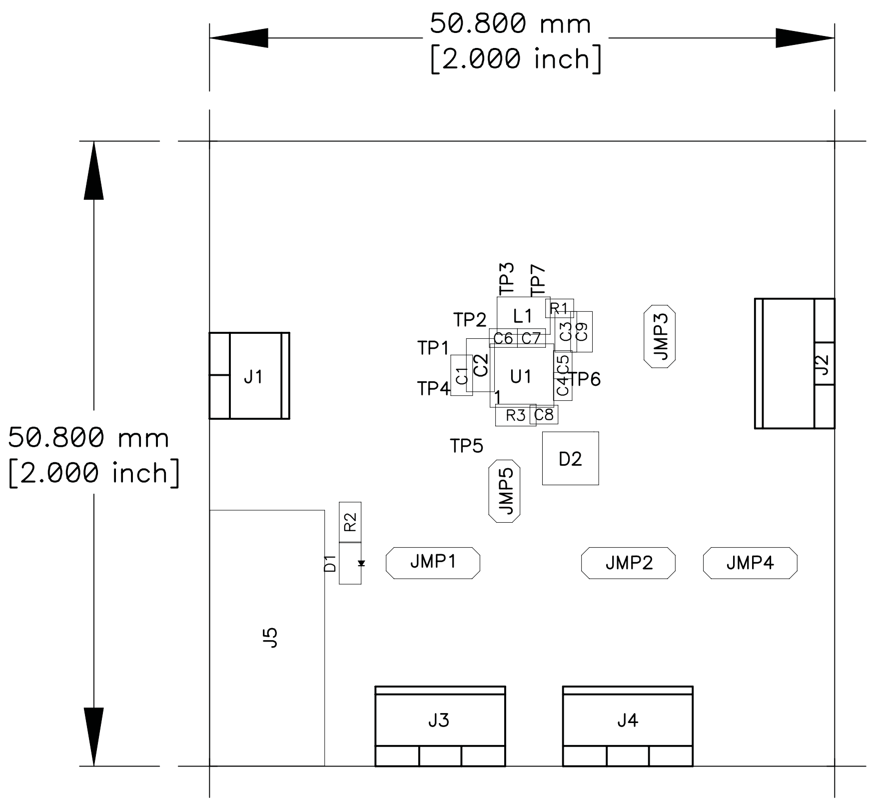


Figure 7. Top Assembly

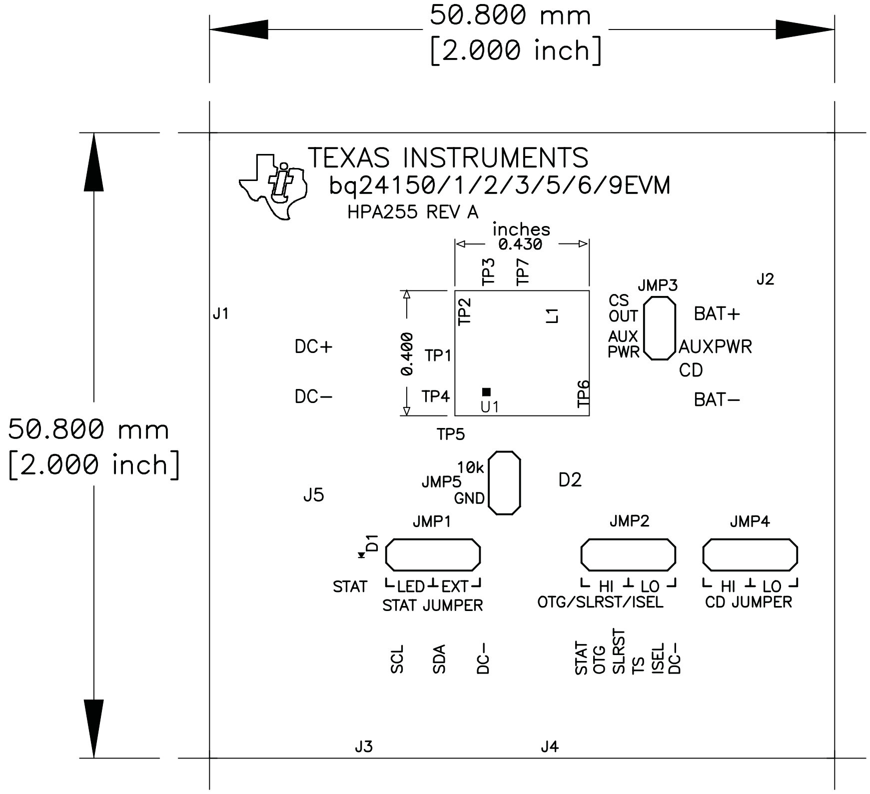
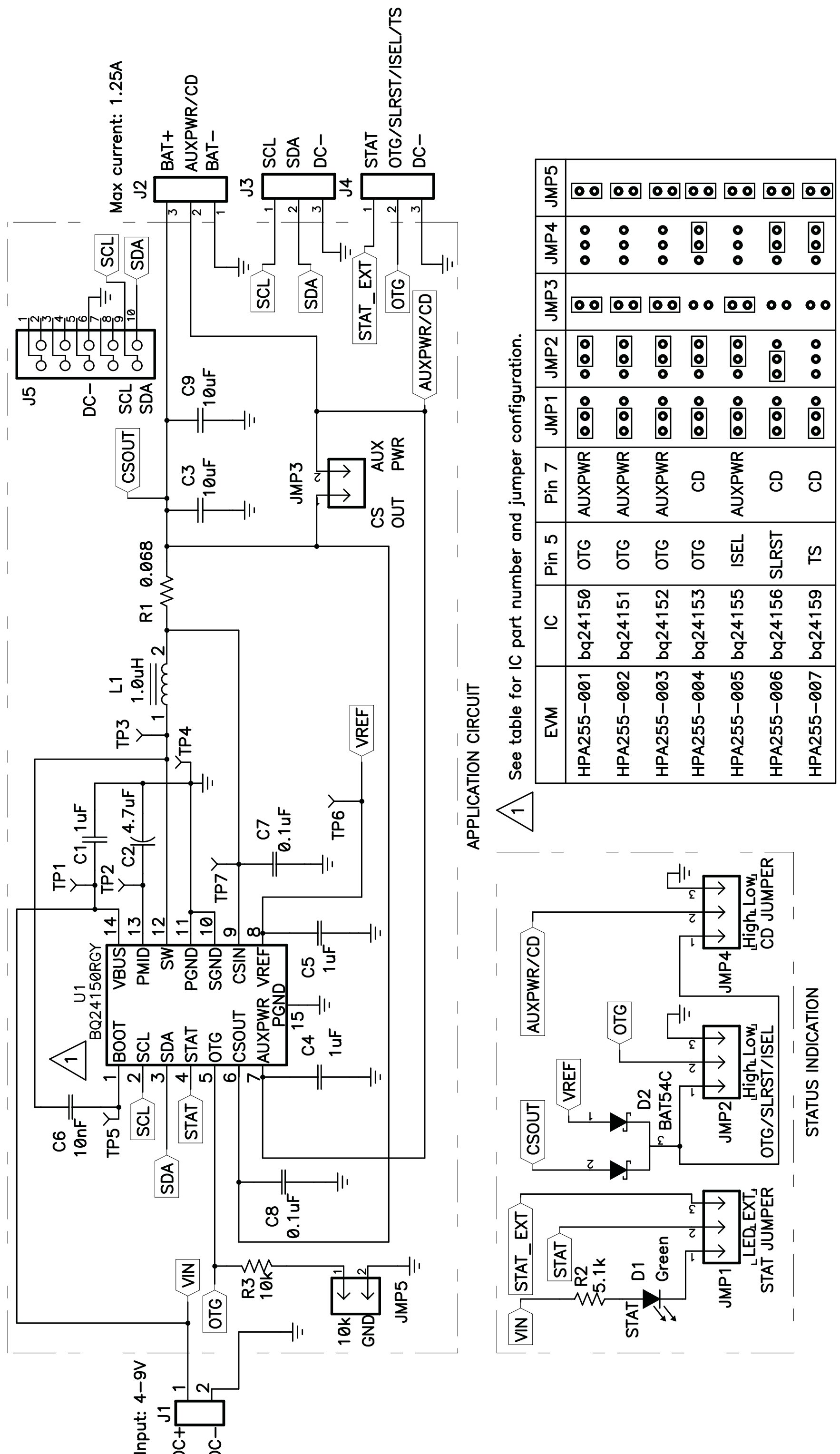


Figure 8. Top Silk

4.2 Schematic



4.3 Bill of Materials

bq24150 -001	bq24151 -002	bq24152 -003	bq24153 -004	bq24155 -005	bq24156 -006	bq24159 -007	RefDes	Value	Description	Size	Part Number	MFR
1	1	1	1	1	1	1	C1	1μF	Capacitor, Ceramic, X5R, 16V, ±10%	603	GRM188R61C105K	Murata
1	1	1	1	1	1	1	C2	4.7μF	Capacitor, Ceramic, X7R, 16V, ±10%	805	GRM21BR71C475K	Murata
2	2	2	2	2	2	2	C3, C9	10μF	Capacitor, Ceramic, X5R, 6.3V, ±20%	603	GRM188R60J106M	Murata
2	2	2	2	2	2	2	C4, C5	1μF	Capacitor, Ceramic, X5R, 10V, ±10%	402	GRM155R61A105K	Murata
1	1	1	1	1	1	1	C6	10nF	Capacitor, Ceramic, X5R, 16V, ±10%	402	GRM155R61C103K	Murata
2	2	2	2	2	2	2	C7, C8	0.1μF	Capacitor, Ceramic, X7R, 16V, ±10%	402	GRM155R71C104K	Murata
1	1	1	1	1	1	1	D1	Green	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	603	LTST-C190GKT	Liteon
1	1	1	1	1	1	1	D2	BAT54C	Diode, Dual Schottky, 200-mA, 30-V	SOT23	BAT54C	Vishay-Liteon
1	1	1	1	1	1	1	J1	ED1514/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED1514/2DS	OST
3	3	3	3	3	3	3	J2–J4	ED1515/3DS	Terminal Block, 3-pin, 6-A, 3,5mm	0.41 x 0.25 inch	ED1515/3DS	OST
1	1	1	1	1	1	1	J5	2510-6002UB	Connector, Male Straight 2x5 pin, 100mil spacing, 4 Wall	0.338 x 0.788 inch	2510-6002UB	3M
3	3	3	3	3	3	3	JMP1–JMP4	PEC03SAAN	Header, 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
2	2	2	2	2	2	2	JMP3,JMP5	PEC02SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
4	4	4	4	2	4	3		929950-00	Shorting jumpers, 2-pin, 100mil spacing,		929950-00	3M/ESD
1	1	1	1	1	1	1	L1	1.0μH	2.5mmx2mm, 1.0μH, ±30%, 1.5A	0.11x0.09 inch	LQM2HPN1R0MJ0 or MIPS2520D1R0 or MDT2520-CN1R0M or CP1008	Murata or FDK or TOKO or Inter-Technical
1	1	1	1	1	1	1	R1	0.068	Resistor, Chip, 68mΩ, 125mW, 5%	402	ERJ-2BWJR068X	Panasonic
1	1	1	1	1	1	1	R2	5.1k	Resistor, Chip, 5.1kΩ, 1/16-W, 5%	603	Std	Std
1	1	1	1	1	1	1	R3	10k	Resistor, Chip, 10kΩ, 1/16-W, 5%	603	Std	Std
1	0	0	0	0	0	0	U1	BQ24150RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24150RGY	TI
0	1	0	0	0	0	0	U1	BQ24151RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24151RGY	TI
0	0	1	0	0	0	0	U1	BQ24152RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24152RGY	TI
0	0	0	1	0	0	0	U1	BQ24153RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24153RGY	TI
0	0	0	0	1	0	0	U1	BQ24155RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24155RGY	TI
0	0	0	0	0	1	0	U1	BQ24156RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24156RGY	TI
0	0	0	0	0	0	1	U1	BQ24159RGY	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	QFN-14	BQ24159RGY	TI
1	1	1	1	1	1	1	--	HPA255	PCB, 2.0 In x 2.0 In x 0.031 In		PCB	Any

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies mut comply with workmanship standards IPC-A-610 Class 2.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4 V to 6 V and the output voltage range of 0 V to 4.44 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 65° C. The EVM is designed to operate properly with certain components above 125° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

IMPORTANT NOTICE