

A

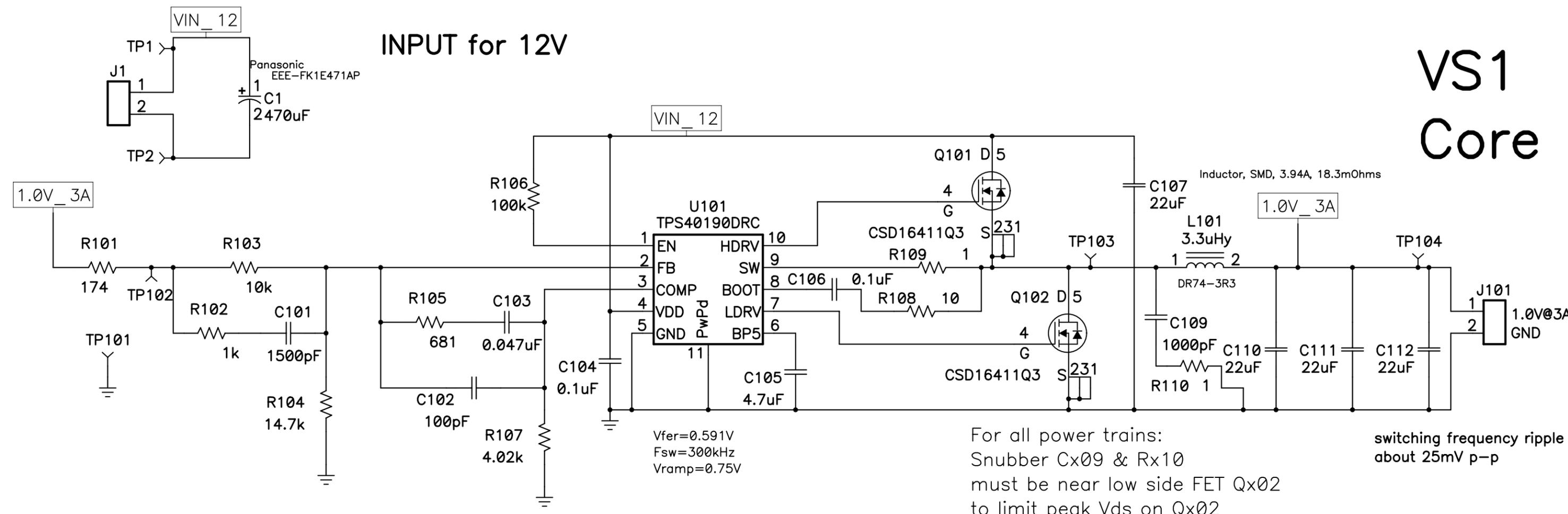
B

C

D

INPUT for 12V

VS1
Core



Texas Instruments

Title 8 switchers & DDR3 off 12V TPS40190		
Size B	Number PMP5018	Rev A
Date August 28, 2009	Drawn by Mandelcorn	
Filename PMP5018_REVA.SCH	Sheet 1 of 7	

1V@3A

A

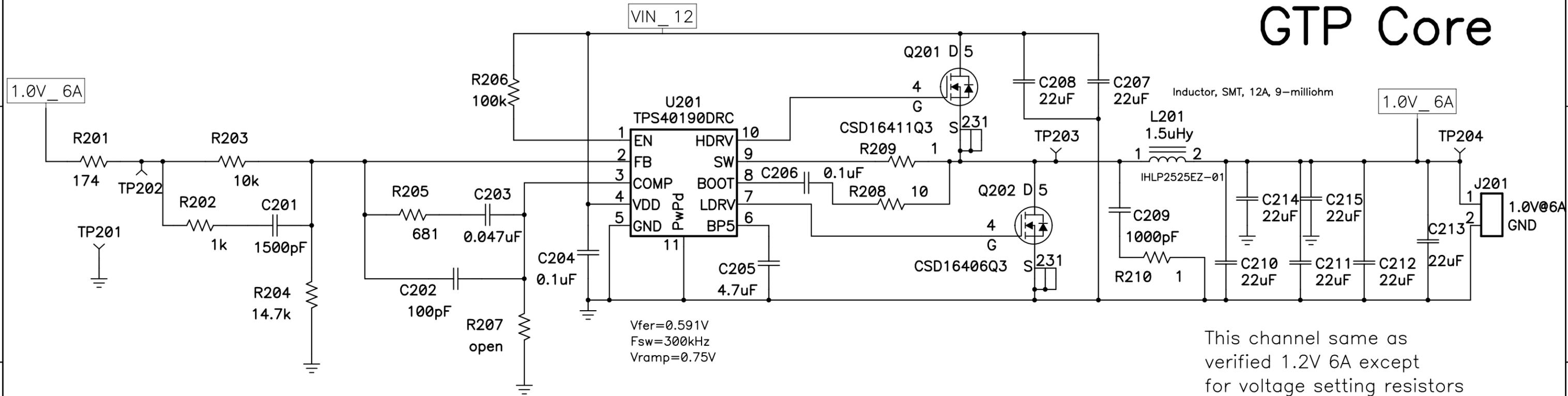
B

C

D

VS2 GTP Core

target 100mV p-p on input



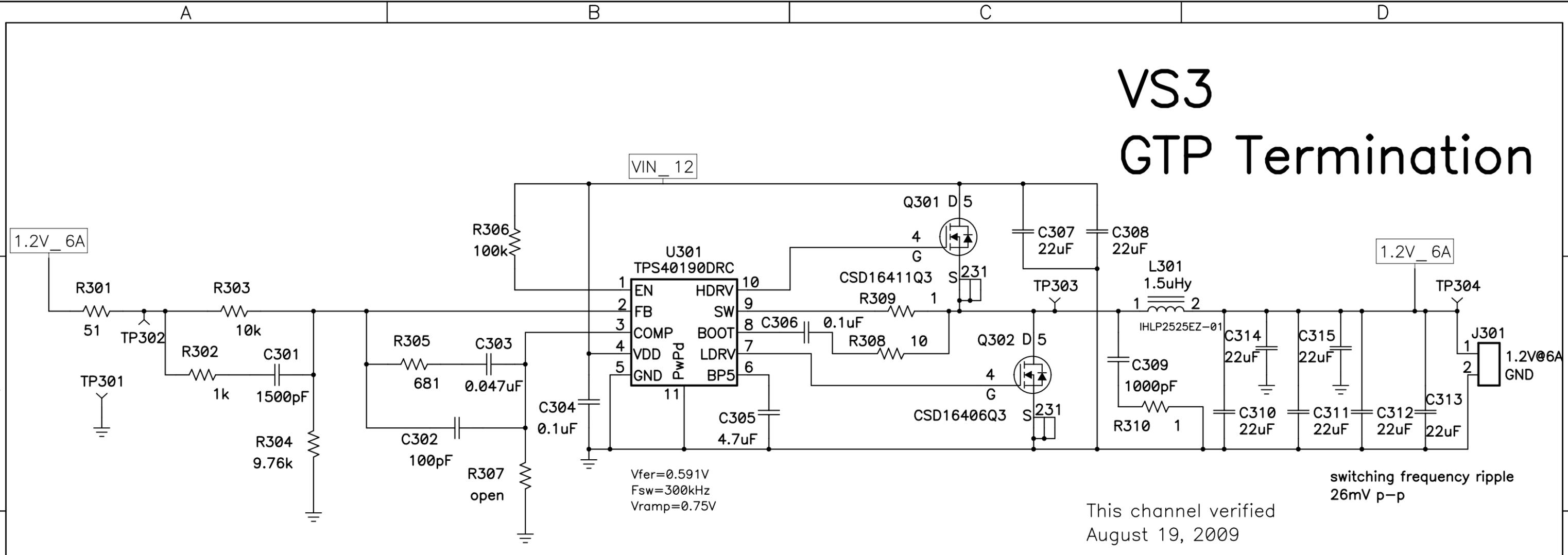
This channel same as verified 1.2V 6A except for voltage setting resistors

1V@6A

Texas Instruments

Title 8 switchers & DDR3 off 12V TPS40190		
Size B	Number PMP5018	Rev A
Date August 28, 2009	Drawn by Mandelcorn	
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VS3 GTP Termination



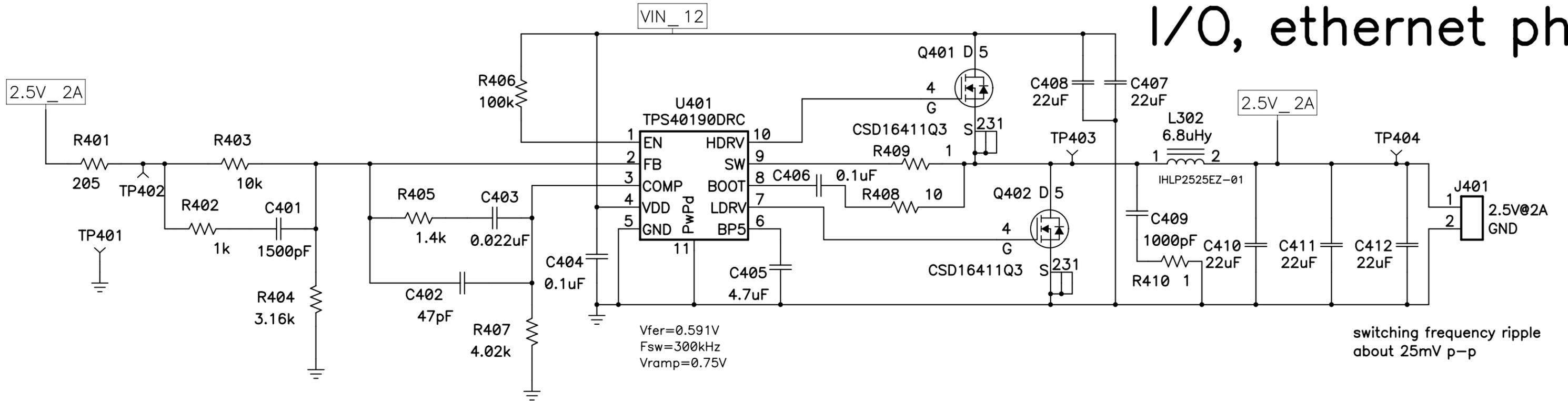
This channel verified
August 19, 2009

switching frequency ripple
26mV p-p

1.2V@6A

Texas Instruments		
Title 8 switchers & DDR3 off 12V TPS40190		
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VS4 I/O, ethernet phy



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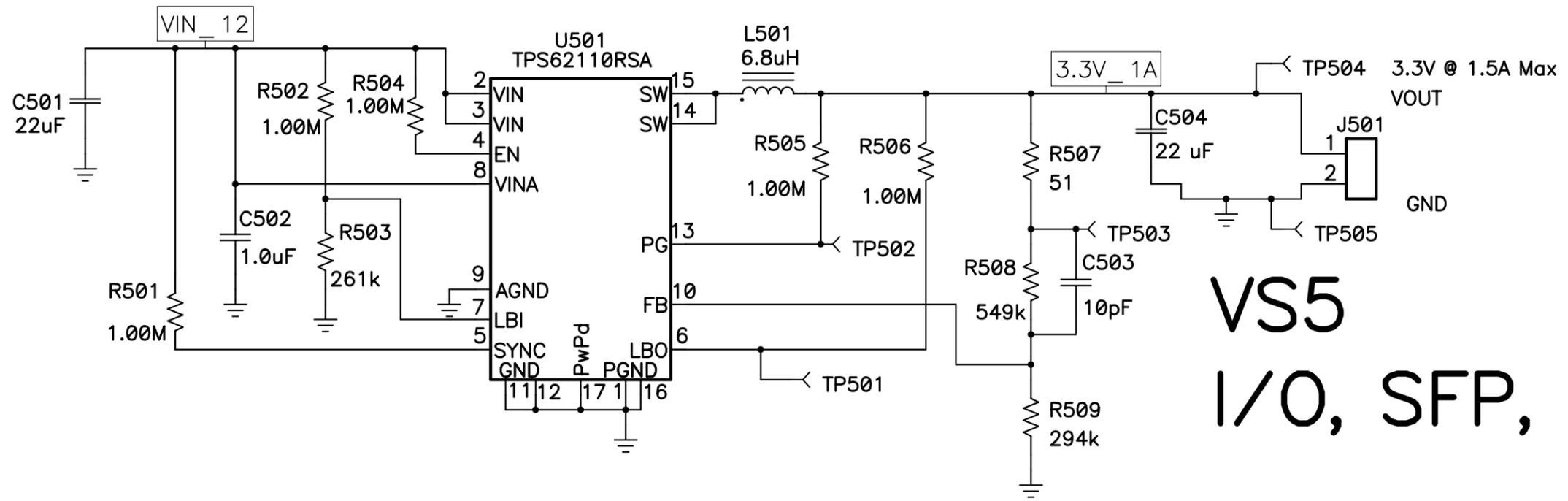
2.5V@2A

A

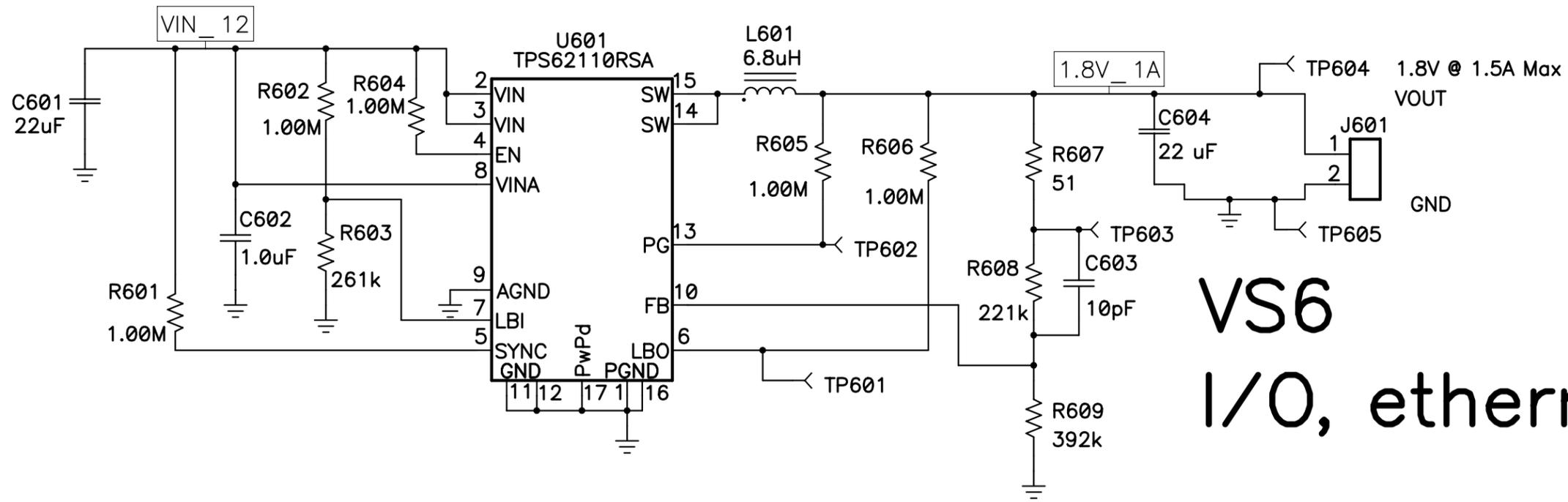
B

C

D



VS5
I/O, SFP, etc.



VS6
I/O, ethernet phy, etc.

Texas Instruments

Title 8 switchers & DDR3 off 12V TPS40190		
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3.3V1A & 1.8V1A

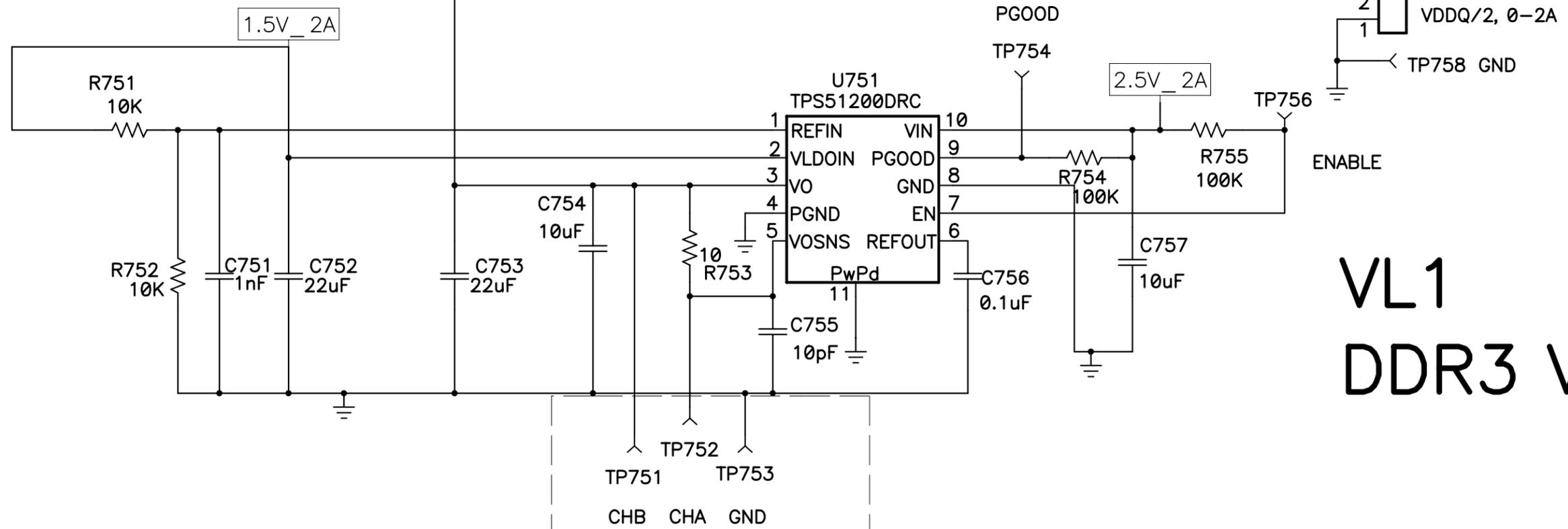
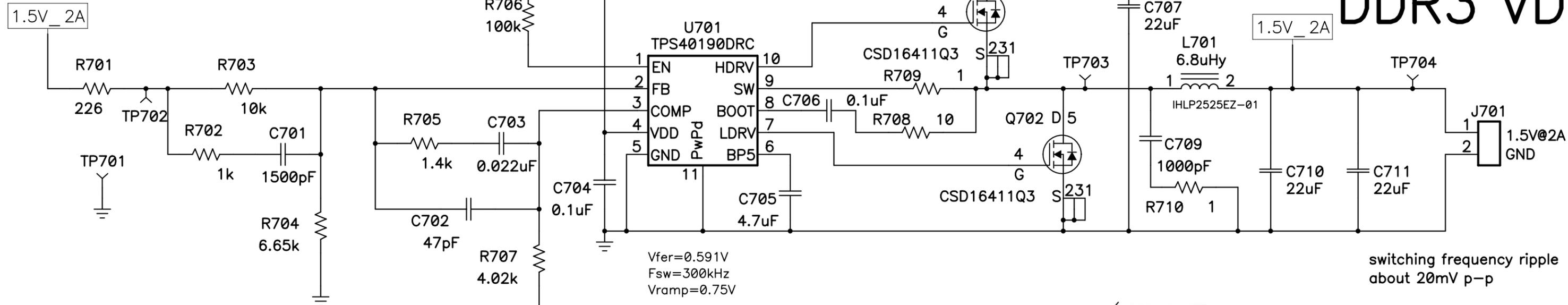
A

B

C

D

VS7 DDR3 VDD



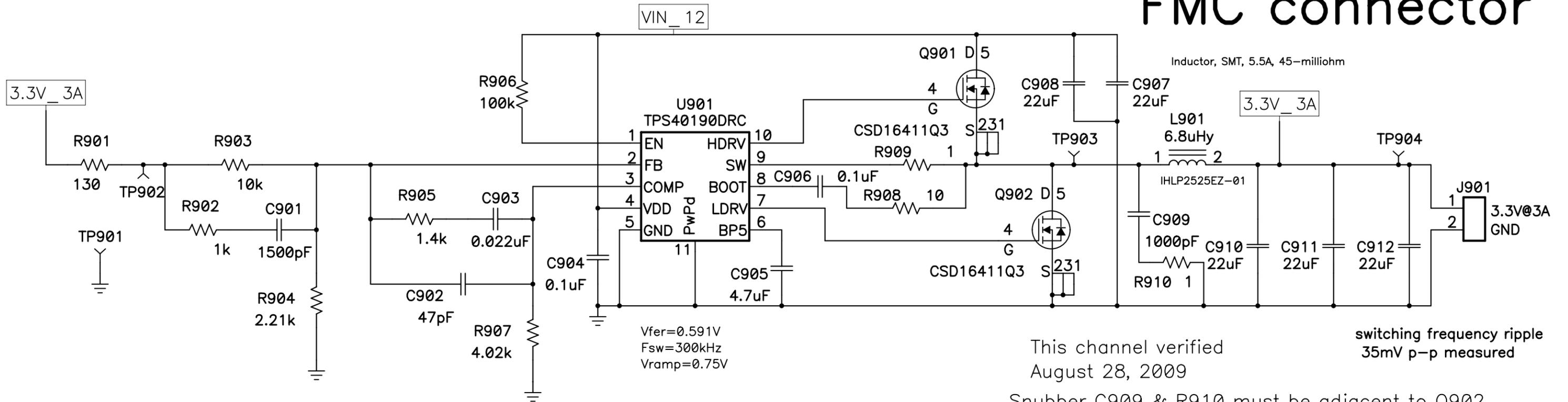
VL1 DDR3 VTT

1.5V & 0.75V 2A

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Title 8 switchers & DDR3 off 12V TPS40190		
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VS9 FMC connector



Vfer=0.591V
Fsw=300kHz
Vramp=0.75V

This channel verified
August 28, 2009

switching frequency ripple
35mV p-p measured

Snubber C909 & R910 must be adjacent to Q902
to limit peak Vds on Q902

3.3V@3A

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Title 8 switchers & DDR3 off 12V TPS40190		
Size B	Number PMP5018	Rev A
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