

LP8764-Q1 / LP8762-Q1 Silicon Revision 2.0 Errata



ABSTRACT

This document describes the known exceptions to functional specifications (advisories) for the LP8764-Q1 Four-Phase, 20-A Buck Converter With Integrated Switches ([SNVSAZ9](#)), device.

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1 Usage Notes and Advisories Matrices

1.1 Usage Notes Matrix

There are no usage notes that are applicable to silicon revision 2.0.

1.2 Advisories Matrix

Table 1-1. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED
		2.0
Serial Peripheral Interface	SDO_SPI signal falling edge slew-rate is reduced	X
Built-in Self Test	Voltage monitor Analog-BIST may cause false over voltage and under voltage interrupts	X
Serial Peripheral Interface	SPI Frame Error is generated during device startup if CS_SPI-pin is low	X
Built-in Self Test	Under voltage and short circuit detection comparators are gated for a short period after Runtime BIST is completed	X
State-machine	LP_STANDBY-state quiescent current consumption is ~3 mA	X
Error Signal Monitor	Error Signal Monitoring (ESM) Fail Interrupt (ESM_MCU_FAIL_INT) operation in level mode operation	X
Serial Peripheral Interface	SPI Frame Error is not detected if SCK_SPI has additional rising edge at the end of communication and the number of clock falling edges is correct	X
Register Map	SOFT_REBOOT bit protection	X
GPIOs	EN_DRV(GPIO1) cannot drive high when VCCA and VIO voltages are different	X
Built-in Self Test	PGOOD signal can be erroneously inactive during runtime BIST	X

2 Nomenclature, Package Symbolization, and Revision Identification

2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. Each device has one of three prefixes: X, P, or null (no prefix) (for example, P876411B4). These prefixes represent evolutionary stages of product development from engineering prototypes (P8764-Q1) through fully qualified production devices and tools (LP8764-Q1).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications. For LP8764-Q1 device the prototype version is indicated by removing the first "L" letter (P8764-Q1)
- null** Production version of the silicon die that is fully qualified.

P8764-Q1 devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

2.2 Devices Supported

This document supports the following devices:

- LP876241B2RQKRQ1
- LP876411B4RQKRQ1
- LP876434B7RQKRQ1
- LP876441B1RQKRQ1
- LP876443B3RQKRQ1

All other LP8764-Q1 / LP8762-Q1 devices comply with the datasheet and are not supported by this Errata document.

2.3 Package Symbolization and Revision Identification

Table 1 describes the device marking, content of the TI_DEVICE_ID and TI_NVM_ID registers and silicon revision of the devices supported by this document.

Table 2-1. Revision Identification

DEVICE MARKING	TI_DEVICE_ID / TI_NVM_ID	SILICON REVISION
LP8762 41B2-Q1	0x8A / 0xB2	2.0
LP8764 11B4-Q1	0x86 / 0xB4	2.0
LP8764 34B7-Q1	0x86 / 0xB7	2.0
LP8764 41B1-Q1	0x86 / 0xB1	2.0
LP8764 43B3-Q1	0x86 / 0xB3	2.0

3 Silicon Revision 2.0 Usage Notes and Advisories

This section lists the usage notes and advisories for this silicon revision.

4 Silicon Revision 2.0 Usage Notes

There are no usage notes that are applicable to silicon revision 2.0.

5 Silicon Revision 2.0 Advisories

The following advisories are known design exceptions to functional specifications. Advisories are numbered in the order in which they were added to this document. Some advisory numbers may be removed in future revisions of this document because the design exception was fixed or documented in the device-specific datasheet or user guide. When items are deleted, the remaining advisory numbers are not re-sequenced.

5.1 Advisories

Advisory 1

SDO_SPI signal falling edge slew-rate is reduced

Revisions Affected

Silicon Revision 2.0

Details

When SPI interface is used, the SDO_SPI (GPIO3) slew-rate for falling edge is reduced. Serial Peripheral Interface (SPI) Electrical characteristics Pos15.10a "New output data valid after SCLK falling, $V_{VIO} = 1.8\text{ V}$ " is max. 72 ns (instead of max. 60 ns) and Pos15.10b "New output data valid after SCLK falling, $V_{VIO} = 3.3\text{ V}$ " is max. 110 ns (instead of max. 60 ns). The new output data validity after the SCK_SPI pin falling edge limits the maximum clock frequency and Pos15.2 Cycle time.

Workaround

The SCK_SPI clock frequency must be selected so that Pos15.10a/b timing parameters can be tolerated by the SPI host.

Advisory 2

Voltage monitor Analog-BIST may cause false over voltage and under voltage interrupts

Revisions Affected

Silicon Revision 2.0

Details

Voltage monitor Analog-BIST function is performed every time when the Buck or VMONx pin voltage monitor is enabled. The Analog-BIST function may cause false over voltage or under voltage interrupt for the tested Buck or VMONx pin voltage monitor, which can generate trigger to state-machine based on the power group selection of the voltage monitor and thus cause unwanted state transition.

Workaround

There are two use cases that requires software workaround:

1) When the voltage monitor for Buck regulator or VMON1/2 pin is enabled by software (I2C or SPI write), the corresponding over voltage and under voltage interrupt masking must be enabled before enabling the voltage monitor. The Analog-BIST is performed for the voltage monitor as described in Datasheet chapter "Output Voltage Monitor and PGOOD Generation". The over voltage and under voltage interrupt masking must be disabled earliest at time calculated by programmed voltage level (V_{out}) divided by the programmed slew-rate and by adding 500 us time.

2) When the software generates Runtime-BIST request, it must enable over voltage and under voltage interrupt masks at least for all enabled Buck and VMON1/2 voltage monitors before requesting the Runtime-BIST. The completion of the successful Runtime-BIST is indicated by BIST_PASS_INT interrupt and after detecting the interrupt the software must disable the over voltage and under voltage interrupt masks. If the Runtime-BIST fails, the device automatically jumps to SAFE RECOVERY state and performs an automatic startup (unless recovery

counter limit is exceeded). During the startup the default NVM settings are read and the over voltage and under voltage interrupt masking is cleared.

The voltage monitor enable events generated by the state-machine are fixed in the state-machine configuration by masking the over-voltage and under voltage interrupts before enabling the voltage monitor and unmasking the corresponding interrupts when the Analog-BIST is done.

Advisory 3

SPI Frame Error is generated during device startup if CS_SPI-pin is low

Revisions Affected

Silicon Revision 2.0

Details

If SPI interface is used and CS_SPI is low when the device is started up (VCCA is rising) and CS_SPI pin rises during mission states, SPI frame error interrupt (COMM_FRM_ERR_INT) is generated.

Workaround

There is no workaround for SPI frame error generation, but the SPI frame error only generates an interrupt (no state transition) and it can be cleared by software after startup.

Advisory 4

Under voltage and short circuit detection comparators are gated for a short period after Runtime BIST is completed

Revisions Affected

Silicon Revision 2.0

Details

After the Runtime BIST is completed, under voltage and short circuit detection comparators are gated for a time period calculated by programmed voltage (Vout) divided by programmed slew-rate, and thus do not monitor the voltage during that time.

Workaround

The under voltage and short circuit detection are automatically enabled after the gating time. There is no workaround for the delayed monitoring.

Advisory 5

LP_STANDBY-state quiescent current consumption is ~3 mA

Revisions Affected

Silicon Revision 2.0

Details

PVIN pin input voltage monitor is disabled in LP_STANDBY state, which causes power stage pull-down to be activated. The pull-down circuitry causes ~3mA input current from PVIN pins. This current does not affect the device operation, but in practise the LP_STANDBY mode becomes useless because it was intended to operate with very low quiescent current consumption.

Workaround

There is no workaround for the issue. STANDBY mode must be used instead of LP_STANDBY mode in the application (LP_STANDBY_SEL bit is set to 0 always).

Advisory 6

Error Signal Monitoring (ESM) Fail Interrupt (ESM_MCU_FAIL_INT) operation in level mode operation

Revisions Affected

Silicon Revision 2.0

Details

When ESM is enabled and nERR_MCU pin is set to low, ESM_MCU_PIN_INT interrupt is generated after a deglitch time and ESM_MCU_FAIL_INT interrupt is generated after delay-1 timer. If the ESM_MCU_FAIL_INT interrupt is cleared during delay-2, the ESM_MCU_FAIL_INT interrupt is generated again after elapse of delay-2 timer (ESM_MCU_RST_INT interrupt is generated at the same time).

Workaround

There is no workaround for the issue. During operation the software must clear all ESM interrupts after detecting those and getting nERR_MCU back to high state.

Advisory 7

SPI Frame Error is not detected if SCK_SPI has additional rising edge at the end of communication and the number of clock falling edges is correct

Revisions Affected

Silicon Revision 2.0

Details

The frame error detection counts only SCK_SPI falling edges when CS_SPI is low. SCK_SPI signal must be low when CS_SPI signal goes low or high (start and end of communication), but this is not checked by the frame error detection. For example, additional SCK_SPI rising edge at the end of the communication is not detected as frame error.

Workaround

There is no workaround for the issue.

Advisory 8

SOFT_REBOOT bit protection

Revisions Affected

Silicon Revision 2.0

Details

SOFT_REBOOT bit cannot be written by I2C or SPI interface during normal operation.

Workaround

There is no workaround for the issue.

Advisory 9

EN_DRV(GPIO1) cannot drive high when VCCA and VIO voltages are different

Revisions Affected

Silicon Revision 2.0

Details

EN_DRV(GPIO1) cannot be driven high if VCCA voltage is different than VIO voltage (more than 10% difference). There is leakage path from VCCA which limits the EN_DRV output high voltage. The EN_DRV(GPIO1) operates correctly when VCCA and VIO are 3.3V.

Workaround

No workaround for the issue. EN_DRV(GPIO1) pin operates correctly when both VCCA and VIO are 3.3V.

Advisory 10

PGOOD signal can be erroneously inactive during runtime BIST

Revisions Affected

Silicon Revision 2.0

Details

During Runtime BIST and just after that the PGOOD signal is forced to inactive level if Buck voltage monitoring or external voltage monitoring (VMON1/2) is selected to control the PGOOD signal. The PGOOD signal is optional selectable function for GPIO1, GPIO6 and GPIO9.

Workaround

There is software workaround that disables buck output voltage monitoring and external voltage monitoring indication to PGOOD signal during Runtime BIST and thus does not force the PGOOD pin to inactive level. Before initiating the Runtime BIST, the software must set PGOOD_SEL_BUCKx and PGOOD_SEL_VMONx bits to '0' (masked). The completion of the successful Runtime-BIST is indicated by BIST_PASS_INT interrupt and after detecting the interrupt the software must wait the longest voltage monitoring ramp time before the software can set the original settings to the PGOOD_SEL_BUCKx and PGOOD_SEL_VMONx bits. The voltage monitoring ramp time for buck and VMON1/2 pin voltage monitoring is calculated by dividing the programmed voltage level by the programmed slew-rate and by adding 500 us time for this workaround.

6 Trademarks

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