Space-Grade, 100-krad, 1.25-V, Low-Noise Voltage Reference Circuit



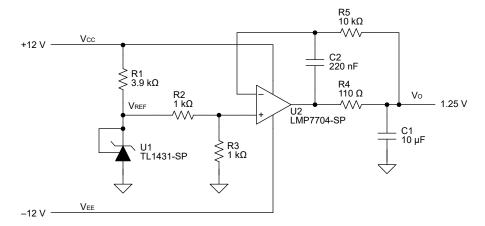
Nigel Smith, Akshat Garg

Design Goals

Parameter	Design Requirement
Supply voltage	±12 V
Output voltage	1.25 V
Output current	1 mA
Output noise	< 25 nV/√Hz from 1 kHz to 10 MHz
Radiation hardness	100 krad(Si)

Design Description

This circuit design uses a low-pass filter and an op amp to reduce the wideband noise generated by a shunt voltage reference. The circuit was originally developed to supply a CCD sensor in a satellite: the shunt reference alone does not meet the performance requirements of the application and needs the additional circuitry to meet the project requirements.



Design Notes

TI has a number of suitable space-qualified voltage references, but for this application the TL1431-SP was selected for its good noise performance and high radiation tolerance. The lowest voltage that U1 can generate is 2.5 V, so R2 and R3 are used to generate a 1.25-V input to U2 (they also attenuate the noise of U1 by a factor of two). Low values are used for R1 and R2 to limit the noise generated by these components. R1 is chosen so that, even with R2 and R3 connected, there is 1 mA of bias current through U1.

R4 and C1 form the low-pass filter that attenuates noise from the voltage reference. With the values shown, the 3-dB frequency of this filter is 145 Hz. The precise values of R4 and C1 are not critical. However, it pays not to make R4 too large, because the op amp has to correct any errors caused by the output current flowing through R4, and if the voltage drop across R4 is too large the op amp may run out of headroom.



R4 and C1 add a pole to the amplifier response; R5 and C2 add a zero that compensates this pole and enables stable operation. R5 and C2 are chosen so that R5 \times C2 = 2 \times R4 \times C1, which minimizes noise gain peaking in the response.

The op amp used for this application should not itself generate significant noise compared to the voltage reference; however, the filter formed by R4 and C1 attenuates whatever noise the op amp does generate. Note that in the case of the LMP7704-SP, with the component values used, current noise is insignificant compared to voltage noise and can be ignored.

Design Steps

- Select resistors R2 and R3 to attenuate the 2.5-V output voltage of the TL1431-SP to 1.25 V. In this case, a value of R2 = R3 = 1 kΩ provides the necessary attenuation and ensures that the thermal noise generated by these resistors is insignificant compared to other noise sources and can be ignored.
- Use the following equation to calculate the current flowing through resistors R2 and R3:

$$I_{(R2)} = I_{(R3)} = \frac{V_{REF}}{R2 + R3} = \frac{2.5 \text{ V}}{1 \text{ k}\Omega + 1 \text{ k}\Omega} = 1.25 \text{ mA}$$

• Use the following equation to calculate the maximum value of R1:

$$R1(max) = \frac{(V_{CC} - V_{REF})}{I_{(U1)} + I_{(R2)}} = \frac{12 \text{ V} - 2.5 \text{ V}}{1 \text{ mA} + 1.25 \text{ mA}} = 4.22 \text{ k}\Omega$$

A value of 3.9 k Ω is therefore suitable for R1.

Choose values for R4 and C1 that will create a pole at the desired cutoff frequency. In this application, a
cutoff frequency of about 150 Hz was selected: this provides sufficient noise attenuation in the frequency
range of interest (1 kHz to 10 MHz). The op amp compensates for the voltage drop across R4, so do not
make it too big. As a general rule, it is recommended to make sure that the voltage drop across R4 is less
than 1 V at maximum output current.

Use the following equation to calculate the RC time constant needed for the desired cutoff frequency:

$$R4 \times C1 = \frac{1}{2\pi f_{co}} = \frac{1}{2 \times \pi \times 150 \text{ Hz}} = 1.06 \text{ ms}$$

Using values of R4 = 110 Ω and C1 = 10 μ F results in a cutoff frequency of 145 Hz.

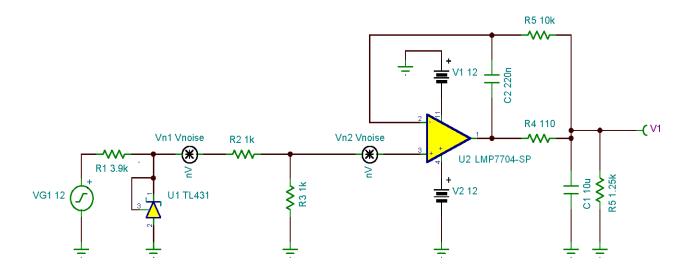
• To minimize noise gain peaking close to the cutoff frequency, choose R5 and C2 so that:

$$R5 \times C2 = 2 \times R4 \times C1 = 2 \times 110 \Omega \times 10 \mu F = 2.2 ms$$

Design Simulations

Simulation Setup

The easiest way to analyze the noise performance of a circuit like this is to use a simulation program such as TINA.



The SPICE macros for the TL431 and LMP7704 included in the standard TINA library¹ do not include models for the noise performance, so separate voltage noise sources must be included in the simulation circuit (see Vn1 and Vn2 in the previous TINA schematic). The macros for the noise sources can be copied from the Vnoise.TSC file referred to in this E2E™ thread, and edited, and three parameters describing the noise characteristic of the devices entered (highlighted in bold in the following macro extract).

```
* BEGIN PROG NSE NANO VOLT/RT-HZ
.SUBCKT VNSE 1 2
* BEGIN SETUP OF NOISE GEN - NANOVOLT/RT-HZ
* INPUT THREE VARIABLES
 SET UP VNSE 1/F
* NV/RHZ AT 1/F FREQ
. PARAM NLF=225
* FREQ FOR 1/F
.PARAM FLW=10
 SET UP VNSE FB
* NV/RHZ FLATBAND
.PARAM NVR=125
* END USER INPUT
* START CALC VALS
.PARAM GLF={PWR(FLW, 0.25)*NLF/1164}
.PARAM RNV={1.184*PWR(NVR,2)}
.MODEL DVN D KF={PWR(FLW,0.5)/1E11}IS=1.0E-16
* END CALC VALS
I1 0 7 10E-3
I2 0 8 10E-3
D1 7 0 DVN
D2 8 0 DVN
E1 3 6
       7 8
           {GLF}
R1 3 0 1E9
R2 3 0 1E9
R3 3 6 1E9
E2 6 4 5 0 10
R4 5 0 {RNV}
R5 5 0 {RNV}
R6 3 4 1E9
R7 4 0 1E9
E3 1 2 3 4 1
```

A more recent model for the LMP7704 does include the noise sources. The model is now uploaded to its product folder on ti.com. When using spice models to evaluate circuit performance, take care to determine which parameters the models do and do not include.



```
C1 1 0 1E-15

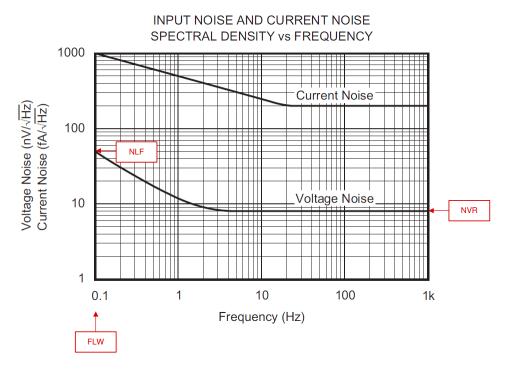
C2 2 0 1E-15

C3 1 2 1E-15

.ENDS

* END PROG NSE NANOV/RT-HZ
```

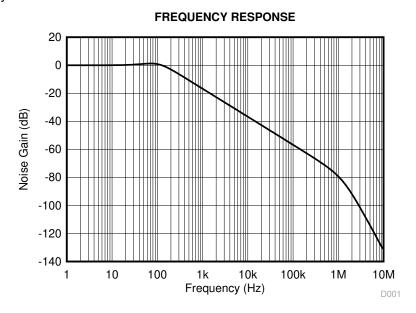
NLF is the magnitude of the noise where the curve crosses the y-axis at the minimum frequency, and FLW is the frequency at which this happens. NVR is the magnitude of the wideband noise. These parameters can easily be taken from the data sheets of the devices (see the following figure). All values entered in the macros must be in nV/\sqrt{Hz} .



Simulation Results

Op amp frequency response

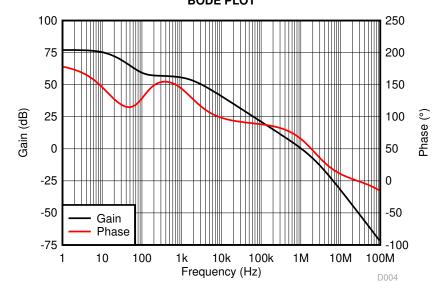
The following figure shows the overall frequency response of the op amp circuit showing negligible gain peaking at the cutoff frequency.



Op amp stability

The following figure shows the bode plot of the op amp circuit. Phase margin is 64° and gain margin is 49 dB.

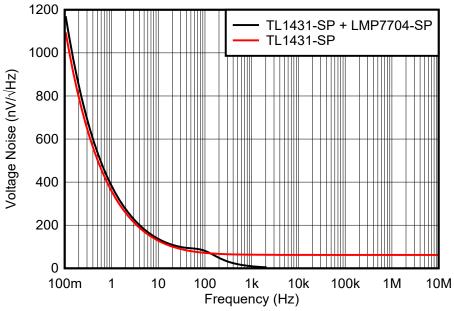
BODE PLOT



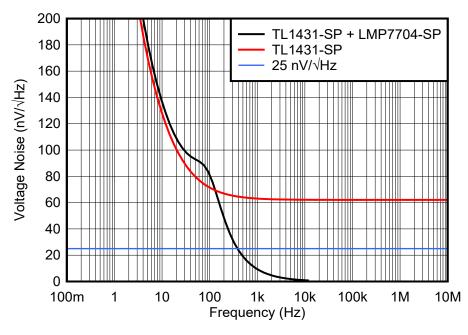
Noise performance

The following figures show the noise performance of the complete circuit with normal and expanded scales. The figures show that noise performance surpasses the design requirement limit of 25 nV/ $\sqrt{\text{Hz}}$ in the frequency range of 1 kHz to 10 MHz.





NOISE PERFORMANCE - EXPANDED SCALE



Design References

See the TINA/Spice: Noise Generator E2E™ thread for more information.

Design Featured Op Amp

LMP7704-SP	
Supply voltage range	2.7 V to 12 V
Offset voltage	±60 μV (Maximum)
Open-loop gain	130 dB
Quiescent current	2.9 μA/amplifier (typical)
Input bias current	±500 fA
Input voltage noise density	9 nV/√Hz (typical)
Input current noise density	1 fA/√Hz (typical)
Total ionizing dose	100 krad(Si)
Single-event latch-up immunity	85 MeV-cm ² /mg
LMF	P7704-SP

Design Featured Voltage Reference

2.5 V to 36 V
1 mA to 100 mA
-1% / +1.6%, @25°C
1.5 μA, typical @ 25°C
0.2 Ω, typical @ 25°C
100 krad(Si)
N/A (bipolar process)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2022, Texas Instruments Incorporated