Application Brief **Protection against Unsuppressed Load Dump in Automotive Systems using LM74930-Q1**

Gorrela Praveen

Introduction

In automotive systems, there is an increasing use of electronic circuits due to pursuit of heightened safety, advanced infotainment connectivity features, innovations in self-driving technology, and the growing emphasis on environmental sustainability and vehicle performance enhancement. These electronic circuits draw power from the battery of the vehicle, where transients can arise due to factors such as abrupt changes in electrical load (for example, engine start or activation of high-power accessories), fluctuations in alternator voltage, and external influences such as electrical interference. The load-dump pulse (which is a high-energy transient) is defined as one of the most destructive pulses defined in ISO 16750-2 The load-dump pulse includes test A and test B, which were previously designated as 5A and 5B in ISO 7637-2. This application brief provides guidance on safeguarding the automotive downstream subsystem from load-dump pulses in 24-V systems using the LM74930-Q1.

Unsuppressed Load Dump

A load dump occurs when the load to which a generator is delivering current is abruptly disconnected. In automotive electronics, this applies to disconnecting a battery while alternator is charging the battery to which other electrical loads are connected. Figure 1 shows a typical load dump condition when the alternator is disconnected from the battery.



Figure 1. Typical Load Dump Condition



Some automotive systems contain centralized load dump suppression which clamps the peak surge voltage to 35 V in 12-V battery systems and 58 V for 28-V battery systems. In designs lacking this centralized suppression, the surge voltage can exhibit higher peak voltages. The unsuppressed load dump transient is defined in ISO 16750-2 standard load dump Test A and the voltage profile is as shown in Figure 2.



Figure 2. Unsuppressed Load Dump Pulse

The typical values of the ISO 16750-2 load dump test A for a 12-V and 24-V battery system is listed in Table 1.

Table 1. Typical Values of the ISO 16750-2 Load
Dump Test A

Parameter	12-V System	24-V System	
Us	79 V to 101 V	151 V to 202 V	
R _i	0.5 Ω to 4 Ω	1 Ω to 8 Ω	
t _d	40 ms to 400 ms	100 ms to 350 ms	
t _r	$\begin{pmatrix} 0\\ 10-5 \end{pmatrix}$ ns		

1



In 24-V battery systems that do not have a centralized load dump suppression scheme, the surge voltage during load dumps can be as high as 202 V and persist for a duration ranging from 100 milliseconds to 350 milliseconds, depending on the specific testing conditions, which can result in a significant energy surge that poses a threat to the downstream electrical components.

Protection against unsuppressed load dump using LM74930-Q1

The basic approach to protect an automotive electronic subsystem from unsuppressed load dump is by using a transient voltage suppressor. The TVS diode absorbs the transient pulse energy and clamps the voltage to within the absolute maximum voltage of the downstream components. The energy dissipated in the TVS depends on the peak transient voltage, clamping voltage, pulse duration, and input impedance of the load-dump source. Finding a single TVS diode with the required peak power rating and pulse duration rating to effectively absorb the maximum energy of the pulse can be challenging. Compounding the issue, the ISO 16750-2 specification requires that the system withstand 10 consecutive pulses with a one minute interval, and a TVS diode can degrade after each load-dump event. Several high-power TVS stacks (SMD sized) are required to clamp to a safe level, which results in an increase in overall design size and BOM cost of the front-end protection circuit. Consequently, relying solely on a TVS diode becomes a challenging approach for designing a cost and size effective system capable of effectively shielding against load-dump pulses.

Automotive subsystems that directly run from battery power typically feature an ideal diode circuit at the front-end to protect the down-stream circuitry from reverse battery connection or dynamic reverse polarity conditions during an inductive load disconnect from the battery. TI's LM74930-Q1 ideal diode controller design (apart from reverse battery protection and reverse current blocking) can protect the subsystem from unsuppressed load dump using the series power path protection technique. The device also offers overcurrent and short circuit protection, which is an option for highpower applications. The LM74930-Q1 configured in common-source topology to provide a 200-V unsuppressed load dump protection with reverse battery protection is shown in Figure 3.



Figure 3. Typical Application Circuit: 200-V Unsuppressed Load Dump Protection with Reverse Battery Protection

MOSFET Q1 is used to turn off or clamp output voltage to an acceptable safe level and protects the MOSFET Q2 and downstream circuitry from an input 200-V transient. Note that in the circuit, only the VS pin is exposed to 200 V and the pin must be protected. A series 10-k Ω resistor and a 60-V rated Zener diode across the VS to GND clamps the voltage on the VS pin to within the recommended operating voltage of the device. The rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can be turned off completely or the output voltage can be clamped to a safe level. The maximum voltage that is allowed to pass through the MOSFETs can be set

2

using the overvoltage threshold by adjusting the R3 and R4 resistors. With the resistor ladder connected to the input supply side, the circuit operates in overvoltage cutoff mode. Connected to the VOUT side, the circuit operates in VOUT clamp mode. The VOUT clamp is achieved by hysteric output on and off control where the HGATE is turned on and off as the output voltage rises above the overvoltage rising threshold and falls below the overvoltage falling threshold respectively.



The VDS rating of the MOSFET Q1 must be minimum 200 V for a output cutoff design where output can reach 0 V while the load dump transient is present and must be a minimum of 164.5 V when output is clamped to 37 V (\pm 1.5 V). Figure 4 and Figure 5 show the unsuppressed load dump protection with a VOUT clamp and OV cutoff operation, respectively.







Figure 5. Unsuppressed Load Dump 200 V: Output Cut-Off (R3 Connected to VBATT)

Power dissipation in MOSFET Q1 on a design where output is clamped is critical. Safe operating area (SOA) characteristics of the MOSFET must be considered with sufficient design margin for reliable operation. LM74930-Q1 also supports overvoltage clamp operation with programmable timer and circuit breaker functionality. To enable device operation in overvoltage clamp with circuit breaker functionality, connect the OVCLAMP pin to the OV pin. The OVCLAMP feature allows the user to select the duration of over voltage clamp operation as per the MOSFET power handling capability and as a result, maintaining operation within the SOA. Figure 6 shows the VOUT clamp operation with a 30-ms timer and circuit breaker functionality.



Figure 6. Unsuppressed Load Dump 200 V: Output Clamp with Timer (OVCLAMP Connected to OV, TMR = 68 nF)

Summary

To maintain passenger safety in automotive applications, electronic subsystems must operate reliably under all circumstances. To achieve this, manufacturers must develop robust subsystem protection mechanisms that protect downstream components against damage from high-energy transient pulse, such as the unsuppressed load-dump pulse. For high power applications, LM74930-Q1 ideal diode controller which drives back-to-back external N-Channel MOSFETs connected in common source topology is an attractive front-end protection design against a 200-V unsuppressed load dump. Designers can select one of the operation modes: output cut-off, output clamp, and output clamp with circuit breaker to protect the downstream systems while maintaining the safe operation of MOSFETs. Test results for ISO 16750-2 load dump pulse A under various operating modes demonstrate the resilience of the LM74930-Q1 based protection design.

3

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2023, Texas Instruments Incorporated