

PCB Design Requirements for VDD_MPU_IVA Power Distribution Network for TI OMAP3630, AM37xx, and DM37xx Microprocessors

The Sitara™ ARM® MPU Applications Team

ABSTRACT

The purpose of a power distribution network (PDN) is to provide clean and reliable power to active devices in the system. The printed circuit board (PCB) is a critical component of the system-level PDN. Therefore, the PCB design is of utmost importance for high-performance low-power microprocessors. This application report provides design requirements and details a step-by-step methodology on how to design the VDD_MPU_IVA PDN on the PCB to comply with the requirements of the TI OMAP3630, AM37xx, and DM37xx microprocessors.

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1 Introduction

This application report provides detail design guidelines and specific recommendations for designing a PCB power delivery network (PDN) for the high performance/low power TI OMAP3630, AM37xx, and DM37xx microprocessors. The approach used here is: outline what the PCB PDN design target requirements are, discuss the fundamental rational behind these requirements and, whenever appropriate, provide suggestions/means that the PCB designers can adopt to validate that the PDN requirements are met.

2 PCB PDN Design Methodology

- **Step 1:** Requirements and guidelines for PCB Stack-up
- **Step 2:** Physical layout optimization of the PDN
- **Step 3:** Static IR drop optimization of PDN
 - Minimize resistance, avoid neck-down, and reduce current density
- **Step 4:** ac resonance Check
 - Target impedance, resonance and anti-resonance peaks, and decoupling optimization scheme (type, placement, and value)
- **Step 5:** Checklist for PDN requirements/specifications

3 Step 1: Requirements and Guidelines for PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the power distribution system. An optimized PCB stack-up for higher power integrity performance can be achieved by following these requirements:

- Power and ground plane pairs/*islands* should be closely coupled together. The capacitance formed between the planes can be used to decouple the power supply at high frequencies. Whenever possible, the power and ground planes should be solid to provide a continuous return path for return current.
- Use a thin dielectric thickness between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (i.e., the dielectric thickness) maximizes the capacitance.
- Keep the power and ground plane pair as close to the TOP and BOTTOM surfaces as possible (see [Figure 1](#)). This will help in minimizing the decoupling capacitors mounting, via, and the power/ground plane pair spreading loop inductance.

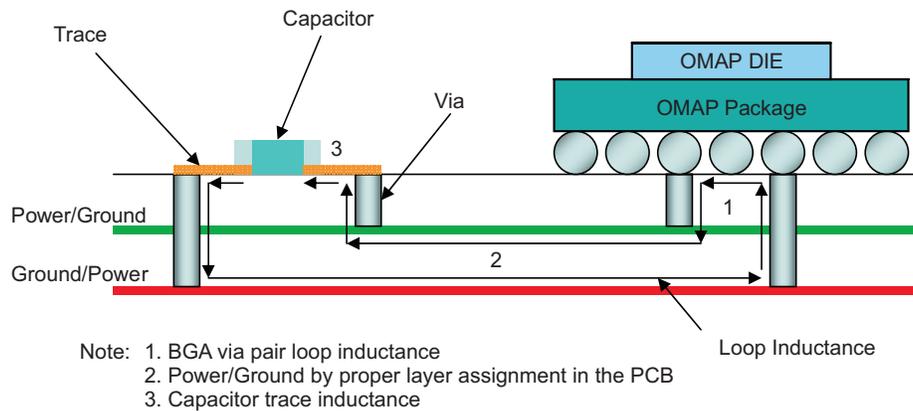


Figure 1. Minimize Loop Inductance by Proper Layer Assignment in the PCB

The placement of power and ground planes in the PCB stack-up (determined by layer assignment) has a significant impact on the parasitic inductances of power current path as shown in Figure 1. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high priority supplies in the top half of the stack-up and low-priority supplies in the bottom half of the stack-up as shown in the following figures.

Figure 2 and Figure 3 show examples of typical PCB stack-up designed with power integrity in mind.

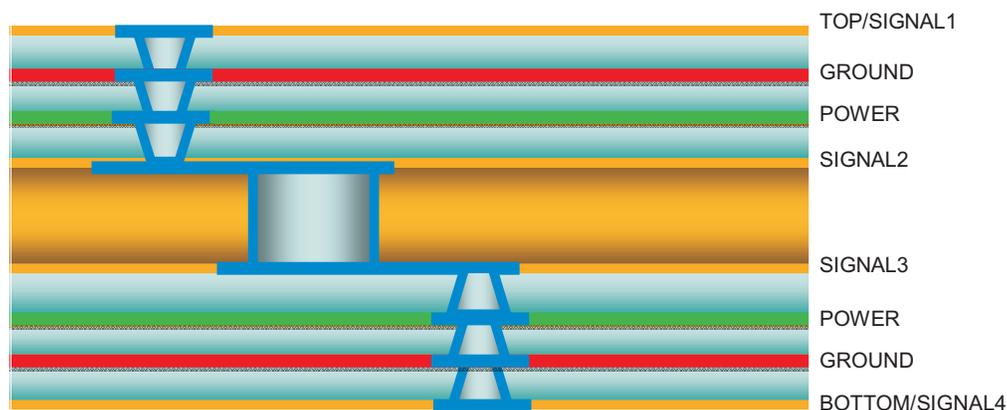


Figure 2. An Example PCB Layer Assignment That Uses High-Density Interconnect (HDI) Vias

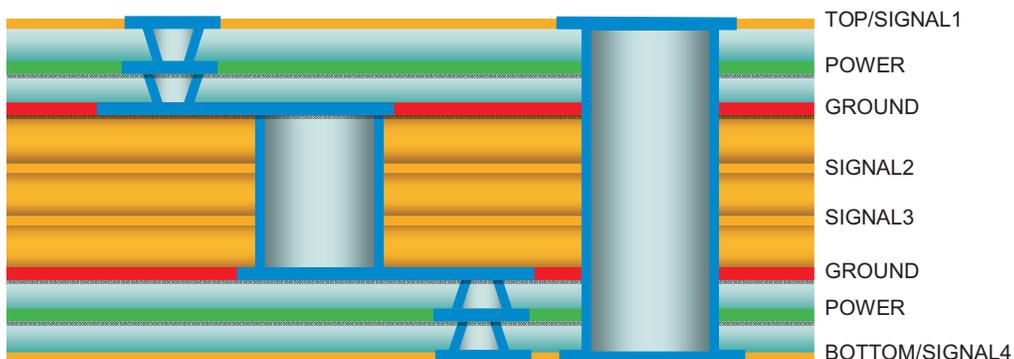


Figure 3. Another 8-Layer PCB Design That Uses Plated Through Hole (PTH) Vias

4 Step 2: Physical Layout Optimization of the PDN

A critical step in designing an optimized PDN is that proper care should be taken to make sure that the initial layout is done with good power integrity design guidelines in mind. What follows are some important requirements that need to be implemented in the PCB PDN design.

- External trace routing between components should be as wide as possible. Wider traces lower the impedance, which reduces the static IR drop and improves high frequency performance of the PDN.
- Whenever possible, use a minimum trace width to solder pad ratio of 1:1 or greater for passive component (e.g., capacitors and resistors) pins and vias. Do not share vias among multiple capacitors.
- Placement of the vias should be as close to the solder pad as possible.

Figure 4 depicts an example of *acceptable* width for power net routing but with *poor* via placement. Figure 5 shows an *improved* power net routing with *appropriate* via assignment and placement, respectively.

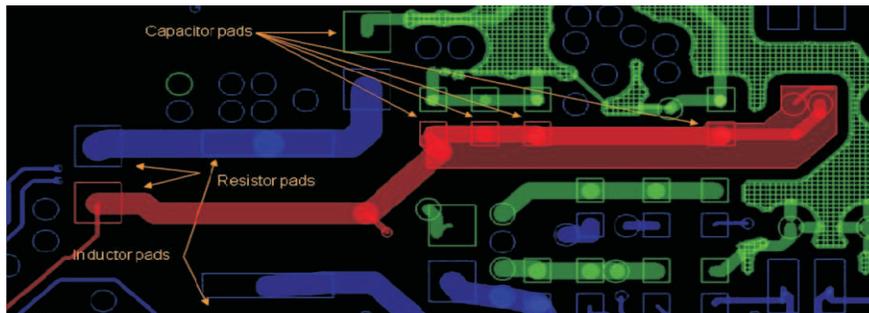


Figure 4. Poor Via Assignment for PDN

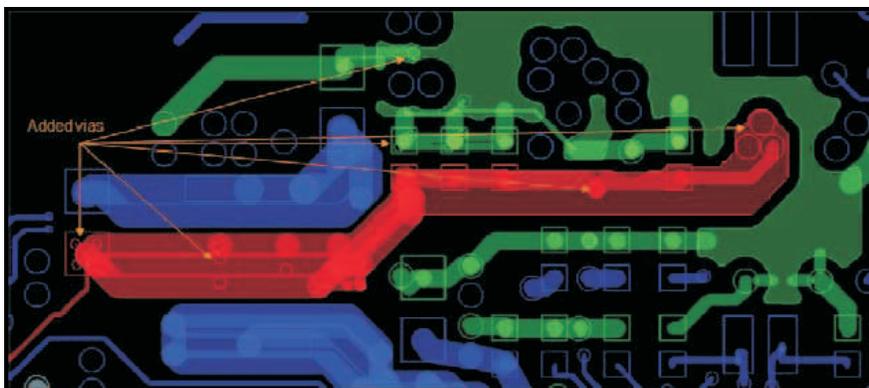


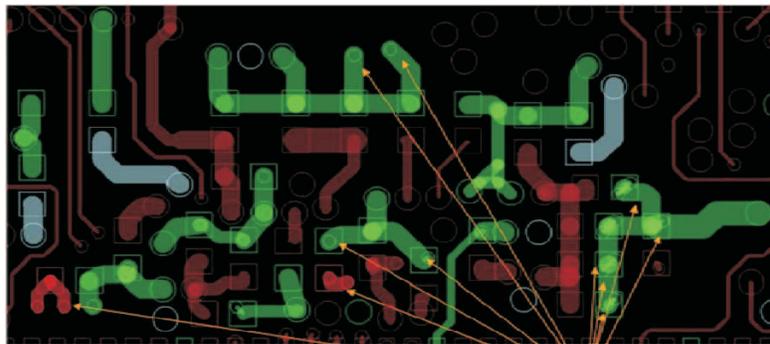
Figure 5. Improved Via Assignment for PDN

- To avoid any *ampacity* issue – maximum current-carrying capacity of each transitional via should be evaluated to determine the appropriate number of vias required to connect components. Figure 6 and Figure 7 are examples of *via starvation* on a power net transitioning from the TOP routing layer to internal layers and the *improved* layout, respectively.
- It is also a good practice to perform static IR drop (discussed in Section 5). This analysis can be used to assess the appropriate number of vias and geometrical trace width dimensions required to meet the expected IR drop requirement.



One via for 5 capacitor pads is NOT good practice

Figure 6. An Example Showing Via Starvation



Added vias

Figure 7. Improved Layout With More Transitional Vias

- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. As discussed in earlier sections, routing power nets in plane provide for more inter-plane capacitance and improve high frequency performance of the PDN.
- Try to avoid different power nets (e.g., VDD_MPU_IVA with VDD_CORE) coupling on the PCB by using *co-planar* shielding whenever appropriate. Figure 8 depicts an example of *co-planar* shielding for power nets.

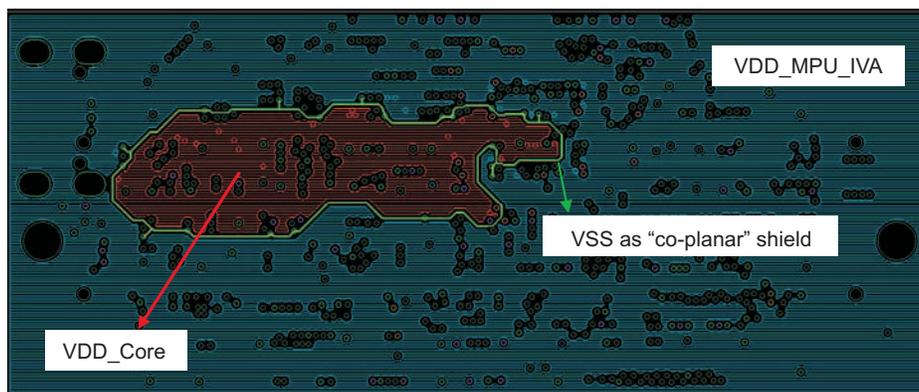


Figure 8. Example of Co-Planar Shielding of Power Net Using Ground Guard-Band

- Decoupling capacitors should be mounted with minimum impact to inductance. A capacitor has characteristics not only of capacitance but also inductance and resistance. Figure 9 shows the parasitic model of a real capacitor. A real capacitor should be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).



Figure 9. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$$

Where

$$\omega = 2\pi f \tag{1}$$

Figure 10 shows the resonant frequency response of a typical capacitor with self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance, reactive capacitance, and inductance as shown in Equation 1.

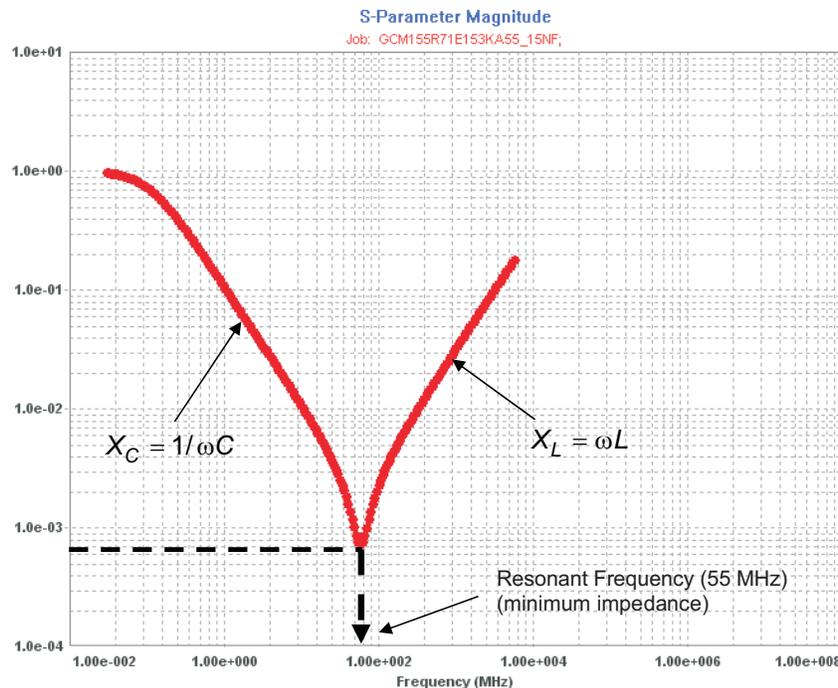


Figure 10. Typical Impedance Profile of a Capacitor

- Since the capacitors have series inductance and resistance that will impact its effectiveness, it is important that the following recommendations are adopted in placing them on the power distribution network. Whenever possible, make sure to mount the capacitor with the geometry that minimizes the mounting inductance and resistance as shown earlier in Figure 1. The capacitor mounting inductance and resistance here includes the inductance and resistance of the pads, trace, and vias.
- The length of trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace should be as short and wide as possible. Wherever possible, minimize the trace length by locating vias near the solder pads. Further improvements can be made by placing vias to the side of capacitor solder pads or doubling the number of vias as shown in Figure 11. If the PCB manufacturing processes allow, and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up (as shown in Figure 1).

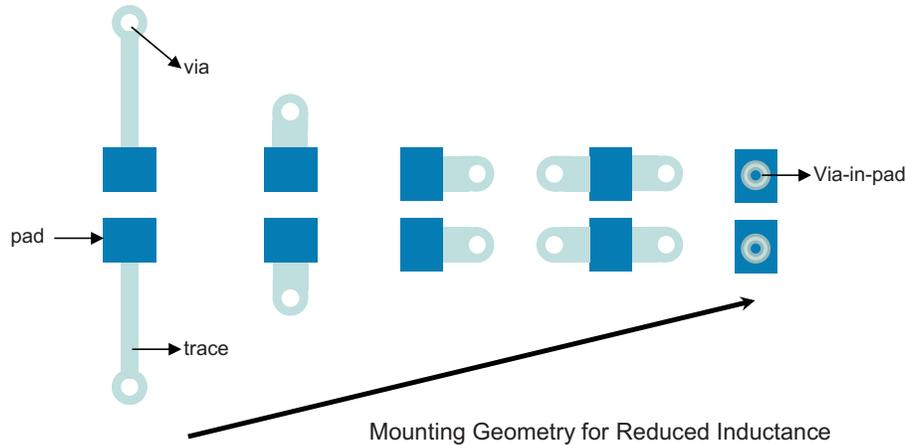


Figure 11. Capacitor Placement Geometry for Improved Mounting Inductance

5 Step 3: Static IR Drop PDN Optimization

Delivering reliable power to circuits is always of critical importance because IR drops can occur on multiple components of the PDN. Power distribution cables, connectors, PCBs, semiconductor packaging, and semiconductors are all example components of the PDN that may contribute to the system level IR drop. Components that are distant from their associated power source are particularly susceptible to IR drop, and designs that rely on battery power must minimize voltage drop to avoid unacceptable power loss. Early DC assessments help determine power distribution basics such as the best available entry point for power, layer stack-up choices, and estimates for the amount of copper needed to carry the current.

The resistance R_s of a plane conductor for a unit length and unit width is called the surface resistivity (Ω s per square).

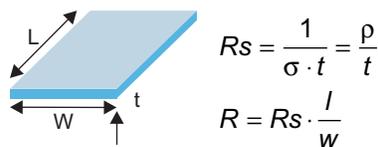


Figure 12. Depiction of Sheet Resistivity and Resistance

Ohm's Law ($V=IR$) relates conduction current to voltage drop, and at dc, the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

Systems with on-board power sources have three primary components that may contribute IR drop; semiconductor, semiconductor package and main PCB. Static IR or dc analysis/design methodology consists of designing the PDN such that the voltage available (under dc operating conditions) to the power and ground pads of the applications processor transistors is within a specified value of the nominal voltage, for proper functionality of the device. The PCB-contribution to the static IR drop budget is defined as the dc voltage drop between the solder pads of the power management integrated circuit (PMIC) or voltage regulator module (VRM) and the BGA solder pads of the applications processor (as shown in Figure 13).

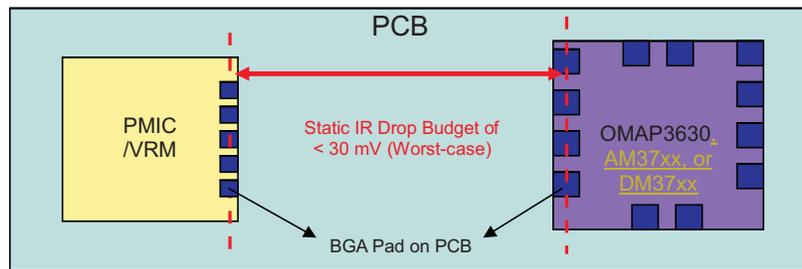


Figure 13. Static IR Drop Budget for PCB Only

Given the total system-level margin allowed for proper device functionality, allowable voltage variation at the power terminals of the applications processor is specified at 2.5% of the nominal voltage. For a 1.2 V supply, this should be ≤ 30 mV. This is ONLY permitted under the assumption that the power source feedback or sense is connected to a point very close to the applications processor, such the DC IR drop is compensated by the power source. If the power source feedback or sense is not connected to a point close to the applications processor, the static IR drop must be controlled to 0.5-1.0% for proper device functionality.

- It is highly recommended the power source feedback or sense line on the PCB is connected as close as physically possible to the applications processor.

To check if the static IR drop is within specification, the PCB designer needs to perform the appropriate analysis and compare the results to the power supply tolerance specification of $\pm 0.5\%/2.5\%$ (based on PMIC/VRM sense design topologies discussed above). To accurately analyze PCB static IR drop, the actual geometry of the PDN must often be properly modeled and simulated to accurately characterize long distribution paths, low weight copper, electro-migration violations of current-carrying vias, and swiss-cheese effects.

It is recommended to perform the following analyses:

- Lumped resistance/IR drop analysis
- Distributed resistance/IR drop analysis

The requirements are to perform both analyses and to show compliance. In the next sections, each methodology is described in detail and examples are provided of analyses flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

5.1 Lumped and Distributed Resistance/IR Drop Analysis Methodology

Lumped methodology consists of grouping all of the power/ground pins of the PMIC and the processor device; this is followed by extracting the lumped resistance or dc voltage drop of the equivalent path by applying a voltage source at the PMIC end and a current sink at the device end. The pin-grouping concept is depicted in Figure 14.

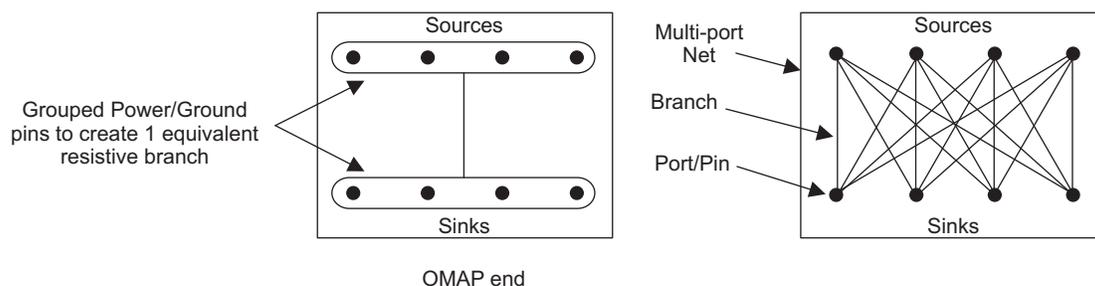


Figure 14. Pin-Grouping Concept: Lumped and Distributed Methodologies

The lumped methodology consists of importing the PCB layout database (from Cadence Allegro or other PCB layout tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness, material properties) of the PCB dielectric and metallization layers. The material properties of dielectric consist of permittivity (Dk) and loss tangent (Df). For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage/current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions/use-modes. After running the simulation, the lumped resistance and lumped IR drop can be examined as shown in [Figure 15](#).

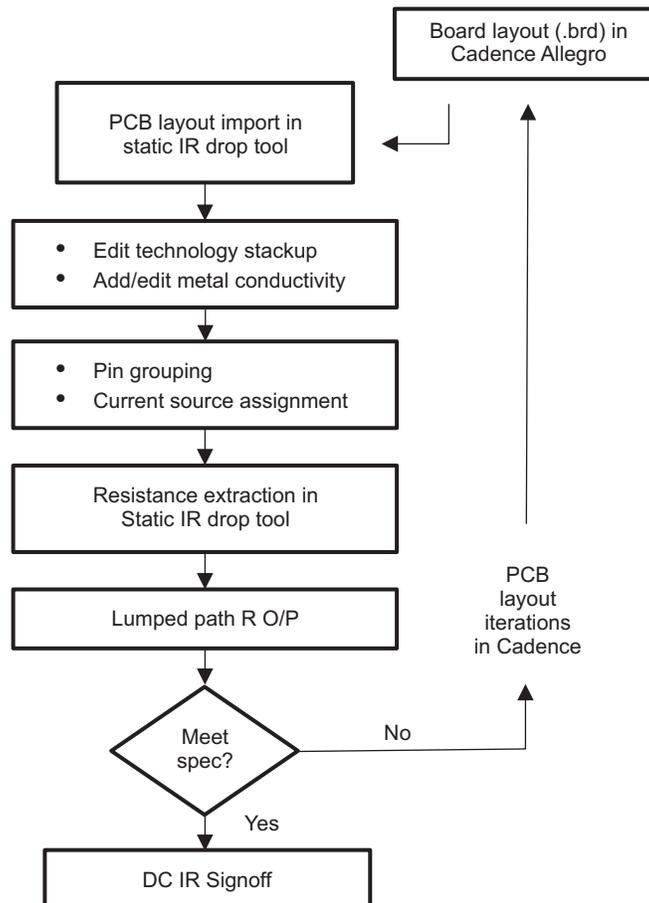


Figure 15. PCB Only Lumped R Extraction Flow

A more accurate analysis is to use average current per-pin assumption and then create a distributed IR drop profile of the PCB. In this analysis, the power and ground pins are left unique instead of lumping them together. If the average-current based analysis is performed, the average per-pin current information is extracted from the device-specification data sheet and the pin count for the specific supply rail. This average current information is then included for analysis as shown in [Figure 16](#).

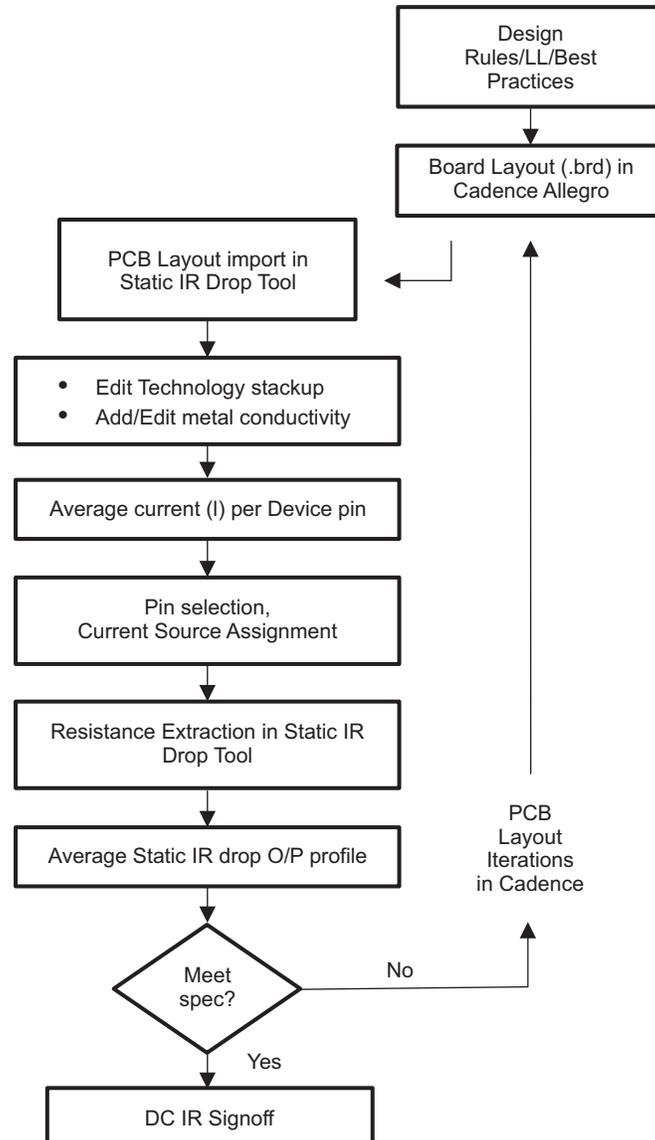


Figure 16. PCB Only Distributed IR Drop Flow

Based on the design guidelines followed by post-layout IR drop analysis, significant improvements in designs can be characterized by the above flow. An example of design improvement has been depicted in [Figure 17](#).

The Static IR drop flow/methodologies in this document have been demonstrated using the TI internal flow. The basic steps can be repeated with other EDA tools. It consists of:

- Translate the post-layout design into the tool
- Define the sources (PMIC/VRM, connectors etc.)
- Define the current sinks for loads, spec it as lumped, distributed based on design requirements
- Ensure that the stack-up, layer thickness, and copper technology properties (thickness, conductivity) is correct
- Set up of appropriate limits for simulation
- Analyses of IR drop simulation data to locate hotspots, neckdowns, electromigration (EM) violations, etc.

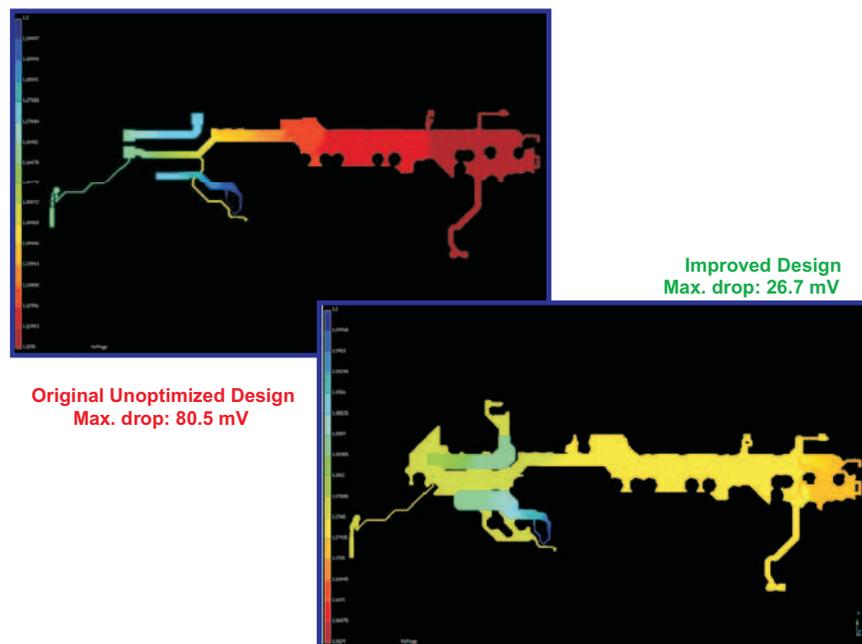


Figure 17. Example Showing IR Drop Improvement Using Distributed IR Drop Flow

6 Step 4: AC Analysis of PCB PDN

The typical elements of the PDN are shown in Figure 18. They include the chip-level power distribution with thin-oxide decoupling capacitors, the package-level power distribution with planes and mid-frequency decoupling capacitors, and the board-level (i.e., PCB) power distribution with planes, low-frequency ceramic and bulk decoupling capacitors, and the PMIC/VRM.

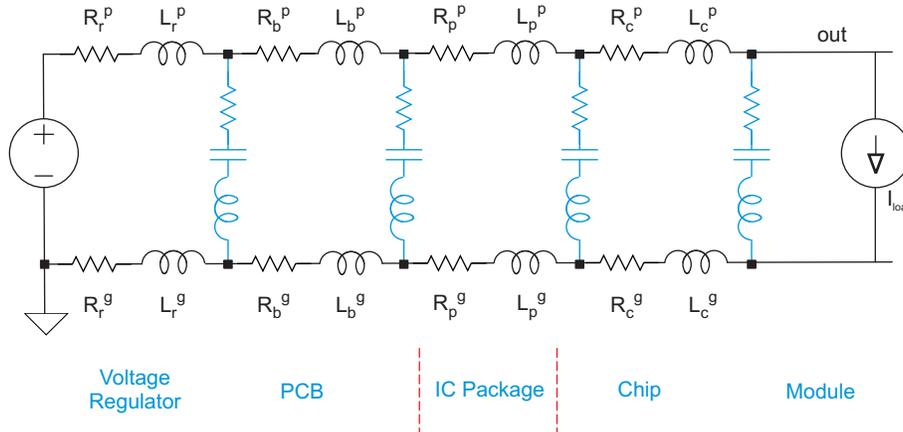


Figure 18. Components of a Typical Power Distribution Network (PDN)

The frequency ranges covered by these elements are shown in Figure 19. The primary focus here is on optimizing the PCB PDN for high performance; the methodology is developed around the areas that the PCB designer has control and can influence early in the design phase.

The typical PCB PDN network contains the following components:

- Power management integrated circuit (PMIC) or voltage regulator module (VRM)
- Bulk and mid-frequency decoupling capacitors
- Parasitics from power/ground plane spreading, BGA vias, and SMT
- Inter-plane capacitance

In the following sections, the purpose of each of the components of the PDN network are reviewed and the requirements for each are stated with examples, whenever appropriate.

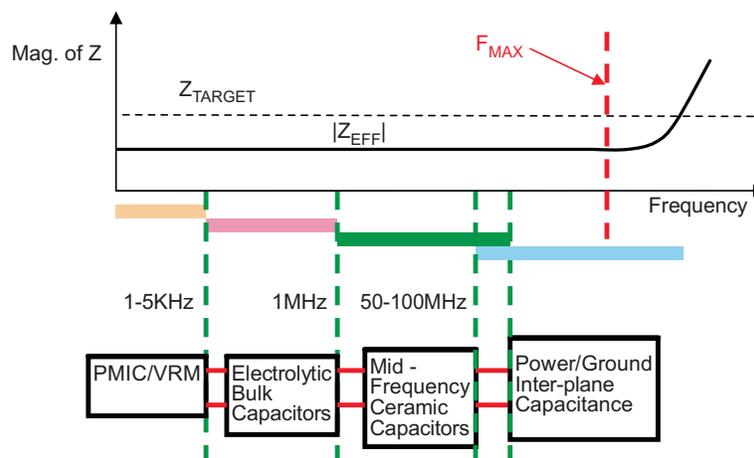


Figure 19. Decoupling Frequency Range of the Components of PCB PDN

The PMIC/VRM or simply voltage regulator device is the first major component of the PDN. It observes its output voltage and adjusts the amount of current being supplied to keep the voltage constant. Most common voltage regulators make this adjustment on the order of milliseconds to microseconds. They are effective at maintaining output voltage for events at all frequencies from dc to a few kilohertz (depending on the regulator dynamic response time). For all transient events that occur at frequencies above this range, there is a time lag before the voltage regulator can respond to the new level of demand. During this time lag the rail suffers from voltage droop. A power delivery network has an impedance (Z_{PDN}) associated with the path from the PMIC/VRM to the applications processor. The magnitude of noise (voltage ripple) seen on a given power rail is proportional to the impedance (Z_{PDN}) and the transient current ($I_{TRANSIENT}$) draw associated with that rail. Figure 20 shows an example of the current transient profile under a switching set-up condition.

Based on Ohm's Law,

$$V_{RIPPLE} = I_{TRANSIENT} * Z_{PDN} \quad (2)$$

Typically the transient current is application specific and is determined by the switching scenario. As a board designer, you have the ability to minimize the voltage ripple by reducing Z_{PDN} either by reducing the inductance or by maximizing the capacitance. To ensure that the voltage ripple noise is within the applications processor specification, the Z_{PDN} must be designed to meet a certain impedance, called the target impedance (Z_{TARGET}). Using the frequency domain target impedance method (FDTIM) to describe the behavior of a power delivery system has been widely accepted.

The key concept of the FDTIM is the determination of the target impedance Z_{TARGET} (see Equation 3) for the power rail under consideration. For reliable operation of a power delivery system, its impedance spectrum needs to be maintained below the target value at the frequencies from dc to F_{MAX} (as shown in Figure 19). F_{MAX} is the point in frequency after which adding a reasonable number of decoupling capacitors does not bring down the power rail impedance $|Z_{EFF}|$ below the target impedance (Z_{TARGET}) due to the dominance of the parasitic planar spreading inductance and package inductances.

$$Z_{TARGET} = \frac{\text{VoltageRail} * \%Ripple}{0.5 * I_{MAX}} \quad (3)$$

For the OMAP3630, AM37xx, and DM37xx devices, the Z_{TARGET} for VDD_MPU_IVA is specified at 96.4 mΩ. This was computed using the Equation 3 and with the following assumptions: the voltage rail (VDD_MPU_IVA) is 1.35 V (max voltage at OPP1G), % ripple allowed is 5% of the maximum voltage, and I_{MAX} is the maximum transient current.

$$Z_{TARGET} = 96.4m\Omega \quad (4)$$

6.1 Selecting Decoupling Capacitors to Meet Z_{TARGET}

To maintain power integrity throughout the entire frequency range of interest, the power distribution network relies on the voltage regulator module (PMIC/VRM), the on-board discrete bulk electrolytic and ceramic decoupling capacitors, and the inter-plane capacitance (capacitance from the power-ground sandwich in the board stack-up).

For a first-order analysis, the PMIC/VRM can be modeled as a series-connected resistor and inductor. The PMIC/VRM, at low frequencies (up to about 1 MHz), has a low output impedance and is capable of responding to the instantaneous requirements of the applications processor. The ESR and ESL values for the PMIC/VRM are very low in the lower frequency range. Beyond lower frequencies, the PMIC/VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement of the device.

The bulk and ceramic discrete decoupling capacitors must provide the required low impedance power source above the frequency where the PMIC/VRM becomes inductive. The effectiveness of the bulk and mid-frequency decoupling capacitors (1 MHz-70 MHz – depending on the capacitors ESL and ESR) is limited by its placement (loop inductance), value, and type.

The bulk capacitors should be located near the entry point of the power supply to the PCB. These decoupling capacitors maintain the PDN impedance at the required value beyond the frequency where the PMIC/VRM becomes inductive and up to the frequency at which mid-frequency capacitors become useful. The mid-frequency SMT capacitors are useful in the 10 to 150 MHz range and higher. These capacitors are primarily ceramic capacitors that come in several dielectric types (NPO, X7R, X5R, and Y5V) and several sizes (1206, 0805, 0603, 0402, etc).

The mid-frequency capacitors are much smaller than the bulk capacitors and therefore can be placed closer to the transistor circuit. Since the ceramic capacitors are smaller, they have lower ESR and ESL and lower capacitance than bulk capacitors, leading to a higher resonance frequency with smaller impedance at resonance. Therefore, ceramic capacitors can be used at higher frequencies. Typical mid-frequency capacitors have capacitance in the range of 1-100nF, ESR in the range of 10-100 mΩ, and ESL in the range of 0.5-1nH.

The concept of *loop inductance* is a useful metric for quantifying the effectiveness of the decoupling capacitors of a power distribution network. Use Equation 5 to calculate the *loop inductance* associated with the decoupling capacitor placement. Once the s-parameter model has been extracted of the power distribution network. Figure 20 shows a typical flow for *loop inductance* extraction.

$$L_{eff} = \frac{\text{imaginary}(Z(\text{power, gnd pads of decap}))}{2 * \pi * \text{frequency}} \tag{5}$$

Where L_{eff} is the effective loop inductance, represents the Z-parameters of the port defined across the power and ground pads of the corresponding decap, the frequency should be chosen in the *flat* region of the z-parameter response, typically in the 50-70 MHz range.

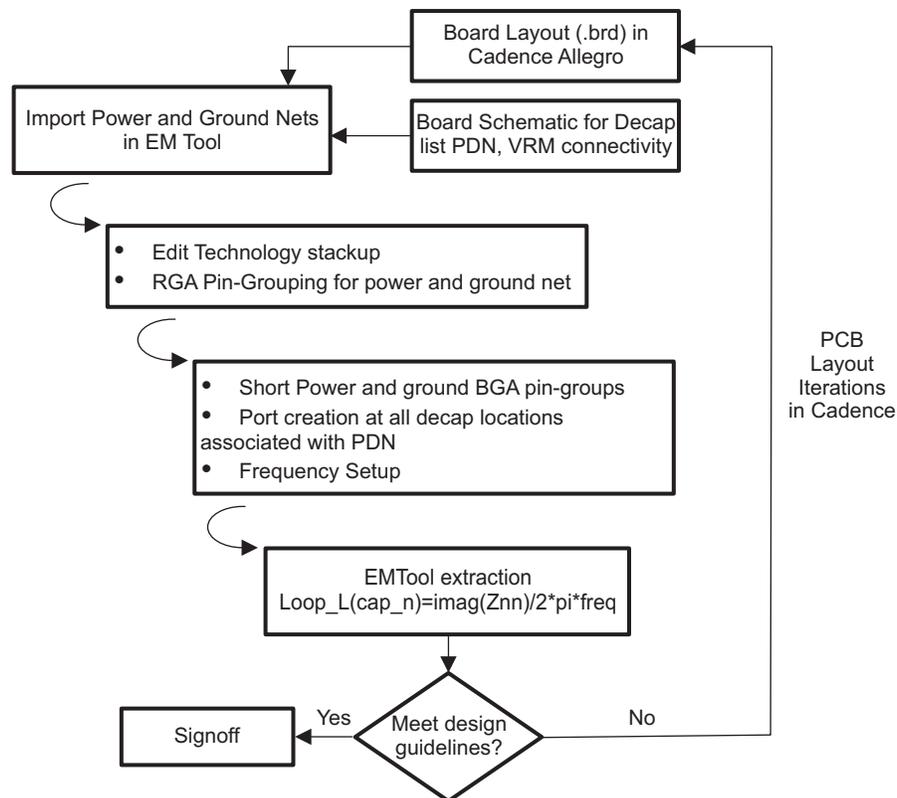


Figure 20. Modeling and Extraction Flow for Extracting Loop Inductance From s-Parameter

6.2 PDN Decoupling Capacitors Requirements

Based on extensive resonance analysis, the decoupling requirements (type, value, and location) and guidelines to properly decouple VDD_MPU_IVA so that the effective impedance remains below Z_{TARGET} within the entire frequency range of interest from DC up to 60-70 MHz are:

- Bulk capacitors: 22 μF[x2] (location as shown in Figure 21)
- If needed (depending on the PCB design performance), 44 μF may be needed for bulk
- Mid-frequency decaps: 100 nF[x8], 47 nF[x2], and 10 nF[x2]
- Total capacitors = 14

| Cap Value | Units | Footprint | Number of Caps | ESR (Ω) | ESL (nH) | Mounting Inductance (nH) | Total Inductance |
|-----------|-------|-----------|----------------|------------------|----------|--------------------------|------------------|
| 22000 | nF | 0603 | 2 | 0.2 | 0.2 | 0.2-0.3 | 0.4-0.5 |
| 100 | nF | 0402 | 8 | 0.2 | 0.2 | 0.2-0.3 | 0.4-0.5 |
| 47 | nF | 0402 | 2 | 0.2 | 0.2 | 0.2-0.3 | 0.4-0.5 |
| 10 | nF | 0402 | 2 | 0.2 | 0.2 | 0.2-0.3 | 0.4-0.5 |
| Total | | | 14 | | | | |

Locations of the decoupling capacitors are very important to reducing loop inductance. Figure 21 shows an example of VDD_MPU_IVA rail with optimal location of decaps that minimize loop inductance.

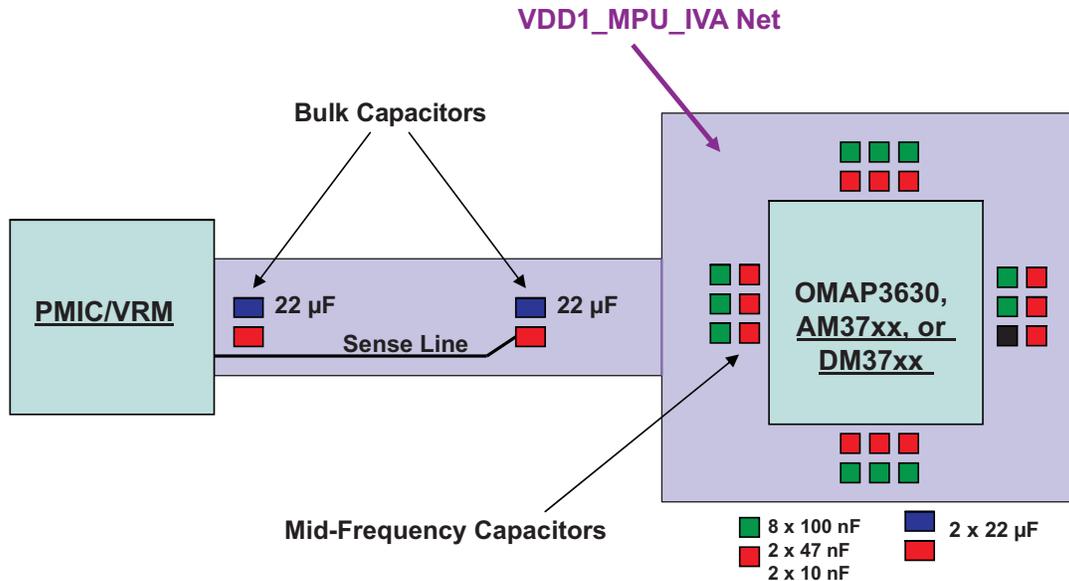


Figure 21. An Example of Decoupling Placement for VDD_MPU_IVA

7 Step 5: Checklist of Requirements/Guidelines/Specifications

• Specifications/Requirements:

- Static IR drop should not exceed more than 30 mV worst case ONLY under optimal sense point location.
- Target impedance should not exceed 96.4 m Ω from dc up to 60-70 MHz on PCB.
- The total loop inductance from any decoupling capacitor to applications processor should be less than 1.5 nH. This includes the capacitor ESL, the via and mounting inductance, and the spreading inductance of the PDN rail.
- Use the decoupling scheme and placement as per Figure 21.

• Stack-up and Layout Recommendations/Guidelines for Optimal PDN Design:

- Placement of the power and ground planes close to the surface where the capacitors are placed is advantageous to reduce the vias inductance. Additionally, use of thinner dielectric between power and ground planes is recommended to increase inter-plane capacitance and reduced via inductance/resistance.
- Use of multiple via pairs for capacitor mounting is helpful to reduce equivalent inductance/resistance.
- Placement of decoupling capacitors as close to the OMAP™ device as possibly is preferred. Use the loop inductance requirements above to guide your placement.
- Use of multiple via pairs for capacitor mounting is helpful to reduce equivalent inductance/resistance.
- Sharing of vias of adjacent capacitors should be avoided.
- Use of short and wide surface traces to connect capacitor pads to the vias connected to the planes below is preferred.

- Opposite current vias should be placed in proximity while same current vias should be distantly placed to account for subtractive versus additive effects of mutual inductance.
- Use of large diameter vias is preferred for reduced inductance/resistance.
- Place the capacitors on the PCB surface (TOP and BOTTOM) closest to their corresponding power and ground planes. This minimizes the via length.
- **Capacitors and Analyses Recommendations:**
 - Perform static IR drop analysis on rail to determine optimal location of sense line. Correct positioning of the PMIC/VRM feedback can cause the PMIC/VRM to increase the voltage to compensate for the IR drop of the PDN. Placing the sense location on the 22 μ F bulk capacitor power pad closest to the applications processor will help offset the IR drop of the rail and is the recommended location.
 - Static IR drop can be reduced by maximizing area and/or length of the net.
 - Maximize the area of the power and ground plane/*island* pair; this helps increase the inter-plane capacitance. The amount of capacitance seen by the power and ground pair sandwich is directly proportional to the relative permittivity of the material (i.e., dielectric constant), the dielectric width, and the length and width of the plane. Use the thinnest dielectric material between the power and ground plane pair.
 - Choose capacitors with small footprint to minimize ESL.
 - When selecting capacitors, choose capacitors with multiple values rather than a large number of capacitors of the same value to meet your target impedance. The impedance peaks in Z-profile are formed by resonance behavior within the power delivery network. High ESR at resonance frequency helps in damping the resonance, thereby reducing the magnitude of the impedance peak. Using a large number of capacitors of the same value significantly reduces the ESR near a self resonant frequency (SRF) and results in a higher magnitude of nearby impedance peaks.

8 Acronyms

Table 1. Acronyms

| | |
|-------|--|
| ac | Alternate current |
| BGA | Ball grid array |
| dc | Direct current (static) |
| Df | Loss tangent |
| Dk | Dielectric constant |
| EDA | Electronic design automation |
| EM | Electromigration |
| ESL | Effective series inductance |
| ESR | Effective series resistance |
| FDTIM | Frequency domain target impedance method |
| HDI | High density interconnect (e.g., buried/blind via) |
| I | Electrical current |
| IR | Product of current (I) x resistance (R) |
| L | Inductance |
| NPO | EIA temperature coefficient for capacitors, ± 30 PPM/°C, -55 to +125°C |
| PCB | Printed circuit board |
| PDN | Power distribution network |
| PMIC | Power management integrated circuit |
| PTH | Plated through hole |
| R | Resistance |
| RLC | Resistance, inductance, and capacitance |
| SMT | Surface mount technology |
| SRF | Self resonant frequency |
| TI | Texas Instruments Incorporated and its subsidiaries |
| V | Electrical potential difference |
| VIP | Via in pad |
| VRM | Voltage regulator module |
| X5R | EIA temperature coefficient for capacitors, $\pm 15\%$, -55 to +85°C |
| X7R | EIA temperature coefficient for capacitors, $\pm 15\%$, -55 to +125°C |
| Y5V | EIA temperature coefficient for capacitors, -82 to +22%, -30 to +85°C |
| Z | Impedance |

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