Technical Article

Layout Matters: Solving Pinout Assignment Issues for DC/DC Converters in WCSP Packages

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The miniaturization trend in consumer electronics has taken hold for good. Consumers are demanding smaller electronics with better features: more flash capacity in solid-state drives, faster smartphones, more integrated communication modules, etc. To achieve this, engineers must look for increasingly power dense solutions. One challenge associated with achieving a high-power-density solution is finding small DC/DC converters with compact external components. When it comes to size, DC/DC converters in wafer chip-scale packages (WCSPs) are smaller than standard quad flat no-lead (QFN) or small-outline transistor (SOT) packages. WCSPs have also lower height than QFN or SOT packages, which can help engineers design not only smaller equipment but also one with a lower profile.

The Trouble with Logic Signal Pins

Although DC/DC converters in WCSP have the size advantage, the pinout assignment of a typical WCSP might prevent engineers from choosing this package. Often, some logic signal pins (like the EN pin or the SDA and SCL pins of the I^2C interface) sit in the middle of the package because other pins with higher priorities in silicon layout (like VIN, AVIN, AGND, PGND and the output sense pins) must connect to the signal traces directly. Because external components should be placed as close to these pins as possible, engineers have to insert small vias for the pins in the middle of the package to achieve proper signal routing during printed circuit board (PCB) layout.

In order to fit in more features (which equals more pins) in one device, engineers increasingly opt for a smaller WCSP pin pitch. While the 0.5-mm or 0.4-mm pitch was used in old devices, nowadays the 0.35-mm pitch is being adopted by many new devices in the market. Once the WCSP pin pitch is 0.35 mm, traditional PCB manufacturing prevents engineers from placing vias in the middle of the package. To address this issue, engineers have to either do away with vias altogether or use an advanced PCB assembly technology, which raises the cost of the overall solution. As a result, engineers have to choose between a larger solution size or a less competitive product.

To address this problem, engineers should consider the pinout assignment when choosing the right buck converters in WSPC for their solutions. TI's TPS62866 is a 6-A synchronous step-down converter which measures only 1.05x1.75x0.5-mm in WCSP. For the same current level buck converters in QFN, the typical package size is 3x3x1-mm. Figure 1 shows the pinout assignment and typical PCB layout of the TPS62866.

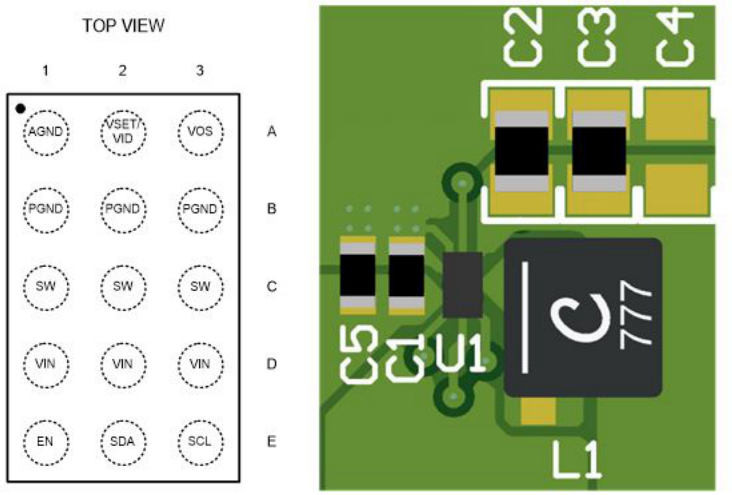

Figure 1. Pinout of the TPS62866 With a Typical PCB Layout

The absence of logic pins in the middle of the integrated circuit means that engineers don't need special vias for PCB routing, even though the pin pitch is 0.35 mm. Such assignment makes it also possible to place all signal traces around the device for direct routing, further saving board space and allowing engineers to shrink the overall power supply solution, leaving more room for the features that consumers crave.

A reasonable pinout assignment is an important feature for DC/DC converters in WCSP packages. The TPS62866 provides a good pinout assignment and implements many features including I^2C interface in a 1.05x1.75x0.5-mm, 0.35-mm pitch WCSP.

Additional Resources

- Read this application note to learn more about the die size BGA (DSBGA) wafer level chip scale package (WLCSP).
- Explore different methods of output-voltage adjustment for DC/DC converters.

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