Technical Article Interlocking Gate Drivers for Improving the Robustness of Three-phase Inverters

TEXAS INSTRUMENTS

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Variable frequency drives (VFDs) are a key part of industrial automation machinery. They help drive pumps, fans, conveyor belts, computer numeric control machines and robotic automation solutions efficiently, helping reduce a factory's total energy consumption. Downtime in a VFD directly translates to machinery downtime, which can lead to factory shutdown and a loss of production. VFD reliability and robustness are key requirements for machine builders and factory owners.

The three-phase inverter structure shown in Figure 1 is the heart of a VFD, converting the rectified mains voltage into a variable frequency and a variable voltage output to the motor. Inverter robustness is a key contributor to the robustness of a VFD.

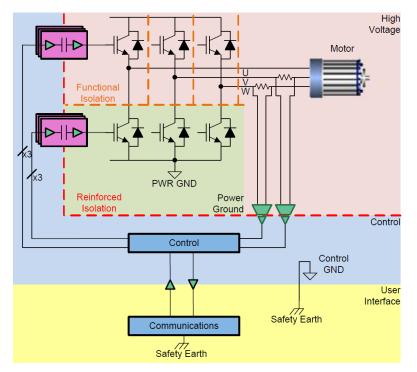


Figure 1. Three-phase Inverter with Isolated Gate Drivers

The key components of a three-phase inverter are the insulated gate bipolar transistor (IGBT) power switches (typically integrated inside a single IGBT module) and the isolated gate drivers that control the IGBT gates. The microcontroller (MCU) generates high- and low-side pulse-width modulation (PWM) signals that are complementary to each other, with a dead-time period inserted during PWM signal transitions. This dead-time period ensures that both the top and bottom IGBT gate signals are not high at the same time.

MCU hardware failures or motor-control software faults can cause both the high- and low-side PWM signals from the MCU to latch high. The result is cross-conduction through the top and bottom IGBTs, leading to a short of the DC bus. Inserting a current sensor into the DC bus can detect overcurrent conditions and disable the gate drivers through the enable/disable pin of the gate driver or the buffer driving the PWM signals to the gate drivers. The delay between sensing overcurrent and shutdown is typically a few microseconds. Repeating this sensing



sequence multiple times could decrease the reliability and lifetime of IGBT switches, however, which is the most expensive semiconductor component inside a VFD.

But what if both gate drivers never responded to spurious PWM sequences? This is possible to implement – without additional external hardware – by using a method called interlocking.

Interlocking High- and Low-side Gate Drivers

In this configuration shown in Figure 2, the anode of the high-side driver's emulated diode is tied to the cathode of the low-side driver's emulated diode. The cathode of the high-side driver's emulated diode is tied to the anode of the low-side driver's emulated diode.

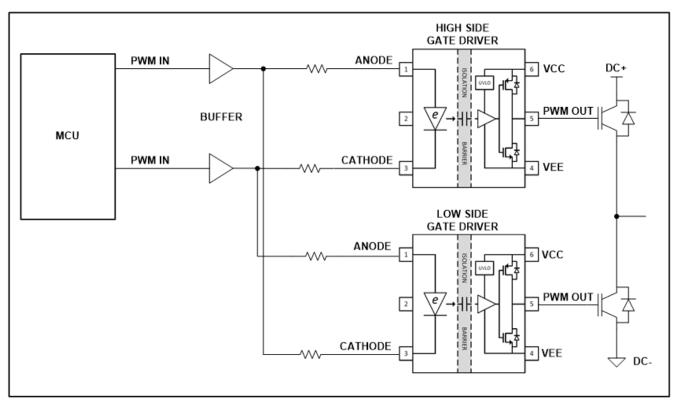


Figure 2. Interlocking Circuit Configuration

TI tested an implementation of the interlocking circuit configuration in the "Three-phase inverter reference design for 200-480 V_{AC} drives with opto-emulated input gate drivers."

Three-phase inverter reference design for 200-480 VAC drivesImage: Download the design today

As shown in Figure 3, during normal operation, the PWM pulses are complementary, either forward-biasing the input emulated diode of the UCC23513 or reverse-biasing the isolated gate driver with a buffer drive voltage of -5 V. The high reverse-voltage-handling capability of the UCC23513's emulated diode enables the handling of reverse voltages that occur in the interlocking configuration. Competing current-controlled capacitive isolated gate drivers do not have high reverse-voltage-handling capability and cannot be interlocked. During the dead-time period, the voltage across the emulated diodes is 0 V.



Figure 3. Normal PWM Operation with Interlocking

Purposefully inserting a negative dead time enables you to check the response of the interlocking circuit to faulty PWM signals from the MCU. In Figure 4, you can see that if both MCU outputs are high, then the outputs of the gate driver are low. Whatever the input PWM signals, the outputs of the high- and low-side gate drivers are never going to be high simultaneously, thus preventing cross-conduction.

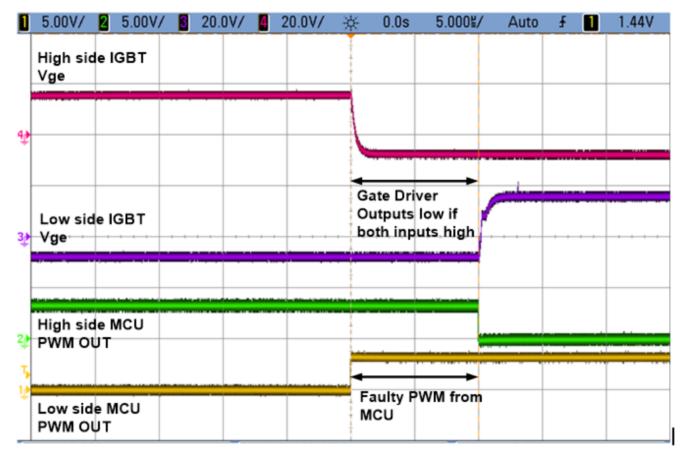


Figure 4. Interlocking Circuit Response to Faulty PWM Input Signals from the MCU



Table 1. Interlocking Operation

MCU PWM output		Output of gate drivers	
High-side PWM	Low-side PWM	High-side PWM	Low-side PWM
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

You could interlock legacy opto-isolated gate drivers, but they do not provide additional benefits like higher working isolation voltages; higher common-mode transient immunity; operation at junction temperatures up to 150°C; and improved switching parameters like lower propagation delay and lower pulse-width distortion.

With the UCC23513 available in an industry-standard six-pin small-outline package, you can easily upgrade the inverter in existing VFDs with a simple swap, without any additional schematic or printed circuit board design changes.

Additional Resources

- Explore TI's motor drive systems portfolio.
- Read more about isolation in AC motor drives in the white paper, "Isolation in AC Motor Drives: Understanding the IEC 61800-5-1 Safety Standard."
- Learn how to solve key isolation challenges in AC motor drive designs in the white paper, "How Capacitive Isolation Solves Key Challenges in AC Motor Drives."
- Check out the TI training, "How High-Voltage Isolation Technology Works."
- Read the e-book: C2000 MCU DesignDRIVE solutions for industrial motor drives

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