Technical Article **Two Ways to Save Power with Low-power Ethernet**



Garrett Yamasaki

"Why is Ethernet so power-hungry?" is a common question. A typical active power 10/100 Mbps Ethernet physical layer (PHY) transceiver consumes 110mW to over 300mW, while a 10/100/1000Mbps Gigabit Ethernet PHY consumes 450mW to over 1,000mW of power. It's not uncommon for an Ethernet PHY to be one of the single largest consumers of power on a board, and to be a significant factor when evaluating the heat budget of an enclosed system. There are various low-power modes conceptualized for Ethernet that reduce overall system power. In this post, I'll discuss two popular power-saving features that enable cooler systems and lower power costs.

Energy-efficient Ethernet

Energy-efficient Ethernet (EEE), as defined in Institute of Electrical and Electronics Engineers (IEEE) 802.3az, is a PHY and media access control (MAC) standard that eliminates idle signaling during times of low channel utilization. As Figure 1 shows, EEE enables periods of low power where the transmitter is disabled during "quiet" times, broken by short refresh periods. These quiet times save power by eliminating the wasteful practice of continuously transmitting idle symbols across an active link, while the refresh periods ensure that the link presence and timing inside of and between the PHYs remains in a valid state.





EEE mode appears transparent to higher layers, as the MAC signals for the PHY exit the EEE state when data is present to transmit. The PHY will exit low-power mode and transmit idle code groups to bring the far-end device out of low power.

For more detailed information about EEE, see the application note, "DP83822 Energy Efficient Ethernet IEEE 802.3az."

1



Wake-on-lan

Wake-on-LAN (WoL) keeps the Ethernet PHY in an active state, but saves power by enabling the system's back-end components (processor, microcontroller (MCU), application-specific integrated circuit (ASIC) or other components) to power down selectively. These back-end components wake up when the Ethernet PHY receives a known "magic" packet.

The WoL scheme enables engineers to save on overall system power while keeping the Ethernet transceiver awake when the system has well-defined stimuli that should trigger wake ups. There are a few different ways to implement WoL, discussed in the application note, "DP83822 Wake-On-LAN."

Figure 2 shows a magic pattern scheme for which the Ethernet PHY will monitor ingress packets before signaling a wake up.



Figure 2. WoL Magic Packet Example

Now that you know of two different ways to save power using the Ethernet PHY, which scheme do you plan to implement within your system? Log in to leave a comment, or join the TI E2E[™] Community Ethernet forum.

Additional Resources

- Learn more about two of the industry's lowest-power 10/100 Ethernet PHYs, the DP83822I and the DP83825I.
- Check out the DP83867IR Gigabit Ethernet PHY.
- View TI's entire Ethernet portfolio.
- Read the application note, "DP83822 Low Power Modes."
- Start your design with EMI/EMC Compliant 10/100 Mbps Ethernet Brick with Fiber or Twisted Pair Interface Reference Design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2023, Texas Instruments Incorporated