Technical Article

Timing Is Everything: Design JESD204B Clocking Using System Reference Modes

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Hello and welcome back to the "Timing is Everything" blog series. In a previous post, Timothy T. talked about the clocking requirements of the JESD204B interface standard that is gaining popularity for its ability to simplify design in high-speed data acquisition systems. In this post, I'm going to talk about the different system reference signal (SYSREF) modes of jitter synthesizers and cleaners, as well as how to use them to maximize the performance of your JESD204B clocking scheme.

The LMK04821 family of devices provide a good case study for this topic because they are high-performance, dual-loop jitter cleaners that can drive up to seven JESD204B converters or logic devices in a subclass-1 clocking scheme with device and SYSREF clocks. Figure 1 is a high level block diagram of a typical JESD204B system with the LMK04821 family devices as clocking solution.

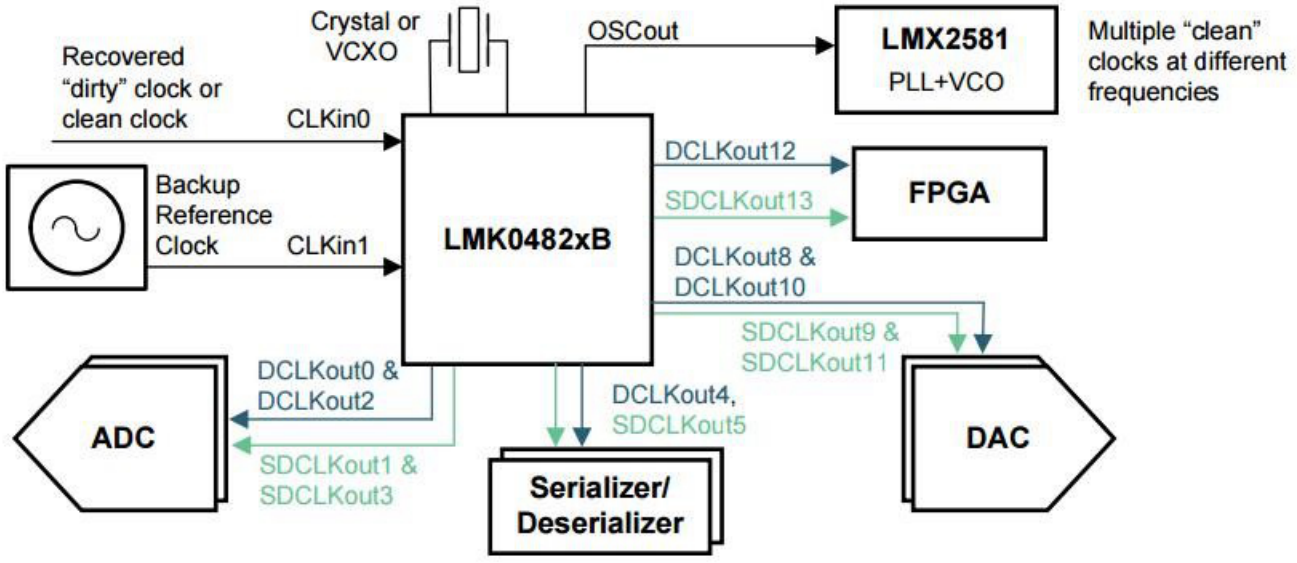

Figure 1. Typical JEDEC JESD204B Application Block Diagram

The LMK04821 generates SYSREF signals with a single SYSREF clock divider from the voltage-controlled oscillator of the second phase-locked loop (PLL) . From the divider, the signal gets distributed to the individual output paths. Each output path contains digital and analog delays to adjust the SYSREF phase in relation to the device clock.

From the JESD204B standard, SYSREF can be in different modes, as shown in Figure 2. It can be a continuous (also known as periodic), gapped periodic or one-shot signal. The continuous and gapped-periodic SYSREF periods must be in an integer multiple of the local multiframe clock (LMFC) in order to avoid SYSREF pulses in the middle of a multiframe.

Continuous mode allows for continuous output. Many developers don't use continuous mode due to crosstalk from SYSREF to the device clock. However, continuous mode enables the system developers to manually set up the correct deterministic-phase relationship between both signals. After the setup it can be changed to gapped-periodic SYSREF.

In gapped-periodic or one-shot modes, the output of the SYSREF clock divider is fed through a pulser to the output paths. The pulser gates the SYSREF signal and lets only a few pulses through. The pulse count can be set to one, two, four or eight pulses. Since there isn't a periodic signal, the crosstalk from SYSREF to the device clock is minimized.

Another type of gapped-periodic SYSREF mode in the LMK0482x is the request mode, which outputs a continuous stream of SYSREF pulses as long as the SYNC/SYSREF_REQ pin is high.

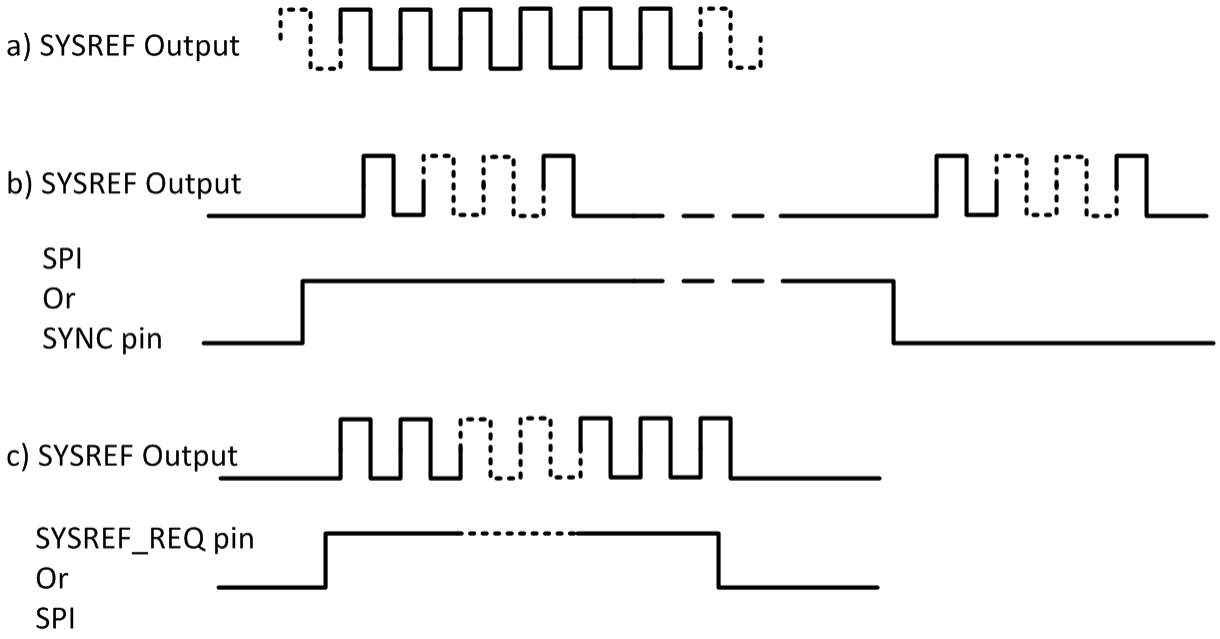

Figure 2. The SYSREF Modes of the LMK0482x Are a) Continuous SYSREF, B) Pulsed SYSREF (One-shot or Gapped Periodic), C) and SYSREF Request (Gapped Periodic)

In LMK04821 devices, the internal SYSREF distribution path is shared with the output-divider synchronization path. Therefore, it needs a specific register write sequence to enable synchronized outputs and glitch-free SYSREF pulse generation. In Figure 3, the methods I've described are listed with their register write sequences. Figure 3 also shows the internal-register field names with content as a decimal value. Steps with the same number are interchangeable.

Step	CONTINUOUS SYSREF		PULSED SYSREF		SYSREF REQUEST		Comments
	(periodic SYSREF)		(one-shot or gapped periodic)		(gapped periodic)		
	Pre-work						
1	SYNC_POL	0	SYNC_POL	0	SYSREF REQUEST	0	
1	SYNC_MODE	1	SYNC_MODE	1	SYNC_MODE	1	
1	SYSREF_MUX	0	SYSREF_MUX	0	SYSREF_MUX	0	
1	SYSREF_DIV	384	SYSREF_DIV	384	SYSREF_DIV	384	Divider determines the SYSREF frequency.
1	Other dividers should be set here. If they change later, another SYNC needs to occur to synchronize them.						
1	SYNC_EN	1	SYNC_EN	1	SYNC_EN	1	
	Preparing SYSREF						
2	SYSREF_PD	0	SYSREF_PD	0	SYSREF_PD	0	
2	SYSREF_DDLY_PD	0	SYSREF_DDLY_PD	0	SYSREF_DDLY_PD	0	
2	DCLKoutX_DDLY_PD	0	DCLKoutX_DDLY_PD	0	DCLKoutX_DDLY_PD	0	Clear this bit for the used DCLKout.
2	SYSREF_PLSR_PD	1	SYSREF_PLSR_PD	0	SYSREF_PLSR_PD	0	
2	SYSREF_PULSE_CNT	x	SYSREF_PULSE_CNT	1	SYSREF_PULSE_CNT	x	Sets the pulse count, e.g.: 1=2pulses. Not needed in continuous or SYSREF request mode.
	Power up SYSREF outputs						
3	SDCLKoutY_PD	0	SDCLKoutY_PD	0	SDCLKoutY_PD	0	Clear this bit for the used SYSREF output.
4	SYSREF_CLR	1	SYSREF_CLR	1	SYSREF_CLR	1	SYSREF_CLR needs to be 1 for 15 VCO cycles.
5	SYSREF_CLR	0	SYSREF_CLR	0	SYSREF_CLR	0	
	Establish deterministic phase relationship between SYSREF and device clock						
6	DCLKoutX_DDLY_CNT	5	DCLKoutX_DDLY_CNT	5	DCLKoutX_DDLY_CNT	5	Sets the digital delay in device clock path.
6	DCLKoutX_DDLY_CNT	5	DCLKoutX_DDLY_CNT	5	DCLKoutX_DDLY_CNT	5	
6	DCLKoutX_HS	0	DCLKoutX_HS	0	DCLKoutX_HS	0	Optional half step.
6	SDCLKoutY_DDLY	2	SDCLKoutY_DDLY	2	SDCLKoutY_DDLY	2	Sets the digital delay in SYSREF path.
6	SDCLKoutY_HS	0	SDCLKoutY_HS	0	SDCLKoutY_HS	0	Optional half step.
6	SYSREF_DDLY	8	SYSREF_DDLY	8	SYSREF_DDLY	8	Sets global digtal delay in SYSREF path.
6	SYNC_DISX	0	SYNC_DISX	0	SYNC_DISX	0	Enables synchronization path to device clock dividers and SYSREF divider.
6	SYNC_DISSYSREF	0	SYNC_DISSYSREF	0	SYNC_DISSYSREF	0	
7	SYNC_POL	1	SYNC_POL	1	SYNC_POL	1	Toggling SYNC_POL or SYNC pin synchronize the dividers.
8	SYNC_POL	0	SYNC_POL	0	SYNC_POL	0	
9	SYNC_DISX	1	SYNC_DISX	1	SYNC_DISX	1	Disables synchronization path at the device clock dividers and SYSREF divider.
9	SYNC_DISSYSREF	1	SYNC_DISSYSREF	1	SYNC_DISSYSREF	1	
	Setting the right SYSREF Mode						
10	SYNC_MODE	x	SYNC_MODE	2	SYNC_MODE	0	
10	SYSREF_MUX	3	SYSREF_MUX	2	SYSREF_MUX	2	Setting of the right SYSREF mode.
10	SYSREF_REQ_EN	0	SYSREF_REQ_EN	0	SYSREF_REQ_EN	1	

Figure 3. Register Write Sequences to Enable Different SYSREF Modes

The JESD204B standard is reducing the layout efforts while introducing serialized data transmission between signal converters and logic devices. By taking full advantage of the SYSREF modes of your JESD204B-enabled clock device, you can easily create deterministic phase relationships in the whole system.

Are there other clock design challenges you'd like us to cover regarding JESD204B designs or others? Let me know by logging in to post a comment below.

Additional Resources

- Read the blog series about JESD204B subclasses.
- Read this blog post about JESD204B subclass-1 clocking timing requirements.
- Read this Analog Applications Journal article, "When is the JESD204B interface the right choice?"
- Get useful design tips on various clock and timing design challenges from the "Timing is Everything" blog series.

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