TI Designs
1-W Small Form Factor Power Supply with Isolated Dual Output for PLC I/O Modules

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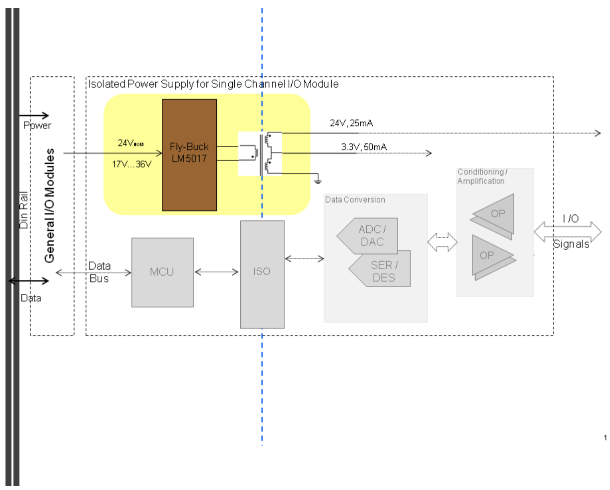
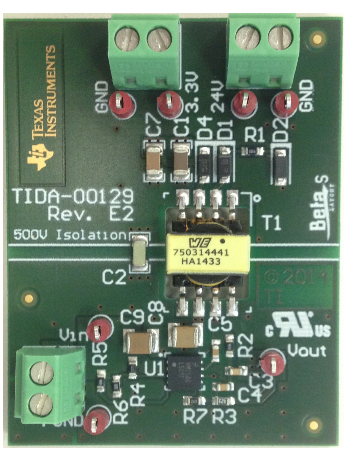
Design Resources

TIDA-00129	Design Files
LM5017	Product Folder
LM5017EVM	EVM Tool Folder





Design Features

- Wide input voltage range: 17 to 36 V (24 V_{NOM})
- Isolated dual output:
  - 24 V_{ISO} with 2 to 25 mA (up to 600 mW)
  - 3.3 V_{ISO} with 35 to 50 mA (up to 165 mW)
- ±10% output voltage accuracy
- IEC 61010-1 compliant (test voltage 860 V_{AC})

Benefits

- Small form factor for space constraint I/O cards: 51 x 40 x 5.97 mm (L x W x H)
- Primary-side regulation, no need for optocoupler, increases lifetime reliability
- Cost effective, lower BOM

Featured Applications

- Programmable logic controllers I/O modules isolated power supply
- 24-V and 3.3-V isolated system and board level
- Isolated power supply for 4 to 20 mA current loop

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1 System Description

1.1 Introduction

A programmable logic controller is a key element for factory automation. The controller monitors and controls machineries in real time to ensure the best process thanks to a flexible number of input/output modules. Each input module is locally responsible for the acquisition and the conversion of data while each output module changes the process with commands sent to actuators. In both cases, the signals exchanged between the modules and the actuators can be either analog or digital, depending on the process level signal needed by the end equipment.

As an illustration of I/O modules, the board reference developed by TI exhibits a digital and an analog input module (see Figure 1 and Figure 2, respectively).

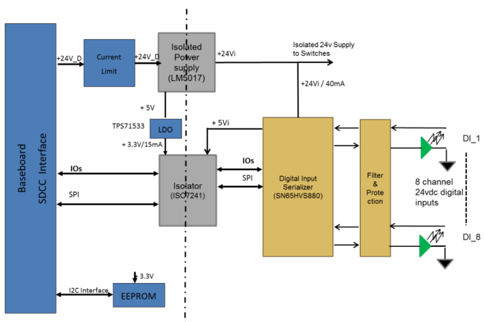


Figure 1. TIDA-00017 Digital Input Module

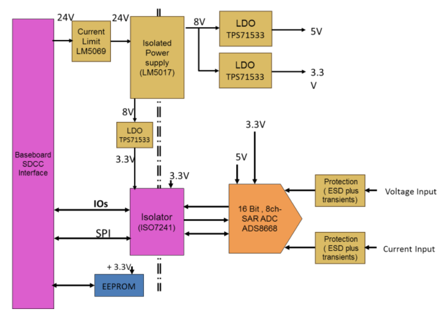


Figure 2. TIDA-00119 Analog Input Module

1.2 Power Supply for PLC I/O Modules Overview

The I/O modules shown in Figure 1 and Figure 2 require data conversion as well as signal conditioning. Depending on the nature of the I/O module (analog or digital), either a digital-to-analog converter (DAC) or a serializer is needed. Locally, most sensors use a 4 to 20-mA loop to acquire and transmit the values measured without noise or line length concerns. One way to implement such a solution is to drive a MOSFET with a standardized 24-V isolated rail to avoid any current return conflicts due to other equipment interconnection.

A single-channel I/O module such as the one shown in Figure 3 is a flexible solution for many needs of the PLC I/O modules. For this reason, this reference design focuses on a modular approach, and more specifically, on the power block.

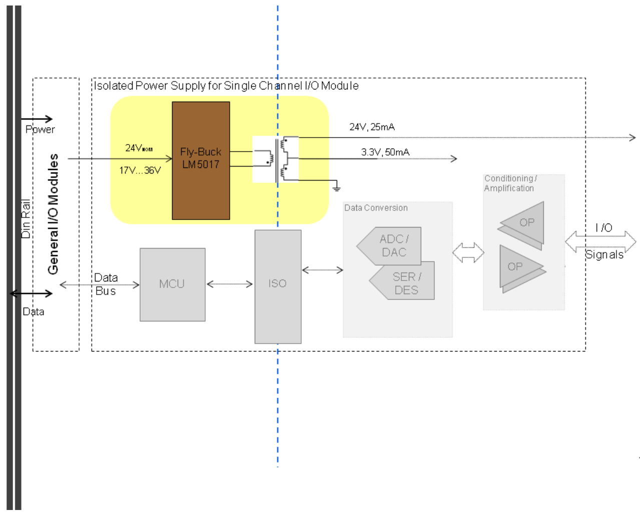


Figure 3. TIDA-00129 Power for Single-Channel Module Block Diagram

This reference design focuses on a versatile isolated dual-output power supply. For signals from sensors, a voltage level of 24 V and a current up to 25 mA are usually defined. For low-power components, 3.3 V and 50 mA are specified.

2 Design Specifications

The TIDA-00129 reference design has the following specifications:

Electrical Specifications:

- V_{IN} = 17 to 36 V_{DC}
- V_{OUT1} = 24 V ±10% at 2 to 25 mA
- V_{OUT2} = 3.3 V ±10% at 35 to 50 mA
- P_{OUT} is approxmimately 1 W
- 85% efficiency at high load

Physical Specifications:

- Total solution height: < 6 mm
- IEC 61010-1 compliant (Test Voltage: 860 V_{AC})

3 Schematic

Figure 4 introduces the TIDA-00129 schematic. A more detailed schematic can be found on the TI website under the TIDA-00129 folder.

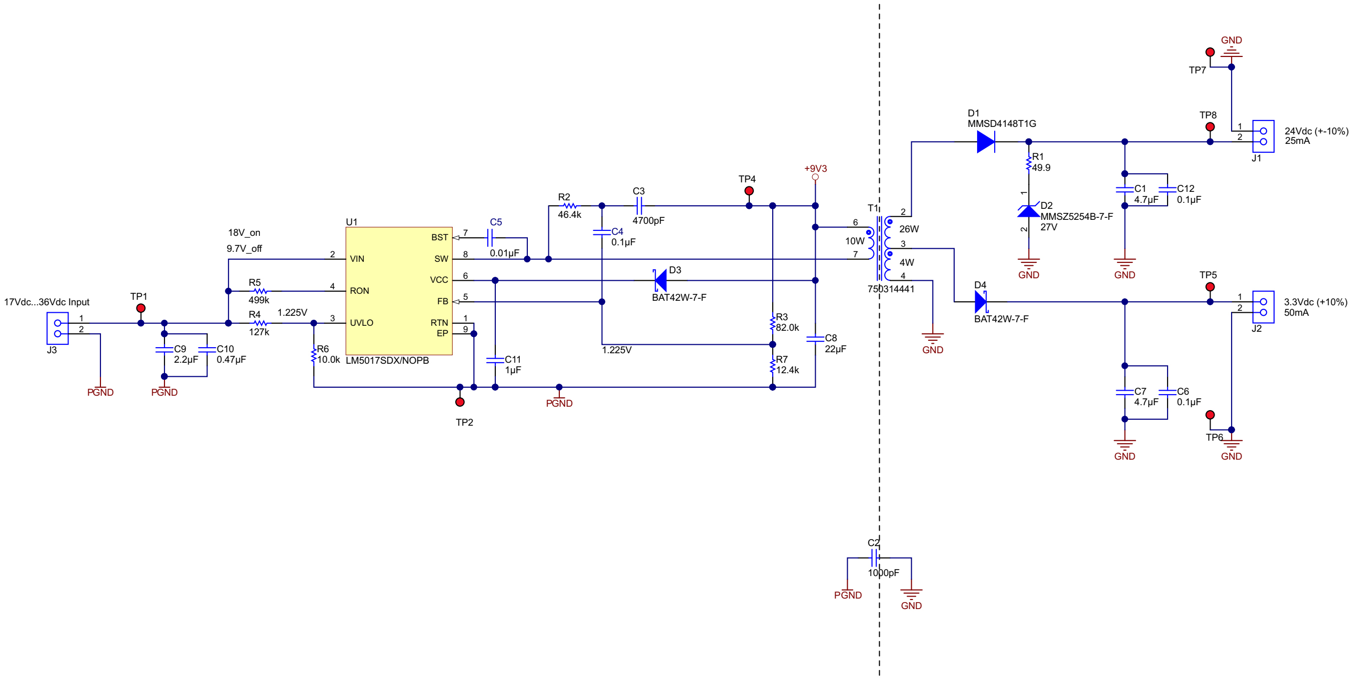


Figure 4. TIDA-00129 Schematic

4 Theory of Operation

Considering the operating power range required, a Fly-Buck™ converter is the best trade-off for the number of components and the need for isolation. This topology also allows design flexibility for a primary nonisolated power supply. The LM5017 and LM5018 devices fulfill these requirements and permit both space reduction and a low cost for the BOM.

Figure 5 shows a simplified design overview of the power supply module. Figure 6 shows the inner architecture of the LM5017 device.

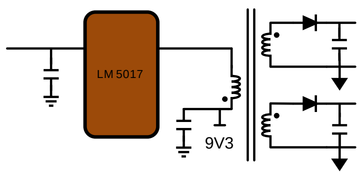


Figure 5. TIDA-00129 Simplified Diagram

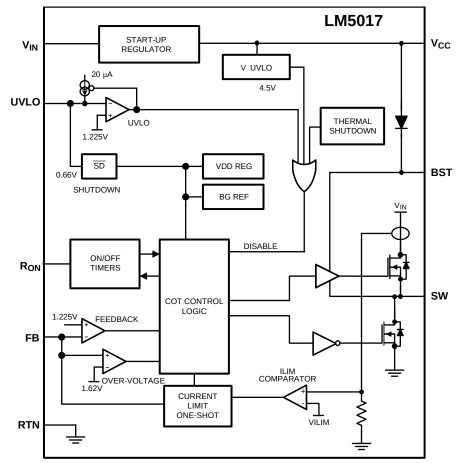


Figure 6. LM5017 Functional Block Diagram

4.1 Primary Side Output Voltage

The output voltage is set with two feedback resistors. To optimize the overall efficiency, V_{OUT} is set higher than the 7.6-V threshold of the internal regulator. Because the output voltage at the primary is not used in the system solution, this voltage is used to power the device, which disables the internal LDO.

$$V_{OUT} = V_{FB}\left(\frac{R_{FB2}}{R_{FB1}} + 1\right) \quad (1)$$

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{V_{FB}} - 1 \quad (2)$$

$$\frac{R_{FB2}}{R_{FB1}} = \frac{9.3}{1.225} - 1 = 6.6 \quad (3)$$

$$R_{FB2} = 82\ k\Omega \text{ and } R_{FB1} = 12.4\ k\Omega \quad (4)$$

4.2 Operating Switching Frequency

Because one of the design priorities is to optimize efficiency, the design keeps the switching frequency as low as possible to minimize switching losses. R_{ON} sets the nominal switching frequency based on Equation 5 through Equation 7.

$$f_{SW} = \frac{V_{OUT}}{K \cdot R_{ON}} \quad (5)$$

$$R_{ON} = \frac{V_{OUT}}{K \cdot f_{SW}} \quad (6)$$

$$R_{ON} = \frac{9.85}{10^{-10} \cdot 200\,k} = 492\,k \quad (7)$$

The design uses a standard 499-kΩ resistor value to ensure a low switching frequency.

4.3 Transformer Selection

To ensure a low-profile solution and a small overall height, carefully choose the geometry and value of the transformer. For the Fly-Buck topology, the transformer choice is not as clear as the choice for a standard forward converter. Part of the complexity comes from the difficulty in estimating the reflected current on the primary side. It is also important to get to a fair trade-off between switching losses and conducted losses. The trade-off especially applies for highly efficient designs, while also considering circulating current.

To reach a close approximation of the geometry and value of the transformer (while simplifying the design), only the highest consuming output is modeled (24 V at 25 mA) in Section 4.3.1.

4.3.1 TINA-TI Spice Simulation

The model shown in Figure 7 allows the following variation:

- V_{IN}: from 17 to 36 V
- L_prim: from 30 µH to 100 µH
- L_leak: from 20 nH to 7 µH

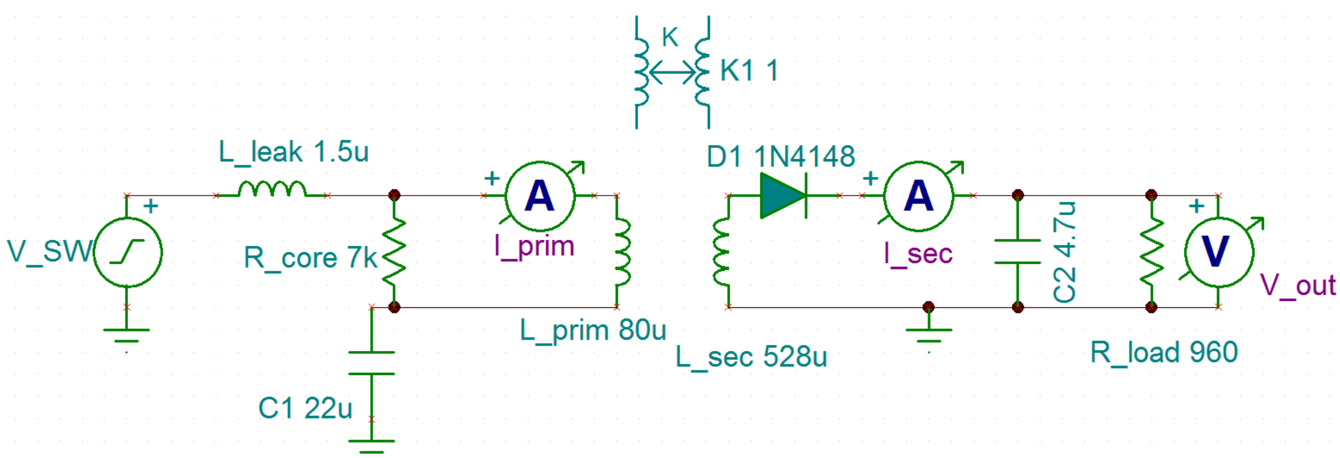


Figure 7. Simplified TINA-TI Schematic of TIDA-00129

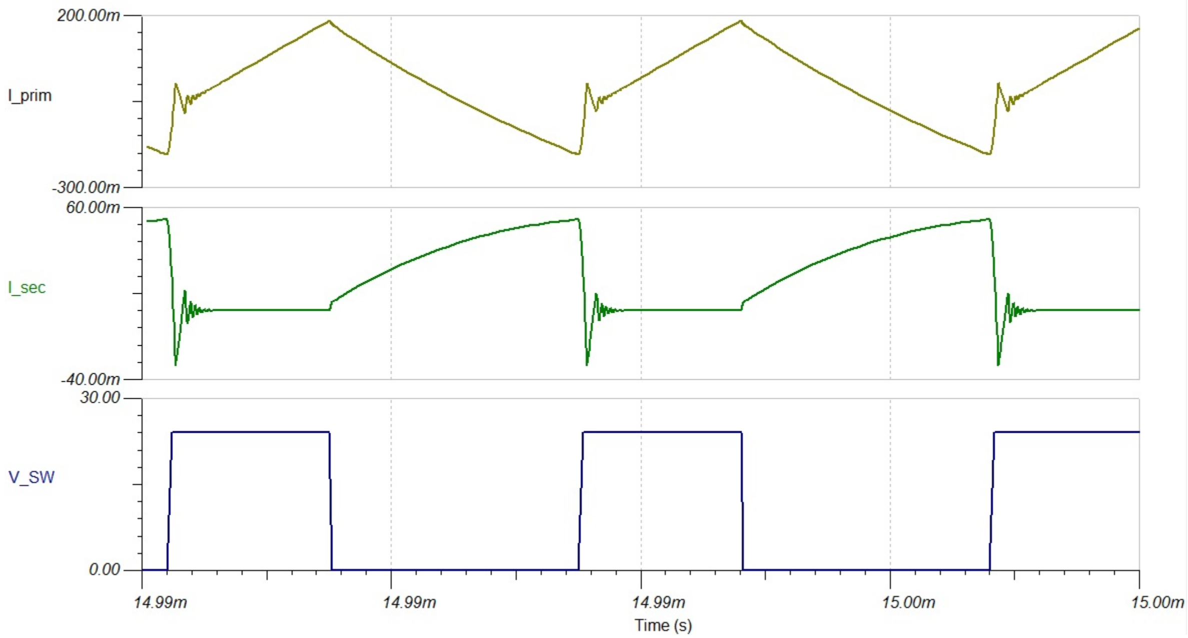


Figure 8. V_{IN} = 24 V, L_prim = 80 µH and L_leak = 7 µH

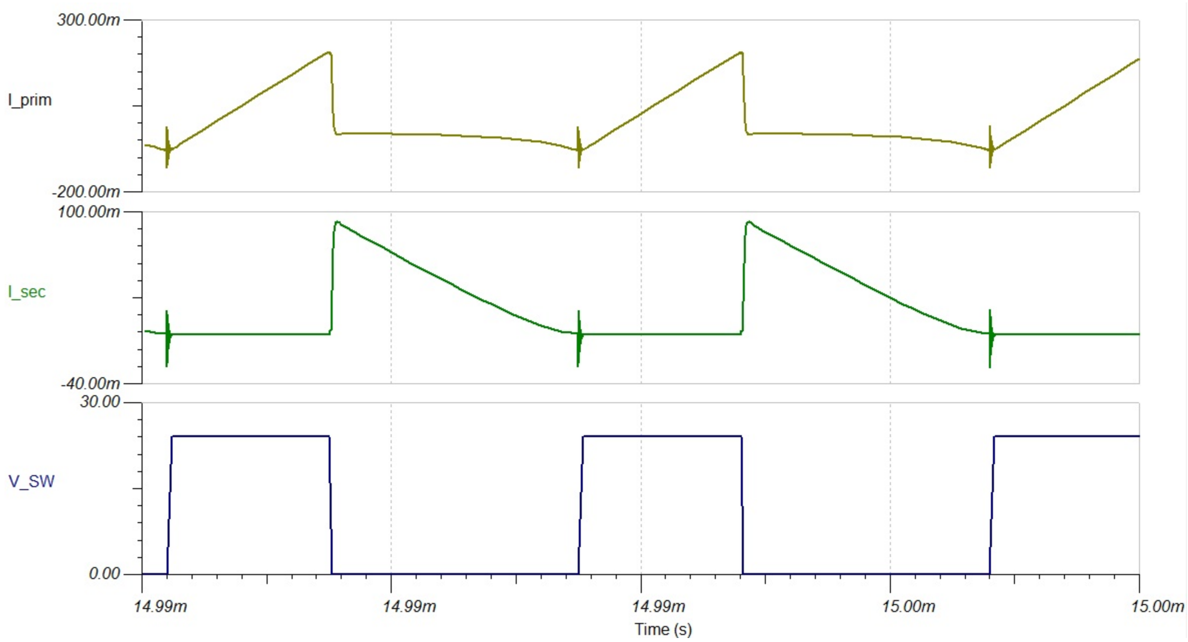


Figure 9. V_{IN} = 24 V, L_prim = 80 µH and L_leak = 20 nH

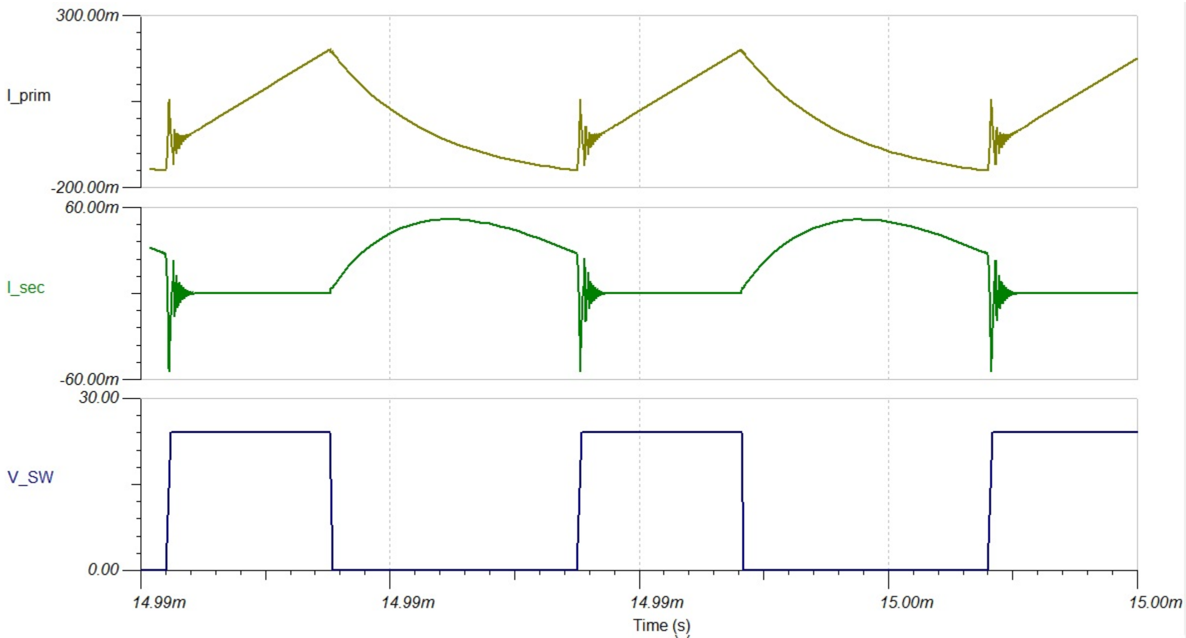


Figure 10. V_{IN} = 24 V, L_prim = 80 µH and L_leak = 1.5 µH

Figure 8, Figure 9, and Figure 10 show the importance of the leakage inductance to optimize the current flow at the primary side at the switching point.

A more detailed approach can be simulated including parasitic capacitances and MOSFET. However, the simulation shown in Section 4.3.1 already gives good transformer specifications.

To optimize the current flow at the primary side at the switching point, the design uses a transformer with L_prim = 80 µH, L_leak = 1.5 µH, and a ER11 core geometry as illustrated in Figure 10.

4.4 Output Ripple Configuration

The LM5017 module uses a constant on-time control scheme which requires appropriate voltage ripple at the feedback node. To ensure the correct ripple injection in the regulation loop, the design uses the following configuration and parameters shown in Figure 11 and Equation 8.

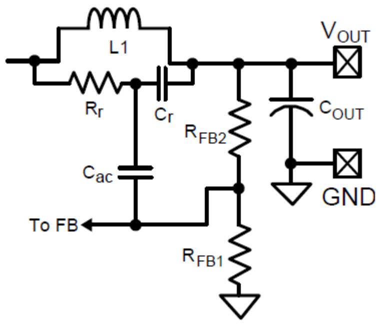


Figure 11. Typical Noise Amplification Scheme

$$RrCr \le \frac{(V_{IN}(MIN) - V_{OUT})T_{ON}}{25\ mV} \quad (8)$$

C_r = 4700 pF

C_{ac} = 100 nF

5 Test Results

Section 5.1 through Section 5.8 introduce the bench tests made on the power supply module.

5.1 Startup and Shutdown of Both Outputs

Figure 12 through Figure 15 show plots reflecting the design behavior during start-up and shut-down mode. All measurements have been taken with both outputs fully loaded (V_{OUT1} = 24 V at 25 mA and V_{OUT2} = 3.3 V at 50 mA).

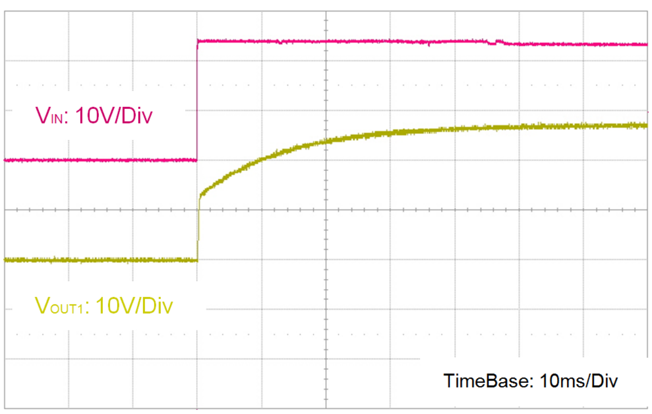


Figure 12. Startup of V_{OUT1} = 24 V

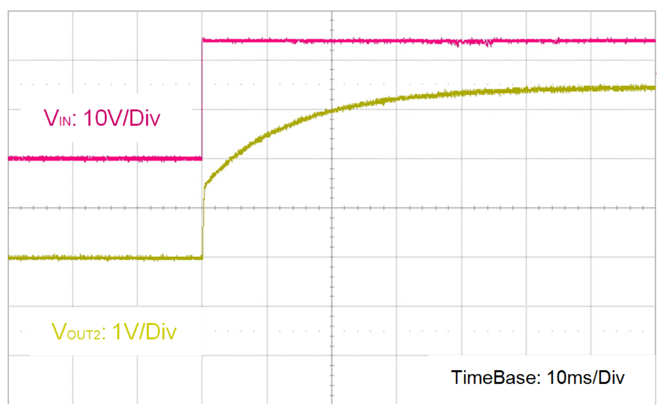


Figure 13. Startup of V_{OUT2} = 3.3 V

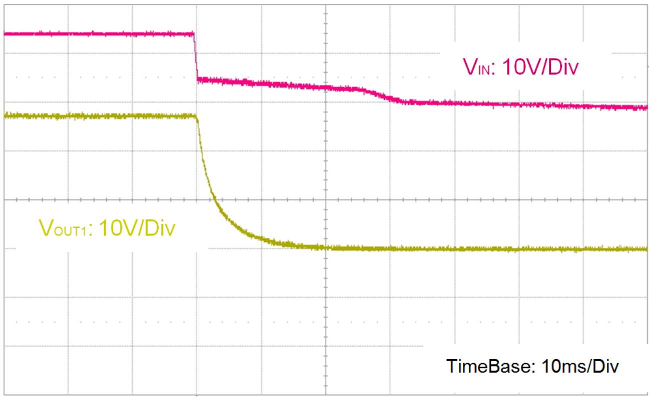


Figure 14. Shutdown of V_{OUT1} = 24 V

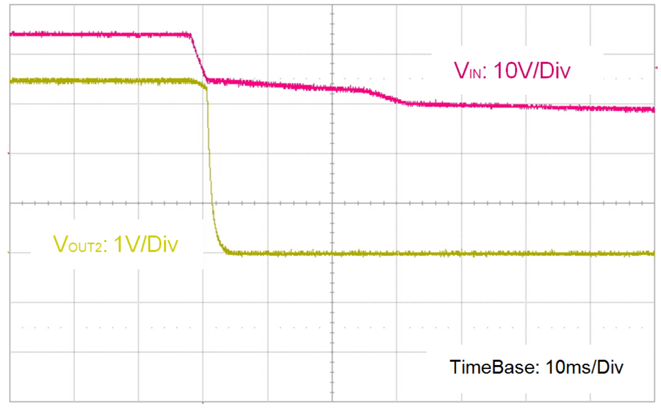


Figure 15. Shutdown of V_{OUT2} = 3.3 V

5.2 Operating Mode and Output Ripple

Figure 16 and Figure 17 are plots captured during tests which show the operating mode of the Fly-Buck at full load.

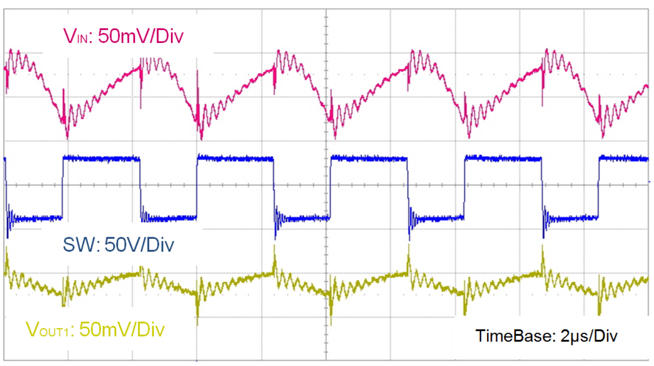


Figure 16. Operating Mode and Output Ripple at V_{OUT1} = 24 V

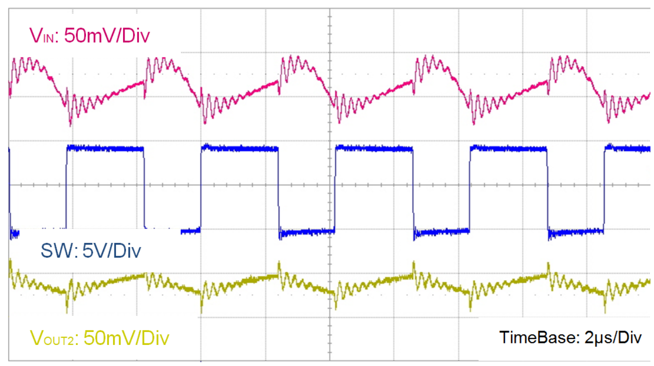


Figure 17. Operating Mode and Output Ripple at V_{OUT2} = 3.3 V

The design shows a 50-mV output ripple on V_{OUT1} and a 40 mV output ripple on the second output (V_{OUT2}).

5.3 Load Transient

Figure 18 shows an overview of the design response to a load step and, as a consequence, the loop stability. The load on the 24-V rail varies from 0 to 25 mA for 80 ms as shown in Figure 18.

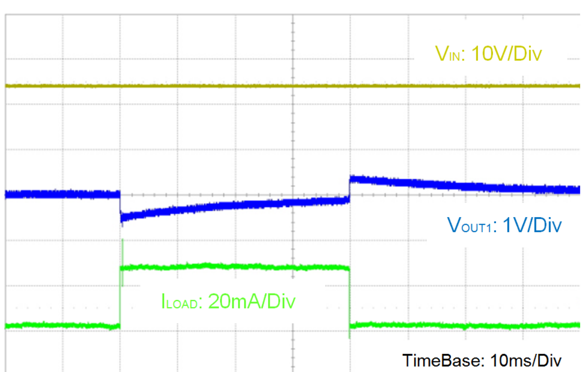


Figure 18. TIDA-00129 24-V Load Transient

5.4 Short Output

To ensure the correct behavior in critical conditions, a short cut on the output has been made and monitored, as shown in Figure 19.

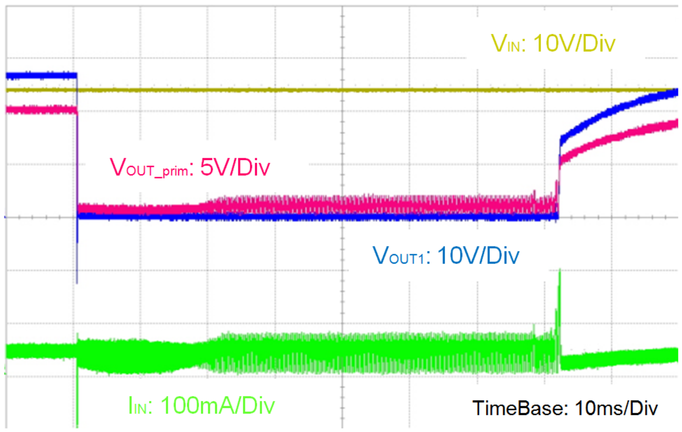


Figure 19. TIDA-00129 24-V Output Shorted

The LM501x family offers various current limits for the same performance, as shown in Table 1. The designer can choose different devices for the end application.

Table 1. LM501x Family Performance

Part Number	MIN Peak Current Limit (A)	I_q (mA)	V_{IN} (V)		V_{OUT} (V)	
			MIN	MAX	MIN	MAX
LM5017	0.7	1.75	7.5	100	1.25	90
LM5018	0.39	1.75	7.5	100	1.25	90

5.5 Load Regulation

The design respects the 10% output voltage accuracy set in the requirements, as shown in Figure 20 and Figure 21. For each load regulation measurement, the other output is fully loaded.

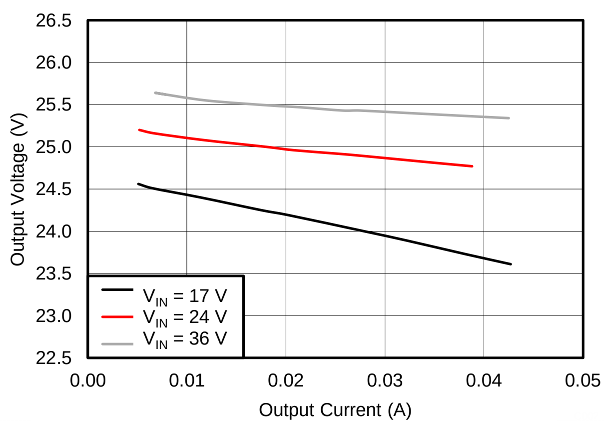


Figure 20. TIDA-00129, 24-V Load Regulation

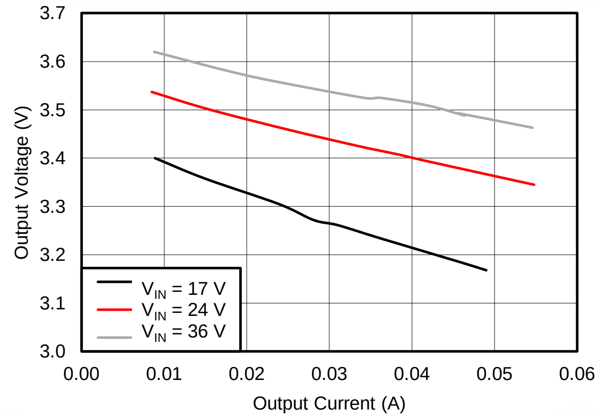


Figure 21. TIDA-00129, 3.3-V Load Regulation

5.6 Line Regulation

Figure 22 and Figure 23 show the output voltage regulation for a wide input voltage range. The red curves show the output voltage regulation while both outputs are fully loaded (respectively, 25 mA for V_{OUT1} = 24 V and 50 mA for V_{OUT2} = 3.3 V). In the other case (the black curve), data have been taken with no load on the main output measured, while the second output is fully loaded.

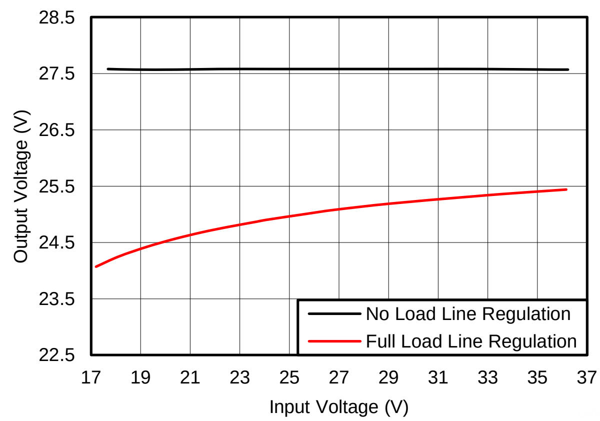


Figure 22. Line Regulation V_{OUT1} = 24 V

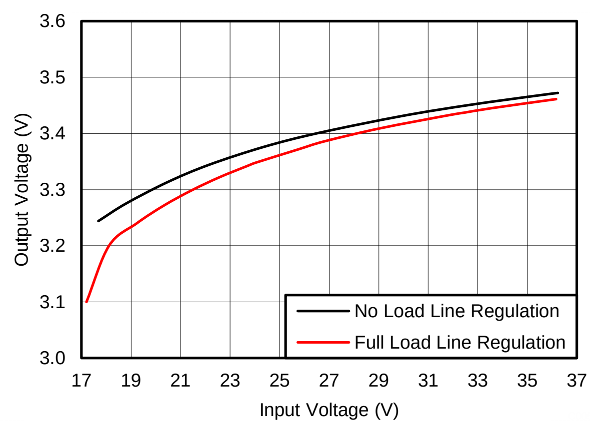


Figure 23. Line Regulation V_{OUT2} = 3.3 V

5.7 Efficiency

Figure 24 shows the overall efficiency of the LM5017 module over the entire output power range for different input voltages. Figure 24 is made with a fixed output power on the least significant output (V_{OUT2} at 50 mA, thus 165 mW), while changing the current on the 24-V output.

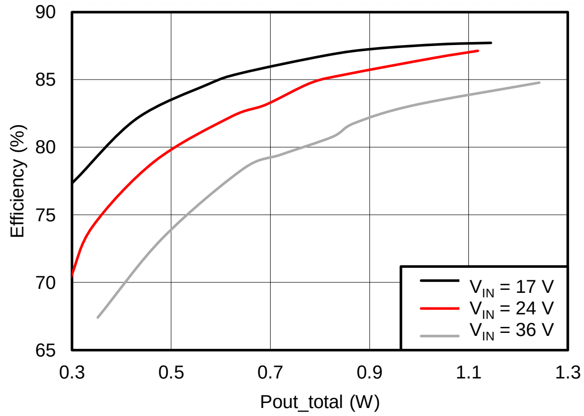
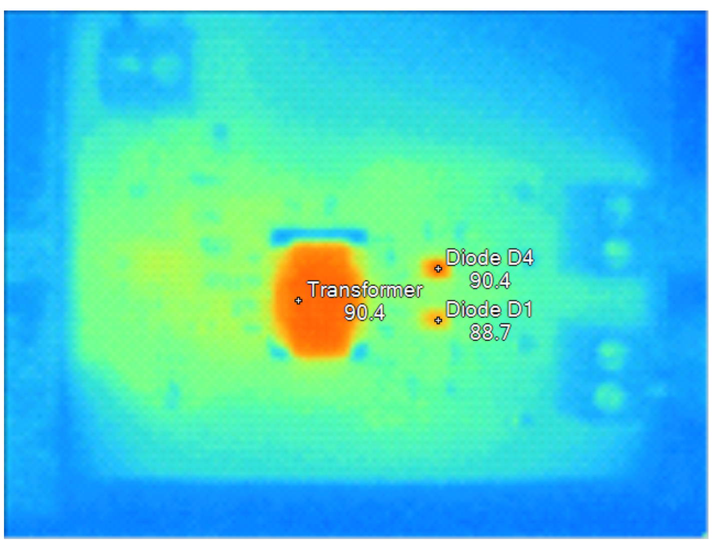


Figure 24. Overall Efficiency versus Output Power

5.8 Thermal Analysis

Efficiency and heat dissipation are major concerns for I/O modules due to their plastic housing. Figure 25 is the thermal image of the module at full load.



Transformer: 32.4°C
Diode D4: 32.1°C
Diode D1: 31.4°C
ΔT= 5°C

Figure 25. TIDA-00129 IR-Analysis (in °F)

6 Conclusion

This power reference design has been developed targeting a PLC I/O single-channel module. The main design goal is to use 6-mm height of the module and 85% efficiency at full load for the best fit in low-profile plastic housing. The TIDA-00129 power design provides isolated dual 24 V and 3.3 V which allows a flexible integration of a 4 to 20-mA current loop and low power components.

To include this design in a process control industry application, extra protection features can be added to ensure stringent EMC requirements fulfillment. As an example, current limit or clamping circuitry can be implemented in cascaded I/O module blocks.

7 PCB Layout

Figure 26 shows the PCB layout design.

Download the Altium project files from TIDA-00129.

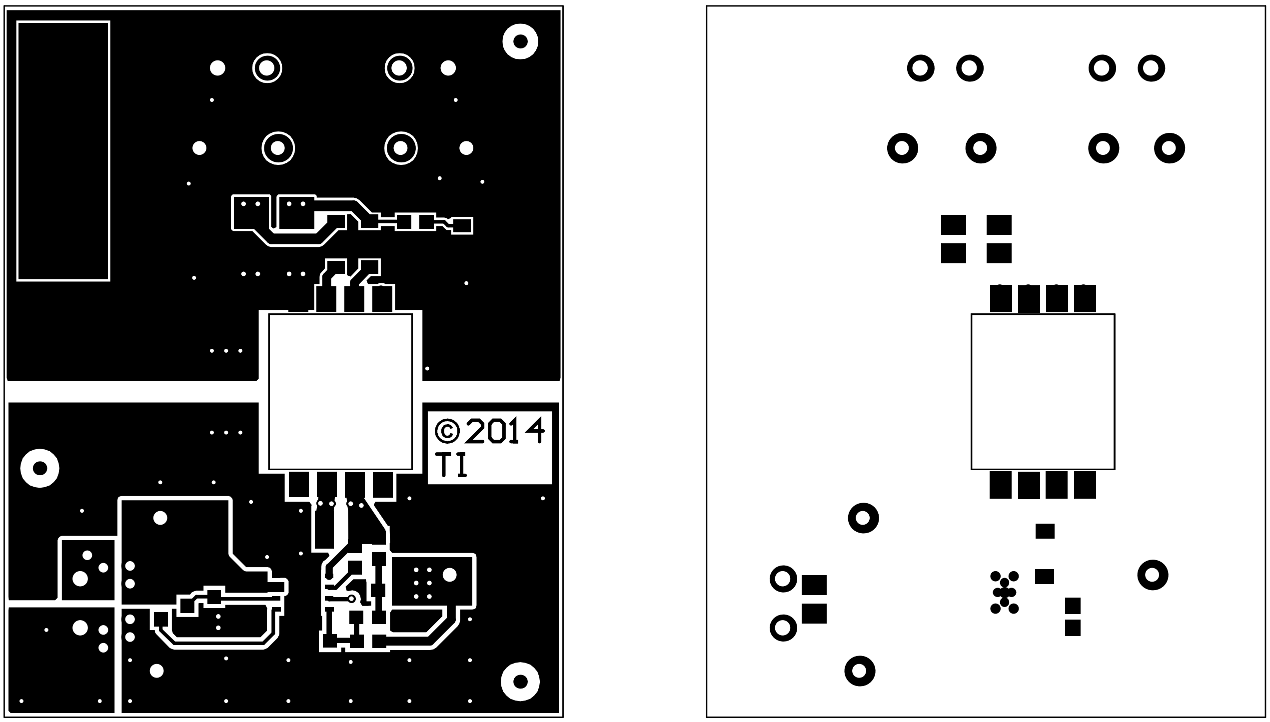


Figure 26. Top and Bottom Layers

8 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00129. Table 2 lists the BOM for the power module.

Table 2. TIDA-00129 Bill of Materials

Designator	Description	Comment	Quantity	Supplier	Part Number
C1	CAP, CERM, 4.7µF, 50V, +/-10%, X7R, 1206	GRM31CR71H475KA12L	1	Digikey	490-6521-2-ND
C2	CAP, CERM, 1000pF, 1000V, +/-5%, C0G/NP0, 1206	VJ1206A102JXGAT5Z	1	Digikey	720-1012-2-ND
C3	CAP, CERM, 4700pF, 100V, +/-10%, X7R, 0603	GCJ188R72A472KA01D	1	Digikey	541-82.0KHCT-ND
C4	CAP, CERM, 0.1µF, 16V, +/-5%, X7R, 0603	0603YC104JAT2A	1	Digikey	478-3726-2-ND
C5	CAP, CERM, 0.01µF, 50V, +/-5%, X7R, 0603	C0603C103J5RACTU	1	Digikey	399-1092-1-ND
C6, C12	CAP, CERM, 0.1µF, 50V, +/-10%, X7R, 0805	08055C104KAT2A	2	Digikey	478-1395-1-ND
C7	CAP, CERM, 4.7µF, 10V, +/-10%, X7R, 1206	GRM31CR71A475KA01L	1	Digikey	490-1805-1-ND
C8	CAP, CERM, 22µF, 16V, +/-10%, X7R, 1210	GRM32ER71C226KE18L	1	Digikey	490-4524-1-ND
C9	CAP, CERM, 2.2µF, 100V, X7R, +/-10%, 1210	C3225X7R2A225K	1	Digikey	445-4497-1-ND
C10	CAP, CERM, 0.47µF, 100V, +/-10%, X7R, 0805	GRM21BR72A474KA73L	1	Digikey	490-3326-2-ND
C11	CAP, CERM, 1µF, 25V, +/-10%, X7R, 0603	GRM188R71E105KA12D	1	Digikey	490-5307-1-ND
D1	Diode, Switching, 100V, 0.2A, SOD-123	MMSD4148T1G	1	Digikey	MMSD4148T1G
D2	Diode, Zener, 27V, 500mW, SOD-123	MMSZ5254B-7-F	1	Digikey	MMSZ5254B-7-F
D3, D4	Diode, Schottky, 30V, 0.2A, SOD-123	BAT42W-7-F	2	Digikey	BAT42W-FDICT-ND
J1, J2, J3	Conn Term Block, 2POS, 3.5mm, TH	1751248	3	Digikey	277-5719-ND
R1	RES, 49.9 Ω, 1%, 0.1W, 0603	RC0603FR-0749R9L	1	Digikey	311-49.9HRCT-ND
R2	RES, 46.4k Ω, 1%, 0.1W, 0603	RC0603FR-0746K4L	1	Digikey	311-46.4KHRCT-ND
R3	RES, 82k Ω, 1%, 0.1W, 0603	CRCW060382K0FKEA	1	Digikey	541-82.0KHCT-ND
R4	RES, 127k Ω, 1%, 0.1W, 0603	RC0603FR-07127KL	1	Digikey	311-127KHRCT-ND
R5	RES, 499k Ω, 1%, 0.1W, 0603	RC0603FR-07499KL	1	Digikey	311-499KHRCT-ND
R6	RES, 10.0k Ω, 1%, 0.1W, 0603	CRCW060310K0FKEA	1	Digikey	541-10.0KHCT-ND
R7	RES, 12.4k Ω, 1%, 0.1W, 0603	CRCW060312K4FKEA	1	Digikey	541-12.4KHCT-ND
T1	Transformer, 80 µH, SMT	750314441 (with PCB cutout) 750315176 (no PCB cutout)	1	Würth Elektronik	750314441 750315176
TP1, TP2, TP4, TP5, TP6, TP7, TP8	Test Point, TH, Miniature, Red	5000	7	Digikey	5000K-ND
U1	IC, 100 V, 600 mA COT Synchronous Buck	LM5017SD	1	Texas Instruments	LM5017SD

9 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00129.

10 Software Files

To download the software files for the reference design, see the design files at TIDA-00129.

11 About the Authors

ROMAIN VISCARDI is a System Engineer at Texas Instruments Germany, where he develops power reference designs for the factory and automation segment. Romain earned his Master of Science in Electrical Engineering (MSEE) from CPE engineering school in Lyon, France.

INGOLF FRANK is a systems engineer in the Texas Instruments Industrial Automation Team, focusing on programmable logic controller I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the Bielefeld University of Applied Sciences at Bielefeld, Germany in 1991.

Revision History

Changes from Original (April 2014) to A Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.