TMS320DM335
Digital Media System-on-Chip (DMSoC)
General-Purpose Input/Output (GPIO)

Reference Guide

Literature Number: SPRUFY8
July 2008
## Contents

Preface ........................................................................................................................................ 6

1 Introduction .................................................................................................................................. 9
   1.1 Purpose of the Peripheral ........................................................................................................... 9
   1.2 Features ..................................................................................................................................... 9
   1.3 Functional Block Diagram .......................................................................................................... 10
   1.4 Industry Standard(s) Compliance Statement ............................................................................. 10

2 Peripheral Architecture .............................................................................................................. 10
   2.1 Clock Control ............................................................................................................................ 10
   2.2 Signal Descriptions .................................................................................................................... 10
   2.3 GPIO Register Structure ........................................................................................................... 11
   2.4 Using a GPIO Signal as an Output .............................................................................................. 13
   2.5 Using a GPIO Signal as an Input ................................................................................................. 14
   2.6 Debounce .................................................................................................................................. 14
   2.7 Reset Considerations .................................................................................................................. 15
   2.8 Interrupt Support ....................................................................................................................... 15
   2.9 EDMA Event Support .................................................................................................................. 18
   2.10 Power Management .................................................................................................................. 18
   2.11 Emulation Considerations ....................................................................................................... 18

3 Registers ....................................................................................................................................... 19
   3.1 Peripheral Identification Register (PID) ..................................................................................... 21
   3.2 GPIO Interrupt Per-Bank Enable Register (BINTEN) ............................................................... 22
   3.3 GPIO Direction Registers (DIRn) .............................................................................................. 23
   3.4 GPIO Output Data Register (OUT_DATA)n .............................................................................. 25
   3.5 GPIO Set Data Register (SET_DATA)n ..................................................................................... 27
   3.6 GPIO Clear Data Register (CLR_DATA)n ................................................................................... 29
   3.7 GPIO Input Data Register (IN_DATA)n ...................................................................................... 31
   3.8 GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG)n ..................................................... 33
   3.9 GPIO Clear Rising EdgeInterrupt Register (CLR_RIS_TRIG)n .................................................. 35
   3.10 GPIO Set Falling EdgeInterrupt Register (SET_FAL_TRIG)n .................................................... 37
   3.11 GPIO Clear Falling EdgeInterrupt Register (CLR_FAL_TRIG)n ................................................ 39
   3.12 GPIO Interrupt Status Register (INTSTATn) .......................................................................... 41
### List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GPIO Peripheral Block Diagram</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
<td>Peripheral Identification Register (PID)</td>
<td>21</td>
</tr>
<tr>
<td>3</td>
<td>GPIO Interrupt Per-Bank Enable Register (BINTEN)</td>
<td>22</td>
</tr>
<tr>
<td>4</td>
<td>GPIO Banks 0 and 1 Direction Register (DIR01)</td>
<td>23</td>
</tr>
<tr>
<td>5</td>
<td>GPIO Banks 2 and 3 Direction Register (DIR23)</td>
<td>23</td>
</tr>
<tr>
<td>6</td>
<td>GPIO Banks 4 and 5 Direction Register (DIR45)</td>
<td>24</td>
</tr>
<tr>
<td>7</td>
<td>GPIO Bank 6 Direction Register (DIR6)</td>
<td>24</td>
</tr>
<tr>
<td>8</td>
<td>GPIO Banks 0 and 1 Output Data Register (OUT_DATA01)</td>
<td>25</td>
</tr>
<tr>
<td>9</td>
<td>GPIO Banks 2 and 3 Output Data Register (OUT_DATA23)</td>
<td>25</td>
</tr>
<tr>
<td>10</td>
<td>GPIO Banks 4 and 5 Output Data Register (OUT_DATA45)</td>
<td>26</td>
</tr>
<tr>
<td>11</td>
<td>GPIO Bank 6 Output Data Register (OUT_DATA6)</td>
<td>26</td>
</tr>
<tr>
<td>12</td>
<td>GPIO Banks 0 and 1 Set Data Register (SET_DATA01)</td>
<td>27</td>
</tr>
<tr>
<td>13</td>
<td>GPIO Banks 2 and 3 Set Data Register (SET_DATA23)</td>
<td>27</td>
</tr>
<tr>
<td>14</td>
<td>GPIO Banks 4 and 5 Set Data Register (SET_DATA45)</td>
<td>28</td>
</tr>
<tr>
<td>15</td>
<td>GPIO Bank 6 Set Data Register (SET_DATA6)</td>
<td>28</td>
</tr>
<tr>
<td>16</td>
<td>GPIO Banks 0 and 1 Clear Data Register (CLR_DATA01)</td>
<td>29</td>
</tr>
<tr>
<td>17</td>
<td>GPIO Banks 2 and 3 Clear Data Register (CLR_DATA23)</td>
<td>29</td>
</tr>
<tr>
<td>18</td>
<td>GPIO Banks 4 and 5 Clear Data Register (CLR_DATA45)</td>
<td>30</td>
</tr>
<tr>
<td>19</td>
<td>GPIO Bank 6 Clear Data Register (CLR_DATA6)</td>
<td>30</td>
</tr>
<tr>
<td>20</td>
<td>GPIO Banks 0 and 1 Input Data Register (IN_DATA01)</td>
<td>31</td>
</tr>
<tr>
<td>21</td>
<td>GPIO Banks 2 and 3 Input Data Register (IN_DATA23)</td>
<td>31</td>
</tr>
<tr>
<td>22</td>
<td>GPIO Banks 4 and 5 Input Data Register (IN_DATA45)</td>
<td>32</td>
</tr>
<tr>
<td>23</td>
<td>GPIO Bank 6 Input Data Register (IN_DATA6)</td>
<td>32</td>
</tr>
<tr>
<td>24</td>
<td>GPIO Banks 0 and 1 Set Rising Edge Interrupt Register (SET_RIS_TRIG01)</td>
<td>33</td>
</tr>
<tr>
<td>25</td>
<td>GPIO Banks 2 and 3 Set Rising Edge Interrupt Register (SET_RIS_TRIG23)</td>
<td>33</td>
</tr>
<tr>
<td>26</td>
<td>GPIO Banks 4 and 5 Set Rising Edge Interrupt Register (SET_RIS_TRIG45)</td>
<td>34</td>
</tr>
<tr>
<td>27</td>
<td>GPIO Bank 6 Set Rising Edge Interrupt Register (SET_RIS_TRIG6)</td>
<td>34</td>
</tr>
<tr>
<td>28</td>
<td>GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG01)</td>
<td>35</td>
</tr>
<tr>
<td>29</td>
<td>GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG23)</td>
<td>35</td>
</tr>
<tr>
<td>30</td>
<td>GPIO Banks 4 and 5 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG45)</td>
<td>36</td>
</tr>
<tr>
<td>31</td>
<td>GPIO Bank 6 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG6)</td>
<td>36</td>
</tr>
<tr>
<td>32</td>
<td>GPIO Banks 0 and 1 Set Falling Edge Interrupt Register (SET_FAL_TRIG01)</td>
<td>37</td>
</tr>
<tr>
<td>33</td>
<td>GPIO Banks 2 and 3 Set Falling Edge Interrupt Register (SET_FAL_TRIG23)</td>
<td>37</td>
</tr>
<tr>
<td>34</td>
<td>GPIO Banks 4 and 5 Set Falling Edge Interrupt Register (SET_FAL_TRIG45)</td>
<td>38</td>
</tr>
<tr>
<td>35</td>
<td>GPIO Bank 6 Set Falling Edge Interrupt Register (SET_FAL_TRIG6)</td>
<td>38</td>
</tr>
<tr>
<td>36</td>
<td>GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG01)</td>
<td>39</td>
</tr>
<tr>
<td>37</td>
<td>GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG23)</td>
<td>39</td>
</tr>
<tr>
<td>38</td>
<td>GPIO Banks 4 and 5 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG45)</td>
<td>40</td>
</tr>
<tr>
<td>39</td>
<td>GPIO Bank 6 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG6)</td>
<td>40</td>
</tr>
<tr>
<td>40</td>
<td>GPIO Banks 0 and 1 Interrupt Status Register (INTSTAT01)</td>
<td>41</td>
</tr>
<tr>
<td>41</td>
<td>GPIO Banks 2 and 3 Interrupt Status Register (INTSTAT23)</td>
<td>41</td>
</tr>
<tr>
<td>42</td>
<td>GPIO Banks 4 and 5 Interrupt Status Register (INTSTAT45)</td>
<td>42</td>
</tr>
<tr>
<td>43</td>
<td>GPIO Bank 6 Interrupt Status Register (INTSTAT6)</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>---</td>
<td>------------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Register Bits and Banks Associated With GPIO Pins</td>
<td>11</td>
</tr>
<tr>
<td>2</td>
<td>GPIO Interrupts to the ARM CPU</td>
<td>15</td>
</tr>
<tr>
<td>3</td>
<td>GPIO Synchronization Events to the EDMA</td>
<td>18</td>
</tr>
<tr>
<td>4</td>
<td>General-Purpose Input/Output (GPIO) Registers</td>
<td>19</td>
</tr>
<tr>
<td>5</td>
<td>Peripheral Identification Register (PID) Field Descriptions</td>
<td>21</td>
</tr>
<tr>
<td>6</td>
<td>GPIO Interrupt Per-Bank Enable Register (BINTEN) Field Descriptions</td>
<td>22</td>
</tr>
<tr>
<td>7</td>
<td>GPIO Direction Register (DIRn) Field Descriptions</td>
<td>24</td>
</tr>
<tr>
<td>8</td>
<td>GPIO Output Data Register (OUT_DATAn) Field Descriptions</td>
<td>26</td>
</tr>
<tr>
<td>9</td>
<td>GPIO Set Data Register (SET_DATAn) Field Descriptions</td>
<td>28</td>
</tr>
<tr>
<td>10</td>
<td>GPIO Clear Data Register (CLR_DATAn) Field Descriptions</td>
<td>30</td>
</tr>
<tr>
<td>11</td>
<td>GPIO Input Data Register (IN_DATAn) Field Descriptions</td>
<td>32</td>
</tr>
<tr>
<td>12</td>
<td>GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIGn) Field Descriptions</td>
<td>34</td>
</tr>
<tr>
<td>13</td>
<td>GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGn) Field Descriptions</td>
<td>36</td>
</tr>
<tr>
<td>14</td>
<td>GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIGn) Field Descriptions</td>
<td>38</td>
</tr>
<tr>
<td>15</td>
<td>GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIGn) Field Descriptions</td>
<td>40</td>
</tr>
<tr>
<td>16</td>
<td>GPIO Interrupt Status Register (INTSTATn) Field Descriptions</td>
<td>42</td>
</tr>
</tbody>
</table>
This document describes the General-Purpose Input/Output (GPIO) on the TMS320DM335 Digital Media System-on-Chip.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation from Texas Instruments

The following documents describe the TMS320DM335 Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

**SPRUF7 — TMS320DM335 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide** This document describes the ARM Subsystem in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

**SPRUF8 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Reference Guide** This document describes the Video Processing Front End (VPFE) in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

**SPRUF9 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Reference Guide** This document describes the Video Processing Back End (VPBE) in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

**SPRUF0 — TMS320DM335 Digital Media System-on-Chip (DMSoC) 64-bit Timer Reference Guide** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM335 Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

**SPRUF1 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Reference Guide** This document describes the serial peripheral interface (SPI) in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.
SPRUFY2 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Reference Guide This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFY3 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Reference Guide This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFY5 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUFY6 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Reference Guide This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC).


SPRUFY8 — TMS320DM335 Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Reference Guide This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUFY9 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Reference Guide This document describes the universal serial bus (USB) controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFZ0 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFZ1 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Reference Guide This document describes the asynchronous external memory interface (EMIF) in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFZ2 — TMS320DM335 Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Reference Guide This document describes the DDR2/mDDR memory controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.
SPRUFZ3 — TMS320DM335 Digital Media System-on-Chip (DMSoC) Audio Serial Port (ASP)

Reference Guide This document describes the operation of the audio serial port (ASP) audio interface in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.

Trademarks
1 Introduction

The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

1.1 Purpose of the Peripheral

Most system on a chip (SoC) devices require some general-purpose input/output (GPIO) functionality in order to interact with other components in the system using low-speed interface pins. The control and use of the GPIO capability on this device is grouped together in the GPIO peripheral and is described in the following sections.

1.2 Features

The GPIO peripheral consists of the following features.

- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers
  - Output register can be read to reflect output drive status.
  - Input register can be read to reflect pin status.
- All GPIO signals can be used as interrupt sources with configurable edge detection.
- All GPIO signals can be used to generate events to the EDMA.
- Programmable debounce circuit provided on GPIO[7:0].
1.3 **Functional Block Diagram**

Figure 1 shows a block diagram of the GPIO peripheral.

![GPIO Peripheral Block Diagram](image)

1.4 **Industry Standard(s) Compliance Statement**

The GPIO peripheral connects to external devices. While it is possible that the software implements some standard connectivity protocol over GPIO, the GPIO peripheral itself is not compliant with any such standards.

2 **Peripheral Architecture**

The following sections describe the GPIO peripheral.

2.1 **Clock Control**

The input clock to the GPIO peripheral is driven by PLL1. The maximum operation speed for the GPIO peripheral is 10 MHz.

2.2 **Signal Descriptions**

The device supports up to 104 signals, GPIO[103:0]. These GPIOs are 3.3V I/O signals. For information on the package pinout of each GPIO signal, refer to the device-specific data manual.
2.3 GPIO Register Structure

The GPIO signals are grouped into banks of 16 signals per bank.

The GPIO configuration registers are organized as one 32-bit register per pair of banks. When there are an odd number of banks, the upper 16-bit of registers for the last pair are reserved and have no effect. For the interrupt configuration, the registers associated with GPIO signals that do not support interrupt capability are also reserved and have no effect. Table 1 shows the banks and register control bit information associated with each GPIO pin on the device. The table can be used to locate the register bits that control each GPIO signal. For detailed information on the GPIO registers, see section Section 3.

Table 1. GPIO Register Bits and Banks Associated With GPIO Pins

<table>
<thead>
<tr>
<th>GPIO Signal</th>
<th>Bank Number</th>
<th>Register Pair Number</th>
<th>Register Field Number</th>
<th>Bit Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0</td>
<td>0</td>
<td>register_name01</td>
<td>field_name00</td>
<td>Bit 0</td>
</tr>
<tr>
<td>GPIO1</td>
<td>0</td>
<td>register_name01</td>
<td>field_name01</td>
<td>Bit 1</td>
</tr>
<tr>
<td>GPIO2</td>
<td>0</td>
<td>register_name01</td>
<td>field_name02</td>
<td>Bit 2</td>
</tr>
<tr>
<td>GPIO3</td>
<td>0</td>
<td>register_name01</td>
<td>field_name03</td>
<td>Bit 3</td>
</tr>
<tr>
<td>GPIO4</td>
<td>0</td>
<td>register_name01</td>
<td>field_name04</td>
<td>Bit 4</td>
</tr>
<tr>
<td>GPIO5</td>
<td>0</td>
<td>register_name01</td>
<td>field_name05</td>
<td>Bit 5</td>
</tr>
<tr>
<td>GPIO6</td>
<td>0</td>
<td>register_name01</td>
<td>field_name06</td>
<td>Bit 6</td>
</tr>
<tr>
<td>GPIO7</td>
<td>0</td>
<td>register_name01</td>
<td>field_name07</td>
<td>Bit 7</td>
</tr>
<tr>
<td>GPIO8</td>
<td>0</td>
<td>register_name01</td>
<td>field_name08</td>
<td>Bit 8</td>
</tr>
<tr>
<td>GPIO9</td>
<td>0</td>
<td>register_name01</td>
<td>field_name09</td>
<td>Bit 9</td>
</tr>
<tr>
<td>GPIO10</td>
<td>0</td>
<td>register_name01</td>
<td>field_name10</td>
<td>Bit 10</td>
</tr>
<tr>
<td>GPIO11</td>
<td>0</td>
<td>register_name01</td>
<td>field_name11</td>
<td>Bit 11</td>
</tr>
<tr>
<td>GPIO12</td>
<td>0</td>
<td>register_name01</td>
<td>field_name12</td>
<td>Bit 12</td>
</tr>
<tr>
<td>GPIO13</td>
<td>0</td>
<td>register_name01</td>
<td>field_name13</td>
<td>Bit 13</td>
</tr>
<tr>
<td>GPIO14</td>
<td>0</td>
<td>register_name01</td>
<td>field_name14</td>
<td>Bit 14</td>
</tr>
<tr>
<td>GPIO15</td>
<td>0</td>
<td>register_name01</td>
<td>field_name15</td>
<td>Bit 15</td>
</tr>
<tr>
<td>GPIO16</td>
<td>1</td>
<td>register_name01</td>
<td>field_name16</td>
<td>Bit 16</td>
</tr>
<tr>
<td>GPIO17</td>
<td>1</td>
<td>register_name01</td>
<td>field_name17</td>
<td>Bit 17</td>
</tr>
<tr>
<td>GPIO18</td>
<td>1</td>
<td>register_name01</td>
<td>field_name18</td>
<td>Bit 18</td>
</tr>
<tr>
<td>GPIO19</td>
<td>1</td>
<td>register_name01</td>
<td>field_name19</td>
<td>Bit 19</td>
</tr>
<tr>
<td>GPIO20</td>
<td>1</td>
<td>register_name01</td>
<td>field_name20</td>
<td>Bit 20</td>
</tr>
<tr>
<td>GPIO21</td>
<td>1</td>
<td>register_name01</td>
<td>field_name21</td>
<td>Bit 21</td>
</tr>
<tr>
<td>GPIO22</td>
<td>1</td>
<td>register_name01</td>
<td>field_name22</td>
<td>Bit 22</td>
</tr>
<tr>
<td>GPIO23</td>
<td>1</td>
<td>register_name01</td>
<td>field_name23</td>
<td>Bit 23</td>
</tr>
<tr>
<td>GPIO24</td>
<td>1</td>
<td>register_name01</td>
<td>field_name24</td>
<td>Bit 24</td>
</tr>
<tr>
<td>GPIO25</td>
<td>1</td>
<td>register_name01</td>
<td>field_name25</td>
<td>Bit 25</td>
</tr>
<tr>
<td>GPIO26</td>
<td>1</td>
<td>register_name01</td>
<td>field_name26</td>
<td>Bit 26</td>
</tr>
<tr>
<td>GPIO27</td>
<td>1</td>
<td>register_name01</td>
<td>field_name27</td>
<td>Bit 27</td>
</tr>
<tr>
<td>GPIO28</td>
<td>1</td>
<td>register_name01</td>
<td>field_name28</td>
<td>Bit 28</td>
</tr>
<tr>
<td>GPIO29</td>
<td>1</td>
<td>register_name01</td>
<td>field_name29</td>
<td>Bit 29</td>
</tr>
<tr>
<td>GPIO30</td>
<td>1</td>
<td>register_name01</td>
<td>field_name30</td>
<td>Bit 30</td>
</tr>
<tr>
<td>GPIO31</td>
<td>1</td>
<td>register_name01</td>
<td>field_name31</td>
<td>Bit 31</td>
</tr>
<tr>
<td>GPIO32</td>
<td>2</td>
<td>register_name23</td>
<td>field_name32</td>
<td>Bit 0</td>
</tr>
<tr>
<td>GPIO33</td>
<td>2</td>
<td>register_name23</td>
<td>field_name33</td>
<td>Bit 1</td>
</tr>
<tr>
<td>GPIO34</td>
<td>2</td>
<td>register_name23</td>
<td>field_name34</td>
<td>Bit 2</td>
</tr>
<tr>
<td>GPIO35</td>
<td>2</td>
<td>register_name23</td>
<td>field_name35</td>
<td>Bit 3</td>
</tr>
<tr>
<td>GPIO36</td>
<td>2</td>
<td>register_name23</td>
<td>field_name36</td>
<td>Bit 4</td>
</tr>
<tr>
<td>GPIO37</td>
<td>2</td>
<td>register_name23</td>
<td>field_name37</td>
<td>Bit 5</td>
</tr>
</tbody>
</table>
Table 1. GPIO Register Bits and Banks Associated With GPIO Pins (continued)

<table>
<thead>
<tr>
<th>GPIO Signal</th>
<th>Bank Number</th>
<th>Register Pair Number</th>
<th>Register Field Number</th>
<th>Bit Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO038</td>
<td>2</td>
<td>register_name23</td>
<td>field_name38</td>
<td>Bit 6</td>
</tr>
<tr>
<td>GPIO039</td>
<td>2</td>
<td>register_name23</td>
<td>field_name39</td>
<td>Bit 7</td>
</tr>
<tr>
<td>GPIO040</td>
<td>2</td>
<td>register_name23</td>
<td>field_name40</td>
<td>Bit 8</td>
</tr>
<tr>
<td>GPIO041</td>
<td>2</td>
<td>register_name23</td>
<td>field_name41</td>
<td>Bit 9</td>
</tr>
<tr>
<td>GPIO042</td>
<td>2</td>
<td>register_name23</td>
<td>field_name42</td>
<td>Bit 10</td>
</tr>
<tr>
<td>GPIO043</td>
<td>2</td>
<td>register_name23</td>
<td>field_name43</td>
<td>Bit 11</td>
</tr>
<tr>
<td>GPIO044</td>
<td>2</td>
<td>register_name23</td>
<td>field_name44</td>
<td>Bit 12</td>
</tr>
<tr>
<td>GPIO045</td>
<td>2</td>
<td>register_name23</td>
<td>field_name45</td>
<td>Bit 13</td>
</tr>
<tr>
<td>GPIO046</td>
<td>2</td>
<td>register_name23</td>
<td>field_name46</td>
<td>Bit 14</td>
</tr>
<tr>
<td>GPIO047</td>
<td>2</td>
<td>register_name23</td>
<td>field_name47</td>
<td>Bit 15</td>
</tr>
<tr>
<td>GPIO048</td>
<td>3</td>
<td>register_name23</td>
<td>field_name48</td>
<td>Bit 16</td>
</tr>
<tr>
<td>GPIO049</td>
<td>3</td>
<td>register_name23</td>
<td>field_name49</td>
<td>Bit 17</td>
</tr>
<tr>
<td>GPIO050</td>
<td>3</td>
<td>register_name23</td>
<td>field_name50</td>
<td>Bit 18</td>
</tr>
<tr>
<td>GPIO051</td>
<td>3</td>
<td>register_name23</td>
<td>field_name51</td>
<td>Bit 19</td>
</tr>
<tr>
<td>GPIO052</td>
<td>3</td>
<td>register_name23</td>
<td>field_name52</td>
<td>Bit 20</td>
</tr>
<tr>
<td>GPIO053</td>
<td>3</td>
<td>register_name23</td>
<td>field_name53</td>
<td>Bit 21</td>
</tr>
<tr>
<td>GPIO054</td>
<td>3</td>
<td>register_name23</td>
<td>field_name54</td>
<td>Bit 22</td>
</tr>
<tr>
<td>GPIO055</td>
<td>3</td>
<td>register_name23</td>
<td>field_name55</td>
<td>Bit 23</td>
</tr>
<tr>
<td>GPIO056</td>
<td>3</td>
<td>register_name23</td>
<td>field_name56</td>
<td>Bit 24</td>
</tr>
<tr>
<td>GPIO057</td>
<td>3</td>
<td>register_name23</td>
<td>field_name57</td>
<td>Bit 25</td>
</tr>
<tr>
<td>GPIO058</td>
<td>3</td>
<td>register_name23</td>
<td>field_name58</td>
<td>Bit 26</td>
</tr>
<tr>
<td>GPIO059</td>
<td>3</td>
<td>register_name23</td>
<td>field_name59</td>
<td>Bit 27</td>
</tr>
<tr>
<td>GPIO060</td>
<td>3</td>
<td>register_name23</td>
<td>field_name60</td>
<td>Bit 28</td>
</tr>
<tr>
<td>GPIO061</td>
<td>3</td>
<td>register_name23</td>
<td>field_name61</td>
<td>Bit 29</td>
</tr>
<tr>
<td>GPIO062</td>
<td>3</td>
<td>register_name23</td>
<td>field_name62</td>
<td>Bit 30</td>
</tr>
<tr>
<td>GPIO063</td>
<td>3</td>
<td>register_name23</td>
<td>field_name63</td>
<td>Bit 31</td>
</tr>
<tr>
<td>GPIO064</td>
<td>4</td>
<td>register_name45</td>
<td>field_name64</td>
<td>Bit 0</td>
</tr>
<tr>
<td>GPIO065</td>
<td>4</td>
<td>register_name45</td>
<td>field_name65</td>
<td>Bit 1</td>
</tr>
<tr>
<td>GPIO066</td>
<td>4</td>
<td>register_name45</td>
<td>field_name66</td>
<td>Bit 2</td>
</tr>
<tr>
<td>GPIO067</td>
<td>4</td>
<td>register_name45</td>
<td>field_name67</td>
<td>Bit 3</td>
</tr>
<tr>
<td>GPIO068</td>
<td>4</td>
<td>register_name45</td>
<td>field_name68</td>
<td>Bit 4</td>
</tr>
<tr>
<td>GPIO069</td>
<td>4</td>
<td>register_name45</td>
<td>field_name69</td>
<td>Bit 5</td>
</tr>
<tr>
<td>GPIO070</td>
<td>4</td>
<td>register_name45</td>
<td>field_name70</td>
<td>Bit 6</td>
</tr>
<tr>
<td>GPIO071</td>
<td>4</td>
<td>register_name45</td>
<td>field_name71</td>
<td>Bit 7</td>
</tr>
<tr>
<td>GPIO072</td>
<td>4</td>
<td>register_name45</td>
<td>field_name72</td>
<td>Bit 8</td>
</tr>
<tr>
<td>GPIO073</td>
<td>4</td>
<td>register_name45</td>
<td>field_name73</td>
<td>Bit 9</td>
</tr>
<tr>
<td>GPIO074</td>
<td>4</td>
<td>register_name45</td>
<td>field_name74</td>
<td>Bit 10</td>
</tr>
<tr>
<td>GPIO075</td>
<td>4</td>
<td>register_name45</td>
<td>field_name75</td>
<td>Bit 11</td>
</tr>
<tr>
<td>GPIO076</td>
<td>4</td>
<td>register_name45</td>
<td>field_name76</td>
<td>Bit 12</td>
</tr>
<tr>
<td>GPIO077</td>
<td>4</td>
<td>register_name45</td>
<td>field_name77</td>
<td>Bit 13</td>
</tr>
<tr>
<td>GPIO078</td>
<td>4</td>
<td>register_name45</td>
<td>field_name78</td>
<td>Bit 14</td>
</tr>
<tr>
<td>GPIO079</td>
<td>4</td>
<td>register_name45</td>
<td>field_name79</td>
<td>Bit 15</td>
</tr>
<tr>
<td>GPIO080</td>
<td>5</td>
<td>register_name45</td>
<td>field_name80</td>
<td>Bit 16</td>
</tr>
<tr>
<td>GPIO081</td>
<td>5</td>
<td>register_name45</td>
<td>field_name81</td>
<td>Bit 17</td>
</tr>
<tr>
<td>GPIO082</td>
<td>5</td>
<td>register_name45</td>
<td>field_name82</td>
<td>Bit 18</td>
</tr>
<tr>
<td>GPIO083</td>
<td>5</td>
<td>register_name45</td>
<td>field_name83</td>
<td>Bit 19</td>
</tr>
</tbody>
</table>
2.4 Using a GPIO Signal as an Output

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction register (DIR). This section describes using the GPIO signal as an output signal.

2.4.1 Configuring a GPIO Output Signal

To configure a given GPIO signal as an output, clear the bit in DIR that is associated with the desired GPIO signal. For detailed information on DIR, see Section 3.

2.4.2 Controlling the GPIO Output Signal State

There are three registers that control the output state driven on a GPIO signal configured as an output:

- GPIO set data register (SET_DATA) controls driving GPIO signals high
- GPIO clear data register (CLR_DATA) controls driving GPIO signals low
- GPIO output data register (OUT_DATA) contains the current state of the output signals

Reading SET_DATA, CLR_DATA, and OUT_DATA returns the output state not necessarily the actual signal state (since some signals may be configured as inputs). The actual signal state is read using the GPIO input data register (IN_DATA) associated with the desired GPIO signal. IN_DATA contains the actual logic state on the external signal.

For detailed information on these registers, see Section 3.

2.4.2.1 Driving a GPIO Output Signal High

To drive a GPIO signal high, use one of the following methods:

- Write a logic 1 to the bit in SET_DATA associated with the desired GPIO signal(s) to be driven high. Bit positions in SET_DATA containing logic 0 do not affect the state of the associated output signals.

Table 1. GPIO Register Bits and Banks Associated With GPIO Pins (continued)

<table>
<thead>
<tr>
<th>GPIO Signal</th>
<th>Bank Number</th>
<th>Register Pair Number</th>
<th>Register Field Number</th>
<th>Bit Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO84</td>
<td>5</td>
<td>register_name45</td>
<td>field_name84</td>
<td>Bit 20</td>
</tr>
<tr>
<td>GPIO85</td>
<td>5</td>
<td>register_name45</td>
<td>field_name85</td>
<td>Bit 21</td>
</tr>
<tr>
<td>GPIO86</td>
<td>5</td>
<td>register_name45</td>
<td>field_name86</td>
<td>Bit 22</td>
</tr>
<tr>
<td>GPIO87</td>
<td>5</td>
<td>register_name45</td>
<td>field_name87</td>
<td>Bit 23</td>
</tr>
<tr>
<td>GPIO88</td>
<td>5</td>
<td>register_name45</td>
<td>field_name88</td>
<td>Bit 24</td>
</tr>
<tr>
<td>GPIO89</td>
<td>5</td>
<td>register_name45</td>
<td>field_name89</td>
<td>Bit 25</td>
</tr>
<tr>
<td>GPIO90</td>
<td>5</td>
<td>register_name45</td>
<td>field_name90</td>
<td>Bit 26</td>
</tr>
<tr>
<td>GPIO91</td>
<td>5</td>
<td>register_name45</td>
<td>field_name91</td>
<td>Bit 27</td>
</tr>
<tr>
<td>GPIO92</td>
<td>5</td>
<td>register_name45</td>
<td>field_name92</td>
<td>Bit 28</td>
</tr>
<tr>
<td>GPIO93</td>
<td>5</td>
<td>register_name45</td>
<td>field_name93</td>
<td>Bit 29</td>
</tr>
<tr>
<td>GPIO94</td>
<td>5</td>
<td>register_name45</td>
<td>field_name94</td>
<td>Bit 30</td>
</tr>
<tr>
<td>GPIO95</td>
<td>5</td>
<td>register_name45</td>
<td>field_name95</td>
<td>Bit 31</td>
</tr>
<tr>
<td>GPIO96</td>
<td>6</td>
<td>register_name6</td>
<td>field_name96</td>
<td>Bit 0</td>
</tr>
<tr>
<td>GPIO97</td>
<td>6</td>
<td>register_name6</td>
<td>field_name97</td>
<td>Bit 1</td>
</tr>
<tr>
<td>GPIO98</td>
<td>6</td>
<td>register_name6</td>
<td>field_name98</td>
<td>Bit 2</td>
</tr>
<tr>
<td>GPIO99</td>
<td>6</td>
<td>register_name6</td>
<td>field_name99</td>
<td>Bit 3</td>
</tr>
<tr>
<td>GPIO100</td>
<td>6</td>
<td>register_name6</td>
<td>field_name100</td>
<td>Bit 4</td>
</tr>
<tr>
<td>GPIO101</td>
<td>6</td>
<td>register_name6</td>
<td>field_name101</td>
<td>Bit 5</td>
</tr>
<tr>
<td>GPIO102</td>
<td>6</td>
<td>register_name6</td>
<td>field_name102</td>
<td>Bit 6</td>
</tr>
<tr>
<td>GPIO103</td>
<td>6</td>
<td>register_name6</td>
<td>field_name103</td>
<td>Bit 7</td>
</tr>
</tbody>
</table>
2.6 **Debounce**

GPIO[7:0] feature a debounce circuit which provides the capability to filter out noise and spurious signals that occur on the input by ignoring switching that occurs faster than a selected rate. This can be useful in systems for debouncing mechanical switches, or for sampling the state of a slowly varying input.

This debounce capability is controlled by the eight DEBOUNCEn (n = 0-7) registers, one each for GPIO0-GPIO7. The DEBOUNCEn registers each contain two bit fields which control the debounce circuit - the ENABLE bit, and the INTERVAL bits. The ENABLE bit controls whether the debounce circuit for the corresponding GPIO pin is enabled or not, and the INTERVAL bits determine the duration of the debounce interval in clock cycles.

2.5.2 **Driving a GPIO Output Signal Low**

To drive a GPIO signal low, use one of the following methods:

- Write a logic 1 to the bit in CLR_DATA associated with the desired GPIO signal(s) to be driven low. Bit positions in CLR_DATA containing logic 0 do not affect the state of the associated output signals.
- Modify the bit in OUT_DATA associated with the desired GPIO signal by using a read-modify-write operation. The logic states driven on the GPIO output signals match the logic values written to all bits in OUT_DATA.

For GPIO signals configured as inputs, the values written to the associated SET_DATA, CLR_DATA, and OUT_DATA bits have no effect.

2.5 **Using a GPIO Signal as an Input**

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction register (DIR). This section describes using the GPIO signal as an input signal.

2.5.1 **Configuring a GPIO Input Signal**

To configure a given GPIO signal as an input, set the bit in DIR that is associated with the desired GPIO signal. For detailed information on DIR, see Section 3.

2.5.2 **Reading a GPIO Input Signal**

The current state of the GPIO signals is read using the GPIO input data register (IN_DATA).

- For GPIO signals configured as inputs, reading IN_DATA returns the state of the input signal synchronized to the GPIO peripheral clock.
- For GPIO signals configured as outputs, reading IN_DATA returns the output value being driven by the device.

Some signals may utilize open-drain output buffers for wired-logic operations. For open-drain GPIO signals, reading IN_DATA returns the wired-logic value on the signal (which will not be driven by the device alone). Information on any signals using open-drain outputs is available in the device data manual.

To use GPIO input signals as interrupt sources, see section Section 2.8.
Once enabled, the debounce circuit stays idle until the input in question changes state. When this occurs, a counter starts counting out the debounce interval selected, and as long as the input stays at the new state until the end of the count, the circuit will pass the new state to the rest of the GPIO logic. If the input changes state again before the end of the count, the counter is reset to zero, and starts counting again. When the debounce circuit is enabled, no input state changes are propagated to the rest of the GPIO logic unless the selected count interval has been counted. Note that this also results in a delay of the length of the interval count until any state changes are propagated to the rest of the GPIO logic. The interval counter is clocked at a rate that is 1/2 of the ARM CPU clock rate.

For more information on DEBOUNCEn register bit field definitions and memory addresses, refer to the TMS320DM335 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide (SPRUFX7).

2.7 Reset Considerations

The GPIO peripheral has two reset sources: software reset and hardware reset.

2.7.1 Software Reset Considerations

A software reset (such as a reset initiated through the emulator) does not modify the configuration and state of the GPIO signals.

2.7.2 Hardware Reset Considerations

A hardware reset does reset the GPIO configuration and data registers to their default states; therefore, affecting the configuration and state of the GPIO signals.

2.8 Interrupt Support

The GPIO peripheral can send an interrupt event to the ARM CPU.

2.8.1 Interrupt Events and Requests

A subset of the GPIO signals can also be configured to generate interrupts. The device supports interrupts from single GPIO signals, interrupts from banks of GPIO signals, or both. The interrupt mapping from the GPIO peripheral to the ARM CPU is shown in Table 2.

<table>
<thead>
<tr>
<th>Interrupt Source</th>
<th>Acronym</th>
<th>ARM Interrupt Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0</td>
<td>GPIO0</td>
<td>44</td>
</tr>
<tr>
<td>GPIO1</td>
<td>GPIO1</td>
<td>45</td>
</tr>
<tr>
<td>GPIO2</td>
<td>GPIO2</td>
<td>46</td>
</tr>
<tr>
<td>GPIO3</td>
<td>GPIO3</td>
<td>47</td>
</tr>
<tr>
<td>GPIO4</td>
<td>GPIO4</td>
<td>48</td>
</tr>
<tr>
<td>GPIO5</td>
<td>GPIO5</td>
<td>49</td>
</tr>
<tr>
<td>GPIO6</td>
<td>GPIO6</td>
<td>50</td>
</tr>
<tr>
<td>GPIO7</td>
<td>GPIO7</td>
<td>51</td>
</tr>
<tr>
<td>GPIO8</td>
<td>GPIO8</td>
<td>52</td>
</tr>
<tr>
<td>GPIO9</td>
<td>GPIO9</td>
<td>53</td>
</tr>
<tr>
<td>GPIO Bank 0</td>
<td>GPIOBNK0</td>
<td>54</td>
</tr>
<tr>
<td>GPIO Bank 1</td>
<td>GPIOBNK1</td>
<td>55</td>
</tr>
<tr>
<td>GPIO Bank 2</td>
<td>GPIOBNK2</td>
<td>56</td>
</tr>
<tr>
<td>GPIO Bank 3</td>
<td>GPIOBNK3</td>
<td>57</td>
</tr>
<tr>
<td>GPIO Bank 4</td>
<td>GPIOBNK4</td>
<td>58</td>
</tr>
<tr>
<td>GPIO Bank 5</td>
<td>GPIOBNK5</td>
<td>59</td>
</tr>
</tbody>
</table>

Table 2. GPIO Interrupts to the ARM CPU
2.8.2 Enabling GPIO Interrupt Events

GPIO interrupt events are enabled in banks of 16 by setting the appropriate bit(s) in the GPIO interrupt per-bank enable register (BINTEN). For example, to enable bank 0 interrupts (events from GPIO[15-0]), set bit 0 in BINTEN; to enable bank 3 interrupts (events from GPIO[63-48]), set bit 3 in BINTEN.

For detailed information on BINTEN, see Section 3.

---

Table 2. GPIO Interrupts to the ARM CPU (continued)

<table>
<thead>
<tr>
<th>Interrupt Source</th>
<th>Acronym</th>
<th>ARM Interrupt Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Bank 6</td>
<td>GPIOBNK6</td>
<td>60</td>
</tr>
</tbody>
</table>
2.8.3 Configuring GPIO Interrupt Edge Triggering

Each GPIO interrupt source can be configured to generate an interrupt on the GPIO signal rising edge, falling edge, both edges, or neither edge (no event). The edge detection is synchronized to the GPIO peripheral module clock.

The following four registers control the configuration of the GPIO interrupt edge detection:

- The GPIO set rising edge interrupt register (SET_RIS_TRIG) enables GPIO interrupts on the occurrence of a rising edge on the GPIO signal.
- The GPIO clear rising edge interrupt register (CLR_RIS_TRIG) disables GPIO interrupts on the occurrence of a rising edge on the GPIO signal.
- The GPIO set falling edge interrupt register (SET_FAL_TRIG) enables GPIO interrupts on the occurrence of a falling edge on the GPIO signal.
- The GPIO clear falling edge interrupt register (CLR_FAL_TRIG) disables GPIO interrupts on the occurrence of a falling edge on the GPIO signal.

To configure a GPIO interrupt to occur only on rising edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_RIS_TRIG
- Write a logic 1 to the associated bit in CLR_FAL_TRIG

To configure a GPIO interrupt to occur only on falling edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_FAL_TRIG
- Write a logic 1 to the associated bit in CLR_RIS_TRIG

To configure a GPIO interrupt to occur on both the rising and falling edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_RIS_TRIG
- Write a logic 1 to the associated bit in SET_FAL_TRIG

To disable a specific GPIO interrupt:

- Write a logic 1 to the associated bit in CLR_RIS_TRIG
- Write a logic 1 to the associated bit in CLR_FAL_TRIG

For detailed information on these registers, see Section 3.

Note that the direction of the GPIO signal does not have to be an input for the interrupt event generation to work. When a GPIO signal is configured as an output, the software can change the GPIO signal state and, in turn, generate an interrupt. This can be useful for debugging interrupt signal connectivity.

2.8.4 GPIO Interrupt Status

The status of GPIO interrupt events can be monitored by reading the GPIO interrupt status register (INTSTAT). Pending GPIO interrupts are indicated with a logic 1 in the associated bit position; interrupts that are not pending are indicated with a logic 0.

For individual GPIO interrupts that are directly routed to the ARM interrupt controller, the interrupt status can be read by reading the associated interrupt flag in the ARM interrupt controller. For the GPIO bank interrupts, INTSTAT can be used to determine which GPIO interrupt occurred. It is the responsibility of software to ensure that all pending GPIO interrupts are appropriately serviced.

Pending GPIO interrupt flags can be cleared by writing a logic 1 to the associated bit position in INTSTAT.

For detailed information on INTSTAT, see Section 3.

2.8.5 Interrupt Multiplexing

No GPIO interrupts are multiplexed with other interrupt functions on the device.
2.9 **EDMA Event Support**

The GPIO peripheral can provide synchronization events to the EDMA. The EDMA events supported on this device are listed in Table 3.

<table>
<thead>
<tr>
<th>Interrupt Source</th>
<th>EDMA Synchronization Event Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0</td>
<td>32</td>
</tr>
<tr>
<td>GPIO1</td>
<td>33</td>
</tr>
<tr>
<td>GPIO2</td>
<td>34</td>
</tr>
<tr>
<td>GPIO3</td>
<td>35</td>
</tr>
<tr>
<td>GPIO4</td>
<td>36</td>
</tr>
<tr>
<td>GPIO5</td>
<td>37</td>
</tr>
<tr>
<td>GPIO6</td>
<td>38</td>
</tr>
<tr>
<td>GPIO7</td>
<td>39</td>
</tr>
<tr>
<td>GPIO8</td>
<td>47</td>
</tr>
<tr>
<td>GPIO9</td>
<td>25</td>
</tr>
<tr>
<td>GPIO Bank 0</td>
<td>40</td>
</tr>
<tr>
<td>GPIO Bank 1</td>
<td>41</td>
</tr>
<tr>
<td>GPIO Bank 2</td>
<td>42</td>
</tr>
<tr>
<td>GPIO Bank 3</td>
<td>43</td>
</tr>
<tr>
<td>GPIO Bank 4</td>
<td>44</td>
</tr>
<tr>
<td>GPIO Bank 5</td>
<td>45</td>
</tr>
<tr>
<td>GPIO Bank 6</td>
<td>46</td>
</tr>
</tbody>
</table>

2.10 **Power Management**

The GPIO peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the GPIO peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the TMS320DM335 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide (SPRUFX7).

When the GPIO peripheral is placed in a low-power state by the PSC, the interrupt generation capability is suspended until the GPIO peripheral is removed from the low-power state. While in the low-power state, the GPIO signals configured as outputs are maintained at their state prior to the GPIO peripheral entering the low-power state.

2.11 **Emulation Considerations**

The GPIO peripheral is not affected by emulation suspend events (such as halts and breakpoints).
3 Registers

Table 4 lists the memory-mapped registers for the general-purpose input/output (GPIO). See the device-specific data manual for the memory address of these registers.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Acronym</th>
<th>Register Description</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>0h</td>
<td>PID</td>
<td>Peripheral Identification Register</td>
<td>Section 3.1</td>
</tr>
<tr>
<td>8h</td>
<td>BINTEN</td>
<td>GPIO Interrupt Per-Bank Enable Register</td>
<td>Section 3.2</td>
</tr>
<tr>
<td>10h</td>
<td>DIR01</td>
<td>GPIO Banks 0 and 1 Direction Register</td>
<td>Section 3.3</td>
</tr>
<tr>
<td>14h</td>
<td>OUT_DATA01</td>
<td>GPIO Banks 0 and 1 Output Data Register</td>
<td>Section 3.4</td>
</tr>
<tr>
<td>18h</td>
<td>SET_DATA01</td>
<td>GPIO Banks 0 and 1 Set Data Register</td>
<td>Section 3.5</td>
</tr>
<tr>
<td>1Ch</td>
<td>CLR_DATA01</td>
<td>GPIO Banks 0 and 1 Clear Data Register</td>
<td>Section 3.6</td>
</tr>
<tr>
<td>20h</td>
<td>IN_DATA01</td>
<td>GPIO Banks 0 and 1 Input Data Register</td>
<td>Section 3.7</td>
</tr>
<tr>
<td>24h</td>
<td>SET_RIS_TRIG01</td>
<td>GPIO Banks 0 and 1 Set Rising Edge Interrupt Register</td>
<td>Section 3.8</td>
</tr>
<tr>
<td>28h</td>
<td>CLR_RIS_TRIG01</td>
<td>GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register</td>
<td>Section 3.9</td>
</tr>
<tr>
<td>2Ch</td>
<td>SET_FAL_TRIG01</td>
<td>GPIO Banks 0 and 1 Set Falling Edge Interrupt Register</td>
<td>Section 3.10</td>
</tr>
<tr>
<td>30h</td>
<td>CLR_FAL_TRIG01</td>
<td>GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register</td>
<td>Section 3.11</td>
</tr>
<tr>
<td>34h</td>
<td>INSTAT01</td>
<td>GPIO Banks 0 and 1 Interrupt Status Register</td>
<td>Section 3.12</td>
</tr>
<tr>
<td>38h</td>
<td>DIR23</td>
<td>GPIO Banks 2 and 3 Direction Register</td>
<td>Section 3.3</td>
</tr>
<tr>
<td>3Ch</td>
<td>OUT_DATA23</td>
<td>GPIO Banks 2 and 3 Output Data Register</td>
<td>Section 3.4</td>
</tr>
<tr>
<td>40h</td>
<td>SET_DATA23</td>
<td>GPIO Banks 2 and 3 Set Data Register</td>
<td>Section 3.5</td>
</tr>
<tr>
<td>44h</td>
<td>CLR_DATA23</td>
<td>GPIO Banks 2 and 3 Clear Data Register</td>
<td>Section 3.6</td>
</tr>
<tr>
<td>48h</td>
<td>IN_DATA23</td>
<td>GPIO Banks 2 and 3 Input Data Register</td>
<td>Section 3.7</td>
</tr>
<tr>
<td>4Ch</td>
<td>SET_RIS_TRIG23</td>
<td>GPIO Banks 2 and 3 Set Rising Edge Interrupt Register</td>
<td>Section 3.8</td>
</tr>
<tr>
<td>50h</td>
<td>CLR_RIS_TRIG23</td>
<td>GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register</td>
<td>Section 3.9</td>
</tr>
<tr>
<td>54h</td>
<td>SET_FAL_TRIG23</td>
<td>GPIO Banks 2 and 3 Set Falling Edge Interrupt Register</td>
<td>Section 3.10</td>
</tr>
<tr>
<td>58h</td>
<td>CLR_FAL_TRIG23</td>
<td>GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register</td>
<td>Section 3.11</td>
</tr>
<tr>
<td>5Ch</td>
<td>INSTAT23</td>
<td>GPIO Banks 2 and 3 Interrupt Status Register</td>
<td>Section 3.12</td>
</tr>
<tr>
<td>60h</td>
<td>DIR45</td>
<td>GPIO Bank 4 and 5 Direction Register</td>
<td>Section 3.3</td>
</tr>
<tr>
<td>64h</td>
<td>OUT_DATA45</td>
<td>GPIO Bank 4 and 5 Output Data Register</td>
<td>Section 3.4</td>
</tr>
<tr>
<td>68h</td>
<td>SET_DATA45</td>
<td>GPIO Bank 4 and 5 Set Data Register</td>
<td>Section 3.5</td>
</tr>
<tr>
<td>6Ch</td>
<td>CLR_DATA45</td>
<td>GPIO Bank 4 and 5 Clear Data Register</td>
<td>Section 3.6</td>
</tr>
<tr>
<td>70h</td>
<td>IN_DATA45</td>
<td>GPIO Bank 4 and 5 Input Data Register</td>
<td>Section 3.7</td>
</tr>
<tr>
<td>74h</td>
<td>SET_RIS_TRIG45</td>
<td>GPIO Bank 4 and 5 Set Rising Edge Interrupt Register</td>
<td>Section 3.8</td>
</tr>
<tr>
<td>78h</td>
<td>CLR_RIS_TRIG45</td>
<td>GPIO Bank 4 and 5 Clear Rising Edge Interrupt Register</td>
<td>Section 3.9</td>
</tr>
<tr>
<td>7Ch</td>
<td>SET_FAL_TRIG45</td>
<td>GPIO Bank 4 and 5 Set Falling Edge Interrupt Register</td>
<td>Section 3.10</td>
</tr>
<tr>
<td>80h</td>
<td>CLR_FAL_TRIG45</td>
<td>GPIO Bank 4 and 5 Clear Falling Edge Interrupt Register</td>
<td>Section 3.11</td>
</tr>
<tr>
<td>84h</td>
<td>INSTAT45</td>
<td>GPIO Bank 4 and 5 Interrupt Status Register</td>
<td>Section 3.12</td>
</tr>
<tr>
<td>88h</td>
<td>DIR6</td>
<td>GPIO Bank 6 Direction Register</td>
<td>Section 3.3</td>
</tr>
<tr>
<td>8Ch</td>
<td>OUT_DATA6</td>
<td>GPIO Bank 6 Output Data Register</td>
<td>Section 3.4</td>
</tr>
<tr>
<td>90h</td>
<td>SET_DATA6</td>
<td>GPIO Bank 6 Set Data Register</td>
<td>Section 3.5</td>
</tr>
<tr>
<td>94h</td>
<td>CLR_DATA6</td>
<td>GPIO Bank 6 Clear Data Register</td>
<td>Section 3.6</td>
</tr>
<tr>
<td>98h</td>
<td>IN_DATA6</td>
<td>GPIO Bank 6 Input Data Register</td>
<td>Section 3.7</td>
</tr>
<tr>
<td>9Ch</td>
<td>SET_RIS_TRIG6</td>
<td>GPIO Bank 6 Set Rising Edge Interrupt Register</td>
<td>Section 3.8</td>
</tr>
<tr>
<td>A0h</td>
<td>CLR_RIS_TRIG6</td>
<td>GPIO Bank 6 Clear Rising Edge Interrupt Register</td>
<td>Section 3.9</td>
</tr>
</tbody>
</table>
### Table 4. General-Purpose Input/Output (GPIO) Registers (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Acronym</th>
<th>Register Description</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>A4h</td>
<td>SET_FAL_TRIG6</td>
<td>GPIO Bank 6 Set Falling Edge Interrupt Register</td>
<td>Section 3.10</td>
</tr>
<tr>
<td>A8h</td>
<td>CLR_FAL_TRIG6</td>
<td>GPIO Bank 6 Clear Falling Edge Interrupt Register</td>
<td>Section 3.11</td>
</tr>
<tr>
<td>ACh</td>
<td>INTSTAT6</td>
<td>GPIO Bank 6 Interrupt Status Register</td>
<td>Section 3.12</td>
</tr>
</tbody>
</table>
3.1 Peripheral Identification Register (PID)

The peripheral identification register (PID) contains identification data (type, class, and revision) for the peripheral. PID is shown in Figure 2 and described in Table 5.

Figure 2. Peripheral Identification Register (PID)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>Reserved</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>23-16</td>
<td>TID</td>
<td>0-Fh</td>
<td>Identifies type of peripheral.</td>
</tr>
<tr>
<td>15-8</td>
<td>CID</td>
<td>0-Fh</td>
<td>Identifies class of peripheral.</td>
</tr>
<tr>
<td>7-0</td>
<td>REV</td>
<td>0-Fh</td>
<td>Identifies revision of peripheral.</td>
</tr>
</tbody>
</table>
3.2 **GPIO Interrupt Per-Bank Enable Register (BINTEN)**

The GPIO interrupt per-bank enable register (BINTEN) is shown in Figure 3 and described in Table 6. For information on which GPIO signals are associated with each bank, see Table 1.

**Figure 3. GPIO Interrupt Per-Bank Enable Register (BINTEN)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-7</td>
<td>Reserved</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>EN6</td>
<td>0</td>
<td>Bank 6 interrupt enable is used to disable or enable the bank 6 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 6 interrupts are enabled.</td>
</tr>
<tr>
<td>5</td>
<td>EN5</td>
<td>0</td>
<td>Bank 5 interrupt enable is used to disable or enable the bank 5 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 5 interrupts are enabled.</td>
</tr>
<tr>
<td>4</td>
<td>EN4</td>
<td>0</td>
<td>Bank 4 interrupt enable is used to disable or enable the bank 4 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 4 interrupts are enabled.</td>
</tr>
<tr>
<td>3</td>
<td>EN3</td>
<td>0</td>
<td>Bank 3 interrupt enable is used to disable or enable the bank 3 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 3 interrupts are enabled.</td>
</tr>
<tr>
<td>2</td>
<td>EN2</td>
<td>0</td>
<td>Bank 2 interrupt enable is used to disable or enable the bank 2 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 2 interrupts are enabled.</td>
</tr>
<tr>
<td>1</td>
<td>EN1</td>
<td>0</td>
<td>Bank 1 interrupt enable is used to disable or enable the bank 1 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 1 interrupts are enabled.</td>
</tr>
<tr>
<td>0</td>
<td>EN0</td>
<td>0</td>
<td>Bank 0 interrupt enable is used to disable or enable the bank 0 interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Bank 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

Legend: R/W = Read/Write; R = Read only; -n = value after reset

**Table 6. GPIO Interrupt Per-Bank Enable Register (BINTEN) Field Descriptions**
3.3 GPIO Direction Registers (DIRn)

The GPIO direction register (DIRn) determines if GPIO pin n in GPIO bank I is an input or an output. Each of the GPIO banks may have up to 16 GPIO pins. By default, all the GPIO pins are configured as inputs (bit value = 1). The GPIO direction register (DIR01) is shown in Figure 4, DIR23 is shown in Figure 5, DIR45 is shown in Figure 6, DIR6 is shown in Figure 7, and described in Table 7. See Table 1 to determine the DIRn bit associated with each GPIO bank and pin number.

Figure 4. GPIO Banks 0 and 1 Direction Register (DIR01)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR31</td>
<td>DIR30</td>
<td>DIR29</td>
<td>DIR28</td>
<td>DIR27</td>
<td>DIR26</td>
<td>DIR25</td>
<td>DIR24</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR23</td>
<td>DIR22</td>
<td>DIR21</td>
<td>DIR20</td>
<td>DIR19</td>
<td>DIR18</td>
<td>DIR17</td>
<td>DIR16</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR15</td>
<td>DIR14</td>
<td>DIR13</td>
<td>DIR12</td>
<td>DIR11</td>
<td>DIR10</td>
<td>DIR9</td>
<td>DIR8</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR7</td>
<td>DIR6</td>
<td>DIR5</td>
<td>DIR4</td>
<td>DIR3</td>
<td>DIR2</td>
<td>DIR1</td>
<td>DIR0</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Figure 5. GPIO Banks 2 and 3 Direction Register (DIR23)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR63</td>
<td>DIR62</td>
<td>DIR61</td>
<td>DIR60</td>
<td>DIR59</td>
<td>DIR58</td>
<td>DIR57</td>
<td>DIR56</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR55</td>
<td>DIR54</td>
<td>DIR53</td>
<td>DIR52</td>
<td>DIR51</td>
<td>DIR50</td>
<td>DIR49</td>
<td>DIR48</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR47</td>
<td>DIR46</td>
<td>DIR45</td>
<td>DIR44</td>
<td>DIR43</td>
<td>DIR42</td>
<td>DIR41</td>
<td>DIR40</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR39</td>
<td>DIR38</td>
<td>DIR37</td>
<td>DIR36</td>
<td>DIR35</td>
<td>DIR34</td>
<td>DIR33</td>
<td>DIR32</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset
Figure 6. GPIO Banks 4 and 5 Direction Register (DIR45)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR95</td>
<td>DIR94</td>
<td>DIR93</td>
<td>DIR92</td>
<td>DIR91</td>
<td>DIR90</td>
<td>DIR89</td>
<td>DIR88</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>DIR87</td>
<td>DIR86</td>
<td>DIR85</td>
<td>DIR84</td>
<td>DIR83</td>
<td>DIR82</td>
<td>DIR81</td>
<td>DIR80</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>DIR79</td>
<td>DIR78</td>
<td>DIR77</td>
<td>DIR76</td>
<td>DIR75</td>
<td>DIR74</td>
<td>DIR73</td>
<td>DIR72</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>DIR71</td>
<td>DIR80</td>
<td>DIR69</td>
<td>DIR88</td>
<td>DIR67</td>
<td>DIR66</td>
<td>DIR65</td>
<td>DIR64</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Figure 7. GPIO Bank 6 Direction Register (DIR6)

<table>
<thead>
<tr>
<th>31</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>R-0</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>R-0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>DIR103</td>
<td>DIR102</td>
</tr>
<tr>
<td>R/W-1</td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. GPIO Direction Register (DIRn) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>DIRn</td>
<td>0</td>
<td>Direction of GPIO pin n. The DIRn bit is used to control the direction (output = 0, input = 1) of pin n on GPIO bank 2I+1. This bit field configures the GPIO pins on GPIO banks 1 and 3. GPIO pin n is an output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>GPIO pin n is an input.</td>
</tr>
<tr>
<td>15-0</td>
<td>DIRn</td>
<td>0</td>
<td>Direction of GPIO pin n. The DIRn bit is used to control the direction (output = 0, input = 1) of pin n on GPIO bank 2I. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. GPIO pin n is an output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>GPIO pin n is an input.</td>
</tr>
</tbody>
</table>
### 3.4 GPIO Output Data Register (OUT_DATA\textsubscript{n})

The GPIO output data register (OUT\_DATA\textsubscript{n}) determines the value driven on the corresponding GPIO pin \( n \) in GPIO bank \( I \), if the pin is configured as an output (DIR\( n = 0 \)). Writes do not affect pins not configured as GPIO outputs. The bits in OUT\_DATA\textsubscript{n} are set or cleared by writing directly to this register. A read of OUT\_DATA\textsubscript{n} returns the value of the register not the value at the pin (that might be configured as an input). The GPIO output data register (OUT\_DATA01) is shown in Figure 8, OUT\_DATA23 is shown in Figure 9, OUT\_DATA45 is shown in Figure 10, OUT\_DATA6 is shown in Figure 11, and described in Table 8. See Table 1 to determine the OUT\_DATA\textsubscript{n} bit associated with each GPIO bank and pin number.

**Figure 8. GPIO Banks 0 and 1 Output Data Register (OUT\_DATA01)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT31</td>
<td>OUT30</td>
<td>OUT29</td>
<td>OUT28</td>
<td>OUT27</td>
<td>OUT26</td>
<td>OUT25</td>
<td>OUT24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT23</td>
<td>OUT22</td>
<td>OUT21</td>
<td>OUT20</td>
<td>OUT19</td>
<td>OUT18</td>
<td>OUT17</td>
<td>OUT16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT15</td>
<td>OUT14</td>
<td>OUT13</td>
<td>OUT12</td>
<td>OUT11</td>
<td>OUT10</td>
<td>OUT9</td>
<td>OUT8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT7</td>
<td>OUT6</td>
<td>OUT5</td>
<td>OUT4</td>
<td>OUT3</td>
<td>OUT2</td>
<td>OUT1</td>
<td>OUT0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

**LEGEND:** R/W = Read/Write; -\( n \) = value after reset

**Figure 9. GPIO Banks 2 and 3 Output Data Register (OUT\_DATA23)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT63</td>
<td>OUT62</td>
<td>OUT61</td>
<td>OUT60</td>
<td>OUT59</td>
<td>OUT58</td>
<td>OUT57</td>
<td>OUT56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT55</td>
<td>OUT54</td>
<td>OUT53</td>
<td>OUT52</td>
<td>OUT51</td>
<td>OUT50</td>
<td>OUT49</td>
<td>OUT48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT47</td>
<td>OUT46</td>
<td>OUT45</td>
<td>OUT44</td>
<td>OUT43</td>
<td>OUT42</td>
<td>OUT41</td>
<td>OUT40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT39</td>
<td>OUT38</td>
<td>OUT37</td>
<td>OUT36</td>
<td>OUT35</td>
<td>OUT34</td>
<td>OUT33</td>
<td>OUT32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

**LEGEND:** R/W = Read/Write; -\( n \) = value after reset
### Table 8. GPIO Output Data Register (OUT\_DATA\text{n}) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>OUT\text{n}</td>
<td>0</td>
<td>Output drive state of GPIO pin \text{n}. The OUT\text{n} bit is used to drive the output (low = 0, high = 1) of pin \text{n} on GPIO bank 2/1 only when pin \text{n} is configured as an output (DIR\text{n} = 0). The OUT\text{n} bit is ignored when GPIO pin \text{n} is configured as an input. This bit field configures the GPIO pins on GPIO banks 1 and 3. GPIO pin \text{n} is driven low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>GPIO pin \text{n} is driven high.</td>
</tr>
<tr>
<td>15-0</td>
<td>OUT\text{n}</td>
<td>0</td>
<td>Output drive state of GPIO pin \text{n}. The OUT\text{n} bit is used to drive the output (low = 0, high = 1) of pin \text{n} on GPIO bank 2/1 only when pin \text{n} is configured as an output (DIR\text{n} = 0). The OUT\text{n} bit is ignored when GPIO pin \text{n} is configured as an input. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. GPIO pin \text{n} is driven low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>GPIO pin \text{n} is driven high.</td>
</tr>
</tbody>
</table>
3.5 **GPIO Set Data Register (SET_DATA\textsubscript{n})**

The GPIO set data register (SET_DATA\textsubscript{n}) controls driving high the corresponding GPIO pin \( n \) in GPIO bank \( i \), if the pin is configured as an output (DIR\( n = 0 \)). Writes do not affect pins not configured as GPIO outputs. The bits in SET_DATA\textsubscript{n} are set or cleared by writing directly to this register. A read of the SET\( n \) bit returns the output drive state of the corresponding GPIO pin \( n \). The GPIO set data register (SET_DATA\textsubscript{01}) is shown in Figure 12, SET_DATA\textsubscript{23} is shown in Figure 13, SET_DATA\textsubscript{45} is shown in Figure 14, SET_DATA\textsubscript{6} is shown in Figure 15, and described in Table 9. See Table 1 to determine the SET_DATA\textsubscript{n} bit associated with each GPIO bank and pin number.

**Figure 12. GPIO Banks 0 and 1 Set Data Register (SET_DATA\textsubscript{01})**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET31</td>
<td>SET30</td>
<td>SET29</td>
<td>SET28</td>
<td>SET27</td>
<td>SET26</td>
<td>SET25</td>
<td>SET24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>SET23</td>
<td>SET22</td>
<td>SET21</td>
<td>SET20</td>
<td>SET19</td>
<td>SET18</td>
<td>SET17</td>
<td>SET16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>SET15</td>
<td>SET14</td>
<td>SET13</td>
<td>SET12</td>
<td>SET11</td>
<td>SET10</td>
<td>SET9</td>
<td>SET8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SET7</td>
<td>SET6</td>
<td>SET5</td>
<td>SET4</td>
<td>SET3</td>
<td>SET2</td>
<td>SET1</td>
<td>SET0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \(-n\) = value after reset

**Figure 13. GPIO Banks 2 and 3 Set Data Register (SET_DATA\textsubscript{23})**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET63</td>
<td>SET62</td>
<td>SET61</td>
<td>SET60</td>
<td>SET59</td>
<td>SET58</td>
<td>SET57</td>
<td>SET56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>SET55</td>
<td>SET54</td>
<td>SET53</td>
<td>SET52</td>
<td>SET51</td>
<td>SET50</td>
<td>SET49</td>
<td>SET48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>SET47</td>
<td>SET46</td>
<td>SET45</td>
<td>SET44</td>
<td>SET43</td>
<td>SET42</td>
<td>SET41</td>
<td>SET40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SET39</td>
<td>SET38</td>
<td>SET37</td>
<td>SET36</td>
<td>SET35</td>
<td>SET34</td>
<td>SET33</td>
<td>SET32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \(-n\) = value after reset
Figure 14. GPIO Banks 4 and 5 Set Data Register (SET_DATA45)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET95</td>
<td>SET94</td>
<td>SET93</td>
<td>SET92</td>
<td>SET91</td>
<td>SET90</td>
<td>SET89</td>
<td>SET88</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET87</td>
<td>SET86</td>
<td>SET85</td>
<td>SET84</td>
<td>SET83</td>
<td>SET82</td>
<td>SET81</td>
<td>SET80</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET79</td>
<td>SET78</td>
<td>SET77</td>
<td>SET76</td>
<td>SET75</td>
<td>SET74</td>
<td>SET73</td>
<td>SET72</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET71</td>
<td>SET70</td>
<td>SET69</td>
<td>SET68</td>
<td>SET67</td>
<td>SET66</td>
<td>SET65</td>
<td>SET64</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Figure 15. GPIO Bank 6 Set Data Register (SET_DATA6)

<table>
<thead>
<tr>
<th>31</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>R-0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET103</td>
<td>SET102</td>
<td>SET101</td>
<td>SET100</td>
<td>SET99</td>
<td>SET98</td>
<td>SET97</td>
<td>SET96</td>
</tr>
<tr>
<td>R/W-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. GPIO Set Data Register (SET_DATA$n$) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>SET$n$</td>
<td>0</td>
<td>Set output drive state of GPIO pin n. The SET$n$ bit is used to set the output of pin n on GPIO bank 2/$i$ + 1 only when pin $n$ is configured as an output (DIR$n$ = 0). The SET$n$ bit is ignored when GPIO pin $n$ is configured as an input. Writing a 1 to the SET$n$ bit sets the output drive state of the corresponding GPIO pin $n$; reading the SET$n$ bit returns the output drive state of the corresponding GPIO pin $n$. This bit field configures the GPIO pins on GPIO banks 1 and 3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>No effect; Set GPIO pin $n$ output to 1.</td>
</tr>
<tr>
<td>15-0</td>
<td>SET$n$</td>
<td>0</td>
<td>Set output drive state of GPIO pin n. The SET$n$ bit is used to set the output of pin n on GPIO bank 2/$i$ only when pin $n$ is configured as an output (DIR$n$ = 0). The SET$n$ bit is ignored when GPIO pin $n$ is configured as an input. Writing a 1 to the SET$n$ bit sets the output drive state of the corresponding GPIO pin $n$; reading the SET$n$ bit returns the output drive state of the corresponding GPIO pin $n$. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>No effect; Set GPIO pin $n$ output to 1.</td>
</tr>
</tbody>
</table>
### 3.6 GPIO Clear Data Register (CLR_DATA\text{n})

The GPIO clear data register (CLR\_DATA\text{n}) controls driving low the corresponding GPIO pin \text{n} in GPIO bank \text{i}, if the pin is configured as an output (DIR\text{n} = 0). Writes do not affect pins not configured as GPIO outputs. The bits in CLR\_DATA\text{n} are set or cleared by writing directly to this register. A read of the CLR\text{n} bit returns the output drive state of the corresponding GPIO pin \text{n}. The GPIO clear data register (CLR\_DATA01) is shown in Figure 16, CLR\_DATA23 is shown in Figure 17, CLR\_DATA45 is shown in Figure 18 CLR\_DATA6 is shown in Figure 19, and described in Table 10. See Table 1 to determine the CLR\_DATA\text{n} bit associated with each GPIO bank and pin number.

#### Figure 16. GPIO Banks 0 and 1 Clear Data Register (CLR\_DATA01)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR31</td>
<td>CLR30</td>
<td>CLR29</td>
<td>CLR28</td>
<td>CLR27</td>
<td>CLR26</td>
<td>CLR25</td>
<td>CLR24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR23</td>
<td>CLR22</td>
<td>CLR21</td>
<td>CLR20</td>
<td>CLR19</td>
<td>CLR18</td>
<td>CLR17</td>
<td>CLR16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR15</td>
<td>CLR14</td>
<td>CLR13</td>
<td>CLR12</td>
<td>CLR11</td>
<td>CLR10</td>
<td>CLR9</td>
<td>CLR8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR7</td>
<td>CLR6</td>
<td>CLR5</td>
<td>CLR4</td>
<td>CLR3</td>
<td>CLR2</td>
<td>CLR1</td>
<td>CLR0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

**LEGEND:** \( R/W \) = Read/Write; \( -n \) = value after reset

#### Figure 17. GPIO Banks 2 and 3 Clear Data Register (CLR\_DATA23)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR63</td>
<td>CLR62</td>
<td>CLR61</td>
<td>CLR60</td>
<td>CLR59</td>
<td>CLR58</td>
<td>CLR57</td>
<td>CLR56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR55</td>
<td>CLR54</td>
<td>CLR53</td>
<td>CLR52</td>
<td>CLR51</td>
<td>CLR50</td>
<td>CLR49</td>
<td>CLR48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR47</td>
<td>CLR46</td>
<td>CLR45</td>
<td>CLR44</td>
<td>CLR43</td>
<td>CLR42</td>
<td>CLR41</td>
<td>CLR40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR39</td>
<td>CLR38</td>
<td>CLR37</td>
<td>CLR36</td>
<td>CLR35</td>
<td>CLR34</td>
<td>CLR33</td>
<td>CLR32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

**LEGEND:** \( R/W \) = Read/Write; \( -n \) = value after reset
**Figure 18. GPIO Banks 4 and 5 Clear Data Register (CLR_DATA45)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR95</td>
<td>CLR94</td>
<td>CLR93</td>
<td>CLR92</td>
<td>CLR91</td>
<td>CLR90</td>
<td>CLR89</td>
<td>CLR88</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>CLR87</td>
<td>CLR86</td>
<td>CLR85</td>
<td>CLR84</td>
<td>CLR83</td>
<td>CLR82</td>
<td>CLR81</td>
<td>CLR80</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>CLR79</td>
<td>CLR78</td>
<td>CLR77</td>
<td>CLR76</td>
<td>CLR75</td>
<td>CLR74</td>
<td>CLR73</td>
<td>CLR72</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLR71</td>
<td>CLR70</td>
<td>CLR69</td>
<td>CLR68</td>
<td>CLR67</td>
<td>CLR66</td>
<td>CLR65</td>
<td>CLR64</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \( \cdot n \) = value after reset

**Figure 19. GPIO Bank 6 Clear Data Register (CLR_DATA6)**

<table>
<thead>
<tr>
<th>31</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>R-0</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>R-0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>CLR103</td>
<td>CLR102</td>
</tr>
<tr>
<td>R/W-0</td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; \( \cdot n \) = value after reset

**Table 10. GPIO Clear Data Register (CLR_DATA\( n \)) Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>CLR( n )</td>
<td>0</td>
<td>Clear output drive state of GPIO pin ( n ). The CLR( n ) bit is used to clear the output of pin ( n ) on GPIO bank 2/ + 1 only when pin ( n ) is configured as an output (DIR( n ) = 0). The CLR( n ) bit is ignored when GPIO pin ( n ) is configured as an input. Writing a 1 to the CLR( n ) bit clears the output drive state of the corresponding GPIO pin ( n ); reading the CLR( n ) bit returns the output drive state of the corresponding GPIO pin ( n ). This bit field configures the GPIO pins on GPIO banks 1 and 3.</td>
</tr>
<tr>
<td>1</td>
<td>No effect.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clear GPIO pin ( n ) output to 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15-0</td>
<td>CLR( n )</td>
<td>0</td>
<td>Clear output drive state of GPIO pin ( n ). The CLR( n ) bit is used to clear the output of pin ( n ) on GPIO bank 2/ only when pin ( n ) is configured as an output (DIR( n ) = 0). The CLR( n ) bit is ignored when GPIO pin ( n ) is configured as an input. Writing a 1 to the CLR( n ) bit clears the output drive state of the corresponding GPIO pin ( n ); reading the CLR( n ) bit returns the output drive state of the corresponding GPIO pin ( n ). This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.</td>
</tr>
<tr>
<td></td>
<td>No effect.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clear GPIO pin ( n ) output to 0.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3.7 **GPIO Input Data Register (IN_DATA\textsubscript{n})**

The current state of the GPIO signals is read using the GPIO input data register (IN_DATA\textsubscript{n}).

- For GPIO signals configured as inputs, reading IN_DATA\textsubscript{n} returns the state of the input signal synchronized to the GPIO peripheral clock.
- For GPIO signals configured as outputs, reading IN_DATA\textsubscript{n} returns the output value being driven by the device.

The GPIO input data register (IN_DATA01) is shown in Figure 20, IN_DATA23 is shown in Figure 21, IN_DATA45 is shown in Figure 22, IN_DATA6 is shown in Figure 23, and described in Table 11. See Table 1 to determine the IN_DATA\textsubscript{n} bit associated with each GPIO bank and pin number.

**Figure 20. GPIO Banks 0 and 1 Input Data Register (IN_DATA01)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN31</td>
<td>IN30</td>
<td>IN29</td>
<td>IN28</td>
<td>IN27</td>
<td>IN26</td>
<td>IN25</td>
<td>IN24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>IN23</td>
<td>IN22</td>
<td>IN21</td>
<td>IN20</td>
<td>IN19</td>
<td>IN18</td>
<td>IN17</td>
<td>IN16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>IN15</td>
<td>IN14</td>
<td>IN13</td>
<td>IN12</td>
<td>IN11</td>
<td>IN10</td>
<td>IN9</td>
<td>IN8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>IN7</td>
<td>IN6</td>
<td>IN5</td>
<td>IN4</td>
<td>IN3</td>
<td>IN2</td>
<td>IN1</td>
<td>IN0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \( -n \) = value after reset

**Figure 21. GPIO Banks 2 and 3 Input Data Register (IN_DATA23)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN63</td>
<td>IN62</td>
<td>IN61</td>
<td>IN60</td>
<td>IN59</td>
<td>IN58</td>
<td>IN57</td>
<td>IN56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>IN55</td>
<td>IN54</td>
<td>IN53</td>
<td>IN52</td>
<td>IN51</td>
<td>IN50</td>
<td>IN49</td>
<td>IN48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>IN47</td>
<td>IN46</td>
<td>IN45</td>
<td>IN44</td>
<td>IN43</td>
<td>IN42</td>
<td>IN41</td>
<td>IN40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>IN39</td>
<td>IN38</td>
<td>IN37</td>
<td>IN36</td>
<td>IN35</td>
<td>IN34</td>
<td>IN33</td>
<td>IN32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \( -n \) = value after reset
Figure 22. GPIO Banks 4 and 5 Input Data Register (IN_DATA45)

<table>
<thead>
<tr>
<th>Bit</th>
<th>IN95</th>
<th>IN94</th>
<th>IN93</th>
<th>IN92</th>
<th>IN91</th>
<th>IN90</th>
<th>IN89</th>
<th>IN88</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>IN87</td>
<td>IN86</td>
<td>IN85</td>
<td>IN84</td>
<td>IN83</td>
<td>IN82</td>
<td>IN81</td>
<td>IN80</td>
</tr>
<tr>
<td></td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>IN79</td>
<td>IN78</td>
<td>IN77</td>
<td>IN76</td>
<td>IN75</td>
<td>IN74</td>
<td>IN73</td>
<td>IN72</td>
</tr>
<tr>
<td></td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>IN71</td>
<td>IN70</td>
<td>IN69</td>
<td>IN68</td>
<td>IN67</td>
<td>IN66</td>
<td>IN65</td>
<td>IN64</td>
</tr>
<tr>
<td></td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \( n \) = value after reset

Figure 23. GPIO Bank 6 Input Data Register (IN_DATA6)

<table>
<thead>
<tr>
<th>Bit</th>
<th>IN103</th>
<th>IN102</th>
<th>IN101</th>
<th>IN100</th>
<th>IN99</th>
<th>IN98</th>
<th>IN97</th>
<th>IN96</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; \( n \) = value after reset

Table 11. GPIO Input Data Register (IN_DATA\( n \)) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>IN( n )</td>
<td>0</td>
<td>Status of GPIO pin ( n ). Reading the IN( n ) bit returns the state of pin ( n ) on GPIO bank ( 2I + 1 ). This bit field returns the status of the GPIO pins on GPIO banks 1 and 3. GPIO pin ( n ) is logic low.</td>
</tr>
<tr>
<td>31-16</td>
<td>IN( n )</td>
<td>1</td>
<td>GPIO pin ( n ) is logic high.</td>
</tr>
<tr>
<td>15-0</td>
<td>IN( n )</td>
<td>0</td>
<td>Status of GPIO pin ( n ). Reading the IN( n ) bit returns the state of pin ( n ) on GPIO bank ( 2I ). This bit field returns the status of the GPIO pins on GPIO banks 0, 2 and 4. GPIO pin ( n ) is logic low.</td>
</tr>
<tr>
<td>15-0</td>
<td>IN( n )</td>
<td>1</td>
<td>GPIO pin ( n ) is logic high.</td>
</tr>
</tbody>
</table>
3.8 GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIGn)

The GPIO set rising edge interrupt register (SET_RIS_TRIGn) enables a rising edge on the GPIO pin to generate a GPIO interrupt. The GPIO set rising edge interrupt register (SET_RIS_TRIG01) is shown in Figure 24, SET_RIS_TRIG23 is shown in Figure 25, SET_RIS_TRIG45 is shown in Figure 26, SET_RIS_TRIG6 is shown in Figure 27, and described in Table 12. See Table 1 to determine the SET_RIS_TRIGn bit associated with each GPIO bank and pin number.

**Figure 24. GPIO Banks 0 and 1 Set Rising Edge Interrupt Register (SET_RIS_TRIG01)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS31</td>
<td>SETRIS30</td>
<td>SETRIS29</td>
<td>SETRIS28</td>
<td>SETRIS27</td>
<td>SETRIS26</td>
<td>SETRIS25</td>
<td>SETRIS24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS23</td>
<td>SETRIS22</td>
<td>SETRIS21</td>
<td>SETRIS20</td>
<td>SETRIS19</td>
<td>SETRIS18</td>
<td>SETRIS17</td>
<td>SETRIS16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS15</td>
<td>SETRIS14</td>
<td>SETRIS13</td>
<td>SETRIS12</td>
<td>SETRIS11</td>
<td>SETRIS10</td>
<td>SETRIS9</td>
<td>SETRIS8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS7</td>
<td>SETRIS6</td>
<td>SETRIS5</td>
<td>SETRIS4</td>
<td>SETRIS3</td>
<td>SETRIS2</td>
<td>SETRIS1</td>
<td>SETRIS0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \( -n \) = value after reset

**Figure 25. GPIO Banks 2 and 3 Set Rising Edge Interrupt Register (SET_RIS_TRIG23)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS63</td>
<td>SETRIS62</td>
<td>SETRIS61</td>
<td>SETRIS60</td>
<td>SETRIS59</td>
<td>SETRIS58</td>
<td>SETRIS57</td>
<td>SETRIS56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS55</td>
<td>SETRIS54</td>
<td>SETRIS53</td>
<td>SETRIS52</td>
<td>SETRIS51</td>
<td>SETRIS50</td>
<td>SETRIS49</td>
<td>SETRIS48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS47</td>
<td>SETRIS46</td>
<td>SETRIS45</td>
<td>SETRIS44</td>
<td>SETRIS43</td>
<td>SETRIS42</td>
<td>SETRIS41</td>
<td>SETRIS40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETRIS39</td>
<td>SETRIS38</td>
<td>SETRIS37</td>
<td>SETRIS36</td>
<td>SETRIS35</td>
<td>SETRIS34</td>
<td>SETRIS33</td>
<td>SETRIS32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \( -n \) = value after reset
Figure 26. GPIO Banks 4 and 5 Set Rising Edge Interrupt Register (SET_RIS_TRIG45)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>SETRISn</td>
<td></td>
<td>Enable rising edge interrupt detection on GPIO pin n. Reading the SETRISn bit returns the state of pin n on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. No effect. Interrupt is caused by a low-to-high transition on GPIO pin n.</td>
</tr>
</tbody>
</table>

Figure 27. GPIO Bank 6 Set Rising Edge Interrupt Register (SET_RIS_TRIG6)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-0</td>
<td>SETRISn</td>
<td></td>
<td>Enable rising edge interrupt detection on GPIO pin n. Reading the SETRISn bit returns the state of pin n on GPIO bank 2I. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. No effect. Interrupt is caused by a low-to-high transition on GPIO pin n.</td>
</tr>
</tbody>
</table>

Table 12. GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIGn) Field Descriptions
3.9 GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGn)

The GPIO clear rising edge interrupt register (CLR_RIS_TRIGn) disables a rising edge on the GPIO pin from generating a GPIO interrupt. The GPIO clear rising edge interrupt register (CLR_RIS_TRIG01) is shown in Figure 28, CLR_RIS_TRIG23 is shown in Figure 29, CLR_RIS_TRIG45 is shown in Figure 30, CLR_RIS_TRIG6 is shown in Figure 31, and described in Table 13. See Table 1 to determine the CLR_RIS_TRIGn bit associated with each GPIO bank and pin number.

Figure 28. GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG01)

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>CLR_RIS31</td>
<td>CLR_RIS30</td>
<td>CLR_RIS29</td>
<td>CLR_RIS28</td>
<td>CLR_RIS27</td>
<td>CLR_RIS26</td>
<td>CLR_RIS25</td>
<td>CLR_RIS24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>CLR_RIS23</td>
<td>CLR_RIS22</td>
<td>CLR_RIS21</td>
<td>CLR_RIS20</td>
<td>CLR_RIS19</td>
<td>CLR_RIS18</td>
<td>CLR_RIS17</td>
<td>CLR_RIS16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>CLR_RIS15</td>
<td>CLR_RIS14</td>
<td>CLR_RIS13</td>
<td>CLR_RIS12</td>
<td>CLR_RIS11</td>
<td>CLR_RIS10</td>
<td>CLR_RIS9</td>
<td>CLR_RIS8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLR_RIS7</td>
<td>CLR_RIS6</td>
<td>CLR_RIS5</td>
<td>CLR_RIS4</td>
<td>CLR_RIS3</td>
<td>CLR_RIS2</td>
<td>CLR_RIS1</td>
<td>CLR_RIS0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Figure 29. GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG23)

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>CLR_RIS63</td>
<td>CLR_RIS62</td>
<td>CLR_RIS61</td>
<td>CLR_RIS60</td>
<td>CLR_RIS59</td>
<td>CLR_RIS58</td>
<td>CLR_RIS57</td>
<td>CLR_RIS56</td>
</tr>
<tr>
<td>R/W-10</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>CLR_RIS55</td>
<td>CLR_RIS54</td>
<td>CLR_RIS53</td>
<td>CLR_RIS52</td>
<td>CLR_RIS51</td>
<td>CLR_RIS50</td>
<td>CLR_RIS49</td>
<td>CLR_RIS48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>CLR_RIS47</td>
<td>CLR_RIS46</td>
<td>CLR_RIS45</td>
<td>CLR_RIS44</td>
<td>CLR_RIS43</td>
<td>CLR_RIS42</td>
<td>CLR_RIS41</td>
<td>CLR_RIS40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLR_RIS39</td>
<td>CLR_RIS38</td>
<td>CLR_RIS37</td>
<td>CLR_RIS36</td>
<td>CLR_RIS35</td>
<td>CLR_RIS34</td>
<td>CLR_RIS33</td>
<td>CLR_RIS32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset
### Figure 30. GPIO Banks 4 and 5 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG45)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>CLRRIS95</td>
<td>R/W-0</td>
<td>Clear rising edge interrupt detection on GPIO pin 95. Reading the CLRRIS95 bit returns the complement state of pin 95 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 95.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS94</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 94. Reading the CLRRIS94 bit returns the complement state of pin 94 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 94.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS93</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 93. Reading the CLRRIS93 bit returns the complement state of pin 93 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 93.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS92</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 92. Reading the CLRRIS92 bit returns the complement state of pin 92 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 92.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS91</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 91. Reading the CLRRIS91 bit returns the complement state of pin 91 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 91.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS90</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 90. Reading the CLRRIS90 bit returns the complement state of pin 90 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 90.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS89</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 89. Reading the CLRRIS89 bit returns the complement state of pin 89 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 89.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS88</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 88. Reading the CLRRIS88 bit returns the complement state of pin 88 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 88.</td>
</tr>
</tbody>
</table>

### Figure 31. GPIO Bank 6 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG6)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved</td>
<td>R-0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reserved</td>
<td>R-0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>CLRRIS71</td>
<td>R/W-0</td>
<td>Clear rising edge interrupt detection on GPIO pin 71. Reading the CLRRIS71 bit returns the complement state of pin 71 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 71.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS70</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 70. Reading the CLRRIS70 bit returns the complement state of pin 70 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 70.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS69</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 69. Reading the CLRRIS69 bit returns the complement state of pin 69 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 69.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS68</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 68. Reading the CLRRIS68 bit returns the complement state of pin 68 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 68.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS67</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 67. Reading the CLRRIS67 bit returns the complement state of pin 67 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 67.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS66</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 66. Reading the CLRRIS66 bit returns the complement state of pin 66 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 66.</td>
</tr>
<tr>
<td></td>
<td>CLRRIS65</td>
<td>R/W-0</td>
<td>Disable rising edge interrupt detection on GPIO pin 65. Reading the CLRRIS65 bit returns the complement state of pin 65 on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin 65.</td>
</tr>
</tbody>
</table>

### Table 13. GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGn) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>CLRRISn</td>
<td>0</td>
<td>Disable rising edge interrupt detection on GPIO pin n. Reading the CLRRISn bit returns the complement state of pin n on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin n.</td>
</tr>
<tr>
<td></td>
<td>CLRRISn</td>
<td>1</td>
<td>Disable rising edge interrupt detection on GPIO pin n. Reading the CLRRISn bit returns the complement state of pin n on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin n.</td>
</tr>
<tr>
<td>15-0</td>
<td>CLRRISn</td>
<td>0</td>
<td>Disable rising edge interrupt detection on GPIO pin n. Reading the CLRRISn bit returns the complement state of pin n on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin n.</td>
</tr>
<tr>
<td></td>
<td>CLRRISn</td>
<td>1</td>
<td>Disable rising edge interrupt detection on GPIO pin n. Reading the CLRRISn bit returns the complement state of pin n on GPIO bank 2I + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. 0: No effect. 1: No interrupt is caused by a low-to-high transition on GPIO pin n.</td>
</tr>
</tbody>
</table>
3.10 GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIGN)

The GPIO set falling edge interrupt register (SET_FAL_TRIGN) enables a falling edge on the GPIO pin to generate a GPIO interrupt. The GPIO set falling edge interrupt register (SET_FAL_TRIG01) is shown in Figure 32, SET_FAL_TRIG23 is shown in Figure 33, SET_FAL_TRIG45 is shown in Figure 34, SET_FAL_TRIG6 is shown in Figure 35, and described in Table 14. See Table 1 to determine the SET_FAL_TRIGN bit associated with each GPIO bank and pin number.

Figure 32. GPIO Banks 0 and 1 Set Falling Edge Interrupt Register (SET_FAL_TRIG01)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETFAL31</td>
<td>SETFAL30</td>
<td>SETFAL29</td>
<td>SETFAL28</td>
<td>SETFAL27</td>
<td>SETFAL26</td>
<td>SETFAL25</td>
<td>SETFAL24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>SETFAL23</td>
<td>SETFAL22</td>
<td>SETFAL21</td>
<td>SETFAL20</td>
<td>SETFAL19</td>
<td>SETFAL18</td>
<td>SETFAL17</td>
<td>SETFAL16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>SETFAL15</td>
<td>SETFAL14</td>
<td>SETFAL13</td>
<td>SETFAL12</td>
<td>SETFAL11</td>
<td>SETFAL10</td>
<td>SETFAL9</td>
<td>SETFAL8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SETFAL7</td>
<td>SETFAL6</td>
<td>SETFAL5</td>
<td>SETFAL4</td>
<td>SETFAL3</td>
<td>SETFAL2</td>
<td>SETFAL1</td>
<td>SETFAL0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Figure 33. GPIO Banks 2 and 3 Set Falling Edge Interrupt Register (SET_FAL_TRIG23)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>SETFAL63</td>
<td>SETFAL62</td>
<td>SETFAL61</td>
<td>SETFAL60</td>
<td>SETFAL59</td>
<td>SETFAL58</td>
<td>SETFAL57</td>
<td>SETFAL56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>SETFAL55</td>
<td>SETFAL54</td>
<td>SETFAL53</td>
<td>SETFAL52</td>
<td>SETFAL51</td>
<td>SETFAL50</td>
<td>SETFAL49</td>
<td>SETFAL48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>SETFAL47</td>
<td>SETFAL46</td>
<td>SETFAL45</td>
<td>SETFAL44</td>
<td>SETFAL43</td>
<td>SETFAL42</td>
<td>SETFAL41</td>
<td>SETFAL40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SETFAL39</td>
<td>SETFAL38</td>
<td>SETFAL37</td>
<td>SETFAL36</td>
<td>SETFAL35</td>
<td>SETFAL34</td>
<td>SETFAL33</td>
<td>SETFAL32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; -n = value after reset
Figure 34. GPIO Banks 4 and 5 Set Falling Edge Interrupt Register (SET_FAL_TRIG45)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>SETFALn</td>
<td>Enable falling edge interrupt detection on GPIO pin n. Reading the SETFALn bit returns the state of pin n on GPIO bank 2 + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. No effect. Interrupt is caused by a high-to-low transition on GPIO pin n.</td>
</tr>
<tr>
<td>15-0</td>
<td>SETFALn</td>
<td>Enable falling edge interrupt detection on GPIO pin n. Reading the SETFALn bit returns the state of pin n on GPIO bank 2I. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. No effect. Interrupt is caused by a high-to-low transition on GPIO pin n.</td>
</tr>
</tbody>
</table>

Figure 35. GPIO Bank 6 Set Falling Edge Interrupt Register (SET_FAL_TRIG6)

Table 14. GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIGn) Field Descriptions
3.11 GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIGn)

The GPIO clear falling edge interrupt register (CLR_FAL_TRIGn) disables a falling edge on the GPIO pin from generating a GPIO interrupt. The GPIO clear falling edge interrupt register (CLR_FAL_TRIG01) is shown in Figure 36, CLR_FAL_TRIG23 is shown in Figure 37, CLR_FAL_TRIG45 is shown in Figure 38, CLR_FAL_TRIG6 is shown in Figure 39, and described in Table 15. See Table 1 to determine the CLR_FAL_TRIGn bit associated with each GPIO bank and pin number.

**Figure 36. GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG01)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRFAL31</td>
<td>CLRFAL30</td>
<td>CLRFAL29</td>
<td>CLRFAL28</td>
<td>CLRFAL27</td>
<td>CLRFAL26</td>
<td>CLRFAL25</td>
<td>CLRFAL24</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>CLRFAL23</td>
<td>CLRFAL22</td>
<td>CLRFAL21</td>
<td>CLRFAL20</td>
<td>CLRFAL19</td>
<td>CLRFAL18</td>
<td>CLRFAL17</td>
<td>CLRFAL16</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>CLRFAL15</td>
<td>CLRFAL14</td>
<td>CLRFAL13</td>
<td>CLRFAL12</td>
<td>CLRFAL11</td>
<td>CLRFAL10</td>
<td>CLRFAL9</td>
<td>CLRFAL8</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLRFAL7</td>
<td>CLRFAL6</td>
<td>CLRFAL5</td>
<td>CLRFAL4</td>
<td>CLRFAL3</td>
<td>CLRFAL2</td>
<td>CLRFAL1</td>
<td>CLRFAL0</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \(-n\) = value after reset

**Figure 37. GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG23)**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRFAL63</td>
<td>CLRFAL62</td>
<td>CLRFAL61</td>
<td>CLRFAL60</td>
<td>CLRFAL59</td>
<td>CLRFAL58</td>
<td>CLRFAL57</td>
<td>CLRFAL56</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>CLRFAL55</td>
<td>CLRFAL54</td>
<td>CLRFAL53</td>
<td>CLRFAL52</td>
<td>CLRFAL51</td>
<td>CLRFAL50</td>
<td>CLRFAL49</td>
<td>CLRFAL48</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>CLRFAL47</td>
<td>CLRFAL46</td>
<td>CLRFAL45</td>
<td>CLRFAL44</td>
<td>CLRFAL43</td>
<td>CLRFAL42</td>
<td>CLRFAL41</td>
<td>CLRFAL40</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLRFAL39</td>
<td>CLRFAL38</td>
<td>CLRFAL37</td>
<td>CLRFAL36</td>
<td>CLRFAL35</td>
<td>CLRFAL34</td>
<td>CLRFAL33</td>
<td>CLRFAL32</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; \(-n\) = value after reset
Figure 38. GPIO Banks 4 and 5 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG45)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRFAL95</td>
<td>CLRFAL94</td>
<td>CLRFAL93</td>
<td>CLRFAL92</td>
<td>CLRFAL91</td>
<td>CLRFAL90</td>
<td>CLRFAL89</td>
<td>CLRFAL88</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>CLRFAL87</td>
<td>CLRFAL86</td>
<td>CLRFAL85</td>
<td>CLRFAL84</td>
<td>CLRFAL83</td>
<td>CLRFAL82</td>
<td>CLRFAL81</td>
<td>CLRFAL80</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>CLRFAL79</td>
<td>CLRFAL78</td>
<td>CLRFAL77</td>
<td>CLRFAL76</td>
<td>CLRFAL75</td>
<td>CLRFAL74</td>
<td>CLRFAL73</td>
<td>CLRFAL72</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLRFAL71</td>
<td>CLRFAL70</td>
<td>CLRFAL69</td>
<td>CLRFAL68</td>
<td>CLRFAL67</td>
<td>CLRFAL66</td>
<td>CLRFAL65</td>
<td>CLRFAL64</td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; _n = value after reset

Figure 39. GPIO Bank 6 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG6)

<table>
<thead>
<tr>
<th>31</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reserved R-0</td>
</tr>
<tr>
<td>15</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Reserved R-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

| CLRFAL103 | CLRFAL102 | CLRFAL101 | CLRFAL100 | CLRFAL99 | CLRFAL98 | CLRFAL97 | CLRFAL96 |
| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; _n = value after reset

Table 15. GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIGn) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>CLRFALn</td>
<td>0</td>
<td>Disable falling edge interrupt detection on GPIO pin n. Reading the CLRFALn bit returns the complement state of pin n on GPIO bank 2/ + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3.</td>
</tr>
<tr>
<td>31-16</td>
<td>CLRFALn</td>
<td>1</td>
<td>No interrupt is caused by a high-to-low transition on GPIO pin n.</td>
</tr>
<tr>
<td>15-0</td>
<td>CLRFALn</td>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td>15-0</td>
<td>CLRFALn</td>
<td>1</td>
<td>Disable falling edge interrupt detection on GPIO pin n. Reading the CLRFALn bit returns the complement state of pin n on GPIO bank 2/ + 4. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.</td>
</tr>
<tr>
<td>15-0</td>
<td>CLRFALn</td>
<td>1</td>
<td>No interrupt is caused by a high-to-low transition on GPIO pin n.</td>
</tr>
</tbody>
</table>
3.12 **GPIO Interrupt Status Register (INTSTATn)**

The status of GPIO interrupt events can be monitored by reading the GPIO interrupt status register (INTSTATn). In the associated bit position, pending GPIO interrupts are indicated with a logic 1 and GPIO interrupts that are not pending are indicated with a logic 0. The GPIO interrupt status register (INTSTAT01) is shown in **Figure 40**, INTSTAT23 is shown in **Figure 41**, INTSTAT45 is shown in **Figure 42**, INTSTAT6 is shown in **Figure 43**, and described in Table 16. See Table 1 to determine the INTSTATn bit associated with each GPIO bank and pin number.

### Figure 40. GPIO Banks 0 and 1 Interrupt Status Register (INTSTAT01)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAT31</td>
<td>STAT30</td>
<td>STAT29</td>
<td>STAT28</td>
<td>STAT27</td>
<td>STAT26</td>
<td>STAT25</td>
<td>STAT24</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>STAT23</td>
<td>STAT22</td>
<td>STAT21</td>
<td>STAT20</td>
<td>STAT19</td>
<td>STAT18</td>
<td>STAT17</td>
<td>STAT16</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>STAT15</td>
<td>STAT14</td>
<td>STAT13</td>
<td>STAT12</td>
<td>STAT11</td>
<td>STAT10</td>
<td>STAT9</td>
<td>STAT8</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>STAT7</td>
<td>STAT6</td>
<td>STATSTAT5</td>
<td>STAT4</td>
<td>STAT3</td>
<td>STAT2</td>
<td>STAT1</td>
<td>STAT0</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; W1C = Write 1 to clear bit (writing 0 has no effect); -n = value after reset

### Figure 41. GPIO Banks 2 and 3 Interrupt Status Register (INTSTAT23)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAT63</td>
<td>STAT62</td>
<td>STAT61</td>
<td>STAT60</td>
<td>STAT59</td>
<td>STAT58</td>
<td>STAT57</td>
<td>STAT56</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>STAT55</td>
<td>STAT54</td>
<td>STAT53</td>
<td>STAT52</td>
<td>STAT51</td>
<td>STAT50</td>
<td>STAT49</td>
<td>STAT48</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>STAT47</td>
<td>STAT46</td>
<td>STATSTAT45</td>
<td>STAT44</td>
<td>STAT43</td>
<td>STAT42</td>
<td>STAT41</td>
<td>STAT40</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>STAT39</td>
<td>STAT38</td>
<td>STAT37</td>
<td>STAT36</td>
<td>STAT35</td>
<td>STAT34</td>
<td>STAT33</td>
<td>STAT32</td>
</tr>
<tr>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
<td>R/W1C-0</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; W1C = Write 1 to clear bit (writing 0 has no effect); -n = value after reset
Figure 42. GPIO Banks 4 and 5 Interrupt Status Register (INTSTAT45)

<table>
<thead>
<tr>
<th>Bit</th>
<th>STAT95</th>
<th>STAT94</th>
<th>STAT93</th>
<th>STAT92</th>
<th>STAT91</th>
<th>STAT90</th>
<th>STAT89</th>
<th>STAT88</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 43. GPIO Bank 6 Interrupt Status Register (INTSTAT6)

<table>
<thead>
<tr>
<th>Bit</th>
<th>STAT95</th>
<th>STAT94</th>
<th>STAT93</th>
<th>STAT92</th>
<th>STAT91</th>
<th>STAT90</th>
<th>STAT89</th>
<th>STAT88</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 16. GPIO Interrupt Status Register (INTSTATn) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>STATn</td>
<td>0</td>
<td>No pending interrupt on GPIO pin n.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Pending interrupt on GPIO pin n.</td>
</tr>
<tr>
<td>15-0</td>
<td>STATn</td>
<td>0</td>
<td>No pending interrupt on GPIO pin n.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Pending interrupt on GPIO pin n.</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to test the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>Audio</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Automotive</td>
</tr>
<tr>
<td>DSP</td>
<td>Broadband</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td>Digital Control</td>
</tr>
<tr>
<td>Interface</td>
<td>Medical</td>
</tr>
<tr>
<td>Logic</td>
<td>Military</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Optical Networking</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Security</td>
</tr>
<tr>
<td>RFID</td>
<td>Telephony</td>
</tr>
<tr>
<td>RF/IF and ZigBee® Solutions</td>
<td>Video &amp; Imaging</td>
</tr>
<tr>
<td></td>
<td>Wireless</td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated