## Contents

### Preface

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Purpose of the Peripheral</td>
<td>12</td>
</tr>
<tr>
<td>1.2 Features</td>
<td>12</td>
</tr>
<tr>
<td>1.3 Industry Standard(s) Compliance Statement</td>
<td>12</td>
</tr>
<tr>
<td>2.19 Performance Monitoring</td>
<td>30</td>
</tr>
<tr>
<td>2.16 ECC</td>
<td>30</td>
</tr>
<tr>
<td>2.15 Emulation Considerations</td>
<td>30</td>
</tr>
<tr>
<td>2.14 EDMA Event Support</td>
<td>30</td>
</tr>
<tr>
<td>2.13 Interrupt Support</td>
<td>30</td>
</tr>
<tr>
<td>2.12 Leveling</td>
<td>30</td>
</tr>
<tr>
<td>2.11 DDR3 SDRAM Memory Initialization</td>
<td>30</td>
</tr>
<tr>
<td>2.7 Refresh Scheduling</td>
<td>26</td>
</tr>
<tr>
<td>2.6 Self-Refresh Mode</td>
<td>26</td>
</tr>
<tr>
<td>2.8 DDR3 SDRAM Memory Controller Interface</td>
<td>23</td>
</tr>
<tr>
<td>2.5 Address Mapping</td>
<td>20</td>
</tr>
<tr>
<td>2.4 Protocol Descriptions</td>
<td>16</td>
</tr>
<tr>
<td>2.3 Signal Descriptions</td>
<td>15</td>
</tr>
<tr>
<td>2.2 SDRAM Memory Map</td>
<td>15</td>
</tr>
<tr>
<td>2.1 Clock Interface</td>
<td>15</td>
</tr>
<tr>
<td>1.4 Industry Standard(s) Compliance Statement</td>
<td>15</td>
</tr>
<tr>
<td>1.3 Industry Standard(s) Compliance Statement</td>
<td>15</td>
</tr>
<tr>
<td>1.1 Purpose of the Peripheral</td>
<td>9</td>
</tr>
<tr>
<td>1.1 Purpose of the Peripheral</td>
<td>11</td>
</tr>
<tr>
<td>1.2 Features</td>
<td>11</td>
</tr>
<tr>
<td>1.3 Industry Standard(s) Compliance Statement</td>
<td>11</td>
</tr>
<tr>
<td>2.19 Performance Monitoring</td>
<td>11</td>
</tr>
<tr>
<td>2.16 ECC</td>
<td>11</td>
</tr>
<tr>
<td>2.15 Emulation Considerations</td>
<td>11</td>
</tr>
<tr>
<td>2.14 EDMA Event Support</td>
<td>11</td>
</tr>
<tr>
<td>2.13 Interrupt Support</td>
<td>11</td>
</tr>
<tr>
<td>2.12 Leveling</td>
<td>11</td>
</tr>
<tr>
<td>2.11 DDR3 SDRAM Memory Initialization</td>
<td>11</td>
</tr>
<tr>
<td>2.7 Refresh Scheduling</td>
<td>11</td>
</tr>
<tr>
<td>2.6 Self-Refresh Mode</td>
<td>11</td>
</tr>
<tr>
<td>2.5 Address Mapping</td>
<td>11</td>
</tr>
<tr>
<td>2.4 Protocol Descriptions</td>
<td>11</td>
</tr>
<tr>
<td>2.3 Signal Descriptions</td>
<td>11</td>
</tr>
<tr>
<td>2.2 SDRAM Memory Map</td>
<td>11</td>
</tr>
<tr>
<td>2.1 Clock Interface</td>
<td>11</td>
</tr>
<tr>
<td>1.4 Industry Standard(s) Compliance Statement</td>
<td>11</td>
</tr>
<tr>
<td>1.3 Industry Standard(s) Compliance Statement</td>
<td>11</td>
</tr>
<tr>
<td>1.1 Purpose of the Peripheral</td>
<td>9</td>
</tr>
</tbody>
</table>
3 Using the DDR3 Memory Controller

3.1 Connecting the DDR3 Memory Controller to DDR3 SDRAM.................................................. 37
3.2 Configuring DDR3 Memory Controller Registers to Meet DDR3 SDRAM Specifications........ 38
   3.2.1 Programming the SDRAM Configuration Register (SDCFG)............................................. 42
   3.2.2 Programming the SDRAM Refresh Control Register (SDRFC).......................................... 42
   3.2.3 Configuring SDRAM Timing Registers (SDTIM1, SDTIM2, SDTIM3, SDTIM4).................... 43

4 DDR3 Memory Controller Registers ................................................................................. 46

   4.1 Module ID and Revision Register (MIDR)............................................................................. 50
   4.2 DDR3 Memory Controller Status Register (STATUS).......................................................... 51
   4.3 SDRAM Configuration Register (SDCFG)........................................................................... 52
   4.4 SDRAM Refresh Control Register (SDRFC)........................................................................ 54
   4.5 SDRAM Timing 1 (SDTIM1) Register.................................................................................... 55
   4.6 SDRAM Timing 2 (SDTIM2) Register.................................................................................... 56
   4.7 SDRAM Timing 3 (SDTIM3) Register.................................................................................... 57
   4.8 SDRAM Timing 4 (SDTIM4) Register.................................................................................... 58
   4.9 Power Management Control Register (PMCTL)................................................................. 59
   4.10 VBUSM Configuration Register (VBUSM_CONFIG)............................................................... 61
   4.11 Performance Counter 1 Register (PERF_CNT_1)................................................................. 62
   4.12 Performance Counter 2 Register (PERF_CNT_2)................................................................. 63
   4.13 Performance Counter Config Register (PERF_CNT_CFG)...................................................... 64
   4.14 Performance Counter Master Region Select Register (PERF_CNT_SEL).............................. 65
   4.15 Performance Counter Time Register (PERF_CNT_TIM)....................................................... 66
   4.16 Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)....................................................... 67
   4.17 Interrupt Status Register (IRQSTATUS_SYS)....................................................................... 68
   4.18 Interrupt Enable Set Register (IRQSTATUS_SET_SYS)......................................................... 69
   4.19 Interrupt Enable Clear Register (IRQSTATUS_CLR_SYS)..................................................... 70
   4.20 SDRAM Output Impedance Calibration Configuration Register (ZQCFG).............................. 71
   4.21 Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)........................................ 72
   4.22 Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP).......................... 73
   4.23 Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP).......................... 74
   4.24 ECC Control Register (ECCCTL)....................................................................................... 75
   4.25 ECC Address Range 1 Register (ECCADDR1)..................................................................... 76
   4.26 ECC Address Range 2 Register (ECCADDR2)..................................................................... 77
   4.27 Read Write Execution Threshold Register (RWTHRESH).................................................... 78
   4.28 1-Bit ECC Error Count Register (ONE_BIT_ECC_ERR_CNT)............................................... 79
   4.29 1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH)....................................... 80
   4.30 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1)............................... 81
   4.31 1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG)............................. 82
   4.32 2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG)............................. 83
   4.33 1-Bit ECC Error Distribution 2 Register (ONE_BIT_ECC_ERR_DIST_2).................................... 84
   4.34 PHY Initialization Register (PIR)....................................................................................... 85
   4.35 PHY General Configuration Register 0 (PGCR0)................................................................. 87
   4.36 PHY General Configuration Register 1 (PGCR1)................................................................. 89
   4.37 PHY General Configuration Register 2 (PGCR2)................................................................. 91
   4.38 PHY General Status Register 0 (PGSR0)............................................................................ 92
   4.39 PHY General Status Register 1 (PGSR1)............................................................................ 94
   4.40 PLL Control Register (PLLCR).......................................................................................... 95
   4.41 PHY Timing Register 0 (PTR0)........................................................................................... 96
   4.42 PHY Timing Register 1 (PTR1)........................................................................................... 97
   4.43 PHY Timing Register 2 (PTR2)........................................................................................... 98
   4.44 PHY Timing Register 3 (PTR3)........................................................................................... 99
   4.45 PHY Timing Register 4 (PTR4).......................................................................................... 100
   4.46 AC I/O Configuration Register (ACIOCR)...................................................................... 101
4.47 DATX8 Common Configuration Register (DXCCR) ................................................................. 102
4.48 DRAM Configuration Register (DCR) .............................................................................. 104
4.49 DRAM Timing Parameters Register 0 (DTPR0) ................................................................. 105
4.50 DRAM Timing Parameters Register 1 (DTPR1) ................................................................. 106
4.51 DRAM Timing Parameters Register 2 (DTPR2) ................................................................. 107
4.52 Mode Register 0 (MR0) ..................................................................................................... 108
4.53 Mode Register 1 (MR1) ..................................................................................................... 110
4.54 Mode Register 2 (MR2) ..................................................................................................... 112
4.55 Mode Register 3 (MR3) ..................................................................................................... 113
4.56 ODT Configuration Register (ODTCR) ............................................................................ 114
4.57 Data Training Configuration Register (DTCR) ................................................................. 115
4.58 Impedance Control Register 0 (ZQnCR0) ........................................................................ 116
4.59 Impedance Control Register 1 (ZQnCR1) ........................................................................ 117
4.60 Impedance Status Register 0 (ZQnSR0) .......................................................................... 118
4.61 Impedance Status Register 1 (ZQnSR1) .......................................................................... 119
4.62 DATX8 General Configuration Register (DXnGCR) ......................................................... 120
4.63 DATX8 General Status Register 0 (DXnGSR0) ................................................................. 122
4.64 DATX8 General Status Register 2 (DXnGSR2) ................................................................. 123
4.65 DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0) ........................................ 124
4.66 DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1) ........................................ 125
4.67 DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2) ........................................ 126
4.68 DATX8 Master Delay Line Register (DXnMDLR) .............................................................. 127
4.69 DATX8 General Timing Register (DXnGTR) ..................................................................... 128

Revision History ......................................................................................................................... 130
Revision History ......................................................................................................................... 130
## List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1</td>
<td>DDR3 Memory Control Signals .....................................................................</td>
<td>15</td>
</tr>
<tr>
<td>2-2</td>
<td>READ Command</td>
<td>19</td>
</tr>
<tr>
<td>2-3</td>
<td>WRITE Command</td>
<td>19</td>
</tr>
<tr>
<td>2-4</td>
<td>Logical Address-to-DDR3 SDRAM Address Map (EBANK=0)</td>
<td>22</td>
</tr>
<tr>
<td>2-5</td>
<td>DDR3 SDRAM Column, Row, and Bank Access (EBANK=0)</td>
<td>22</td>
</tr>
<tr>
<td>2-6</td>
<td>DDR3 Memory Controller FIFO Block Diagram</td>
<td>23</td>
</tr>
<tr>
<td>2-7</td>
<td>Data Bus Obfuscation</td>
<td>33</td>
</tr>
<tr>
<td>3-1</td>
<td>Connecting Two 16 MB x 16 x 8 Banks (4Gb Total) Devices</td>
<td>39</td>
</tr>
<tr>
<td>3-2</td>
<td>Connecting One 8 MB x 16 x 8 Banks (1Gb Total) Device</td>
<td>40</td>
</tr>
<tr>
<td>3-3</td>
<td>Connecting Two 16 MB x 8 x 8 Banks (2Gb Total) Devices</td>
<td>41</td>
</tr>
<tr>
<td>4-1</td>
<td>Module ID and Revision Register (MIDR)</td>
<td>50</td>
</tr>
<tr>
<td>4-2</td>
<td>DDR3 Memory Controller Status Register (STATUS)</td>
<td>51</td>
</tr>
<tr>
<td>4-3</td>
<td>SDRAM Configuration Register (SDCFG)</td>
<td>52</td>
</tr>
<tr>
<td>4-4</td>
<td>SDRAM Refresh Control Register (SDRFC)</td>
<td>54</td>
</tr>
<tr>
<td>4-5</td>
<td>SDRAM Timing 1 (SDTIM1) Register</td>
<td>55</td>
</tr>
<tr>
<td>4-6</td>
<td>SDRAM Timing 2 (SDTIM2) Register</td>
<td>56</td>
</tr>
<tr>
<td>4-7</td>
<td>SDRAM Timing 3 (SDTIM3) Register</td>
<td>57</td>
</tr>
<tr>
<td>4-8</td>
<td>SDRAM Timing 4 (SDTIM4) Register</td>
<td>58</td>
</tr>
<tr>
<td>4-9</td>
<td>Power Management Control Register (PMCTL)</td>
<td>59</td>
</tr>
<tr>
<td>4-10</td>
<td>VBUSM Configuration Register (VBUSM_CONFIG)</td>
<td>61</td>
</tr>
<tr>
<td>4-11</td>
<td>Performance Counter 1 Register (PERF_CNT_1)</td>
<td>62</td>
</tr>
<tr>
<td>4-12</td>
<td>Performance Counter 2 Register (PERF_CNT_2)</td>
<td>63</td>
</tr>
<tr>
<td>4-13</td>
<td>Performance Counter Config Register (PERF_CNT_CFG)</td>
<td>64</td>
</tr>
<tr>
<td>4-14</td>
<td>Performance Counter Master Region Select Register (PERF_CNT_SEL)</td>
<td>65</td>
</tr>
<tr>
<td>4-15</td>
<td>Performance Counter Time Register (PERF_CNT_TIM)</td>
<td>66</td>
</tr>
<tr>
<td>4-16</td>
<td>Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)</td>
<td>67</td>
</tr>
<tr>
<td>4-17</td>
<td>Interrupt Status Register (IRQSTATUS_SYS)</td>
<td>68</td>
</tr>
<tr>
<td>4-18</td>
<td>Interrupt Enable Set Register (IRQSTATUS_SET_SYS)</td>
<td>69</td>
</tr>
<tr>
<td>4-19</td>
<td>Interrupt Enable Clear Register (IRQSTATUS_CLR_SYS)</td>
<td>70</td>
</tr>
<tr>
<td>4-20</td>
<td>SDRAM Output Impedance Calibration Configuration Register (ZQCFG)</td>
<td>71</td>
</tr>
<tr>
<td>4-21</td>
<td>Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)</td>
<td>72</td>
</tr>
<tr>
<td>4-22</td>
<td>Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)</td>
<td>73</td>
</tr>
<tr>
<td>4-23</td>
<td>Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)</td>
<td>74</td>
</tr>
<tr>
<td>4-24</td>
<td>ECC Control Register (ECCCTL)</td>
<td>75</td>
</tr>
<tr>
<td>4-25</td>
<td>ECC Address Range 1 Register (ECCADDR1)</td>
<td>76</td>
</tr>
<tr>
<td>4-26</td>
<td>ECC Address Range 2 Register (ECCADDR2)</td>
<td>77</td>
</tr>
<tr>
<td>4-27</td>
<td>Read Write Execution Threshold Register (RWTHRESH)</td>
<td>78</td>
</tr>
<tr>
<td>4-28</td>
<td>1-Bit ECC Error Count Register (ONE_BIT_ECC_ERR_CNT)</td>
<td>79</td>
</tr>
<tr>
<td>4-29</td>
<td>1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRESH)</td>
<td>80</td>
</tr>
<tr>
<td>4-30</td>
<td>1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1)</td>
<td>81</td>
</tr>
<tr>
<td>4-31</td>
<td>1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG)</td>
<td>82</td>
</tr>
<tr>
<td>4-32</td>
<td>2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG)</td>
<td>83</td>
</tr>
<tr>
<td>4-33</td>
<td>1-Bit ECC Error Distribution 2 Register (ONE_BIT_ECC_ERR_DIST_2)</td>
<td>84</td>
</tr>
<tr>
<td>4-34</td>
<td>PHY Initialization Register (PIR)</td>
<td>85</td>
</tr>
<tr>
<td>4-35</td>
<td>PHY General Configuration Register 0 (PGCR0)</td>
<td>87</td>
</tr>
<tr>
<td>4-36</td>
<td>PHY General Configuration Register 1 (PGCR1)</td>
<td>89</td>
</tr>
<tr>
<td>4-37</td>
<td>PHY General Configuration Register 2 (PGCR2)</td>
<td>91</td>
</tr>
</tbody>
</table>
4-38. PHY General Status Register 0 (PGSR0) ................................................................. 92
4-39. PHY General Status Register 1 (PGSR1) ................................................................. 94
4-40. PLL Control Register (PLLCR) ........................................................................... 95
4-41. PHY Timing Register 0 (PTR0) ........................................................................... 96
4-42. PHY Timing Register 1 (PTR1) ........................................................................... 97
4-43. PHY Timing Register 2 (PTR2) ........................................................................... 98
4-44. PHY Timing Register 3 (PTR3) ........................................................................... 99
4-45. PHY Timing Register 4 (PTR4) ........................................................................... 100
4-46. AC I/O Configuration Register (ACIOCR) ...................................................... 101
4-47. DATX8 Common Configuration Register (DXCCR) ...................................... 102
4-48. DRAM Configuration Register (DCR) ............................................................... 104
4-49. DRAM Timing Parameters Register 0 (DTPR0) ................................................ 105
4-50. DRAM Timing Parameters Register 1 (DTPR1) ................................................ 106
4-51. DRAM Timing Parameters Register 2 (DTPR2) ................................................ 107
4-52. Mode Register 0 (MR0) ................................................................................... 108
4-53. Mode Register 1 (MR1) ................................................................................... 110
4-54. Mode Register 2 (MR2) ................................................................................... 112
4-55. Mode Register 3 (MR3) ................................................................................... 113
4-56. ODT Configuration Register (ODTCR) ............................................................ 114
4-57. Data Training Configuration Register (DTCR) ................................................ 115
4-58. Impedance Control Register 0 (ZQnCR0) ............................................................ 116
4-59. Impedance Control Register 1 (ZQnCR1) ............................................................ 117
4-60. Impedance Status Register 0 (ZQnSR0) ............................................................... 118
4-61. Impedance Status Register 1 (ZQnSR1) ............................................................... 119
4-62. DATX8 General Configuration Register (DXnGCR) ........................................ 120
4-63. DATX8 General Status Register 0 (DXnGSR0) .................................................. 122
4-64. DATX8 General Status Register 2 (DXnGSR2) .................................................. 123
4-65. DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0) ......................... 124
4-66. DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1) ......................... 125
4-67. DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2) ......................... 126
4-68. DATX8 Master Delay Line Register (DXnMDLR) ............................................... 127
4-69. DATX8 General Timing Register (DXnGTR) ..................................................... 128
<table>
<thead>
<tr>
<th></th>
<th>List of Tables</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1.</td>
<td>DDR3 Memory Controller Signal Descriptions</td>
<td>15</td>
</tr>
<tr>
<td>2-2.</td>
<td>DDR3 SDRAM Commands</td>
<td>16</td>
</tr>
<tr>
<td>2-3.</td>
<td>Truth Table for DDR3 SDRAM Commands</td>
<td>17</td>
</tr>
<tr>
<td>2-4.</td>
<td>Bank Configuration Register Fields for Address Mapping</td>
<td>20</td>
</tr>
<tr>
<td>2-5.</td>
<td>Logical Address-to-SDRAM Address Mapping</td>
<td>21</td>
</tr>
<tr>
<td>2-6.</td>
<td>DDR3 Memory Controller FIFO Description</td>
<td>23</td>
</tr>
<tr>
<td>2-7.</td>
<td>Device and DDR3 Memory Controller Reset Relationship</td>
<td>27</td>
</tr>
<tr>
<td>2-8.</td>
<td>Turnaround Time</td>
<td>28</td>
</tr>
<tr>
<td>2-9.</td>
<td>DDR3 SDRAM Extended Mode Register 2 Configuration</td>
<td>29</td>
</tr>
<tr>
<td>2-10.</td>
<td>DDR3 SDRAM Extended Mode Register 1 Configuration</td>
<td>29</td>
</tr>
<tr>
<td>2-11.</td>
<td>DDR3 SDRAM Mode Register 0 Configuration</td>
<td>29</td>
</tr>
<tr>
<td>2-12.</td>
<td>Performance Counter Filter Configuration</td>
<td>35</td>
</tr>
<tr>
<td>3-1.</td>
<td>SDCFG Configuration</td>
<td>42</td>
</tr>
<tr>
<td>3-2.</td>
<td>DDR3 Memory Refresh Specification</td>
<td>42</td>
</tr>
<tr>
<td>3-3.</td>
<td>See the register section for the SDTIM* register where the field exists</td>
<td>43</td>
</tr>
<tr>
<td>3-4.</td>
<td>See the register section for the SDTIM* register where the field exists</td>
<td>44</td>
</tr>
<tr>
<td>3-5.</td>
<td>See the register section for the SDTIM* register where the field exists</td>
<td>44</td>
</tr>
<tr>
<td>4-1.</td>
<td>DDR3 Memory Controller Registers (See datasheet memory map for base address)</td>
<td>46</td>
</tr>
<tr>
<td>4-2.</td>
<td>DDR3 PHY Registers (See device datasheet for base address)</td>
<td>47</td>
</tr>
<tr>
<td>4-3.</td>
<td>Module ID and Revision Register (MIDR) Field Descriptions</td>
<td>50</td>
</tr>
<tr>
<td>4-4.</td>
<td>DDR3 Memory Controller Status Register (STATUS) Field Descriptions</td>
<td>51</td>
</tr>
<tr>
<td>4-5.</td>
<td>SDRAM Configuration Register (SDCFG) Field Descriptions</td>
<td>52</td>
</tr>
<tr>
<td>4-6.</td>
<td>SDRAM Refresh Control (SDRFC) Register Field Descriptions</td>
<td>54</td>
</tr>
<tr>
<td>4-7.</td>
<td>SDRAM Timing 1 (SDTIM1) Register Field Descriptions</td>
<td>55</td>
</tr>
<tr>
<td>4-8.</td>
<td>SDRAM Timing 2 (SDTIM2) Register Field Descriptions</td>
<td>56</td>
</tr>
<tr>
<td>4-9.</td>
<td>SDRAM Timing 3 (SDTIM3) Register Field Descriptions</td>
<td>57</td>
</tr>
<tr>
<td>4-10.</td>
<td>SDRAM Timing 4 (SDTIM4) Register Field Descriptions</td>
<td>58</td>
</tr>
<tr>
<td>4-11.</td>
<td>Power Management Control Register (PMCTL) Field Descriptions</td>
<td>59</td>
</tr>
<tr>
<td>4-12.</td>
<td>VBUSM Configuration Register (VBUSM_CONFIG) Field Descriptions</td>
<td>61</td>
</tr>
<tr>
<td>4-13.</td>
<td>Performance Counter 1 Register (PERF_CNT_1) Field Descriptions</td>
<td>62</td>
</tr>
<tr>
<td>4-14.</td>
<td>Performance Counter 2 Register (PERF_CNT_2) Field Descriptions</td>
<td>63</td>
</tr>
<tr>
<td>4-15.</td>
<td>Performance Counter Config Register (PERF_CNT_CFG) Field Descriptions</td>
<td>64</td>
</tr>
<tr>
<td>4-16.</td>
<td>Performance Counter Master Region Select Register (PERF_CNT_SEL) Field Descriptions</td>
<td>65</td>
</tr>
<tr>
<td>4-17.</td>
<td>Performance Counter Time Register (PERF_CNT_TIM) Field Descriptions</td>
<td>66</td>
</tr>
<tr>
<td>4-18.</td>
<td>Interrupt Raw Status Register (IRQSTATUS_RAW_SYS) Field Descriptions</td>
<td>67</td>
</tr>
<tr>
<td>4-19.</td>
<td>Interrupt Status Register (IRQSTATUS_SYS) Field Descriptions</td>
<td>68</td>
</tr>
<tr>
<td>4-20.</td>
<td>Interrupt Enable Set Register (IRQSTATUS_SET_SYS) Field Descriptions</td>
<td>69</td>
</tr>
<tr>
<td>4-21.</td>
<td>Interrupt Enable Clear Register (IRQSTATUS_CLR_SYS) Field Descriptions</td>
<td>70</td>
</tr>
<tr>
<td>4-22.</td>
<td>SDRAM Output Impedance Calibration Configuration Register (ZQCFG) Field Descriptions</td>
<td>71</td>
</tr>
<tr>
<td>4-23.</td>
<td>Priority to Class-Of-Service Mapping Register (PRICOSMAP) Field Descriptions</td>
<td>72</td>
</tr>
<tr>
<td>4-24.</td>
<td>Master ID to Class-Of-Service Mapping 1 Register (MSTID_COS_1_MAP) Field Descriptions</td>
<td>73</td>
</tr>
<tr>
<td>4-25.</td>
<td>Master ID to Class-Of-Service Mapping 2 Register (MSTID_COS_2_MAP) Field Descriptions</td>
<td>74</td>
</tr>
<tr>
<td>4-26.</td>
<td>ECC Control Register (ECCCTL) Field Descriptions</td>
<td>75</td>
</tr>
<tr>
<td>4-27.</td>
<td>ECC Address Range 1 Register Field Descriptions</td>
<td>76</td>
</tr>
<tr>
<td>4-28.</td>
<td>ECC Address Range 2 Register Field Descriptions</td>
<td>77</td>
</tr>
<tr>
<td>4-29.</td>
<td>Read Write Execution Threshold Register (RWTHRESH) Field Descriptions</td>
<td>78</td>
</tr>
<tr>
<td>4-30.</td>
<td>1-Bit ECC Error Count Register Field Descriptions</td>
<td>79</td>
</tr>
<tr>
<td>Table Number</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>-------------</td>
<td>------------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>4-31</td>
<td>1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH) Field Descriptions</td>
<td>80</td>
</tr>
<tr>
<td>4-32</td>
<td>1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1) Field Descriptions</td>
<td>81</td>
</tr>
<tr>
<td>4-33</td>
<td>1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG) Field Descriptions</td>
<td>82</td>
</tr>
<tr>
<td>4-34</td>
<td>2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG) Field Descriptions</td>
<td>83</td>
</tr>
<tr>
<td>4-35</td>
<td>1-Bit ECC Error Distribution 2 register (ONE_BIT_ECC_ERR_DIST_2) Field Descriptions</td>
<td>84</td>
</tr>
<tr>
<td>4-36</td>
<td>PHY Initialization Register (PIR) Field Descriptions</td>
<td>85</td>
</tr>
<tr>
<td>4-37</td>
<td>PHY General Configuration Register 0 (PGCR0) Field Descriptions</td>
<td>87</td>
</tr>
<tr>
<td>4-38</td>
<td>PHY General Configuration Register 1 (PGCR1) Field Descriptions</td>
<td>89</td>
</tr>
<tr>
<td>4-39</td>
<td>PHY General Configuration Register 2 (PGCR2) Field Descriptions</td>
<td>91</td>
</tr>
<tr>
<td>4-40</td>
<td>PHY General Status Register 0 (PGSR0) Field Descriptions</td>
<td>92</td>
</tr>
<tr>
<td>4-41</td>
<td>PHY General Status Register 1 (PGSR1) Field Descriptions</td>
<td>94</td>
</tr>
<tr>
<td>4-42</td>
<td>PLL Control Register (PLLCCR) Field Descriptions</td>
<td>95</td>
</tr>
<tr>
<td>4-43</td>
<td>PHY Timing Register 0 (PTR0) Field Descriptions</td>
<td>96</td>
</tr>
<tr>
<td>4-44</td>
<td>PHY Timing Register 1 (PTR1) Field Descriptions</td>
<td>97</td>
</tr>
<tr>
<td>4-45</td>
<td>PHY Timing Register 2 (PTR2) Field Descriptions</td>
<td>98</td>
</tr>
<tr>
<td>4-46</td>
<td>PHY Timing Register 3 (PTR3) Field Descriptions</td>
<td>99</td>
</tr>
<tr>
<td>4-47</td>
<td>PHY Timing Register 4 (PTR4) Field Descriptions</td>
<td>100</td>
</tr>
<tr>
<td>4-48</td>
<td>AC I/O Configuration Register (ACIOCR) Field Descriptions</td>
<td>101</td>
</tr>
<tr>
<td>4-49</td>
<td>DATX8 Common Configuration Register (DXCCR) Field Descriptions</td>
<td>102</td>
</tr>
<tr>
<td>4-50</td>
<td>DRAM Configuration Register (DCR) Field Descriptions</td>
<td>104</td>
</tr>
<tr>
<td>4-51</td>
<td>DRAM Timing Parameters Register 0 (DTPR0) Field Descriptions</td>
<td>105</td>
</tr>
<tr>
<td>4-52</td>
<td>DRAM Timing Parameters Register 1 (DTPR1) Field Descriptions</td>
<td>106</td>
</tr>
<tr>
<td>4-53</td>
<td>DRAM Timing Parameters Register 2 (DTPR2) Field Descriptions</td>
<td>107</td>
</tr>
<tr>
<td>4-54</td>
<td>Mode Register 0 (MR0) Field Descriptions</td>
<td>108</td>
</tr>
<tr>
<td>4-55</td>
<td>Mode Register 1 (MR1) Field Descriptions</td>
<td>110</td>
</tr>
<tr>
<td>4-56</td>
<td>Mode Register 2 (MR2) Field Descriptions</td>
<td>112</td>
</tr>
<tr>
<td>4-57</td>
<td>Mode Register 3 (MR3) Field Descriptions</td>
<td>113</td>
</tr>
<tr>
<td>4-58</td>
<td>ODT Configuration Register (ODTCR) Field Descriptions</td>
<td>114</td>
</tr>
<tr>
<td>4-59</td>
<td>Data Training Configuration Register (DTCR) Field Descriptions</td>
<td>115</td>
</tr>
<tr>
<td>4-60</td>
<td>Impedance Control Register 0 (ZQnCR0) Field Descriptions</td>
<td>116</td>
</tr>
<tr>
<td>4-61</td>
<td>Impedance Control Register 1 (ZQnCR1) Field Descriptions</td>
<td>117</td>
</tr>
<tr>
<td>4-62</td>
<td>Impedance Status Register 0 (ZQnSR0) Field Descriptions</td>
<td>118</td>
</tr>
<tr>
<td>4-63</td>
<td>Impedance Status Register 1 (ZQnSR1) Field Descriptions</td>
<td>119</td>
</tr>
<tr>
<td>4-64</td>
<td>DATX8 General Configuration Register (DXnGCR) Field Descriptions</td>
<td>120</td>
</tr>
<tr>
<td>4-65</td>
<td>DATX8 General Status Register 0 (DXnGSR0) Field Descriptions</td>
<td>122</td>
</tr>
<tr>
<td>4-66</td>
<td>DATX8 General Status Register 2 (DXnGSR2) Field Descriptions</td>
<td>123</td>
</tr>
<tr>
<td>4-67</td>
<td>DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0) Field Descriptions</td>
<td>124</td>
</tr>
<tr>
<td>4-68</td>
<td>DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1) Field Descriptions</td>
<td>125</td>
</tr>
<tr>
<td>4-69</td>
<td>DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2) Field Descriptions</td>
<td>126</td>
</tr>
<tr>
<td>4-70</td>
<td>DATX8 Master Delay Line Register (DXnMDLR) Field Descriptions</td>
<td>127</td>
</tr>
<tr>
<td>4-71</td>
<td>DATX8 General Timing Register (DXnGTR) Field Descriptions</td>
<td>128</td>
</tr>
</tbody>
</table>
About This Manual

The DDR3 memory controller is used to interface with JESD79-3C standard compliant SDRAM devices. Memory types such as DDR1 SDRAM, DDR2 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR3 memory controller SDRAM can be used for program and data storage.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

---

**NOTE:** Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

---

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

---

**CAUTION**

Indicates the possibility of service interruption if precautions are not taken.

---

**WARNING**

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

<table>
<thead>
<tr>
<th>C66x CorePac User Guide</th>
<th>SPRUGW0</th>
</tr>
</thead>
<tbody>
<tr>
<td>C66x CPU and Instruction Set Reference Guide</td>
<td>SPRUGH7</td>
</tr>
<tr>
<td>Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide</td>
<td>SPRUGS5</td>
</tr>
<tr>
<td>External Memory Interface (EMIF16) for KeyStone Devices User Guide</td>
<td>SPRUGZ3</td>
</tr>
<tr>
<td>Interrupt Controller (INTC) for KeyStone Devices User Guide</td>
<td>SPRUGW4</td>
</tr>
</tbody>
</table>
This document describes the operation of the DDR3 module in the KeyStone II devices. (Refer to the device-specific data manual for exact device applicability.) The DDR3 module is accessible across all the cores and all system masters that are not cores.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 Purpose of the Peripheral</td>
<td>12</td>
</tr>
<tr>
<td>1.2 Features</td>
<td>12</td>
</tr>
<tr>
<td>1.3 Industry Standard(s) Compliance Statement</td>
<td>12</td>
</tr>
</tbody>
</table>
1.1 Purpose of the Peripheral

The DDR3 memory controller is used to interface with JESD79-3E standard compliant SDRAM devices. Memory types such as DDR1 SDRAM, DDR2 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR3 memory controller SDRAM can be used for program and data storage. The KeyStone II devices have one (DDR3A) or two (DDR3A and DDR3B) instances depending on the device variant. See the KeyStone II Data Manual. DDR3A is accessed via the MSMC module whereas DDR3B is connected directly to the TeraNet.

1.2 Features

The DDR3 controller supports the following features:

- Supports JEDEC standard JESD79-3E – DDR3 compliant devices
- 33-bit address for 8 GB of address space
- 16/32/64-bit data bus width support
- CAS latencies: 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16
- 1, 2, 4, and 8 internal banks
- Burst Length: 8
- Burst Type: sequential
- 8GB address space available over one or two chip selects
- Page sizes: 256, 512, 1024, and 2048-word
- SDRAM auto initialization from reset or configuration change
- Self-refresh mode
- Prioritized refresh scheduling
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Big and little endian modes
- ECC on SDRAM data bus (read-modify-write (RMW) ECC to support sub quanta accesses to ECC space (see the section on ECC for applicable device))
- 8-bit ECC per 64-bit data quanta without additional cycle latency
- Two latency classes supported
- UDIMM Address mirroring is supported
- RDIMM is not supported

1.3 Industry Standard(s) Compliance Statement

The DDR3 controller is compliant with the JESD79-3E DDR3 SDRAM standard.
The DDR3 controller interfaces with most standard DDR3 SDRAM devices. It supports self-refresh mode and prioritized refresh. In addition, it provides flexibility through programmable parameters such as the refresh rate, CAS latency, and many SDRAM timing parameters. The following sections describe the architecture of the DDR3 controller as well as how to interface and configure it to perform read and write operations to DDR3 SDRAM devices. Examples for interfacing the DDR3 controller to a common DDR3 SDRAM device are shown in Section 3.1.

### Chapter 2: Peripheral Architecture

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1  Clock Interface</td>
<td>15</td>
</tr>
<tr>
<td>2.2  SDRAM Memory Map</td>
<td>15</td>
</tr>
<tr>
<td>2.3  Signal Descriptions</td>
<td>15</td>
</tr>
<tr>
<td>2.4  Protocol Descriptions</td>
<td>16</td>
</tr>
<tr>
<td>2.5  Address Mapping</td>
<td>20</td>
</tr>
<tr>
<td>2.6  DDR3 Memory Controller Interface</td>
<td>23</td>
</tr>
<tr>
<td>2.7  Refresh Scheduling</td>
<td>26</td>
</tr>
<tr>
<td>2.8  Self-Refresh Mode</td>
<td>26</td>
</tr>
<tr>
<td>2.9  Reset Considerations</td>
<td>27</td>
</tr>
<tr>
<td>2.10 Turnaround Time</td>
<td>28</td>
</tr>
<tr>
<td>2.11 DDR3 SDRAM Memory Initialization</td>
<td>28</td>
</tr>
<tr>
<td>2.12 Leveling</td>
<td>30</td>
</tr>
<tr>
<td>2.13 Interrupt Support</td>
<td>30</td>
</tr>
<tr>
<td>2.14 EDMA Event Support</td>
<td>30</td>
</tr>
<tr>
<td>2.15 Emulation Considerations</td>
<td>30</td>
</tr>
<tr>
<td>2.16 ECC</td>
<td>30</td>
</tr>
<tr>
<td>2.17 Data Bus Obfuscation</td>
<td>33</td>
</tr>
<tr>
<td>2.18 Power Management</td>
<td>34</td>
</tr>
<tr>
<td>2.19 Performance Monitoring</td>
<td>34</td>
</tr>
</tbody>
</table>
2.1 Clock Interface

There are two clocking schemes in the DDR3 controller - the clocking scheme used to drive the DDR3 controller and the clocking scheme used to drive the DDR3 I/O interface. The DDR3A controller is clocked by DSP/2 clock domain and the DDR3B controller is clocked by DSP/3 clock domain. The I/O interface is driven by the DDR3 A/B memory clock (half the data rate).

2.2 SDRAM Memory Map

On KeyStone II devices, both DDR3A and DDR3B have their own controller configuration space and PHY configuration space. For information describing the DDR3 A/B memory map, see the device-specific data manual.

2.3 Signal Descriptions

The DDR3 memory controller signals are shown in Figure 2-1 and described in Figure 2-1.

- The maximum data bus is 64-bits wide.
- The address bus is 33-bits wide.
- Two differential output clocks driven by internal clock sources.
- Command signals: Row and column address strobe, write enable strobe, data strobe, and data mask.
- Two chip selects and two clock enable signals.

![Figure 2-1. DDR3 Memory Control Signals](image-url)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDRCB [7:0]</td>
<td>Bidirectional data bus (check bits) for ECC byte lane. Input for data reads and output for data writes.</td>
</tr>
<tr>
<td>DDRA [15:0]</td>
<td>External address output.</td>
</tr>
<tr>
<td>DDRCE0</td>
<td>Active-low chip enable for memory space CE0. DDRCE0z is used to enable the DDR3 SDRAM memory device during external memory accesses.</td>
</tr>
</tbody>
</table>
Table 2-1. DDR3 Memory Controller Signal Descriptions (continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDRCE1</td>
<td>Active-low chip enable for memory space CE1. DDRCE1z is used to enable the DDR3 SDRAM memory device during external memory accesses.</td>
</tr>
<tr>
<td>DDRDQM [8:0]</td>
<td>Active-high output data mask.</td>
</tr>
<tr>
<td>DDR3CLKOUTP [1:0]/DDR3CLKOUTN [1:0]</td>
<td>Differential clock outputs.</td>
</tr>
<tr>
<td>DDRCKE [1:0]</td>
<td>Clock enable (used for self-refresh mode).</td>
</tr>
<tr>
<td>DDRCAS</td>
<td>Active-low column address strobe.</td>
</tr>
<tr>
<td>DRRAS</td>
<td>Active-low row address strobe.</td>
</tr>
<tr>
<td>DDRWE</td>
<td>Active-low write enable.</td>
</tr>
<tr>
<td>DDRDQSP [8:0]/DDRDQSN [8:0]</td>
<td>Differential data strobe bidirectional signals.</td>
</tr>
<tr>
<td>DDRDT [1:0]</td>
<td>On-die termination signal(s) to external DDR3 SDRAM</td>
</tr>
<tr>
<td>DDRBA [2:0]</td>
<td>Bank-address control outputs</td>
</tr>
<tr>
<td>VREFSSTTL</td>
<td>DDR3 Memory Controller reference voltage. This voltage must be supplied externally. For more details, see the device-specific data manual.</td>
</tr>
</tbody>
</table>

2.4 Protocol Descriptions

The DDR3 memory controller supports the DDR3 SDRAM commands listed in Table 2-2.

Table 2-2. DDR3 SDRAM Commands

<table>
<thead>
<tr>
<th>Command</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACT</td>
<td>Activates the selected bank and row.</td>
</tr>
<tr>
<td>PREA</td>
<td>Precharge all command. Deactivates (precharges) all banks.</td>
</tr>
<tr>
<td>PRE</td>
<td>Precharge single command. Deactivates (precharges) a single bank.</td>
</tr>
<tr>
<td>DES</td>
<td>Device Deselect.</td>
</tr>
<tr>
<td>EMRS</td>
<td>Extended Mode Register set. Allows altering the contents of the mode register.</td>
</tr>
<tr>
<td>MRS</td>
<td>Mode register set. Allows altering the contents of the mode register.</td>
</tr>
<tr>
<td>NOP</td>
<td>No operation.</td>
</tr>
<tr>
<td>PDE</td>
<td>Power down entry</td>
</tr>
<tr>
<td>PDX</td>
<td>Power down exit</td>
</tr>
<tr>
<td>RD</td>
<td>Inputs the starting column address and begins the read operation.</td>
</tr>
<tr>
<td>REF</td>
<td>Autorefresh cycle</td>
</tr>
<tr>
<td>SRE</td>
<td>Self-refresh entry</td>
</tr>
<tr>
<td>SRX</td>
<td>Self-refresh exit</td>
</tr>
<tr>
<td>WR</td>
<td>Inputs the starting column address and begins the write operation.</td>
</tr>
<tr>
<td>ZQCS</td>
<td>ZQ Calibration short operation</td>
</tr>
<tr>
<td>ZQCL</td>
<td>ZQ Calibration long operation</td>
</tr>
</tbody>
</table>
Table 2-3 shows the signal truth table for the DDR3 SDRAM commands.

### Table 2-3. Truth Table for DDR3 SDRAM Commands

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Previous Cycle</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>BA</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>Current Cycle</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>L</td>
<td>BA</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>DDRBA [1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDRBA [2:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR[15:13]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR[12]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR[10]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR[9:0],[11]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACT</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>BA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PREA</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>H</td>
<td>V</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>PRE</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>BA</td>
<td>V</td>
<td>V</td>
<td>L</td>
<td>BA</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>MRS</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>BA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EMRS(2)</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>BA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD (BL8)</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>BA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WR (BL8)</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>BA</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REF</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRE(3)</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRX(3)(4)</td>
<td>L</td>
<td>H</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOP</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DES(5)</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDE(6)</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDX(6)</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZQCL</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZQCS</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) LEGEND: H = Logic High, L = Logic Low, X = Don’t Care, RA = Row Address, CA = Column Address, RFU = Reserved for future use, V = Valid
(2) For extended mode register set (EMRS) command, bank address (BA) pins select an extended mode register (EMR).
(3) ODT function is not available during self-refresh.
(4) Self-refresh exit (SRE) is asynchronous.
(5) The Deselct (DES) command performs the same function as No Operation (NOP).
(6) The Power down mode does not perform any self-refresh operation.

### 2.4.1 Mode Register Set (MRS or EMRS)

DDR3 SDRAM contains mode and extended mode registers that configure the DDR3 memory for operation. These registers control burst type, burst length, CAS latency, DLL enable/disable, etc.

The DDR3 memory controller programs the mode and extended mode registers of the DDR3 memory by issuing MRS and EMRS commands. MRS and EMRS commands can be issued during DDR3 initialization as well as during normal operation as long as the external SDRAM is in idle state. When the MRS or EMRS command is executed, the value on DDRBA [1:0] selects the mode register to be written and the data on DDRA [12:0] is loaded into the register. DDRA [15:13] and DDRBA [2] are reserved and are programmed to 0 during MRS (or EMRS).

Each mode register allows programming of different sets of DDR3 SDRAM parameters. The DDR3 memory controller programs the mode registers in compliance with the JEDEC JESD79-3E spec. For more information about mode registers and how they are programmed, see the JEDEC spec.
2.4.2 Refresh Mode

The DDR3 memory controller issues refresh commands (REF) to the DDR3 SDRAM device. REF is automatically preceded by a Precharge-all (PREA) command, ensuring the deactivation of all CE spaces and banks selected.

Following the PREA command, the DDR3 memory controller begins performing refreshes at a rate defined by the refresh rate (REFRESH_RATE) field in the SDRAM refresh control register (SDRFC). In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for efficient operation, refresh commands can be postponed a maximum of 8 times. Also, at any given time a maximum of 16 refresh commands can be issued within a 2 xtREFI interval. For more information on refresh command timing, see the JEDEC spec.

2.4.3 Activation

The ACTIVE command is used to open (or activate) a row in a specific bank for a subsequent access. DDRBA [2:0] select the bank, and the address provided on DDRA[15:0] selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

When the DDR3 memory controller issues an ACT command, a delay of tRCD is incurred before a read or write command is issued. Reads or writes to the currently active row and bank of memory can achieve much higher throughput than reads or writes to random areas because every time a new row is accessed, the ACT command must be issued and a delay of tRCD incurred.

2.4.4 Deactivation

The precharge command is used to deactivate the open row in a particular bank (PRE) or the open row in all banks (PREA). The bank(s) will be available for a subsequent row activation a specified time (tRP) after the precharge command is issued, except in the case of concurrent auto precharge, where a read or write command to a different bank is allowed as along as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. A PRE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. During a PREA command, DDRA [10] is driven high to ensure deactivation of all banks.

2.4.5 READ Command

Figure 2-2 shows the DDR3 memory controller performing a read burst from DDR3 SDRAM. The READ command initiates a burst read operation to an active row. The column address is driven on DDRA [15:0], and the bank address is driven on DDRBA [2:0].

The DDR3 memory controller uses a burst length of 8, and has a programmable CAS latency of 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 or 16. The CAS latency is five cycles in Figure 2-2. In this figure it has been programmed to CL + 1. Because the default burst size is 8, the DDR3 memory controller returns 8 words of data for every read command. Word size is nothing but the DDR3 interface bus width.

If additional accesses are not pending to the DDR3 memory controller, the read burst completes and the unneeded data is disregarded. If additional accesses are pending, based on the arbitration result, the DDR3 memory controller can terminate the read burst and start a new read burst.
2.4.6  **Write (WR) Command**

Prior to a WRT command, the desired bank and row are activated by the ACT command. Following the WRT command, a write latency is incurred. Write latency is equal to CAS latency minus 1. All writes have a burst length of 8.

Figure 2-3 shows the timing for a write on the DDR3 memory controller. If the transfer request is for less than 8 words, depending on the scheduling result and the pending commands, the DDR3 memory controller can:

- Mask out the additional data using DDRDQM outputs
- Terminate the write burst and start a new write burst

### Figure 2-3. WRITE Command

NOP commands are shown for ease of illustration; other commands may be valid at these times
2.5 Address Mapping

The DDR3 memory controller views external DDR3 SDRAM as one continuous block of memory across the two chip-selects. If smaller devices are used, the memory is seen to roll over. The DDR3 memory controller receives DDR3 memory access requests along with a 33-bit logical address from the rest of the system. The controller uses the logical address to generate a row/page, column, bank address, and chip select for the DDR3 SDRAM. The number of bank and column address bits used is determined by the IBANK and PAGESIZE fields. The chip selection pins used are determined by the EBANK field (Table 2-4).

Table 2-4. Bank Configuration Register Fields for Address Mapping

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Bit Value</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBANK</td>
<td>0</td>
<td>1 bank</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>2 banks</td>
</tr>
<tr>
<td></td>
<td>2h</td>
<td>4 banks</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>8 banks</td>
</tr>
<tr>
<td>PAGESIZE</td>
<td>0</td>
<td>256 words (requires 8 column address bits)</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>512 words (requires 9 column address bits)</td>
</tr>
<tr>
<td></td>
<td>2h</td>
<td>1024 words (requires 10 column address bits)</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>2048 words (requires 11 column address bits)</td>
</tr>
<tr>
<td>EBANK</td>
<td>0</td>
<td>Use only chip enable 0 for all SDRAM accesses</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Use chip enables 0 and 1 for SDRAM accesses</td>
</tr>
</tbody>
</table>

**NOTE:** IBANK should always be programmed to 3h since DDR3 memory devices offer only 8-bank support unlike DDR2 with the option of 4-bank or 8-bank memory devices.

As the source address increments across SDRAM page boundaries, the DDR3 controller moves to the same page in the next bank on the current device (chip select).

After the page has been accessed in all banks of the current device, the same page is accessed in all banks in the next device. This is followed by accessing the next page in the first device and the process continues. To the DDR3 SDRAM, this process looks as shown on Figure 2-5. Thus, the DDR3 controller exploits this traversal across internal banks and chip selects while remaining on the same page to maximize the number of open SDRAM banks within the overall SDRAM space. See Figure 2-5.

Thus 16 banks (eight internal banks across two chip selects) can be kept open at a time, interleaving among all of them.
### Table 2-5. Logical Address-to-SDRAM Address Mapping

<table>
<thead>
<tr>
<th>ROW SIZE</th>
<th>nrb</th>
<th>EBANK</th>
<th>ncs</th>
<th>IBANK</th>
<th>nbb</th>
<th>PAGE SIZE</th>
<th>ncb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Don’t care</td>
<td>16 bits</td>
<td>0</td>
<td>0 bits</td>
<td>0</td>
<td>0 bits</td>
<td>0</td>
<td>8 bits</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1 bit</td>
<td>1</td>
<td>1 bit</td>
<td>1</td>
<td>9 bits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>2 bits</td>
<td>2</td>
<td>2 bits</td>
<td>2</td>
<td>10 bits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>3 bits</td>
<td>3</td>
<td>3 bits</td>
<td>3</td>
<td>11 bits</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Logical address mapping for row address</th>
<th>Logical address mapping for chip select</th>
<th>Logical address mapping for bank address[1:0]</th>
<th>Logical address mapping for column address</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>M3+nrb-1</td>
<td>M3+1</td>
<td>M3=M2+ncs-1</td>
<td>M2+1</td>
</tr>
</tbody>
</table>

**NOTE:** N=1 for 16-bit SDRAM, N=2 for 32-bit SDRAM and N=3 for 64-bit SDRAM. ROWSIZE is kept for legacy reasons but is not used by the DDR3 controller. nrb = Number of row bits. ncs = Number of chip select bits. nbb = Number of bank select bits determined by bank address [2:0].
Figure 2-4. Logical Address-to-DDR3 SDRAM Address Map (EBANK=0)

<table>
<thead>
<tr>
<th>Col. 0</th>
<th>Col. 1</th>
<th>Col. 2</th>
<th>Col. 3</th>
<th>Col. 4</th>
<th>* * *</th>
<th>Col. M-1</th>
<th>Col. M</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row 0, bank 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row 0, bank 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row 0, bank 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row 0, bank P</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>Row 1, bank 0</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>Row 1, bank 1</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>Row 1, bank 2</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>Row 1, bank P</td>
</tr>
<tr>
<td>*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row N, bank 0</td>
</tr>
<tr>
<td>*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row N, bank 1</td>
</tr>
<tr>
<td>*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Row N, bank 2</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>Row N, bank P</td>
</tr>
</tbody>
</table>

A. M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

Figure 2-5. DDR3 SDRAM Column, Row, and Bank Access (EBANK=0)

A. M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.
### 2.6 DDR3 Memory Controller Interface

To move data efficiently from on-chip resources to an external DDR3 SDRAM device, the DDR3 memory controller makes use of a Command FIFO, a Write Data FIFO, a Write Status FIFO, a Read Command FIFO, and two Read Data FIFOs and command and data schedulers. Table 2-6 describes the purpose of each FIFO. Figure 2-6 shows the block diagram of the DDR3 memory controller FIFOs. Commands, write data, and read data arrive at the DDR3 memory controller parallel to each other. The same peripheral bus is used to write and read data from external memory as well as internal memory-mapped registers (MMR).

#### Table 2-6. DDR3 Memory Controller FIFO Description

<table>
<thead>
<tr>
<th>FIFO</th>
<th>Description</th>
<th>Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>Stores all commands coming from on-chip requestors</td>
<td>16</td>
</tr>
<tr>
<td>Write Data</td>
<td>Stores write data coming from on-chip requestors to memory</td>
<td>20 (512-bit wide)</td>
</tr>
<tr>
<td>Write Status</td>
<td>Stores the write status information for each write transaction</td>
<td>7</td>
</tr>
<tr>
<td>Read Command</td>
<td>Stores all read transactions that are to be issued to on-chip requestors</td>
<td></td>
</tr>
<tr>
<td>SDRAM Read Data</td>
<td>Stores read data coming from SDRAM memory to on-chip requestors</td>
<td>28</td>
</tr>
<tr>
<td>Register Read Data</td>
<td>Stores read data coming from MMRs to on-chip requestors</td>
<td>2 (256-bit wide)</td>
</tr>
</tbody>
</table>

#### Figure 2-6. DDR3 Memory Controller FIFO Block Diagram

* Not all devices have this feature. Check the ECC section for details.
2.6.1 Arbitration

The DDR3 memory controller performs command reordering and scheduling in an attempt to achieve efficient transfers with maximum throughput. The goal is to maximize the utilization of the data, address, and command buses while hiding the overhead of opening and closing DDR3 SDRAM rows. Command reordering takes place within the command FIFO.

The DDR3 memory controller examines all the commands stored in the command FIFO to schedule commands to the external memory. For each master, the DDR3 memory controller reorders the commands based on the following rules:

• The DDR3 controller will advance a read command before an older write command from the same master if the read is to a different block address (2048 bytes) and the read priority is equal to or greater than the write priority.

• The DDR3 controller will block a read command, regardless of the master or priority if that read command is to the same block address (2048 bytes) as an older write command.

Thus, one pending read or write for a master might exist.

• Among all pending reads, the DDR3 controller selects all reads that have their corresponding SDRAM banks already open.

• Among all pending writes, the DDR3 controller selects all writes that have their corresponding SDRAM banks already open.

As a result of the above reordering, several pending reads and writes may exist that have their corresponding banks open. The highest priority read is selected from pending reads, and the highest priority write from pending writes. If two or more commands have the highest priority, the oldest command is selected. As a result, there might exist a final read and a final write command. Either the read or the write command will be selected depending on the value programmed in the Section 4.27.

The DDR3 controller supports interleaving of commands for maximum efficiency. In other words, the controller will partially execute one command and switch to executing another higher priority command before finishing the first command.

Apart from reads and writes the DDR3 controller also needs to open and close SDRAM banks, and maintain the refresh counts for an SDRAM. The priority of SDRAM commands with respect to refresh levels are as follows:

1. (Highest priority) SDRAM refresh request due to Refresh Must level of refresh urgency reached.
2. Read request without a higher priority write (from the reordering algorithm above)
3. Write request.
4. SDRAM Activate commands.
5. SDRAM Deactivate commands.
6. SDRAM Power-Down request.
7. SDRAM refresh request due to Refresh May or Release level of refresh urgency reached.
8. (Lowest priority) SDRAM self-refresh request.
2.6.2 **Command Starvation**

While running the scheduling algorithm described in Section 2.6.1, the DDR3 memory controller is subject to the following:

1. A continuous stream of high priority commands can block lower priority commands.
2. A continuous stream of SDRAM commands to a row in an open bank can block commands to another row in the same bank.

To avoid a continuous blocking effect, the priority of the oldest command is momentarily raised over all other commands when the latency counter for the oldest command expires. The latency counter for the oldest command (PR_OLD_COUNT) is configurable in the Latency Configuration Register. In addition to this, the order of command accesses can also be tailored by grouping commands into two categories or “classes” and assigning different latency expiration counters to each category. See Section 2.6.4 for more information.

On top of the above scheduling, the highest priority condition is a removal of hard or soft reset. If this occurs, the DDR3 controller abandons whatever it is currently doing and commences its startup sequence. In this case, commands and data stored in the FIFOs are lost. The startup sequence also commences whenever the SDRAM Config register is written and INITREF_DIS field in SDRAM Refresh Control register (SDRFC) is set to 0. In this case, commands and data stored in the FIFOs are not lost. The DDR3 controller will ensure that in-flight read or write transactions to the SDRAM are complete before starting the initialization sequence.

2.6.3 **Possible Race Condition**

A race condition may exist when certain masters write data to the DDR3 memory controller. For example, if master A passes a software message via a buffer in DDR3 memory and does not wait for indication that the write completes, when master B attempts to read the software message it may read stale data and therefore receive an incorrect message. In order to confirm that a write from master A has landed before a read from master B is performed, master A must wait for the write to complete before indicating to master B that the data is ready to be read. For example, an EDMA transfer controller should wait for the transfer completion event to occur before signaling a CorePac to read the message from DDR3.

If master A does not wait for indication that a write is complete, it must perform the following workaround:

1. Perform the required write.
2. Perform a dummy write to the DDR3 memory controller module ID and revision register.
3. Perform a dummy read to the DDR3 memory controller module ID and revision register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.

2.6.4 **Class of Service**

The commands in the Command FIFO can be mapped to two classes of service: 1 and 2. The mapping of commands to a particular class of service can be done based on the priority or the master ID. The mapping based on priority can be done by setting the appropriate values in the Priority to Class of Service Mapping register. The mapping based on master ID can be done by setting the appropriate values of master ID and the masks in the Master ID to Class of Service Mapping registers.

There are three master ID and mask values that can be set for each class of service. In conjunction with the masks, each class of service can have a maximum of 144 master IDs mapped to it. For example, a master ID value of 0xFF along with a mask value of 0x3 will map all master IDs from 0xF8 to 0xFF to that particular class of service. By default all commands will be mapped to class of service 2.

Each class of service has an associated latency counter. The value of this counter can be set in the Latency Configuration register. When the latency counter for a command expires, i.e., reaches the value programmed for the class of service that the command belongs to, that command will be the one that is executed next. If there is more that one command that has expired latency counters, the command with the highest priority will be executed first. One exception to this rule is as follows: if any of the commands with the expired latency counters is also the oldest command in the queue, that command will be executed first irrespective of priority. This is done to prevent a continuous block effect as described in Section 2.6.1.
2.7 Refresh Scheduling

The DDR3 controller uses two counters to schedule AUTO REFRESH commands:

- a 13-bit decrementing refresh interval counter
- a four-bit refresh backlog counter

The interval counter is loaded with the REFRESH_RATE field value at reset. The interval counter decrements by one each cycle until it reaches zero at which point it reloads from REFRESH_RATE and restarts decrementing. The counter also reloads and restarts decrementing whenever the REFRESH_RATE field is updated.

The refresh backlog counter records the number of AUTO REFRESH commands that are currently outstanding. The backlog counter increments by one each time the interval counter reloads (unless it has reached its maximum value of 15). The backlog counter decrements by one each time the DDR3 controller issues an AUTO REFRESH command (unless it is already at zero). Following a refresh command, the DDR3 memory controller waits T_RFC cycles, defined in the SDRAM timing 3 register (SDTIM1), before rechecking the refresh urgency level.

For the range of values that the backlog counter can take, there are three levels of urgency with which the DDR3 controller should perform an auto refresh cycle (in which it issues AUTO REFRESH commands), as follows:

- Refresh May level is reached whenever the backlog count is greater than 0, to indicate that there is a refresh backlog, so if the DDR3 controller is not busy and none of the SDRAM banks are open, it should perform an auto refresh cycle.
- Refresh Release level is reached whenever the backlog count is greater than 4, to indicate that the refresh backlog is getting high, so if the DDR3 controller is not busy it should perform an auto refresh cycle even if any banks are open.
- Refresh Must level is reached whenever the backlog count is greater than 7, to indicate that the refresh backlog is getting excessive and the DDR3 controller should perform an auto refresh cycle before servicing any new memory access requests.

The DDR3 controller starts servicing new memory accesses after Refresh Release level is cleared. If any of the commands in the Command FIFO have class-of-service latency counters that are expired, the DDR3 controller will not wait for Refresh Release level to be cleared but will only perform one refresh command and exit the refresh state.

The refresh counters do not operate when SDRAM has been put into self-refresh mode. Also, the refresh counters start tracking the missed refreshes only after initialization is complete.

2.8 Self-Refresh Mode

The DDR3 memory controller supports self-refresh mode for low power. The controller maintains DDRCKE low to maintain the self-refresh state. In self-refresh, the memory maintains valid data while consuming a minimal amount of power.

Self-refresh mode is set by programming the LP_MODE in the Power Management Control register (PMCTL) to 2. The controller automatically puts the SDRAM into self-refresh after the controller is idle for SR_TIM DDR3CLKOUT cycles. (See Section 4.9 for more information.)

The memory is brought out of self-refresh under any of the following conditions:

- If the LP_MODE field is set not equal to 2
- A memory access is requested
- SR_TIM bit in PMCTL is cleared

In a situation where memory accesses and a self-refresh command are sent to the DDR3 memory controller, the controller always prioritizes the memory access. Thus, if a reset is triggered when memory accesses and a self-refresh command are queued in the controller, it is likely that self-refresh will not be entered.

The user must ensure that all memory accesses have been completed, and verify that self-refresh is set in the STATUS register before initiating a reset.
NOTE: The DDR3 memory controller completes all pending memory accesses and refreshes before it puts SDRAM into self-refresh. If a request for a memory access is received, the DDR3 memory controller services the memory access request then returns to the self-refresh state upon completion.

2.8.1 Extended Temperature Range

The normal operating temperature range for DDR3 SDRAMs is typically 0 to 85°C. When operating in self-refresh mode within the extended temperature range (85°C to 95°C), the memory device must be refreshed at 2× the normal refresh rate. For this purpose, either the auto self-refresh (ASR) or self-refresh temperature (SRT) feature should be used. Under normal operating conditions, both ASR and SRT should be disabled (equal to 0). When ASR is enabled, the internal refresh rate of the SDRAM automatically switches to 2× the refresh rate when the operating case temperature Tc is greater than 85°C when in Self-refresh mode. When SRT is enabled, the internal refresh rate of the SDRAM is forced to 2× the refresh rate regardless of Tc. Both SRT and ASR cannot be enabled at the same time. One must be disabled if the other is enabled.

NOTE: ASR and SRT are used only in self-refresh mode (LP_MODE=0×2). When operating in extended temperature range with LP_MODE = 0×0 (not in self-refresh), it is up to the user to program the manual refresh rate to 2× the normal refresh rate for proper operation. If it is guaranteed that Tc will exceed 85°C, it is recommended that SRT=1 to force the refresh rate to 2× regardless of operating temperature.

2.9 Reset Considerations

The DDR3 memory controller can be reset through a hard reset or a soft reset. A hard reset resets the state machine, the FIFOs, and the internal registers. A soft reset only resets the state machine and the FIFOs. A soft reset does not reset the internal registers except for the interrupt registers. Register accesses cannot be performed while either reset is asserted.

The DDR3 memory controller hard and soft reset are derived from device-level resets. Table 2-7 shows the relationship between the device-level resets and the DDR3 memory controller resets. For more information on the device-level resets, see the device-specific data manual.

<table>
<thead>
<tr>
<th>DDR3 Memory Controller</th>
<th>Reset Effect</th>
<th>Initiated by</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hard reset</td>
<td>Resets control logic and all DDR3 memory controller registers</td>
<td>• Please refer to the reset controller description in your device data manual</td>
</tr>
<tr>
<td>Soft reset</td>
<td>Resets control logic and interrupt registers</td>
<td>• Please refer to the reset controller description in your device data manual</td>
</tr>
</tbody>
</table>
2.10 Turnaround Time

Table 2-8 shows the turn around time that the DDR3 memory controller introduces on the data bus for various back-to-back accesses. Note that the DDR3 memory controller takes advantage of the CAS latencies and packs the commands as close as possible on the control bus to introduce the following turn around time on the data bus.

<table>
<thead>
<tr>
<th>Previous Access</th>
<th>Next Access</th>
<th>Turnaround Time (DDR3 memory clock cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDRAM Write</td>
<td>SDRAM Write to same chip select</td>
<td>0</td>
</tr>
<tr>
<td>SDRAM Write</td>
<td>SDRAM Write to different chip select</td>
<td>T CSTA + 1</td>
</tr>
<tr>
<td>SDRAM Read</td>
<td>SDRAM Read to same chip select</td>
<td>0</td>
</tr>
<tr>
<td>SDRAM Read</td>
<td>SDRAM Read to different chip select</td>
<td>T CSTA + 1</td>
</tr>
<tr>
<td>SDRAM Write</td>
<td>SDRAM Read</td>
<td>T WTR + 1 + CL</td>
</tr>
<tr>
<td>SDRAM Read</td>
<td>SDRAM Write</td>
<td>T_RTW + 1</td>
</tr>
</tbody>
</table>

2.11 DDR3 SDRAM Memory Initialization

DDR3 SDRAM initialization is achieved by programming memory mapped registers in the DDR3 controller configuration space and the DDR3 PHY configuration space in a specific sequence. The software programming sequence is described in the Keystone II DDR3 Initialization Application Note. This sequence of software programming steps, causes the controller to issue MRS and EMRS commands to program mode and extended mode registers in the SDRAM device. These registers control parameters such as burst type, burst length, and CAS latency. The sequence of commands during the initialization sequence described in Section 2.11.1. The initialization sequence performed by the DDR3 memory controller is compliant with the JESD79-3E specification.

The DDR3 memory controller performs the initialization sequence under the following conditions:

• Automatically following a hard or soft reset (see Section 2.11.1)
• Following a write to the SDRAM configuration register (SDCFG) (see Section 2.11.1)

At the end of the initialization sequence, the DDR3 memory controller performs an auto-refresh cycle, leaving the DDR3 memory controller in an idle state with all banks deactivated.

During the initialization sequence, the DDR3 memory controller issues MRS and EMRS commands that configure the DDR3 SDRAM mode registers with the values described in Table 2-9 and Table 2-10.

When a reset occurs, the DDR3 memory controller immediately begins the initialization sequence. Under this condition, commands and data stored in the DDR3 memory controller FIFOs will be lost. However, when the initialization sequence is initiated by a write to the SDCFG Register, data and commands stored in the DDR3 memory controller FIFOs will not be lost and the DDR3 memory controller will ensure read and write commands are completed before starting the initialization sequence.

As the default values of the Mode Register (MR) and extended mode registers 1, 2, 3 are not defined, contents of Mode/Extended Mode Registers must be fully initialized and/or reinitialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode/Extended Mode Registers can be altered by re-executing the MRS/EMRS command during normal operation. The mode/extended mode registers are selected by varying the bank address bits BA [1:0]. BA [2] and A [15:13] are reserved for future use and must be programmed to zero.

The extended mode register 3 is configured with a value of 0h.
### Table 2-9. DDR3 SDRAM Extended Mode Register 2 Configuration

<table>
<thead>
<tr>
<th>Mode Register Bit</th>
<th>Mode Register Field</th>
<th>Init Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-11</td>
<td>Reserved</td>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10-9</td>
<td>Rtt_WR</td>
<td>SDCFG.DYN _ODT and MR2.RTTWR</td>
<td>Dynamic ODT value from SDRAM Config Register and MR2.RTTWR (program both to same value)</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>SRT</td>
<td>MR2 .SRT</td>
<td>Self-Refresh temperature range from MR2 register</td>
</tr>
<tr>
<td>6</td>
<td>ASR</td>
<td>MR2 .ASR</td>
<td>Auto self-refresh enable from MR2 register</td>
</tr>
<tr>
<td>5-3</td>
<td>CWL</td>
<td>SDCFG.CWL</td>
<td>CAS write latency from SDRAM Config register</td>
</tr>
<tr>
<td>2-0</td>
<td>PASR</td>
<td>SDRCR.PASR</td>
<td>Partial array self-refresh from SDRAM Refresh Control register</td>
</tr>
</tbody>
</table>

(1) Bank Address bits to select EMR 2 are BA [1:0] = 0x2.

### Table 2-10. DDR3 SDRAM Extended Mode Register 1 Configuration

<table>
<thead>
<tr>
<th>Mode Register Bit</th>
<th>Mode Register Field</th>
<th>Init Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Qoff</td>
<td>0x0</td>
<td>Output Buffer Enabled</td>
</tr>
<tr>
<td>11</td>
<td>TDQS</td>
<td>0x0</td>
<td>TDQS enable/disable</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>Rtt_nom</td>
<td>SDCFG.DDRTERM[2]</td>
<td>DDR3 termination resistor value from SDRAM Config register</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>Level</td>
<td>0x0</td>
<td>Write Leveling Disabled</td>
</tr>
<tr>
<td>6</td>
<td>Rtt_nom</td>
<td>SDCFG.DDRTERM[1]</td>
<td>DDR3 termination resistor value from SDRAM Config register</td>
</tr>
<tr>
<td>5</td>
<td>Output driver impedance</td>
<td>SDCFG.SDRAM _DRIVE[1]</td>
<td>SDRAM drive strength from SDRAM Config register</td>
</tr>
<tr>
<td>4-3</td>
<td>Additive Latency</td>
<td>0x0</td>
<td>Additive latency = 0</td>
</tr>
<tr>
<td>2</td>
<td>Rtt_nom</td>
<td>SDCFG.DDRTERM[0]</td>
<td>DDR3 termination resistor value from SDRAM Config register</td>
</tr>
<tr>
<td>1</td>
<td>Output driver impedance</td>
<td>SDCFG.SDRAM _DRIVE[0]</td>
<td>SDRAM drive strength from SDRAM Config register</td>
</tr>
<tr>
<td>0</td>
<td>DLL Enable</td>
<td>0x0</td>
<td>DLL enable/disable from SDRAM Config register</td>
</tr>
</tbody>
</table>

(1) Bank Address bits to select EMR 1 are BA [1:0] = 0x1.

### Table 2-11. DDR3 SDRAM Mode Register 0 Configuration

<table>
<thead>
<tr>
<th>Mode Register Bit</th>
<th>Mode Register Field</th>
<th>Init Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>DLL control for Precharge PD</td>
<td>0x0</td>
<td>Fast exit active powerdown exit time</td>
</tr>
<tr>
<td>11-9</td>
<td>Write Recovery</td>
<td>SDTIM1.T_WR</td>
<td>Write recovery for auto precharge from SDAM Timing 1 Register</td>
</tr>
<tr>
<td>8</td>
<td>DLL Reset</td>
<td>0x1</td>
<td>DLL Reset</td>
</tr>
<tr>
<td>7</td>
<td>Mode</td>
<td>0x0</td>
<td>Normal Mode from SDRAM Config Register</td>
</tr>
<tr>
<td>6-4</td>
<td>CAS Latency</td>
<td>SDCFG.CL[3:1]</td>
<td>CAS Latency from SDRAM Config Register</td>
</tr>
<tr>
<td>3</td>
<td>Read Burst Type</td>
<td>0x0</td>
<td>sequential/interleave burst type</td>
</tr>
<tr>
<td>2</td>
<td>CAS Latency</td>
<td>SDCFG.CL[0]</td>
<td>CAS Latency from SDRAM Config Register</td>
</tr>
<tr>
<td>1-0</td>
<td>Burst length</td>
<td>0x0</td>
<td>Burst length of 8</td>
</tr>
</tbody>
</table>

(1) Bank Address bits to select MR are BA [1:0] = 0x0.
2.11.1 DDR3 Initialization Sequence

On coming out of reset if the SDRAM_TYPE field in the SDRAM Config register is equal to 3 and the INITREF_DIS bit in the SDRAM Refresh Control register is set to 0, the DDR3 Controller performs a DDR3 SDRAM initialization sequence. The sequence follows the JEDEC standard. Please refer to the JEDEC spec for the initialization sequence.

The DDR3 memory controller also performs the initialization sequence whenever the SDRAM Config register is written. But in this case, the sequence starts at step 3. The DDR3 memory controller does not perform any transactions until the DDR3 initialization sequence is complete.

2.12 Leveling

The DDR3 controller supports leveling to compensate for the command and DQS skew as a result of the fly-by topology. Leveling compensates the skew for both reads and writes. Unlike Keystone I devices, the controller in Keystone II devices does not require the user to program initial leveling values (INIT_RATIOs) to establish the starting point of the search window before triggering hardware leveling. The logic inside the DDR PHY is able to automatically search for and determine the optimal starting point when leveling and training sequence is triggered by writing to the PHY Initialization Register (PIR). Please refer to the DDR3 initialization application note for software programming sequence to initialize DDR3 on Keystone II devices.

2.13 Interrupt Support

The DDR3 memory controller generates one error interrupt. Please check the section on interrupts in the device data manual for details on how the ECC error interrupt is routed. The source of the interrupt can be checked in the Interrupt Raw Status Register.

2.14 EDMA Event Support

The DDR3 memory controller is a DMA slave peripheral and therefore does not generate EDMA events. Data read and write requests may be made directly by masters including the EDMA controller.

2.15 Emulation Considerations

The DDR3 memory controller will remain fully functional during emulation halts to allow emulation access to external memory.

2.16 ECC

For data integrity, the DDR3 memory controller supports ECC on the data written to or read from the ECC protected address ranges in memory. The ECC algorithm is a single-error-correct-double-error-detect (SECDED) algorithm and uses the (72,64) Hamming code. Eight-bit ECC is calculated over 64-bit data quanta. ECC is enabled by setting ECC_EN = 1 in the ECC Control register and DXEN=1 in the DATX8 8 General configuration register (DX8GCR register). ECC is disabled by setting ECC_EN and DXEN=0. By default, ECC_EN=0 and DXEN=1. The address ranges can be programmed in the ECC Address Range 1 and 2 register. The system must ensure that any bursts accesses starting in the ECC protected region must not cross over into the unprotected region and vice-versa. The controller on some KeyStone II devices supports an additional read-modify-write (RMW) feature. This feature can be enabled by programming RMW_EN = 1 in the ECC Control register.

For memory controllers that do not support RMW, all accesses to ECC protected space must be 64-bit aligned and multiples of 64 bits.

For memory controllers that support RMW, ECC protected space can be used regardless of the alignment or quanta conditions, if RMW_EN=1. If RMW_EN=0, the controller will again assume the same 64-bit alignment and quanta conditions.

Silicon rev 1.0 and 1.1 of K2K and K2H device family do not support RMW. Other K2K and K2H silicon revisions and all revisions in the K2E and K2L family support RMW.
NOTE: The ECC is stored inside the SDRAM during writes. After enabling ECC and before performing any functional reads or writes, all DDR3 memory space configured as ECC should be first written with known data that is 64-bit aligned and multiples of 64-bit. This is to ensure the correct ECC values are stored in the ECC SDRAM prior to functional use.

If the RMW ECC feature is not supported (or is disabled for the devices that do support it), a write access with byte count that is not a multiple of 64-bit quanta, or with a non-64-bit-aligned address performed within the address range protected by ECC, will result in a write ECC error interrupt. In this case, the DDR3 memory controller writes to the SDRAM. However, the ECC value written to the SDRAM will be corrupted. The controller will NOT trigger a write ECC error if a write access with a multiple of 64-bit quanta and with 64-bit-aligned address but with partial byte enables set, is performed within the address range protected by ECC (this can be the case if the Multicore Navigator PktDMA writes to a descriptor placed in DDR3). The data and corrupted ECC value will be written to the SDRAM, but will go undetected and may be detected as 1-bit or 2-bit errors when read back.

When RMW is enabled (ECC_EN=1 and RMW_EN=1), the controller will perform a RMW operation if a write results in a sub-64-bit access. For details on how the RMW operations are performed, refer to Section 2.16.1.1.

The ECC is read and verified during reads if ECC_EN=1 and ECC_VERIFY_EN=1 in the ECC control register. Similar to RMW, K2K and K2H silicon revisions 1.0 and 1.1 do not support ECC_VERIFY_EN, but K2K and K2H revisions beyond rev1.1 and all K2E/K2L revisions support it. For the latter, ECC verification is disabled during reads if ECC_VERIFY_EN=0.

If there is a one-bit error, the DDR3 memory controller corrects the data and sends it on the read interface. For 2-bit errors, the DDR3 memory controller generates a read ECC error interrupt. Note that in both cases, the data in SDRAM is still corrupted. It is the responsibility of system software to go and correct the data in the SDRAM.

NOTE: The user should note that the single error correct, double error detect (SECDED) algorithm used by the ECC logic cannot detect more than 2-bit errors per 64-bit quanta. For these errors, the output of the algorithm is unknown i.e. it may erroneously detect as 1-bit, 2-bit or no errors. More than 2-bit errors are expected to be very rare in a well designed system.

See Section 4.24 through Section 4.26 for ECC-related registers.

NOTE: To disable ECC, program ECC_EN=0 in the ECC Control register (inside DDR3 controller) and DXEN=0 in the DATX8 8 General Configuration Register (see the DDR PHY registers) before triggering the leveling sequence in the PHY Initialization Register. By default, DXEN =1 so ECC byte lane will be enabled from the perspective of the PHY.

### 2.16.1 ECC Feature Enhancements

#### 2.16.1.1 Read-modify-write

As seen in Figure 2-6, the Read-Modify-Write (RMW) module is placed prior to internal FIFO logic of the controller. The RMW module splits all writes to an SDRAM into a burst size of 64-bytes and converts any sub-quanta write into a RMW of aligned burst size (64 bytes). A quanta is defined as 8 bytes. Read bursts are not fragmented.

The RMW module has been designed such that normal aligned ECC block read or write bursts are unaffected. That is, they pass through without adding delay as well as maintaining all memory coherence. If RMW module detects write data that does not form a complete quanta, a read for that burst (64 bytes) is then issued by the controller. This return data burst is then merged with the sub-quanta write data and the modified 64-byte burst is then written to the SDRAM. For write commands with partial byte enables (such as those introduced by a Packet DMA peripheral), the active byte enables are passed through without any latency, but a write-read-modify-write (wRMW) is performed for the burst with partial byte enables.
The controller maintains coherence across all outstanding commands in the command FIFO whether or not they are affected by the RMW module and also follows the normal command arbitration outlined in section 2.6.1. The above RMW process for sub-quanta writes means the execution of the write command will be delayed compared to if the command was not sub-quanta and was 64-bit aligned.

2.16.1.2 Logging 1-bit ECC Error Address

For 1-bit ECC error, the controller logs the starting address of the SDRAM burst in an internal 2-deep address FIFO. This internal FIFO stores the first two 1-bit ECC errors. The 1-Bit ECC Error Address Log register will display the address on top of the internal FIFO. Software must write a 0x1 to the 1-bit ECC Address Log register to pop the FIFO and display the next address stored. The FIFO will be loaded with the address for the next 1-bit ECC error if it is not full. It must be noted that no address comparison will be performed, i.e., if a single address has ECC errors back-to-back, that address will be logged twice.

2.16.1.3 Counting the Number of 1-bit ECC Errors

The number of 1-bit ECC errors can be counted using the 1-Bit ECC Error Count register. The controller also supports programming a threshold and a window in the 1-Bit ECC Error Threshold register. The window is programmed in number of refresh periods. When the programmed window value is a 0, i.e., window is disabled, and the internal error count exceeds the programmed threshold, the controller will generate a 1-bit ECC error interrupt. When servicing the interrupt, software will need to set the error count with a value less than the threshold for the interrupt to be triggered again. When the programmed window value is non-zero, i.e., window is enabled, the controller will generate a 1-bit ECC error interrupt only if the internal error count exceeds the programmed threshold in that window. The internal error count is reset every time the window expires. Software can use this to gauge the degree of 1-bit ECC errors occurring in the system.

2.16.1.4 Diagnosing the Data bus bit on which 1-bit ECC Errors Occur

For diagnosis, the controller supports 1-Bit ECC Error Distribution register that represent whether an error has occurred in a given bit location on the data. This is advantageous to detect whether the errors are random or systemic. The distribution register will be overlay of all 1-bit ECC errors until the software clears the register. Therefore, multiple bits could be set as a result of multiple 1-bit ECC errors occurring over multiple read accesses.

For 2-bit ECC errors, the controller will generate a 2-bit ECC error interrupt. It must be noted that the controller will detect but not correct 2-bit ECC errors. The controller will generate an ECC error interrupt and send the resultant data from the ECC correction logic. The read data received from the memory may have further been corrupted by the ECC correction logic since it will have attempted to correct the read data but failed due to uncorrectable error.

2.16.1.5 Logging 2-bit ECC Error Address

For all uncorrectable ECC errors listed above, the controller will log the starting address of the SDRAM burst in the 2-Bit ECC Error Address Log register. The register will show the address of the first uncorrectable error. After the software clears the register, it will be loaded with the address for the next uncorrectable error.

Please check the section on interrupts in the device data manual for details on how the ECC error interrupt is routed. The source of the ECC error interrupt can be checked in the Interrupt Raw Status Register.
### 2.17 Data Bus Obfuscation

For security, the controller supports obfuscation for data written to the SDRAM. Data written to the memory mapped registers is not obfuscated.

**NOTE:** Obfuscation is available only on secure TI SoCs. For more information, contact a TI sales office for additional information.

The obfuscation scheme is shown in the figure below.

**Figure 2-7. Data Bus Obfuscation**

Obfuscation is enabled by setting the OBFUSCATION_ENABLE bit inside the Security Manager to 1. This causes the obfuscation key to be latched inside the controller. The 16-bit key should be programmed by software inside the Security Manager.

**NOTE:** Since the key is latched when obfuscation is enabled, the key should not be modified further.

The key is further modified to create a 64-bit new key. Data going out from the controller during writes will be obfuscated and data coming back during reads will be de-obfuscated. As seen from the figure, the obfuscation logic makes use of the upper address bits to ensure that obfuscation is different for different regions of memory.

Further, the data is also XOR’d with four copies of the 16-bit rotated address and the new key to ensure that obfuscation is also unique for each 1KB page of memory.

Enabling obfuscation does not increase the latency on command execution.
2.18 Power Management

2.18.1 SDRAM Self-Refresh Mode

(See Section 2.8.)

2.18.2 SDRAM Power-Down Mode

The DDR3 memory controller supports power-down mode. Automatic power-down is enabled by setting the LP_MODE field in the Power Management Control register (PMCTL) to 4. The memory is put into power-down after the controller is idle for PD_TIM number of DDR3CLKOUT cycles. In power-down mode, the DDR3 memory controller does not stop the clocks to the memory. The controller maintains DDRCKE low to maintain the power-down state. When the SDRAM is in power-down, the DDR3 memory controller services register accesses as normal.

The memory is brought out of power-down under any of the following conditions:

- If the LP_MODE field is set not equal to 4
- A memory access is requested
- Refresh Must level is reached

2.19 Performance Monitoring

The DDR3 controller provides a set of performance counter registers which can be used to monitor or calculate the bandwidth and efficiency of the DDR traffic. The counters can be configured to count events such as total number of SDRAM accesses, SDRAM activates, reads, write and so on. The Performance Counter 1 and 2 Registers (PERF_CNT_1 and PERF_CNT_2) act as two 32-bit counters that are able to count events independent of each other. To provide more granularity the counters can also be configured to filter events originating from a particular master or address space. The events to be counted and filter enabled are programmed in the Performance Counter Config Register (PERF_CNT_CFG). The actual value of the filter is programmed in Performance Counter Master Region Select Register (PERF_CNT_SEL). The counters start counting the events independently when commands enter the Command FIFO.

The CNTRN_CFG (N=1,2) fields in the PERF_CNT_CFG register are used to select the event for the counter to count. The PERF_CNT_CFG also includes options to enable or disable the master (CNTRN_MSTID_EN) and address space (CNTRN_REGION_EN) filters for each counter. The filters are disabled by default. If the respective filters are enabled, the master ID value and region select options can be programmed in the PERF_CNT_SEL register. It should be noted that the master ID and region select filters apply only to a certain subset of events that can be counted. The table below shows the events for which the filters are applicable.
### Table 2-12. Performance Counter Filter Configuration

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Total SDRAM accesses</td>
<td>NA</td>
<td>0 - Disable, 1 - Enable</td>
</tr>
<tr>
<td>0x1</td>
<td>Total SDRAM activates</td>
<td>NA</td>
<td>0 - Disable, 1 - Enable</td>
</tr>
<tr>
<td>0x2</td>
<td>Total Reads</td>
<td>0 - Disable, 1 - Enable</td>
<td>0 - Disable, 1 - Enable</td>
</tr>
<tr>
<td>0x3</td>
<td>Total Writes</td>
<td>0 - Disable, 1 - Enable</td>
<td>0 - Disable, 1 - Enable</td>
</tr>
<tr>
<td>0x4</td>
<td>Number of DDR/2 clock cycles Command FIFO is full</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0x5</td>
<td>Number of DDR/2 clock cycles Write Data FIFO is full</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0x6</td>
<td>Number of DDR/2 clock cycles Read Data FIFO is full</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0x7</td>
<td>Number of DDR/2 clock cycles Write Status FIFO is full</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0x8</td>
<td>Number of priority elevations</td>
<td>0 - Disable, 1 - Enable</td>
<td>0 - Disable, 1 - Enable</td>
</tr>
<tr>
<td>0x9</td>
<td>Number of DDR/2 clock cycles that a command was pending</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0xA</td>
<td>Number of DDR/2 clock cycles for which DDR i/f was transferring data</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0xB (only applies to devices that support RMW)</td>
<td>Number of SDRAM read bursts resulting from RMW and wRMW accesses</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0xC (only applies to devices that support RMW)</td>
<td>Number of SDRAM write bursts resulting from RMW and wRMW accesses</td>
<td>NA</td>
<td>0 - Disable, 1 - Enable</td>
</tr>
<tr>
<td>0x D - 0XF</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

See Chapter 4 for details on Performance counter registers.
The following sections show various ways to connect the DDR3 memory controller to DDR3 memory devices. The steps required to configure the DDR3 memory controller for external memory access are also described.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 Connecting the DDR3 Memory Controller to DDR3 SDRAM</td>
<td>38</td>
</tr>
<tr>
<td>3.2 Configuring DDR3 Memory Controller Registers to Meet DDR3 SDRAM Specifications</td>
<td>42</td>
</tr>
</tbody>
</table>
3.1 Connecting the DDR3 Memory Controller to DDR3 SDRAM

The following figures show high-level views of the three memory topologies:

- Figure 3-1
- Figure 3-2
- Figure 3-3

All DDR3 SDRAM devices must comply with the JESD79-3C standard.

Not all of the memory topologies shown may be supported by your device. For more information, see the device-specific data manual.

The printed-circuit-board (PCB) layout rules and connection requirements between the DSP and the memory device are described in a separate document. For more information, see the device-specific data manual.
Figure 3-1. Connecting Two 16 MB x 16 x 8 Banks (4Gb Total) Devices
Figure 3-2. Connecting One 8 MB x 16 x 8 Banks (1Gb Total) Device
Figure 3-3. Connecting Two 16 MB x 8 x 8 Banks (2Gb Total) Devices
3.2 Configuring DDR3 Memory Controller Registers to Meet DDR3 SDRAM Specifications

The DDR3 memory controller allows a high degree of programmability for shaping DDR3 accesses. This provides the DDR3 memory controller with the flexibility to interface with a variety of DDR3 devices. By programming the SDRAM Configuration Register (SDCFG), SDRAM Refresh Control Register (SDRFC), SDRAM Timing 1 Register (SDTIM1), SDRAM Timing 2 Register (SDTIM2), SDRAM Timing 3 Register (SDTIM3) and SDRAM Timing 4 Register (SDTIM4), the DDR3 memory controller can be configured to meet the data sheet specification for JESD79-3E compliant DDR3 SDRAM devices. The timing values also need to be programmed in the DRAM Timing Parameter Registers 0-2 inside the PHY block.

As an example, the following sections describe how to configure each of these registers for access to two 1 Gb, 16-bit wide DDR3 SDRAM devices connected as shown on Figure 3-2, where each device has the following configuration:

- Maximum data rate: 1333 MHz
- Number of banks: 8
- Page size: 1024 words
- CAS latency: 9

It is assumed that the frequency of the DDR3 memory controller clock (DDR3CLKOUT) is set to 666.5 MHz.

3.2.1 Programming the SDRAM Configuration Register (SDCFG)

The SDRAM configuration register (SDCFG) contains register fields that configure the DDR3 memory controller to match the data bus width, CAS latency, number of banks, and page size of the attached DDR3 memory.

Table 3-1 shows the resulting SDCFG configuration.

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
<th>Function Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDRAM_TYPE</td>
<td>0x3h</td>
<td>SDRAM Type Select – DDR3</td>
</tr>
<tr>
<td>NM</td>
<td>1h</td>
<td>To configure the DDR3 memory controller for a 32-bit data bus width.</td>
</tr>
<tr>
<td>CL</td>
<td>10h</td>
<td>To select a CAS latency of 9.</td>
</tr>
<tr>
<td>IBANK</td>
<td>3h</td>
<td>To select 8 internal DDR3 banks.</td>
</tr>
<tr>
<td>EBANK</td>
<td>0</td>
<td>To select only DCE0z to be used.</td>
</tr>
<tr>
<td>PAGESIZE</td>
<td>2h</td>
<td>To select 1024-word page size.</td>
</tr>
</tbody>
</table>

3.2.2 Programming the SDRAM Refresh Control Register (SDRFC)

The SDRAM refresh control register (SDRFC) configures the DDR3 memory controller to meet the refresh requirements of the attached DDR3 device. SDRFC also allows the DDR3 memory controller to enter and exit self refresh.

The REFRESH_RATE field in SDRFC is defined as the rate at which the attached DDR3 device is refreshed in DDR3 cycles. The value of this field may be calculated using the following equation:

\[
\text{REFRESH RATE} = \frac{\text{DDR3CLKOUT frequency} \times \text{memory refresh period}}{1000}\times 2^n
\]

According to the DDR3 JEDEC standard, on reset de-assertion the DDRCKE pin must remain low for at least 500µs before becoming active during power-up initialization. This is achieved by programming a 500 µs refresh period in the SDRFC prior to initialization.

Table 3-2 shows the DDR3-1333 refresh rate specification.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{REFI})</td>
<td>Refresh interval to be programmed during power-up initialization</td>
<td>500 µs</td>
</tr>
<tr>
<td>(t_{	ext{REFI}})</td>
<td>Average Periodic Refresh Interval (after power-up initialization)</td>
<td>7.8 µs</td>
</tr>
</tbody>
</table>
The refresh rate of 500 µs to be programmed during power-up initialization should be calculated equal to a divide-by-16 value as follows. The DDR3 controller takes care of the divide-by-16 internal logic.

\[
\text{REFRESH\_RATE} = \frac{(666.5 \text{ MHz} \times 500 \mu\text{s})}{16} = 515\text{Ch} \quad (2)
\]

After power-up initialization, the refresh rate of 7.8 µs should be programmed as follows:

\[
\text{REFRESH\_RATE} = 666.5 \text{ MHz} \times 7.8 \mu\text{s} = 1450\text{h} \quad (3)
\]

**NOTE:** SRT and ASR should be programmed in the MR2 register inside the DDR PHY config space.

### 3.2.3 Configuring SDRAM Timing Registers (SDTIM1, SDTIM2, SDTIM3, SDTIM4)

The SDRAM timing 1 register (SDTIM1), SDRAM timing 2 register (SDTIM2), SDRAM timing 3 register (SDTIM3), SDRAM timing 4 register (SDTIM4) configure the DDR3 memory controller to meet the datasheet timing parameters of the attached DDR3 device. Each field in SDTIM1, SDTIM2, SDTIM3, SDTIM4 corresponds to a timing parameter in the DDR3 datasheet specification. Table 3-3, Table 3-4, and Table 3-5 show the register field name and corresponding DDR3 datasheet parameter name and value. These tables also provide a formula to calculate the register field value and show the resulting calculation. Each of the equations includes a minus 1 because the register fields are defined in terms of DDR3 clock cycles minus 1. (See Section 4.5- Section 4.8 for more information.). Some of these timing parameters will also have to be programmed in the DRAM Timing Parameter Registers (See Section 4.49 - Section 4.51).

The objective behind programming the timing values is to calculate them in terms of DRAM clock cycles and round off to the next highest integer value. For example, at 666.5 MHz, the clock period \(t_{\text{CK}} = 1.5\) ns. So 13.5 ns will be programmed as \((13.5/1.5) - 1 = 9 - 1 = 8\) DDR3 clock cycles and 14ns will be 9 DDR3 clock cycles.

**Table 3-3. See the register section for the SDTIM* register where the field exists**

<table>
<thead>
<tr>
<th>Register Field Name</th>
<th>DDR3 SDRAM Datasheet Parameter Name</th>
<th>Description</th>
<th>Datasheet Value (ns)</th>
<th>Formula (Register Field must be &gt;=)</th>
<th>Field Value (h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_RP</td>
<td>(t_{\text{RP}})</td>
<td>Precharge to Activate or Refresh command</td>
<td>13.5</td>
<td>((t_{\text{RP}}/t_{\text{CK}}) - 1)</td>
<td>8</td>
</tr>
<tr>
<td>T_RCD</td>
<td>(t_{\text{RCD}})</td>
<td>Activate command to Read/Write command</td>
<td>13.5</td>
<td>((t_{\text{RCD}}/t_{\text{CK}}) - 1)</td>
<td>8</td>
</tr>
<tr>
<td>T_WR</td>
<td>(t_{\text{WR}})</td>
<td>Write recovery time</td>
<td>6</td>
<td>((t_{\text{WR}}/t_{\text{CK}}) - 1)</td>
<td>3</td>
</tr>
<tr>
<td>T_RAS</td>
<td>(t_{\text{RAS}})</td>
<td>Active to precharge command</td>
<td>36</td>
<td>((t_{\text{RAS}}/t_{\text{CK}}) - 1)</td>
<td>17</td>
</tr>
<tr>
<td>T_RC</td>
<td>(t_{\text{RC}})</td>
<td>Activate to Activate command in same bank</td>
<td>49.5</td>
<td>((t_{\text{RC}}/t_{\text{CK}}) - 1)</td>
<td>20</td>
</tr>
<tr>
<td>T_RRD</td>
<td>(t_{\text{RRD}})</td>
<td>Activate to Activate in different bank</td>
<td>(t_{\text{FAW}} = 30\mu\text{s})</td>
<td>((t_{\text{FAW}}(4t_{\text{CK}})/t_{\text{CK}})) - 1)</td>
<td>4</td>
</tr>
<tr>
<td>T_WTR</td>
<td>(t_{\text{WTR}})</td>
<td>Write to Read command delay</td>
<td>6</td>
<td>((t_{\text{WTR}}/t_{\text{CK}}) - 1)</td>
<td>3</td>
</tr>
</tbody>
</table>
Table 3-4. See the register section for the SDTIM* register where the field exists

<table>
<thead>
<tr>
<th>Register Field Name</th>
<th>DDR3 SDRAM Datasheet Parameter Name</th>
<th>Description</th>
<th>Datasheet Value (ns)</th>
<th>Formula (Register Field must be &gt;=)</th>
<th>Field Value (h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_RTP</td>
<td>t_{RTP}</td>
<td>Read to precharge command delay</td>
<td>6</td>
<td>(t_{RTP}/t_{CK}) – 1</td>
<td>3</td>
</tr>
<tr>
<td>T_CKE</td>
<td>t_{CKE}</td>
<td>CKE minimum pulse width</td>
<td>3(t_{CK} cycles)</td>
<td>(t_{CKE} – 1)</td>
<td>2</td>
</tr>
<tr>
<td>T_XP</td>
<td>t_{XP}</td>
<td>Power-down exit to non-read command</td>
<td>5(t_{CK} cycles)</td>
<td>(t_{XP} – 1)</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 3-5. See the register section for the SDTIM* register where the field exists

<table>
<thead>
<tr>
<th>Register Field Name</th>
<th>DDR3 SDRAM Datasheet Parameter Name</th>
<th>Description</th>
<th>Datasheet Value (ns)</th>
<th>Formula (Register Field must be &gt;=)</th>
<th>Field Value (h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_CSTA</td>
<td>DDR controller parameter</td>
<td>Refer to SDTIM 4 Register</td>
<td>—</td>
<td>—</td>
<td>5</td>
</tr>
<tr>
<td>T_RFC</td>
<td>t_{RFC}</td>
<td>Refresh cycle time</td>
<td>110</td>
<td>(t_{RFC}/t_{CK}) – 1</td>
<td>49</td>
</tr>
<tr>
<td>T_ZQCS</td>
<td>t_{ZQCS}</td>
<td>ZQCS command time</td>
<td>64(t_{CK} cycles)</td>
<td>(t_{ZQCS} – 1)</td>
<td>3F</td>
</tr>
</tbody>
</table>
Table 4-1 lists the memory-mapped registers for the DDR3 memory controller. For the memory address of these registers, see the device-specific data manual.

### Table 4-1. DDR3 Memory Controller Registers (See datasheet memory map for base address)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Acronym</th>
<th>Register Description</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td>MIDR</td>
<td>Module ID and Revision Register</td>
<td>Section 4.1</td>
</tr>
<tr>
<td>004h</td>
<td>STATUS</td>
<td>DDR3 Memory Controller Status Register</td>
<td>Section 4.2</td>
</tr>
<tr>
<td>008h</td>
<td>SDCFG</td>
<td>SDRAM Configuration Register</td>
<td>Section 4.3</td>
</tr>
<tr>
<td>010h</td>
<td>SDRFC</td>
<td>SDRAM Refresh Control Register</td>
<td>Section 4.4</td>
</tr>
<tr>
<td>018h</td>
<td>SDTIM1</td>
<td>SDRAM Timing 1 Register</td>
<td>Section 4.5</td>
</tr>
<tr>
<td>01Ch</td>
<td>SDTIM2</td>
<td>SDRAM Timing 2 Register</td>
<td>Section 4.6</td>
</tr>
<tr>
<td>020h</td>
<td>SDTIM3</td>
<td>SDRAM Timing 3 Register</td>
<td>Section 4.7</td>
</tr>
<tr>
<td>028h</td>
<td>SDTIM4</td>
<td>SDRAM Timing 4 Register</td>
<td>Section 4.8</td>
</tr>
<tr>
<td>038h</td>
<td>PMCTL</td>
<td>Power Management Control Register</td>
<td>Section 4.9</td>
</tr>
<tr>
<td>0x54h</td>
<td>LAT_CONFIG</td>
<td>VBUSM Configuration Register</td>
<td>Section 4.10</td>
</tr>
<tr>
<td>0x80</td>
<td>PERF_CNT_1</td>
<td>Performance Counter 1 Register</td>
<td>Section 4.11</td>
</tr>
<tr>
<td>0x84</td>
<td>PERF_CNT_2</td>
<td>Performance Counter 2 Register</td>
<td>Section 4.12</td>
</tr>
<tr>
<td>0x88</td>
<td>PERF_CNT_CFG</td>
<td>Performance Counter Config Register</td>
<td>Section 4.13</td>
</tr>
<tr>
<td>0x8C</td>
<td>PERF_CNT_SEL</td>
<td>Performance Counter Master Region Select Register</td>
<td>Section 4.14</td>
</tr>
<tr>
<td>0x90</td>
<td>PERF_CNT_TIM</td>
<td>Performance Counter Time Register</td>
<td>Section 4.15</td>
</tr>
<tr>
<td>0A4h</td>
<td>IRQSTATUS_RAW_SYS</td>
<td>Interrupt Raw Status Register</td>
<td>Section 4.16</td>
</tr>
<tr>
<td>0ACh</td>
<td>IRQ_STATUS_SYS</td>
<td>Interrupt Status Register</td>
<td>Section 4.17</td>
</tr>
<tr>
<td>0B4h</td>
<td>IRQENABLE_SET_SYS</td>
<td>Interrupt Enable Set Register</td>
<td>Section 4.18</td>
</tr>
<tr>
<td>0BCh</td>
<td>IRQENABLE_CLR_SYS</td>
<td>Interrupt Enable Clear Register</td>
<td>Section 4.19</td>
</tr>
<tr>
<td>0C8h</td>
<td>ZQCONFIG</td>
<td>SDRAM Output Impedance Calibration Configuration Register</td>
<td>Section 4.20</td>
</tr>
<tr>
<td>100h</td>
<td>PRI_COS_MAP</td>
<td>Priority To Class-Of-Service Mapping Register</td>
<td>Section 4.21</td>
</tr>
<tr>
<td>104h</td>
<td>MSTID_COS_1_MAP</td>
<td>Master ID to Class-Of-Service 1 Mapping Register</td>
<td>Section 4.22</td>
</tr>
<tr>
<td>108h</td>
<td>MSTID_COS_2_MAP</td>
<td>Master ID to Class-Of-Service 2 Mapping Register</td>
<td>Section 4.23</td>
</tr>
<tr>
<td>110h</td>
<td>ECCCTL</td>
<td>ECC Control Register</td>
<td>Section 4.24</td>
</tr>
<tr>
<td>114h</td>
<td>ECCADDR1</td>
<td>ECC Address Range 1 Register</td>
<td>Section 4.25</td>
</tr>
<tr>
<td>118h</td>
<td>ECCADDR2</td>
<td>ECC Address Range 2 Register</td>
<td>Section 4.26</td>
</tr>
<tr>
<td>120h</td>
<td>RWTHRESH</td>
<td>Read Write Execution Threshold Register</td>
<td>Section 4.27</td>
</tr>
<tr>
<td>130h</td>
<td>ONE_BIT_ECC_ERR_CNT</td>
<td>1-Bit ECC Error Count Register</td>
<td>Section 4.28</td>
</tr>
<tr>
<td>134h</td>
<td>ONE_BIT_ECC_ERR_THRSH</td>
<td>1-Bit ECC Error Threshold Register</td>
<td>Section 4.29</td>
</tr>
<tr>
<td>138h</td>
<td>ONE_BIT_ECC_ERR_DST_1</td>
<td>1-Bit ECC Error Distribution 1 Register</td>
<td>Section 4.30</td>
</tr>
<tr>
<td>13Ch</td>
<td>ONE_BIT_ECC_ERR_ADDR_LOG_1</td>
<td>1-Bit ECC Error Address Log Register</td>
<td>Section 4.31</td>
</tr>
<tr>
<td>140h</td>
<td>TWO_BIT_ECC_ERR_ADDR_LOG_1</td>
<td>2-Bit ECC Error Address Log Register</td>
<td>Section 4.32</td>
</tr>
<tr>
<td>144h</td>
<td>ONE_BIT_ECC_ERR_DST_2</td>
<td>1-Bit ECC Error Distribution 2 Register</td>
<td>Section 4.33</td>
</tr>
<tr>
<td>Offset</td>
<td>Acronym</td>
<td>Register Description</td>
<td>Section</td>
</tr>
<tr>
<td>--------</td>
<td>---------</td>
<td>----------------------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>004h</td>
<td>PIR</td>
<td>PHY Initialization Register</td>
<td>Section 4.34</td>
</tr>
<tr>
<td>008h</td>
<td>PGCR0</td>
<td>PHY General Configuration Register 0</td>
<td>Section 4.35</td>
</tr>
<tr>
<td>00Ch</td>
<td>PGCR1</td>
<td>PHY General Configuration Register 1</td>
<td>Section 4.36</td>
</tr>
<tr>
<td>010h</td>
<td>PGSR0</td>
<td>PHY General Status Register 0</td>
<td>Section 4.38</td>
</tr>
<tr>
<td>014h</td>
<td>PGSR1</td>
<td>PHY General Status Register 1</td>
<td>Section 4.39</td>
</tr>
<tr>
<td>018h</td>
<td>PLLCR</td>
<td>PLL Control Register</td>
<td>Section 4.40</td>
</tr>
<tr>
<td>01Ch</td>
<td>PTR0</td>
<td>PHY Timing Register 0</td>
<td>Section 4.41</td>
</tr>
<tr>
<td>020h</td>
<td>PTR1</td>
<td>PHY Timing Register 1</td>
<td>Section 4.42</td>
</tr>
<tr>
<td>024h</td>
<td>PTR2</td>
<td>PHY Timing Register 2</td>
<td>Section 4.43</td>
</tr>
<tr>
<td>028h</td>
<td>PTR3</td>
<td>PHY Timing Register 3</td>
<td>Section 4.44</td>
</tr>
<tr>
<td>02Ch</td>
<td>PTR4</td>
<td>PHY Timing Register 4</td>
<td>Section 4.45</td>
</tr>
<tr>
<td>038h</td>
<td>ACIOCR</td>
<td>AC I/O Configuration Register</td>
<td>Section 4.46</td>
</tr>
<tr>
<td>03Ch</td>
<td>DXCCR</td>
<td>DATX8 Common Configuration Register</td>
<td>Section 4.47</td>
</tr>
<tr>
<td>044h</td>
<td>DCR</td>
<td>DRAM Configuration Register</td>
<td>Section 4.48</td>
</tr>
<tr>
<td>048h</td>
<td>DTPR0</td>
<td>DRAM Timing Parameters Register 0</td>
<td>Section 4.49</td>
</tr>
<tr>
<td>04Ch</td>
<td>DTPR1</td>
<td>DRAM Timing Parameters Register 1</td>
<td>Section 4.50</td>
</tr>
<tr>
<td>050h</td>
<td>DTPR2</td>
<td>DRAM Timing Parameters Register 2</td>
<td>Section 4.51</td>
</tr>
<tr>
<td>054h</td>
<td>MR0</td>
<td>Mode Register 0</td>
<td>Section 4.52</td>
</tr>
<tr>
<td>058</td>
<td>MR1</td>
<td>Mode Register 1</td>
<td>Section 4.53</td>
</tr>
<tr>
<td>05C</td>
<td>MR2</td>
<td>Mode Register 2</td>
<td>Section 4.54</td>
</tr>
<tr>
<td>060h</td>
<td>MR3</td>
<td>Mode Register 3</td>
<td>Section 4.55</td>
</tr>
<tr>
<td>064</td>
<td>ODTCR</td>
<td>ODT Configuration Register</td>
<td>Section 4.56</td>
</tr>
<tr>
<td>068</td>
<td>DTCR</td>
<td>Data Training Configuration Register</td>
<td>Section 4.57</td>
</tr>
<tr>
<td>08C</td>
<td>PGCR2</td>
<td>PHY General Configuration Register 2</td>
<td>Section 4.37</td>
</tr>
<tr>
<td>180h</td>
<td>ZQOCR0</td>
<td>ZQ 0 Impedance Control Register 0</td>
<td>Section 4.58</td>
</tr>
<tr>
<td>184h</td>
<td>ZQOCR1</td>
<td>ZQ 0 Impedance Control Register 1</td>
<td>Section 4.59</td>
</tr>
<tr>
<td>188h</td>
<td>ZQOSR0</td>
<td>ZQ 0 Impedance Status Register 0</td>
<td>Section 4.60</td>
</tr>
<tr>
<td>18Ch</td>
<td>ZQOSR1</td>
<td>ZQ 0 Impedance Status Register 1</td>
<td>Section 4.61</td>
</tr>
<tr>
<td>190h</td>
<td>ZQ1CR0</td>
<td>ZQ 1 Impedance Control Register 0</td>
<td>Section 4.58</td>
</tr>
<tr>
<td>194h</td>
<td>ZQ1CR1</td>
<td>ZQ 1 Impedance Control Register 1</td>
<td>Section 4.59</td>
</tr>
<tr>
<td>198h</td>
<td>ZQ1SR0</td>
<td>ZQ 1 Impedance Status Register 0</td>
<td>Section 4.60</td>
</tr>
<tr>
<td>19Ch</td>
<td>ZQ1SR1</td>
<td>ZQ 1 Impedance Status Register 1</td>
<td>Section 4.61</td>
</tr>
<tr>
<td>1A0h</td>
<td>ZQ2CR0</td>
<td>ZQ 2 Impedance Control Register 0</td>
<td>Section 4.58</td>
</tr>
<tr>
<td>1A4h</td>
<td>ZQ2CR1</td>
<td>ZQ 2 Impedance Control Register 1</td>
<td>Section 4.59</td>
</tr>
<tr>
<td>1A8h</td>
<td>ZQ2SR0</td>
<td>ZQ 2 Impedance Status Register 0</td>
<td>Section 4.60</td>
</tr>
<tr>
<td>1Ah</td>
<td>ZQ2SR1</td>
<td>ZQ 2 Impedance Status Register 1</td>
<td>Section 4.61</td>
</tr>
<tr>
<td>1B0h</td>
<td>ZQ3CR0</td>
<td>ZQ 3 Impedance Control Register 0</td>
<td>Section 4.58</td>
</tr>
<tr>
<td>1B4h</td>
<td>ZQ3CR1</td>
<td>ZQ 3 Impedance Control Register 1</td>
<td>Section 4.59</td>
</tr>
<tr>
<td>1B8h</td>
<td>ZQ3SR0</td>
<td>ZQ 3 Impedance Status Register 0</td>
<td>Section 4.60</td>
</tr>
<tr>
<td>1BCh</td>
<td>ZQ3SR1</td>
<td>ZQ 3 Impedance Status Register 1</td>
<td>Section 4.61</td>
</tr>
<tr>
<td>1Ch</td>
<td>D0GCR</td>
<td>DATX8 0 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>1C4h</td>
<td>D0GSR0</td>
<td>DATX8 0 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>1Ch</td>
<td>D0GSR1</td>
<td>DATX8 0 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>1E0h</td>
<td>D0LC0LDR0</td>
<td>DATX8 0 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>1E4h</td>
<td>D0LC0LDR1</td>
<td>DATX8 0 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>1E8h</td>
<td>D0LC0LDR2</td>
<td>DATX8 0 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>1Ec</td>
<td>D0M0DLR</td>
<td>DATX8 0 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>1F0h</td>
<td>D0GTR</td>
<td>DATX8 0 General Timing Register</td>
<td>Section 4.69</td>
</tr>
</tbody>
</table>
### Table 4-2. DDR3 PHY Registers (See device datasheet for base address) (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Acronym</th>
<th>Register Description</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1F4h</td>
<td>DX0GSR2</td>
<td>DATX8 0 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>200h</td>
<td>DX1GCR</td>
<td>DATX8 1 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>204h</td>
<td>DX1GSR0</td>
<td>DATX8 1 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>208h</td>
<td>DX1GSR1</td>
<td>DATX8 1 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>220h</td>
<td>DX1LCDLR0</td>
<td>DATX8 1 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>224h</td>
<td>DX1LCDLR1</td>
<td>DATX8 1 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>228h</td>
<td>DX1LCDLR2</td>
<td>DATX8 1 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>22Ch</td>
<td>DX1MDLR</td>
<td>DATX8 1 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>230h</td>
<td>DX1GTR</td>
<td>DATX8 1 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>234h</td>
<td>DX1GSR2</td>
<td>DATX8 1 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>240h</td>
<td>DX2GCR</td>
<td>DATX8 2 General Configuration Register</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>244h</td>
<td>DX2GSR0</td>
<td>DATX8 2 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>248h</td>
<td>DX2GSR1</td>
<td>DATX8 2 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>260h</td>
<td>DX2LCDLR0</td>
<td>DATX8 2 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>264h</td>
<td>DX2LCDLR1</td>
<td>DATX8 2 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>268h</td>
<td>DX2LCDLR2</td>
<td>DATX8 2 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>26Ch</td>
<td>DX2MDLR</td>
<td>DATX8 2 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>270h</td>
<td>DX2GTR</td>
<td>DATX8 2 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>274h</td>
<td>DX2GSR2</td>
<td>DATX8 2 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>280h</td>
<td>DX3GCR</td>
<td>DATX8 3 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>284h</td>
<td>DX3GSR0</td>
<td>DATX8 3 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>288h</td>
<td>DX3GSR1</td>
<td>DATX8 3 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>2A0h</td>
<td>DX3LCDLR0</td>
<td>DATX8 3 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>2A4h</td>
<td>DX3LCDLR1</td>
<td>DATX8 3 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>2A8h</td>
<td>DX3LCDLR2</td>
<td>DATX8 3 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>2ACh</td>
<td>DX3MDLR</td>
<td>DATX8 3 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>2B0h</td>
<td>DX3GTR</td>
<td>DATX8 3 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>2B4h</td>
<td>DX3GSR2</td>
<td>DATX8 3 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>2C0h</td>
<td>DX4GCR</td>
<td>DATX8 4 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>2C4h</td>
<td>DX4GSR0</td>
<td>DATX8 4 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>2C8h</td>
<td>DX4GSR1</td>
<td>DATX8 4 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>2E0h</td>
<td>DX4LCDLR0</td>
<td>DATX8 4 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>2E4h</td>
<td>DX4LCDLR1</td>
<td>DATX8 4 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>2E8h</td>
<td>DX4LCDLR2</td>
<td>DATX8 4 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>2ECh</td>
<td>DX4MDLR</td>
<td>DATX8 4 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>2F0h</td>
<td>DX4GTR</td>
<td>DATX8 4 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>2F4h</td>
<td>DX4GSR2</td>
<td>DATX8 4 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>300h</td>
<td>DX5GCR</td>
<td>DATX8 5 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>304h</td>
<td>DX5GSR0</td>
<td>DATX8 5 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>308h</td>
<td>DX5GSR1</td>
<td>DATX8 5 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>320h</td>
<td>DX5LCDLR0</td>
<td>DATX8 5 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>324h</td>
<td>DX5LCDLR1</td>
<td>DATX8 5 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>328h</td>
<td>DX5LCDLR2</td>
<td>DATX8 5 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>32Ch</td>
<td>DX5MDLR</td>
<td>DATX8 5 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>330h</td>
<td>DX5GTR</td>
<td>DATX8 5 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>334h</td>
<td>DX5GSR2</td>
<td>DATX8 5 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>340h</td>
<td>DX6GCR</td>
<td>DATX8 6 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>Offset</td>
<td>Acronym</td>
<td>Register Description</td>
<td>Section</td>
</tr>
<tr>
<td>-------</td>
<td>-----------</td>
<td>-----------------------------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>344h</td>
<td>DX6GSR0</td>
<td>DATX8 6 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>348h</td>
<td>DX6GSR1</td>
<td>DATX8 6 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>360h</td>
<td>DX6LCDLR0</td>
<td>DATX8 6 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>364h</td>
<td>DX6LCDLR1</td>
<td>DATX8 6 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>368h</td>
<td>DX6LCDLR2</td>
<td>DATX8 6 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>36Ch</td>
<td>DX6MDLR</td>
<td>DATX8 6 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>370h</td>
<td>DX6GTR</td>
<td>DATX8 6 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>374h</td>
<td>DX6GSR2</td>
<td>DATX8 6 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>380h</td>
<td>DX7GCR</td>
<td>DATX8 7 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>384h</td>
<td>DX7GSR0</td>
<td>DATX8 7 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>388h</td>
<td>DX7GSR1</td>
<td>DATX8 7 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>3A0h</td>
<td>DX7LCDLR0</td>
<td>DATX8 7 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>3A4h</td>
<td>DX7LCDLR1</td>
<td>DATX8 7 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>3A8h</td>
<td>DX7LCDLR2</td>
<td>DATX8 7 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>3ACh</td>
<td>DX7MDLR</td>
<td>DATX8 7 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>3B0h</td>
<td>DX7GTR</td>
<td>DATX8 7 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>3B4h</td>
<td>DX7GSR2</td>
<td>DATX8 7 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>3C0h</td>
<td>DX8GCR</td>
<td>DATX8 8 General Configuration Register</td>
<td>Section 4.62</td>
</tr>
<tr>
<td>3C4h</td>
<td>DX8GSR0</td>
<td>DATX8 8 General Status Register 0</td>
<td>Section 4.63</td>
</tr>
<tr>
<td>3C8h</td>
<td>DX8GSR1</td>
<td>DATX8 8 General Status Register 1</td>
<td>Section 4.64</td>
</tr>
<tr>
<td>3E0h</td>
<td>DX8LCDLR0</td>
<td>DATX8 8 Local Calibrated Delay Line Register 0</td>
<td>Section 4.65</td>
</tr>
<tr>
<td>3E4h</td>
<td>DX8LCDLR1</td>
<td>DATX8 8 Local Calibrated Delay Line Register 1</td>
<td>Section 4.66</td>
</tr>
<tr>
<td>3E8h</td>
<td>DX8LCDLR2</td>
<td>DATX8 8 Local Calibrated Delay Line Register 2</td>
<td>Section 4.67</td>
</tr>
<tr>
<td>3ECh</td>
<td>DX8MDLR</td>
<td>DATX8 8 Master Delay Line Register</td>
<td>Section 4.68</td>
</tr>
<tr>
<td>3F0h</td>
<td>DX8GTR</td>
<td>DATX8 8 General Timing Register</td>
<td>Section 4.69</td>
</tr>
<tr>
<td>3F4h</td>
<td>DX8GSR2</td>
<td>DATX8 8 General Status Register 2</td>
<td>Section 4.64</td>
</tr>
</tbody>
</table>
## 4.1 Module ID and Revision Register (MIDR)

The Module ID and Revision register contains the revision number and identification data of the DDR3 peripheral, and is described in the following figure and table.

### Figure 4-1. Module ID and Revision Register (MIDR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>REG_SCHEME</td>
<td>R</td>
<td>Value = 0x1. Used to distinguish between old and current revision schemes. 0 means old scheme. 1 means new scheme.</td>
</tr>
<tr>
<td>29-28</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0</td>
</tr>
<tr>
<td>27-16</td>
<td>MOD_ID</td>
<td>R</td>
<td>Value = 0x46 Module ID Bits</td>
</tr>
<tr>
<td>15-11</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x3 or 0x6 Reserved. The reserved field always reads as 0x3 or 0x6. A value written to this field has no effect.</td>
</tr>
<tr>
<td>10-8</td>
<td>MJ_REV</td>
<td>R</td>
<td>Value = 0x4 Major Revision</td>
</tr>
<tr>
<td>7-6</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>5-0</td>
<td>MIN_REV</td>
<td>R</td>
<td>Value = 0x1 or 0x2 Minor Revision</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual

### Table 4-3. Module ID and Revision Register (MIDR) Field Descriptions
4.2 DDR3 Memory Controller Status Register (STATUS)

This register contains the status of the DDR3 module and is described in the following figure and table.

**Figure 4-2. DDR3 Memory Controller Status Register (STATUS)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>BE</td>
<td>R</td>
<td>Big Endian. Reflects the value on the BIG_ENDIAN port that defines whether the EMIF is in big or little-endian mode</td>
</tr>
<tr>
<td>30-29</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0. This field is tied off to 0x1.</td>
</tr>
</tbody>
</table>
| 28  | OBF_STAT | R         | Obfuscation Status.  
  • 0 = Obfuscation disabled.  
  • 1 = Obfuscation enabled. |
| 27  | SELF_REF | R         | Self refresh mode status.  
  • 0 = SDRAM is not in self refresh mode.  
  • 1 = SDRAM is in self refresh mode. |
| 26  | PWRDN   | R         | Power down status.  
  • 0 = SDRAM is not in power down mode.  
  • 1 = SDRAM is in power down mode. |
| 25-3 | Reserved | R         | Reserved. A value written to this field has no effect |
| 2   | IFRDY   | R         | DDR3 memory controller interface logic ready bit. The interface logic controls the signals used to communicate with DDR3 SDRAM devices. This bit displays the status of the interface logic.  
  • 0 = Interface logic is not ready; either powered down, not ready, or not locked.  
  • 1 = Interface logic is powered up, locked and ready for operation. |
| 1-0 | Reserved | R         | Value = 0. Reserved. The reserved bit location is always read as 0. A value written to this field has no effect. |

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual.
4.3 SDRAM Configuration Register (SDCFG)

The SDRAM Configuration Register (SDCFG) contains fields that program the DDR3 memory controller to meet the specifications of the DDR3 memory. These fields configure the DDR3 memory controller to match the data bus width, CAS latency, number of internal banks, and page size of the external DDR3 memory. For more information on initializing the configuration registers of the DDR3 memory controller, see Section 3.2.

![Figure 4-3. SDRAM Configuration Register (SDCFG)](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-29</td>
<td>SDRAM_TYPE</td>
<td>RW</td>
<td>Value = 3 SDRAM type selection. Set to 3 for DDR3. All other values reserved.</td>
</tr>
<tr>
<td>28</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>27-25</td>
<td>DDR_TERM</td>
<td>RW</td>
<td>Defines termination resistor value.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Disables termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = RZQ/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 2 = RZQ/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 3 = RZQ/6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 4 = RZQ/12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 5 = RZQ/8</td>
</tr>
<tr>
<td>24</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>23-22</td>
<td>DYN_ODT</td>
<td>RW</td>
<td>Dynamic On-Die Termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Turn off dynamic ODT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = RZQ/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 2 = RZQ/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All other values reserved.</td>
</tr>
<tr>
<td>21-17</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>16-14</td>
<td>CWL</td>
<td>RW</td>
<td>CAS Write Latency. Lower value gives better performance.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = CAS write latency of 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = CAS write latency of 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 2 = CAS write latency of 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 3 = CAS write latency of 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 4 = CAS write latency of 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 5 = CAS write latency of 10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 6 = CAS write latency of 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 7 = CAS write latency of 12</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - = value after reset; -x, value is indeterminate — see the device-specific data manual.
### Table 4-5. SDRAM Configuration Register (SDCFG) Field Descriptions (continued)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
</table>
| 13-12 | NM    | RW        | DDR3 data bus width. A write to this bit field will cause the memory controller to start SDRAM initialization sequence.  
  - 0 = 64-bit bus width.  
  - 1 = 32-bit bus width.  
  - 2 = 16-bit bus width.  
  All other values reserved. |
| 11-8  | CL    | RW        | CAS Latency. The value of this field defines the CAS latency, to be used when accessing connected SDRAM devices. A write to this field will cause the DDR3 memory controller to start the SDRAM initialization sequence.  
  - 2 = CAS latency of 5.  
  - 4 = CAS latency of 6.  
  - 6 = CAS latency of 7.  
  - 8 = CAS latency of 8.  
  - 10 = CAS latency of 9.  
  - 12 = CAS latency of 10.  
  - 14 = CAS latency of 11.  
  - 16 = CAS latency of 12.  
  - 18 = CAS latency of 13.  
  - 20 = CAS latency of 14.  
  - 22 = CAS latency of 15.  
  - 24 = CAS latency of 16.  
  All other values are reserved. |
| 7     | Reserved | R     | Value = 0  
  Reserved. The reserved bit location is always read as 0. A value written to this field has no effect. |
| 6-5   | IBANK  | RW      | Internal SDRAM bank setup bits. Defines number of banks inside connected SDRAM devices. A write to this bit will cause the DDR3 memory controller to start SDRAM initialization sequence. Values 4-7 are reserved for this field. A word is equal to the bus width of the individual SDRAM devices used (example, 1 byte for x8 and 2 bytes for x16 devices)  
  - 0 = One bank SDRAM devices.  
  - 1 = Two bank SDRAM devices.  
  - 2 = Four bank SDRAM devices.  
  - 3 = Eight bank SDRAM devices. |
| 4     | Reserved | R     | Value = 0  
  Reserved. The reserved bit location is always read as 0. A value written to this field has no effect. |
| 3     | EBANK  | RW      | External chip select setup. Defines whether SDRAM accesses use 1 or 2 chip select lines as follows:  
  - 0 = Use DCE0# for all SDRAM accesses.  
  - 1 = Use DEC0# and DCE1# for SDRAM accesses. |
| 2     | Reserved | R     | Value = 0  
  Reserved. The reserved bit location is always read as 0. A value written to this field has no effect. |
| 1-0   | PAGESIZE | RW      | Page size bits. Defines internal page size of the external DDR3 memory. A write to this bit will cause the DDR3 memory controller to start the SDRAM initialization sequence. Values 4-7 are reserved for this field. A word is equal to the bus width of the individual SDRAM devices used (example, 1 byte for x8 and 2 bytes for x16 devices)  
  - 0 = 256-word page requiring 8 column address bits.  
  - 1 = 512-word page requiring 9 column address bits.  
  - 2 = 1024-word page requiring 10 column address bits.  
  - 3 = 2048-word page requiring 11 column address bits. |
4.4 SDRAM Refresh Control Register (SDRFC)

The SDRAM Refresh Control Register (SDRFC) is used to configure the DDR3 memory controller to:

- Enter and Exit the self-refresh state.
- Meet the refresh requirements of the attached DDR3 device by programming a rate at which the DDR3 memory controller issues autorefresh commands.

The SDRFC register is described in the following figure and table.

![Figure 4-4. SDRAM Refresh Control Register (SDRFC)](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>INITREF_DIS</td>
<td>RW</td>
<td>Initialization and Refresh Disable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Normal operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = Disables SDRAM initialization and refreshes, but carries out SDRAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>write/read transactions</td>
</tr>
<tr>
<td>30-16</td>
<td>Reserved</td>
<td>R</td>
<td>Reserved.</td>
</tr>
<tr>
<td>15-0</td>
<td>REFRESH_RATE</td>
<td>RW</td>
<td>The value in this field is used to define the rate at which connected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDRAM devices will be refreshed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>REFRESH_RATE = Refresh period * DDR3 clock frequency.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; \( n \) = value after reset; \( -x \), value is indeterminate — see the device-specific data manual.
4.5 SDRAM Timing 1 (SDTIM1) Register

SDRAM Timing 1 register (SDTIM1) configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. Note that DDR3CLKOUT is equal to the period of the DDR3CLKOUT signal. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM1 register is described in the following figure and table.

Figure 4-5. SDRAM Timing 1 (SDTIM1) Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-30</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0&lt;br&gt;Reserved. The reserved bit location is always read as 0. A value written to this field has no effect</td>
</tr>
<tr>
<td>29-25</td>
<td>T_WR</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from the last write transfer to a precharge command, minus 1. The value of this parameter can be derived from the ( t_{\text{WR}} ) AC timing parameter in the DDR3 memory data sheet. Calculate using the formula:&lt;br&gt;( T_{\text{WR}} = \left( \frac{t_{\text{WR}}}{t_{\text{CK}}} \right) - 1 )</td>
</tr>
<tr>
<td>24-18</td>
<td>T_RAS</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to precharge command, minus 1. The value of this parameter can be derived from the minimum value of the ( t_{\text{RAS}} ) AC timing parameter in the DDR3 memory data sheet. Calculate using the formula:&lt;br&gt;( T_{\text{RAS}} = \left( \frac{t_{\text{RAS}}}{t_{\text{CK}}} \right) - 1 )</td>
</tr>
<tr>
<td>17-10</td>
<td>T_RC</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to an activate command, minus 1. The value of this parameter can be derived from the ( t_{\text{RC}} ) AC timing parameter in the DDR3 memory data sheet. Calculate using the formula:&lt;br&gt;( T_{\text{RC}} = \left( \frac{t_{\text{RC}}}{t_{\text{CK}}} \right) - 1 )</td>
</tr>
<tr>
<td>9-4</td>
<td>T_RRD</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from an activate to an activate in a different bank, minus 1. The value of this parameter can be derived from the ( t_{\text{RRD}} ) AC timing parameter in the DDR3 memory data sheet. Calculate using the formula:&lt;br&gt;( T_{\text{RRD}} = \left( \frac{t_{\text{FAW}}}{(4t_{\text{CK}})} \right) - 1 )</td>
</tr>
<tr>
<td>3-0</td>
<td>T_WTR</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from the last write to a read command, minus 1. The value of this parameter can be derived from the ( t_{\text{WTR}} ) AC timing parameter in the DDR3 memory data sheet. Convert the ( t_{\text{WTR}} ) value from the memory datasheet into ns before using the formula below. Calculate using the formula:&lt;br&gt;( T_{\text{WTR}} = \left( \frac{t_{\text{WTR}}}{t_{\text{CK}}} \right) - 1 )</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual.
4.6  SDRAM Timing 2 (SDTIM2) Register

Like the SDRAM Timing 1 register (SDTIM1), the SDRAM Timing 2 register (SDTIM2) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM2 register is described in the following figure and table.

![Figure 4-6. SDRAM Timing 2 (SDTIM2) Register](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-13</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>12-10</td>
<td>T_RTW</td>
<td>RW</td>
<td>Minimum number of DDR3CLKOUT cycles between read and write date phases, minus 1. This is not an SDRAM timing parameter. The value depends on the board topology supported. For single rank: reg_t_RTW= (((2*dqs_delay_for_cs0)+tDQSCK+wr_leveling_tolerance)/clock_period)-1 For dual rank: reg_t_RTW= ((dqs_delay_for_cs0+dqs_delay_for_cs1+absolute(command_delay_for_cs0-command_delay_for_cs1)+tDQSCK+wr_leveling_tolerance)/clock_period)-1</td>
</tr>
<tr>
<td>9-5</td>
<td>T_RP</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from a precharge command to a refresh or activate command, minus 1. The value of this parameter can be derived from the t_RP AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: T_RP = (t_RP/t_CK) - 1</td>
</tr>
<tr>
<td>4-0</td>
<td>T_RCD</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to a read or write command, minus 1. The value of this parameter can be derived from the t_RCD AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: T_RCD = (t_RCD/t_CK) - 1</td>
</tr>
</tbody>
</table>
4.7 SDRAM Timing 3 (SDTIM3) Register

Like the SDRAM Timing 1 and 2 registers (SDTIM1 & SDTIM2), the SDRAM Timing 3 register (SDTIM3) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM3 register is described in the following figure and table.

**Figure 4-7. SDRAM Timing 3 (SDTIM3) Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>T_XP</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from Power down exit to any command other than a read command, minus 1. The value of this parameter can be derived from the ( t_{XP} ) AC timing parameter in the DDR3 memory data sheet. Convert the ( t_{XP} ) datasheet parameter value into ns before using formula below. Calculate using the formula: ( T_{XP} = \left( \frac{t_{XP}}{t_{CK}} \right) - 1 )</td>
</tr>
<tr>
<td>27-18</td>
<td>T_XSNR</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from a self-refresh exit to a command that does not require a locked DLL, minus 1. The value of this parameter can be derived from the ( t_{XS} ) AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: ( T_{XSNR} = \left( \frac{t_{XS}}{t_{CK}} \right) - 1 )</td>
</tr>
<tr>
<td>17-8</td>
<td>T_XSRD</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from a self-refresh exit to a command that requires a locked DLL, minus 1. The value of this parameter can be derived from the ( t_{XSDLL} ) AC timing parameter in the DDR3 memory data sheet. This parameter typically appears in the datasheet in terms of ( t_{CK} ) clock cycles. Calculate using the formula: ( T_{XSRD} = t_{XSDLL} - 1 )</td>
</tr>
<tr>
<td>7-4</td>
<td>T_RTP</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles from the last read to precharge command, minus 1. The value of this parameter can be derived from the ( t_{RTP} ) AC timing parameter in the DDR3 memory data sheet. Convert the ( t_{RTP} ) datasheet parameter value into ns before using formula below. Calculate using the formula: ( T_{RTP} = \left( \frac{t_{RTP}}{t_{CK}} \right) - 1 )</td>
</tr>
<tr>
<td>3-0</td>
<td>T_CKE</td>
<td>RW</td>
<td>These bits specify the minimum number of DDR3CLKOUT cycles between transitions on the DSDCKE pin, minus 1. The value of this parameter can be derived from the ( t_{CKE} ) AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: ( T_{CKE} = \left( \frac{t_{CKE}}{t_{CK}} \right) - 1 )</td>
</tr>
</tbody>
</table>
4.8 SDRAM Timing 4 (SDTIM4) Register

Like the SDRAM Timing 1, 2 and 3 registers, the SDRAM Timing 4 register (SDTIM4) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM4 register is described in the following figure and table.

Figure 4-8. SDRAM Timing 4 (SDTIM4) Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>T_CSTA</td>
<td>RW</td>
<td>Minimum DDR3CLKOUT cycles between write-to-write or read-to-read data phases to different chip selects, minus 1.</td>
</tr>
</tbody>
</table>
| 27-24 | T_CKESR    | RW        | Value = 0
Minimum DDR3CLKOUT cycles for which DDR3 should remain in self-refresh. This parameter typically appears as number of t\textsubscript{ck} clock cycles.
T\textsubscript{CKESR} = (t\textsubscript{CKESR}/t\textsubscript{CK}) – 1 |
| 23-16 | ZQ_ZQCS    | RW        | These bits specify the minimum number of DDR3CLKOUT cycles for a ZQCS command, minus 1. The value of this parameter can be derived from the t\textsubscript{ZQCS} AC timing parameter in the DDR3 memory data sheet. This parameter typically appears as number of t\textsubscript{ck} clock cycles. Calculate using the formula:
ZQ\_ZQCS = t\textsubscript{ZQCS} – 1 |
| 15-14 | Reserved   | R         | Value = 0
Reserved. The reserved bit location is always read as 0. A value written to this field has no effect. |
| 13-4  | T_RFC      | RW        | These bits specify the minimum number of DDR3CLKOUT cycles from a refresh or load mode command to a refresh or activate command, minus 1. The value of this parameter can be derived from the t\textsubscript{RFC} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula:
T\_RFC = (t\textsubscript{RFC}/t\textsubscript{CK}) – 1 |
| 3-0   | T_RAS_MAX  | RW        | This field must always be programmed to 0xF. |
4.9 Power Management Control Register (PMCTL)

The PMCTL register is described in the following figure and table.

Figure 4-9. Power Management Control Register (PMCTL)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved. The reserved bit location is always read as 0. A value written to this field has no effect</td>
</tr>
<tr>
<td>15-12</td>
<td>PD_TIM</td>
<td>RW</td>
<td>Power Management timer for power-down. The DDR3 memory controller will put the SDRAM in power-down mode after the DDR3 controller is idle for PD_TIM number of DDR3CLKOUT cycles and if LP_MODE is set to 4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Immediately enter power-down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = Enter power-down after 16 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 2 = Enter power-down after 32 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 3 = Enter power-down after 64 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 4 = Enter power-down after 128 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 5 = Enter power-down after 256 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 6 = Enter power-down after 512 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 7 = Enter power-down after 1024 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 8 = Enter power-down after 2048 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 9 = Enter power-down after 4096 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 10 = Enter power-down after 8912 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 11 = Enter power-down after 16384 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 12 = Enter power-down after 32768 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 13 = Enter power-down after 65536 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 14 = Enter power-down after 131072 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 15 = Enter power-down after 262144 clocks</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved. The reserved bit location is always read as 0. A value written to this field has no effect</td>
</tr>
<tr>
<td>10-8</td>
<td>LP_MODE</td>
<td>RW</td>
<td>Automatic power management enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 2 = Self-refresh mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 4 = Power-down mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All other values will disable automatic power management.</td>
</tr>
</tbody>
</table>
Table 4-11. Power Management Control Register (PMCTL) Field Descriptions (continued)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7-4 | SR_TIM | RW | Power management timer for self-refresh. The DDR3 memory controller will put the external SDRAM in self-refresh mode after DDR3 controller has been idle for these number of DDR3CLKOUT cycles and LP_MODE is set to 2.  
  • 0 = Immediately enter self-refresh  
  • 1 = Enter self-refresh after 16 clocks  
  • 2 = Enter self-refresh after 32 clocks  
  • 3 = Enter self-refresh after 64 clocks  
  • 4 = Enter self-refresh after 128 clocks  
  • 5 = Enter self-refresh after 256 clocks  
  • 6 = Enter self-refresh after 512 clocks  
  • 7 = Enter self-refresh after 1024 clocks  
  • 8 = Enter self-refresh after 2048 clocks  
  • 9 = Enter self-refresh after 4096 clocks  
  • 10 = Enter self-refresh after 8912 clocks  
  • 11 = Enter self-refresh after 16384 clocks  
  • 12 = Enter self-refresh after 32768 clocks  
  • 13 = Enter self-refresh after 65536 clocks  
  • 14 = Enter self-refresh after 131072 clocks  
  • 15 = Enter self-refresh after 262144 clocks |
| 3-0 | Reserved | R | Reserved |
4.10 VBUSM Configuration Register (VBUSM_CONFIG)

The VBUSM_CONFIG register is described in the following figure and table.

**Figure 4-10. VBUSM Configuration Register (VBUSM_CONFIG)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>23-16</td>
<td>COS_COUNT_1</td>
<td>RW</td>
<td>Value = 0xFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Priority raise counter for Class of Service 1. Number of DDR3CLKOUT cycles after which the DDR3 controller momentarily raises the priority of Class of Service 1 commands in Command FIFO. Number of clock cycles = COS_COUNT_1 x 16 clocks</td>
</tr>
<tr>
<td>15-8</td>
<td>COS_COUNT_2</td>
<td>RW</td>
<td>Value = 0xFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Priority raise counter for Class of Service 2. Number of DDR3CLKOUT cycles after which the DDR3 controller momentarily raises the priority of Class of Service 2 commands in Command FIFO. Number of clock cycles = COS_COUNT_2 x 16 clocks</td>
</tr>
<tr>
<td>7-0</td>
<td>PR_OLD_COUNT</td>
<td>RW</td>
<td>Value = 0xFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Priority raise old counter. Number of DDR3CLKOUT cycles after which DDR3 controller momentarily raises the priority of the oldest command in Command FIFO. Number of clock cycles = PR_OLD_COUNT x 16 clocks</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual
4.11 Performance Counter 1 Register (PERF_CNT_1)

The PERF_CNT_1 register is described in the following figure and table.

Figure 4-11. Performance Counter 1 Register (PERF_CNT_1)

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>COUNTER_1</td>
<td>R</td>
<td>32-bit counter can be programmed as specified in the Performance Counter Config and Performance Counter Master Region Select registers.</td>
</tr>
</tbody>
</table>
```

Legend: R = Read only; W = Write only; \( n \) = value after reset; \( x \), value is indeterminate — see the device-specific data manual.
4.12 Performance Counter 2 Register (PERF_CNT_2)

The PERF_CNT_2 register is described in the following figure and table.

Figure 4-12. Performance Counter 2 Register (PERF_CNT_2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>COUNTER_2</td>
<td>R</td>
<td>32-bit counter can be programmed as specified in the Performance Counter Config and Performance Counter Master Region Select registers.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - = value after reset; -x, value is indeterminate — see the device-specific data manual
4.13 Performance Counter Config Register (PERF_CNT_CFG)

The PERF_CNT_CFG register is described in the following figure and table.

Figure 4-13. Performance Counter Config Register (PERF_CNT_CFG)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>CNTR2_MSTID_EN</td>
<td>RW</td>
<td>Master ID filter enable for Performance Counter 2 Register. Set to 1 to enable filtering of events for counter 2 by Master ID. Refer to your device data manual for the master IDs of various masters.</td>
</tr>
<tr>
<td>30</td>
<td>CNTR2_REGION_EN</td>
<td>RW</td>
<td>Memory space region enable for Performance Counter 2 Register. Set to 1 to enable filtering of events for counter 2 by the accessed memory region.</td>
</tr>
<tr>
<td>29-20</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved</td>
</tr>
<tr>
<td>19-16</td>
<td>CNTR2_CFG</td>
<td>RW</td>
<td>Filter configuration selected for Performance Counter 2. This field selects the type of event to count for Counter 2. Refer to Table 2-12 for various configuration options.</td>
</tr>
<tr>
<td>15</td>
<td>CNTR1_MSTID_EN</td>
<td>RW</td>
<td>Master ID filter enable for Performance Counter 1 Register. Set to 1 to enable filtering of events for counter 1 by Master ID. Refer to your device data manual for the master IDs of various masters.</td>
</tr>
<tr>
<td>14</td>
<td>CNTR1_REGION_EN</td>
<td>RW</td>
<td>Memory space region enable for Performance Counter 1 Register. Set to 1 to enable filtering of events for counter 1 by the accessed memory region.</td>
</tr>
<tr>
<td>13-4</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved</td>
</tr>
<tr>
<td>3-0</td>
<td>CNTR1_CFG</td>
<td>RW</td>
<td>Filter configuration selected for Performance Counter 1. This field selects the type of event to count for Counter 1. Refer to Table 2-12 for various configuration options.</td>
</tr>
</tbody>
</table>
4.14 Performance Counter Master Region Select Register (PERF_CNT_SEL)

For events that can be configured to enable master ID and/or memory region filters, the value of the master ID and the region select options for the counters are programmed in the PERF_CNT_SEL register. The PERF_CNT_SEL register is described in the following figure and table.

![Figure 4-14. Performance Counter Master Region Select Register (PERF_CNT_SEL)](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>MSTID2</td>
<td>RW</td>
<td>Master ID for Performance Counter 2 Register. Refer to your device data manual for the master IDs of various masters.</td>
</tr>
<tr>
<td>23-20</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved</td>
</tr>
<tr>
<td>19-16</td>
<td>REGION_SEL2</td>
<td>RW</td>
<td>Region select for Performance Counter 2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0x0 - DDR3 memory space</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0x7 - DDR3 controller memory mapped registers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All other values are reserved</td>
</tr>
<tr>
<td>15-8</td>
<td>MSTID1</td>
<td>RW</td>
<td>Master ID for Performance Counter 1 Register. Refer to your device data manual for the master IDs of various masters.</td>
</tr>
<tr>
<td>7-4</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved</td>
</tr>
<tr>
<td>3-0</td>
<td>REGION_SEL1</td>
<td>RW</td>
<td>Region select for Performance Counter 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0x0 - DDR3 memory space</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0x7 - DDR3 controller memory mapped registers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All other values are reserved</td>
</tr>
</tbody>
</table>
4.15 Performance Counter Time Register (PERF_CNT_TIM)

The PERF_CNT_TIM register is described in the following figure and table.

**Figure 4-15. Performance Counter Time Register (PERF_CNT_TIM)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>TOTAL_TIME</td>
<td>R</td>
<td>32-bit counter continuously counts number of DDR/2 clock cycles elapsed after the controller is brought out of reset.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; \( n \) = value after reset; \(-x\), value is indeterminate — see the device-specific data manual
4.16 Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)

The IRQSTATUS_RAW_SYS register is described in the following figure and table.

**Table 4-18. Interrupt Raw Status Register (IRQSTATUS_RAW_SYS) Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-6</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved</td>
</tr>
<tr>
<td>5</td>
<td>1B_ECC_ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Raw status of 1-bit ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>4</td>
<td>2B_ECC_ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Raw status of 2-bit ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>3</td>
<td>WR_ECC_ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Raw status of write ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>2-1</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved</td>
</tr>
<tr>
<td>0</td>
<td>ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Raw status of system VBUSM interrupt for command or address error. Writing a 1 sets the raw status. Writing a 0 has no effect.</td>
</tr>
</tbody>
</table>
4.17 Interrupt Status Register (IRQSTATUS_SYS)

The IRQSTATUS_SYS register is described in the following figure and table.

Figure 4-17. Interrupt Status Register (IRQSTATUS_SYS)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-6| Reserved           | R         | Value = 0x0 
Reserved. |
| 5   | 1B_ECC_ERR_SYS    | WOC       | Value = 0x0 
Enabled status of 1-bit ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect. |
| 4   | 2B_ECC_ERR_SYS    | WOC       | Value = 0x0 
Enabled status of 2-bit ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect. |
| 3   | WR_ECC_ERR_SYS    | WOC       | Value = 0x0 
Enabled status of write ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect. |
| 2-1 | Reserved           | R         | Value = 0x0 
Reserved. |
| 0   | ERR_SYS            | WOC       | Value = 0x0 
Enabled status of system VBUSM interrupt for command or address error. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect. |

Legend: R = Read only; WOC = write one to clear; - n = value after reset; -x, value is indeterminate — see the device-specific data manual.
4.18 Interrupt Enable Set Register (IRQSTATUS_SET_SYS)

The IRQSTATUS_SET_SYS register is described in the following figure and table.

**Figure 4-18. Interrupt Enable Set Register (IRQSTATUS_SET_SYS)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-6</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved.</td>
</tr>
<tr>
<td>5</td>
<td>1B_ECC_ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Enabled set for 1-bit ECC error interrupt. Writing a 1 will enable the read ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>4</td>
<td>2B_ECC_ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Enabled set for 2-bit ECC error interrupt. Writing a 1 will enable the read ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>3</td>
<td>WR_ECC_ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Enabled set for write ECC error interrupt. Writing a 1 will enable the write ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>2-1</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved.</td>
</tr>
<tr>
<td>0</td>
<td>ERR_SYS</td>
<td>WOS</td>
<td>Value = 0x0 Enable set for system VBUSM interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; WOS = Write one to set; n = value after reset; -x, value is indeterminate — see the device-specific data manual
4.19 Interrupt Enable Clear Register (IRQSTATUS CLR_SYS)

The IRQSTATUS_CLR_SYS register is described in the following figure and table.

Figure 4-19. Interrupt Enable Clear Register (IRQSTATUS_CLR_SYS)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-6</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved.</td>
</tr>
<tr>
<td>5</td>
<td>1B_ECC_ERR_SYS</td>
<td>WOC</td>
<td>Value = 0x0 Enabled clear for 1-bit ECC error interrupt. Writing a 1 will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>disable the read ECC error interrupt, clear this bit as well as the bit in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>4</td>
<td>2B_ECC_ERR_SYS</td>
<td>WOC</td>
<td>Value = 0x0 Enabled clear for 2-bit ECC error interrupt. Writing a 1 will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>disable the read ECC error interrupt, clear this bit as well as the bit in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>3</td>
<td>WR_ECC_ERR_SYS</td>
<td>WOC</td>
<td>Value = 0x0 Enabled clear for write ECC error interrupt. Writing a 1 will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>disable the write ECC error interrupt, clear this bit as well as the bit in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Interrupt Enable Clear Register. Writing a 0 has no effect.</td>
</tr>
<tr>
<td>2-1</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0x0 Reserved.</td>
</tr>
<tr>
<td>0</td>
<td>ERR_SYS</td>
<td>WOC</td>
<td>Value = 0x0 Enable clear for system VBUSM interrupt for command or address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>error. Writing a 1 will disable the interrupt, and clear this bit as well as</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; WOC = Write one to clear; - n = value after reset; -x, value is indeterminate — see the device-specific data manual.
4.20 SDRAM Output Impedance Calibration Configuration Register (ZQCFG)

The ZQCFG register is described in the following figure and table.

Figure 4-20. SDRAM Output Impedance Calibration Configuration Register (ZQCFG)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ZQ_CS1EN</td>
<td>RW</td>
<td>ZQ calibration for CS1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Disable ZQ calibration for CS1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = Enable ZQ calibration for CS1</td>
</tr>
<tr>
<td>30</td>
<td>ZQ_CS0EN</td>
<td>RW</td>
<td>ZQ calibration for CS0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Disable ZQ calibration for CS0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = Enable ZQ calibration for CS0</td>
</tr>
<tr>
<td>29</td>
<td>ZQ_DUALCALEN</td>
<td>RW</td>
<td>ZQ Dual Calibration enable. Allows both ranks to be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>calibrated simultaneously. A value written to this</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>field has no effect.</td>
</tr>
<tr>
<td>28</td>
<td>ZQ_SFEXITEN</td>
<td>RW</td>
<td>ZQCL on Self-refresh, Active power-down and precharge</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>power-down exit enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0 = Disable ZQCL on Self-refresh, Active power-down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>and precharge power-down exit enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 1 = Enable ZQCL on Self-refresh, Active power-down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>and precharge power-down exit enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Set this value to 1 to issue a ZQCL command upon</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>self-refresh exit.</td>
</tr>
<tr>
<td>27-19</td>
<td>Reserved</td>
<td>R</td>
<td>Value = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved. The reserved bit location is always read</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>18-16</td>
<td>ZQ_ZQCL_MULT</td>
<td>RW</td>
<td>Number of ZQCS intervals that make up a ZQCL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>interval, minus one. ZQCS interval is defined</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>by ZQ_ZQSCS field in SDRAM Timing 3 (SDTIM3) register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The value of this parameter can be derived using the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>formula:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>T_ZQ_ZQCL_MULT = (T_MAX / T_ZQCS - 1)</td>
</tr>
<tr>
<td>15-0</td>
<td>ZQ_REFINTERVAL</td>
<td>RW</td>
<td>Number of refresh periods between ZQCS commands,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>minus one. This field supports between one refresh</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>period to 256 ms between ZQCS calibration commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Refresh period is defined by REFRESH_RATE field in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDRAM Refresh control (SDRFC) register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ZQ_REFINTERVAL = number of refresh periods between</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ZQCS commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The interval is calculated as 0.5% / (Tsens x Tdriftrate) + (Vsens x Vdriftrate).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Tsens = max (dRTTdT, dRONdTM) from the memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>device datasheet.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vsens = max (dRTTdV, dRONdVM) from the memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>device datasheet.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Tdriftrate = drift rate in °C/second. This is the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>temperature drift rate that the SDRAM is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>subject to in the application. Vdriftrate = drift</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>rate in mV/second. This is the voltage drift rate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>that the SDRAM is subject to in the application.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Example:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If Tsens = 1.5%/°C, Vsens = 0.15%/mV, Tdriftrate = 1.2°C/second and Vdriftrate = 10mV/second,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Interval = 0.5[(1.5 x 1.2) + (0.15 x 10)] = 152ms.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Since refresh interval = 7.8µs, ZQ_REFINTERVAL = 152ms/7.8µs = 0x4C1F</td>
</tr>
</tbody>
</table>
4.21 Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)

The PRI_COS_MAP register is described in the following figure and table.

**Figure 4-21. Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | PRI_COS_MAP_EN | Value = 0x0
Priority to Class-of-service mapping
• 0 = Disable Priority to Class-of-service mapping
• 1 = Enable Priority to Class-of-service mapping |
| 30-16 | Reserved   | Value = 0
Reserved. The reserved bit location is always read as 0. A value written to this field has no effect. |
| 15-14 | PRI_7_COS  | Class-of-service for commands with priority of 7 (lowest priority).
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 13-12 | PRI_6_COS  | Class-of-service for commands with priority of 6.
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 11-10 | PRI_5_COS  | Class-of-service for commands with priority of 5.
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 9-8  | PRI_4_COS  | Class-of-service for commands with priority of 4.
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 7-6  | PRI_3_COS  | Class-of-service for commands with priority of 3.
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 5-4  | PRI_2_COS  | Class-of-service for commands with priority of 2.
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 3-2  | PRI_1_COS  | Class-of-service for commands with priority of 1.
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
| 1-0  | PRI_0_COS  | Class-of-service for commands with priority of 0 (highest priority).
• 1= Map to Class-of-service 1
• 2= Map to Class-of-service 2
• 0 or 3 will not assign any class of service. |
4.22 Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)

The MSTID_COS_1_MAP register is described in the following figure and table.

**Figure 4-22. Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>MSTID_COS_1_MAP_EN</td>
<td>Master ID to Class-of-service 1 mapping.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 0 = Disable Master ID to Class-of-service 1 mapping</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 = Enable Master ID to Class-of-service 1 mapping</td>
</tr>
</tbody>
</table>
| 30-23| MSTID_1_COS_1 | Value = 0x0
Master ID value 1 for Class-of-service 1. |
| 22-20| MSK_1_COS_1   | Mask for master ID value 1 for Class-of-service 1.                         |
|     |               | • 0 = Disable masking                                                       |
|     |               | • 1 = Mask master ID bit 0                                                  |
|     |               | • 2 = Mask master ID bits 1-0                                               |
|     |               | • 3 = Mask master ID bits 2-0                                               |
| 19-12| MSTID_2_COS_1 | Value = 0x0
Master ID value 2 for Class-of-service 1. |
| 11-10| MSK_2_COS_1   | Mask for master ID value 2 for Class-of-service 1.                         |
|     |               | • 0 = Disable masking                                                       |
|     |               | • 1 = Mask master ID bit 0                                                  |
|     |               | • 2 = Mask master ID bits 1-0                                               |
|     |               | • 3 = Mask master ID bits 2-0                                               |
| 9-2 | MSTID_3_COS_1 | Value = 0x0
Master ID value 3 for Class-of-service 1. |
| 1-0 | MSK_3_COS_1   | Mask for master ID value 3 for Class-of-service 1.                         |
|     |               | • 0 = Disable masking                                                       |
|     |               | • 1 = Mask master ID bit 0                                                  |
|     |               | • 2 = Mask master ID bits 1-0                                               |
|     |               | • 3 = Mask master ID bits 2-0                                               |

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual

**Table 4-24. Master ID to Class-Of-Service Mapping 1 Register (MSTID_COS_1_MAP) Field Descriptions**
Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)

The MSTID_COS_2_MAP register is described in the following figure and table.

![Figure 4-23. Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)](image_url)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | MSTID_COS_2_MAP_EN | Master ID to Class-of-service 2 mapping.  
  • 0 = Disable Master ID to Class-of-service 2 mapping  
  • 1 = Enable Master ID to Class-of-service 2 mapping |
| 30-23 | MSTID_1_COS_2 | Value = 0x0  
  Master ID value 1 for Class-of-service 2. |
| 22-20 | MSK_1_COS_2 | Mask for master ID value 1 for Class-of-service 2.  
  • 0 = Disable masking  
  • 1 = Mask master ID bit 0  
  • 2 = Mask master ID bits 1-0  
  • 3 = Mask master ID bits 2-0 |
| 19-12 | MSTID_2_COS_2 | Value = 0x0  
  Master ID value 2 for Class-of-service 2. |
| 11-10 | MSK_2_COS_2 | Mask for master ID value 2 for Class-of-service 2.  
  • 0 = Disable masking  
  • 1 = Mask master ID bit 0  
  • 2 = Mask master ID bits 1-0  
  • 3 = Mask master ID bits 2-0 |
| 9-2  | MSTID_3_COS_2 | Value = 0x0  
  Master ID value 3 for Class-of-service 2. |
| 1-0  | MSK_3_COS_2 | Mask for master ID value 3 for Class-of-service 2.  
  • 0 = Disable masking  
  • 1 = Mask master ID bit 0  
  • 2 = Mask master ID bits 1-0  
  • 3 = Mask master ID bits 2-0 |

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-25. Master ID to Class-Of-Service Mapping 2 Register (MSTID_COS_2_MAP) Field Descriptions
### 4.24 ECC Control Register (ECCCTL)

The ECCCTL register is described in the following figure and table.

![Figure 4-24. ECC Control Register (ECCCTL)]

### Table 4-26. ECC Control Register (ECCCTL) Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ECC_EN</td>
<td><strong>ECC enable.</strong> Enabling ECC will cause the DDR3 controller to start the SDRAM initialization sequence.**</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 0 = Disable ECC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 = Enable ECC</td>
</tr>
<tr>
<td>30</td>
<td>ECC_ADDR_RNG_PROT</td>
<td><strong>This bit is used to determine whether ECC calculation is allowed within address ranges described by ECC Address Range 1 and 2 Registers, provided ECC_EN is set to enable ECC.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 0 = Disable ECC calculation within address ranges defined in ECC Address Range 1 and 2 registers and enable calculation for accesses outside of these address ranges</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 = Enable ECC calculation within address ranges defined in ECC Address Range 1 and 2 registers and disable calculation for accesses outside of these address ranges</td>
</tr>
<tr>
<td>29</td>
<td>ECC_VERIFY_EN</td>
<td><strong>0 - Disable ECC verification for read accesses when ECC_EN=1.</strong> <strong>1- Enable ECC verification for read accesses when ECC_EN=1.</strong> This field is ignored if ECC_EN=0. Note that this field is available only on K2K and K2H silicon revisions above 1.1. It is available on all revisions of the K2E and K2L families.</td>
</tr>
<tr>
<td>28</td>
<td>RMW_EN</td>
<td><strong>0 - Disable read-modify-write functionality for sub-quanta accesses when ECC_EN=1.</strong>  <strong>1 - Enable read-modify-write functionality for sub-quanta accesses when ECC_EN=1.</strong> This field is ignored if ECC_EN=0. Note that this field is available only on K2K and K2H silicon revisions above 1.1. It is available on all revisions of the K2E and K2L families.</td>
</tr>
<tr>
<td>27-2</td>
<td>Reserved</td>
<td>Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>1</td>
<td>ECC_ADDR_RNG_2_EN</td>
<td><strong>ECC Address Range 2 enable.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 0 = Disable ECC Address Range 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 = Enable ECC Address Range 2</td>
</tr>
<tr>
<td>0</td>
<td>ECC_ADDR_RNG_1_EN</td>
<td><strong>ECC Address Range 1 enable.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 0 = Disable ECC Address Range 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 = Enable ECC Address Range 1</td>
</tr>
</tbody>
</table>
4.25 ECC Address Range 1 Register (ECCADDR1)

The ECCADDR1 register is described in the following figure and table.

**Figure 4-25. ECC Address Range 1 Register (ECCADDR1)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>ECC_END_ADDR_1</td>
<td>End address [32-17] of 33-bit address for ECC address range 1</td>
</tr>
<tr>
<td>15-0</td>
<td>ECC_STRT_ADDR_1</td>
<td>Start address [32-17] of 33-bit address for ECC address range 1</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

**Table 4-27. ECC Address Range 1 Register Field Descriptions**

- **NOTE:** The range is inclusive of start and end addresses.
4.26 ECC Address Range 2 Register (ECCADDR2)

The ECCADDR2 register is described in the following figure and table.

Figure 4-26. ECC Address Range 2 Register (ECCADDR2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>ECC_END_ADDR_2</td>
<td>End address [32-17] of 33-bit address for ECC address range 2</td>
</tr>
<tr>
<td>15-0</td>
<td>ECC_STRT_ADDR_2</td>
<td>Start address [32-17] of 33-bit address for ECC address range 2</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

NOTE: The range is inclusive of start and end addresses.
4.27 Read Write Execution Threshold Register (RWTHRESH)

The RWTHRESH register is described in the following figure and table.

**Figure 4-27. Read Write Execution Threshold Register (RWTHRESH)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-13</td>
<td>Reserved</td>
<td>Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>12-8</td>
<td>WR_THRSH</td>
<td>Write Threshold. Number of SDRAM write bursts after which the arbitration will switch to executing read commands. The value programmed is always minus 1 the required number.</td>
</tr>
<tr>
<td>7-5</td>
<td>Reserved</td>
<td>Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.</td>
</tr>
<tr>
<td>4-0</td>
<td>RD_THRSH</td>
<td>Read Threshold. Number of SDRAM read bursts after which the arbitration will switch to executing write commands. The value programmed is always minus 1 the required number.</td>
</tr>
</tbody>
</table>
4.28 1-Bit ECC Error Count Register (ONE_BIT_ECC_ERR_CNT)

The ONE_BIT_ECC_ERR_CNT register is described in the following figure and table.

**Figure 4-28. 1-Bit ECC Error Count Register (ONE_BIT_ECC_ERR_CNT)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>1B_ECC_ERR_CNT</td>
<td>WS</td>
<td>32-bit counter that displays the number of 1-bit ECC errors. Writing a value will decrement the count by that value.</td>
</tr>
</tbody>
</table>
4.29 1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH)

The ONE_BIT_ECC_ERR_THRSH register is described in the following figure and table.

**Figure 4-29. 1-Bit ECC Error Threshold Register (ONE_BIT_ECC_ERR_THRSH)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>1B_ECC_ERR_THRSH</td>
<td>RW</td>
<td>1-bit ECC error threshold. The DDR3 controller will generate an interrupt when the 1-bit ECC error count is greater than this threshold. A value of 0 will disable the generation of interrupt.</td>
</tr>
<tr>
<td>23-16</td>
<td>Reserved</td>
<td>R</td>
<td>Reserved for future use</td>
</tr>
<tr>
<td>15-0</td>
<td>1B_ECC_ERR_WIN</td>
<td>RW</td>
<td>1-bit ECC error window in number of refresh periods. The controller will generate an interrupt when the 1-bit ECC error count is equal to or greater than the threshold within this window. A value of 0 will disable the window. Refresh period is defined by REFRESH_RATE in SDRAM Refresh Control register.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; \( n \) = value after reset; \( -x \), value is indeterminate — see the device-specific data manual.
4.30 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1)

The ONE_BIT_ECC_ERR_DIST_1 register is described in the following figure and table.

**Figure 4-30. 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1)**

<table>
<thead>
<tr>
<th>31-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1B_ECC_ERR_DST_1</td>
</tr>
<tr>
<td>WOC=0x0</td>
</tr>
</tbody>
</table>

Legend: R = Read only; WOC = Write one to clear; -n = value after reset; -x, value is indeterminate — see the device-specific data manual.

**Table 4-32. 1-Bit ECC Error Distribution 1 Register (ONE_BIT_ECC_ERR_DIST_1) Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>1B_ECC_ERR_DST_1</td>
<td>WOC</td>
<td>1-bit ECC error distribution over data bus bits 31:0. A value of 1 on a bit indicates 1-bit error on the corresponding bit on the data bus. Writing a 1 to any bit will clear that bit. Writing a 0 has no effect.</td>
</tr>
</tbody>
</table>
4.31 1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG)

The ONE_BIT_ECC_ERR_ADDR_LOG register is described in the following figure and table.

**Figure 4-31. 1-Bit ECC Error Address Log Register (ONE_BIT_ECC_ERR_ADDR_LOG)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>1B_ECC_ERR_ADDR</td>
<td>RW</td>
<td>1-bit ECC error address. Most significant bits of the starting address of the first two SDRAM bursts that had the 1-bit ECC error. This field displays the first address logged in the 2 deep address logging FIFO. Writing a 0x1 will pop one element of the FIFO. Writing a 0x2 will pop both the elements of the FIFO. Writing any other value has no effect.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; \(-n\) = value after reset; \(-x\), value is indeterminate — see the device-specific data manual.
2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG)

The TWO_BIT_ECC_ERR_ADDR_LOG register is shown in the figure and table below.

Figure 4-32. 2-Bit ECC Error Address Log Register (TWO_BIT_ECC_ERR_ADDR_LOG)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>2B_ECC_ERR_ADDR</td>
<td>RW</td>
<td>2-bit ECC error address. Most significant bits of the starting address of the first SDRAM burst that had the 2-bit ECC error. Writing a 0x1 will clear this field. Writing any other value has no effect.</td>
</tr>
</tbody>
</table>
The ONE_BIT_ECC_ERR_DIST_2 register is described in the figure and table below.

**Figure 4-33. 1-Bit ECC Error Distribution 2 Register (ONE_BIT_ECC_ERR_DIST_2)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>1B_ECC_ERR_DST_2</td>
<td>WOC</td>
<td>1-bit ECC error distribution over data bus bits 63:32. A value of 1 on a bit indicates 1-bit error on the corresponding bit on the data bus. Writing a 1 to any bit will clear that bit. Writing a 0 has no effect.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; WOC = Write one to clear; - n = value after reset; -x, value is indeterminate — see the device-specific data manual
4.34 PHY Initialization Register (PIR)

The PHY Initialization register is used to configure and control initialization of the DDR3 PHY. This includes the triggering of certain initialization routines, as well as reset of the PHY and/or the PLLs used in the PHY. Any PIR register bit used to trigger an initialization routine (bits 0 to 15) is self clearing and is set to 0 once the initialization is done. Any configuration register write that sets the PIR[INIT] register bit triggers initialization as selected by the other PIR register bits. The completion status of this initialization can be checked by polling the PHY General Status Register 0.

Figure 4-34. PHY Initialization Register (PIR)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>INITBYP</td>
<td>Reset = 0x0 Initialization Bypass: Bypasses or stops, if set, all initialization routines currently running, including PHY initialization, DRAM initialization, and PHY training. Initialization may be triggered manually using INIT and the other relevant bits of the PIR register. This bit is self-clearing.</td>
</tr>
<tr>
<td>30</td>
<td>ZCALBYP</td>
<td>Reset = 0x0 Impedance Calibration Bypass: Bypasses or stops, if set, impedance calibration of all ZQ control blocks that automatically triggers after reset. Impedance calibration may be triggered manually using INIT and ZCAL bits of the PIR register. This bit is self-clearing.</td>
</tr>
<tr>
<td>29</td>
<td>DCALBYP</td>
<td>Reset = 0x0 Digital Delay Line (DDL) Calibration Bypass: Bypasses or stops, if set, DDL calibration that automatically triggers after reset. DDL calibration may be triggered manually using INIT and DCAL bits of the PIR register. This bit is self-clearing.</td>
</tr>
<tr>
<td>28</td>
<td>LOCKBYP</td>
<td>Reset = 0x0 PLL Lock Bypass: Bypasses or stops, if set, the waiting of PLLs to lock. PLL lock wait is automatically triggered after reset. PLL lock wait may be triggered manually using INIT and PLLLOCK bits of the PIR register. This bit is self-clearing.</td>
</tr>
<tr>
<td>27</td>
<td>CLRSR</td>
<td>Reset = 0x0 Clear Status Registers: A write of ‘1’ to this bit will clear (reset to ‘0’) all status registers, including PGSR and DXnGSR. The clear status register bit is self-clearing. Note, this bit does not clear the PGSR.IDONE bit. If the IDONE bit is set it remains at 1'b1 to indicate the PUB has competed its task. This bit is primarily for debug purposes and is typically not needed during normal functional operation. It can be used when PGSR.IDONE=1, to manually clear the PGSR status bits, although starting a new init process will automatically clear the PGSR status bits. Or it can be used to manually clear the DXnGSR status bits, although starting a new data training process will automatically clear the DXnGSR status bits.</td>
</tr>
<tr>
<td>26-19</td>
<td>Reserved</td>
<td>Reset = 0x0 Returns zeros on reads.</td>
</tr>
<tr>
<td>18</td>
<td>CTLDINIT</td>
<td>Reset = 0x0 Controller DRAM Initialization: Indicates if set that DRAM initialization will be performed by the controller. Otherwise if not set it indicates that DRAM initialization will be performed using the built-in initialization sequence or using software through the configuration port.</td>
</tr>
<tr>
<td>17</td>
<td>PLLBYP</td>
<td>Reset = 0x0 PLL Bypass: A setting of 1 on this bit will put all PHY PLLs in bypass mode.</td>
</tr>
</tbody>
</table>
### Table 4-36. PHY Initialization Register (PIR) Field Descriptions (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>ICPC</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Initialization Complete Pin Configuration: Specifies how the DFI initialization complete output pin (dfi_init_complete) should be used to indicate the status of initialization.&lt;br&gt;Valid value are:&lt;br&gt;• 0 = Asserted after PHY initialization (DLL locking and impedance calibration) is complete.&lt;br&gt;• 1 = Asserted after PHY initialization is complete and the triggered the PUB initialization (DRAM initialization, data training, or initialization trigger with no selected initialization) is complete.</td>
</tr>
<tr>
<td>15</td>
<td>WREYE</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Write Data Eye Training: Executes a PUB training routine to maximize the write data eye.</td>
</tr>
<tr>
<td>14</td>
<td>RDEYE</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Read Data Eye Training: Executes a PUB training routine to maximize the read data eye.</td>
</tr>
<tr>
<td>13</td>
<td>WRDSKW</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Write Data Bit Deskew: Executes a PUB training routine to deskew the DQ bits during write</td>
</tr>
<tr>
<td>12</td>
<td>RDDSKW</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Read Data Bit Deskew: Executes a PUB training routine to deskew the DQ bits during read</td>
</tr>
<tr>
<td>11</td>
<td>WLADJ</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Write Leveling Adjust (DDR3 Only): Executes a PUB training routine that readjusts the write latency used during write in case the write leveling routine changed the expected latency.</td>
</tr>
<tr>
<td>10</td>
<td>QSGATE</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Read DQS Gate Training: Executes a PUB training routine to determine the optimum position of the read data DQS strobe for maximum system timing margins</td>
</tr>
<tr>
<td>9</td>
<td>WL</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Write Leveling (DDR3 Only): Executes a PUB write leveling routine.</td>
</tr>
<tr>
<td>8</td>
<td>DRAMINIT</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; DRAM Initialization: Executes the DRAM initialization sequence</td>
</tr>
<tr>
<td>7</td>
<td>DRAMRST</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; DRAM Reset: Issues a reset to the DRAM (by driving the DRAM reset pin low) and wait 200us. This can be triggered in isolation or with the full DRAM initialization (DRAMINIT). For the later case, the reset is issued and 200us is waited before starting the full initialization sequence.</td>
</tr>
<tr>
<td>6</td>
<td>PHYRST</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; PHY Reset: Resets the AC and DATX8 modules by asserting the AC/DATX8 reset pin.</td>
</tr>
<tr>
<td>5</td>
<td>DCAL</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Digital Delay Line (DDL) Calibration: Performs PHY delay line calibration.</td>
</tr>
<tr>
<td>4</td>
<td>PLLINIT</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; PLL Initialization: Executes the PLL initialization sequence which includes correct driving of PLL power-down, reset and gear shift pins, and then waiting for the PHY PLLs to lock.</td>
</tr>
<tr>
<td>3-2</td>
<td>Reserved</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Returns zeros on reads</td>
</tr>
<tr>
<td>1</td>
<td>ZCAL</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Impedance Calibration: Performs PHY impedance calibration. When set the impedance calibration will be performed in parallel with PHY initialization (PLL initialization + DDL calibration + PHY reset).</td>
</tr>
<tr>
<td>0</td>
<td>INIT</td>
<td><strong>Reset = 0x0</strong>&lt;br&gt; Initialization Trigger: A write of ‘1’ to this bit triggers the DDR system initialization, including PHY initialization, DRAM initialization, and PHY training. The exact initialization steps to be executed are specified in bits 1 to 15 of this register. A bit setting of 1 means the step will be executed as part of the initialization sequence, while a setting of ‘0’ means the step will be bypassed. The initialization trigger bit is self-clearing.</td>
</tr>
</tbody>
</table>
4.35 PHY General Configuration Register 0 (PGCR0)

PGCR0-2 are used for miscellaneous PHY configurations such as enabling VT drift compensation and setting up write-leveling.

Figure 4-35. PHY General Configuration Register 0 (PGCR0)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-26| CKEN     | Reset = 101010b. Controls whether the CK going to the SDRAM is enabled (toggling) or disabled (static value) and whether the CK is inverted. Two bits for each of the up to three CK pairs. Valid values for the two bits are:
  • 00 = CK disabled (Driven to constant 0)
  • 01 = CK toggling with inverted polarity
  • 10 = CK toggling with normal polarity (This should be the default setting)
  • 11 = CK disabled (Driven to constant 1)
  TI recommends that this field be always programmed to 101010b. |
| 25-19| Reserved | Reset = 0x0. Returns zeros on reads.                                          |
| 18-14| DTOSEL   | Reset = 0x0. Digital Test Output Select: Selects the PHY digital test output that should be driven onto PHY digital test output (phy_dto) pin. Valid values are:
  • 00000 = DATX8 0 PLL digital test output
  • 00001 = DATX8 1 PLL digital test output
  • 00010 = DATX8 2 PLL digital test output
  • 00011 = DATX8 3 PLL digital test output
  • 00100 = DATX8 4 PLL digital test output
  • 00101 = DATX8 5 PLL digital test output
  • 00110 = DATX8 6 PLL digital test output
  • 00111 = DATX8 7 PLL digital test output
  • 01000 = DATX8 8 PLL digital test output
  • 01001 = AC PLL digital test output
  • 01010 – 01111 = Reserved
  • 10000 = DATX8 0 delay line digital test output
  • 10001 = DATX8 1 delay line digital test output
  • 10010 = DATX8 2 delay line digital test output
  • 10011 = DATX8 3 delay line digital test output
  • 10100 = DATX8 4 delay line digital test output
  • 10101 = DATX8 5 delay line digital test output
  • 10110 = DATX8 6 delay line digital test output
  • 10111 = DATX8 7 delay line digital test output
  • 11000 = DATX8 8 delay line digital test output
  • 11001 = AC delay line digital test output
  • 11010 – 11111 = Reserved |

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual.
<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13-12</td>
<td>OSCWDL</td>
<td>Reset = 0x3 Scatters which of the two write leveling LCDLs is active. Delay select value of the inactive LCDL is set to zero while delay select</td>
</tr>
<tr>
<td></td>
<td></td>
<td>value of the active LCDL can be varied by the input write leveling delay select pin. Valid values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 00 = No WL LCDL is active</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 01 = DDR WL LCDL is active</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 10 = SDR WL LCDL is active</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 11 = Both LCDLs are active</td>
</tr>
<tr>
<td>11-9</td>
<td>OSCDIV</td>
<td>Reset = 0x7 Specifies the factor by which the delay line oscillator mode output is divided down before it is output on the delay line digital</td>
</tr>
<tr>
<td></td>
<td></td>
<td>test output pin dl_dto. Valid values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 000 = Divide by 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 001 = Divide by 256</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 010 = Divide by 512</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 011 = Divide by 1024</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 100 = Divide by 2048</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 101 = Divide by 4096</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 110 = Divide by 8192</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 111 = Divide by 65536</td>
</tr>
<tr>
<td>8</td>
<td>OSCEN</td>
<td>Reset = 0x0 Enables, if set, the delay line oscillation.</td>
</tr>
<tr>
<td>7</td>
<td>DLTST</td>
<td>Reset = 0x0 A write of '1' to this bit will trigger delay line oscillator mode period measurement. This bit is not self clearing and needs to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>be reset to '0' before the measurement can be re-triggered.</td>
</tr>
<tr>
<td>6</td>
<td>DLTMODE</td>
<td>Reset = 0x0 Selects, if set, the delay line oscillator test mode.</td>
</tr>
<tr>
<td>5</td>
<td>RDBVT</td>
<td>Reset = 0x1 Enables, if set the VT drift compensation of the read data bit delay lines</td>
</tr>
<tr>
<td>4</td>
<td>WDBVT</td>
<td>Reset = 0x1 Enables, if set the VT drift compensation of the write data bit delay lines</td>
</tr>
<tr>
<td>3</td>
<td>RGLVT</td>
<td>Reset = 0x1 Enables, if set the VT drift compensation of the read DQS gating LCDL</td>
</tr>
<tr>
<td>2</td>
<td>RDLVT</td>
<td>Reset = 0x1 Enables, if set the VT drift compensation of the read DQS LCDL</td>
</tr>
<tr>
<td>1</td>
<td>WDLVT</td>
<td>Reset = 0x1 Enables, if set the VT drift compensation of the write DQ LCDL</td>
</tr>
<tr>
<td>0</td>
<td>WLLLVT</td>
<td>Reset = 0x1 Enables, if set, the VT drift compensation of the write leveling LCDL</td>
</tr>
</tbody>
</table>
4.36 **PHY General Configuration Register 1 (PGCR1)**

PGCR0-2 are used for miscellaneous PHY configurations such as enabling VT drift compensation and setting up write-leveling.

**Figure 4-36. PHY General Configuration Register 1 (PGCR1)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>LBMODE</td>
<td>Loopback Mode: Indicates, if set, that the PHY/PUB is in loopback mode</td>
</tr>
<tr>
<td>30-29</td>
<td>LBGDQS</td>
<td>Loopback DQS Gating: Selects the DQS gating mode that should be used when the PHY is in loopback mode, including BIST loopback mode. Valid values are: • 00 = DQS gate is always on • 01 = DQS gate training will be triggered on the PUB • 10 = DQS gate is set manually using software • 11 = Reserved</td>
</tr>
<tr>
<td>28</td>
<td>LBDQSS</td>
<td>Loopback DQS Shift: Selects how the read DQS is shifted during loopback to ensure that the read DQS is centered into the read data eye. Valid values are: • 0 = PUB sets the read DQS LCDL to 0; DQS is already shifted 90 degrees by write path • 1 = The read DQS shift is set manually through software</td>
</tr>
<tr>
<td>27</td>
<td>IOLB</td>
<td>I/O Loop-Back Select: Selects where inside the I/O the loop-back of signals happens. Valid values are: • 0 = Loopback is after output buffer; output enable must be asserted • 1 = Loopback is before output buffer; output enable is don’t care</td>
</tr>
<tr>
<td>26</td>
<td>INHVT</td>
<td>VT Calculation Inhibit: Inhibits calculation of the next VT compensated delay line values. A value of 1 will inhibit the VT calculation. This bit should be set to 1 during writes to the delay line registers. This bit should NOT be set to 1 until after PHY initialization completes</td>
</tr>
<tr>
<td>25</td>
<td>PHYHRST</td>
<td>PHY High-Speed Reset: A write of ‘0’ to this bit resets the AC and DATX8 macros without resetting PUB RTL logic. This bit is not self-clearing and a ‘1’ must be written to de-assert the reset</td>
</tr>
<tr>
<td>24-23</td>
<td>ZCKSEL</td>
<td>Impedance Clock Divider Select: Selects the divide ratio for the clock used by the impedance control logic relative to the clock used by the memory controller and SDRAM. Valid values are: • 00 = Divide by 2 • 01 = Divide by 8 • 10 = Divide by 32 • 11 = Divide by 64 TI recommends that this field be always programmed to 01b.</td>
</tr>
<tr>
<td>Bits</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>----------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>22-15</td>
<td>DDLMT</td>
<td>Reset = 0x1&lt;br&gt;Delay Line VT Drift Limit: Specifies the minimum change in the delay line VT drift in one direction which should result in the assertion of the delay line VT drift status signal (vt_drift). The limit is specified in terms of delay select values. A value of 0 disables the assertion of delay line VT drift status signal.</td>
</tr>
<tr>
<td>14-13</td>
<td>FDEPTH</td>
<td>Reset = 0x2&lt;br&gt;Filter Depth: Specifies the number of measurements over which all AC and DATX8 initial period measurements, that happen after reset or when calibration is manually triggered, are averaged. Valid values are:&lt;br&gt;- 00 = 2&lt;br&gt;- 01 = 4&lt;br&gt;- 10 = 8&lt;br&gt;- 11 = 16</td>
</tr>
<tr>
<td>12-11</td>
<td>LPFDEPTH</td>
<td>Reset = 0x0&lt;br&gt;Low-Pass Filter Depth: Specifies the number of measurements over which MDL period measurements are filtered. This determines the time constant of the low pass filter. Valid values are:&lt;br&gt;- 00 = 2&lt;br&gt;- 01 = 4&lt;br&gt;- 10 = 8&lt;br&gt;- 11 = 16</td>
</tr>
<tr>
<td>10</td>
<td>LPFEN</td>
<td>Reset = 0x1&lt;br&gt;Low-Pass Filter Enable: Enables, if set, the low pass filtering of MDL period measurements.</td>
</tr>
<tr>
<td>9</td>
<td>MDLEN</td>
<td>Reset = 0x0&lt;br&gt;Master Delay Line Enable: Enables, if set, the AC master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or on when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high.</td>
</tr>
<tr>
<td>8-7</td>
<td>IODDRM</td>
<td>Reset = 0x0&lt;br&gt;This field should be programmed to 0x1 if using DDR3 and 0x2 if using DDR3L.&lt;br&gt;- 1 = DDR3&lt;br&gt;- 2 = DDR3L</td>
</tr>
<tr>
<td>6</td>
<td>WLSELT</td>
<td>Reset = 0x0&lt;br&gt;Write Leveling Select Type: Selects the encoding type for the write leveling select signal depending on the desired setup/hold margins for the internal pipelines. Valid values are:&lt;br&gt;- 0 = Setup margin of 90 degrees and hold margin of 90 degrees&lt;br&gt;- 1 = Setup margin of 135 degrees and hold margin of 45 degrees</td>
</tr>
<tr>
<td>5-3</td>
<td>Reserved</td>
<td>Reset = 0x0&lt;br&gt;Return zeros on reads.</td>
</tr>
<tr>
<td>2</td>
<td>WSTEP</td>
<td>Reset = 0x0&lt;br&gt;Write Leveling Step: Specifies the number of delay step-size increments during each step of write leveling. Valid values are:&lt;br&gt;- 0 = 32 step sizes&lt;br&gt;- 1 = 1 step size</td>
</tr>
<tr>
<td>1</td>
<td>WMODE</td>
<td>Reset = 0x1&lt;br&gt;Write Leveling (Software) Mode: Indicates if set that the PHY is in software write leveling mode in which software executes single steps of DQS pulsing by writing '1' to PIR.WL. The write leveling DQ status from the DRAM is captured in DXnGSR0.WLDQ</td>
</tr>
<tr>
<td>0</td>
<td>PDDISDX</td>
<td>Reset = 0x1&lt;br&gt;Power Down Disabled Byte: Indicates if set that the PLL and I/Os of a disabled byte should be powered down</td>
</tr>
</tbody>
</table>
4.37 PHY General Configuration Register 2 (PGCR2)

PGCR0-2 are used for miscellaneous PHY configurations such as enabling VT drift compensation and setting up write-leveling.

![Figure 4-37. PHY General Configuration Register 2 (PGCR2)](image)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>DYNACPDD</td>
<td>Dynamic AC Power Down Driver: Powers down, when set, the output driver on I/O for the address and bank address lines</td>
</tr>
<tr>
<td>30-28</td>
<td>Reserved</td>
<td>Reset = 0x0. These bits should be always programmed to 0.</td>
</tr>
<tr>
<td>27-20</td>
<td>DTPMXTMR</td>
<td>Reset = 0xF. Data Training PUB Mode Timer Exit: Specifies the number of controller clocks to wait when entering and exiting pub mode data training. The default value ensures controller refreshes do not cause memory model errors when entering and exiting data training. The value should be increased if controller initiated SDRAM ZQ short or long operation may occur just before or just after the execution of data training.</td>
</tr>
<tr>
<td>19</td>
<td>FXDLAT</td>
<td>Reset = 0x0. Fixed Latency: Specified whether all reads should be returned to the controller with a fixed read latency. Enabling fixed read latency increases the read latency. Valid values are: • 0 = Disable fixed read latency • 1 = Enable fixed read latency Fixed read latency is calculated as (12 + (maximum DXnGTR.RxDGSL)/2) half data rate clock cycles.</td>
</tr>
<tr>
<td>18</td>
<td>NOBUB</td>
<td>Reset = 0x0. No Bubbles: Specified whether reads should be returned to the controller with no bubbles. Enabling no-bubble reads increases the read latency. Valid values are: • 0 = Bubbles are allowed during reads • 1 = Bubbles are not allowed during reads</td>
</tr>
<tr>
<td>17-0</td>
<td>IREFPRD</td>
<td>Reset = 0x12480. Refresh Period: Indicates the period in clock cycles after which the PUB has to issue a refresh command to the SDRAM. This is derived from the maximum refresh interval from the datasheet, tRFC(max) or REFI, divided by the clock cycle time. A further 400 clocks must be subtracted from the derived number to account for command flow and missed slots of refreshes in the internal PUB blocks. The default corresponds to DDR3 9<em>7.8us at 1066MHz (DDR3-2133) when a burst of 9 refreshes are issued at every refresh interval. TI recommends tREFPRD be programmed to 5</em>tREFI.</td>
</tr>
</tbody>
</table>
4.38 PHY General Status Register 0 (PGSR0)

PGSR0-1 are general status registers for the PHY. They indicate, among other things, whether initialization, write leveling or period measurement calibrations are done.

**Figure 4-38. PHY General Status Register 0 (PGSR0)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31   | APLOCK     | Reset = 0x0
AC PLL Lock: Indicates, if set, that AC PLL has locked. This is a direct status of the AC PLL lock pin |
| 30-28| Reserved   | Reset = 0x0
Returns zeros on reads. |
| 27   | WEERR      | Reset = 0x0
Write Eye Training Error: Indicates if set that there is an error in write eye training. |
| 26   | REERR      | Reset = 0x0
Read Eye Training Error: Indicates if set that there is an error in read eye training |
| 25   | WDERR      | Reset = 0x0
Write Bit Deskew Error: Indicates if set that there is an error in write bit deskew |
| 24   | RDERR      | Reset = 0x0
Read Bit Deskew Error: Indicates if set that there is an error in read bit deskew |
| 23   | WLAERR     | Reset = 0x0
Write Leveling Adjustment Error: Indicates if set that there is an error in write leveling adjustment |
| 22   | QSGERR     | Reset = 0x0
DQS Gate Training Error: Indicates if set that there is an error in DQS gate training. |
| 21   | WLERR      | Reset = 0x0
Write Leveling Error: Indicates if set that there is an error in write leveling. |
| 20   | ZCERR      | Reset = 0x0
Impedance Calibration Error: Indicates if set that there is an error in impedance calibration. |
| 19-12| Reserved   | Reset = 0x0
Returns zeros on reads. |
| 11   | WEDONE     | Reset = 0x0
Write Eye Training Done: Indicates if set that write eye training has completed |
| 10   | REDONE     | Reset = 0x0
Read Eye Training Done: Indicates if set that read eye training has completed |
| 9    | WDDONE     | Reset = 0x0
Write Bit Deskew Done: Indicates if set that write bit deskew has completed. |
| 8    | RDDONE     | Reset = 0x0
Read Bit Deskew Done: Indicates if set that read bit deskew has completed. |
| 7    | WLADONE    | Reset = 0x0
Write Leveling Adjustment Done: Indicates if set that write leveling adjustment has completed |
| 6    | QSGDONE    | Reset = 0x0
DQS Gate Training Done: Indicates if set that DQS gate training has completed. |

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual
<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>WLDONE</td>
<td>Reset = 0x0&lt;br&gt;Write Leveling Done: Indicates if set that write leveling has completed.</td>
</tr>
<tr>
<td>4</td>
<td>DIDONE</td>
<td>Reset = 0x0&lt;br&gt;DRAM Initialization Done: Indicates if set that DRAM initialization has completed</td>
</tr>
<tr>
<td>3</td>
<td>ZCDONE</td>
<td>Reset = 0x0&lt;br&gt;Impedance Calibration Done: Indicates if set that impedance calibration has completed</td>
</tr>
<tr>
<td>2</td>
<td>DCDONE</td>
<td>Reset = 0x0&lt;br&gt;Digital Delay Line (DDL) Calibration Done: Indicates if set that DDL calibration has completed</td>
</tr>
<tr>
<td>1</td>
<td>PLDONE</td>
<td>Reset = 0x0&lt;br&gt;PLL Lock Done: Indicates if set that PLL locking has completed.</td>
</tr>
<tr>
<td>0</td>
<td>IDONE</td>
<td>Reset = 0x0&lt;br&gt;Initialization Done: Indicates if set that the DDR system initialization has completed. This bit is set after all the selected initialization routines in PIR register have completed.</td>
</tr>
</tbody>
</table>
PHY General Status Register 1 (PGSR1)

PGSR0-1 are general status registers for the PHY. They indicate, among other things, whether initialization, write leveling or period measurement calibrations are done.

**Figure 4-39. PHY General Status Register 1 (PGSR1)**

<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0x0</td>
<td>R</td>
<td>0x0</td>
<td>R</td>
<td>0x0</td>
<td>R</td>
<td>0x0</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual

### Table 4-41. PHY General Status Register 1 (PGSR1) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31   | Reserved | Reset = 0x0  
Returns zeros on reads. |
| 30   | VTSTOP | Reset = 0x0  
VT Stop: Indicates if set that the VT calculation logic has stopped computing the next values for the VT compensated delay line values. After assertion of the PGCR.INHVT, the VTSTOP bit should be read to ensure all VT compensation logic has stopped computations before writing to the delay line registers |
| 29-25| Reserved | Reset = 0x0  
Returns zeros on reads. |
| 24-1 | DLTCODE| Reset = 0x0  
Delay Line Test Code: Returns the code measured by the PHY control block that corresponds to the period of the AC delay line digital test output. |
| 0    | DLTDONE| Reset = 0x0  
Delay Line Test Done: Indicates, if set, that the PHY control block has finished doing period measurement of the AC delay line digital test output |
4.40 PLL Control Register (PLLCR)

The PLLCR register provides miscellaneous controls of the PLLs used in the AC and DATX8 macros, including PLL test modes and PLL bypass.

Figure 4-40. PLL Control Register (PLLCR)

![Figure 4-40. PLL Control Register (PLLCR)](image)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>BYP</td>
<td>Reset = 0x0                    PLL Bypass: Bypasses the PLL if set to 1.</td>
</tr>
<tr>
<td>30</td>
<td>PLLRST</td>
<td>Reset = 0x0                    PLL Rest: Resets the PLLs by driving the PLL reset pin. This bit is not self-clearing and a '0' must be written to de-assert the reset.</td>
</tr>
<tr>
<td>29</td>
<td>PLLPD</td>
<td>Reset = 0x0                    PLL Power Down: Puts the PLLs in power down mode by driving the PLL power down pin. This bit is not self-clearing and a '0' must be written to de-assert the power-down</td>
</tr>
<tr>
<td>28-20</td>
<td>Reserved</td>
<td>Reset = 0x0                    Returns zeros on reads.</td>
</tr>
</tbody>
</table>
| 19-18| FRQSEL      | Reset = 0x0                    PHY PLL reference frequency select: Selects the operating range of the PHY PLL. Valid values are:  
|        |             | 00 = PHY PLL reference clock ranges from 335 MHz to 533 MHz                 |
|        |             | 01 = PHY PLL reference clock ranges from 225 MHz to 385 MHz                 |
|        |             | 10 = Reserved                  Reserved                                      |
|        |             | 11 = PHY PLL reference clock ranges from 166 MHz to 275 MHz                 |
| 17    | QPMODE      | Reset = 0x0                    PLL Quadrature Phase Mode: Enables, if set, the quadrature phase clock outputs. This mode is not used in this version of the PHY |
| 16-13 | CPPC        | Reset = 0xE                    Charge Pump Proportional Current Control   |
| 12-11 | CPIC        | Reset = 0x0                    Charge Pump Integrating Current Control    |
| 10    | GSHIFT      | Gear Shift: Enables, if set, rapid locking mode.                            |
| 9-0   | Reserved    | Reset = 0x0                    Reads return zeros                           |

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual
PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

Table 4-43. PHY Timing Register 0 (PTR0) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-21</td>
<td>tPLLPD</td>
<td>PLL Power-Down Time: Number of configuration clock cycles that the PLL must remain in power-down mode, i.e. number of clock cycles from when PLL power-down pin is asserted to when PLL power-down pin is de-asserted. This must correspond to a value that is equal to or more than 1us. Default value corresponds to 1us.</td>
</tr>
<tr>
<td>20-6</td>
<td>tPLLGS</td>
<td>PLL Gear Shift Time: Number of configuration clock cycles from when the PLL reset pin is de-asserted to when the PLL gear shift pin is de-asserted. This must correspond to a value that is equal to or more than 4us. Default value corresponds to 4us.</td>
</tr>
<tr>
<td>5-0</td>
<td>tPHYRST</td>
<td>PHY Reset Time: Number of configuration clock cycles that the PHY reset must remain asserted after PHY calibration is done before the reset to the PHY is de-asserted. This is used to extend the reset to the PHY so that the reset is asserted for some clock cycles after the clocks are stable. TI recommends setting this to 15.</td>
</tr>
</tbody>
</table>
4.42 PHY Timing Register 1 (PTR1)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e., JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

![Figure 4-42. PHY Timing Register 1 (PTR1)](https://www.ti.com/lit/ml/sw486e/sw486e.pdf)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-16| tPLLLOCK     | Reset = 0xD056
PLL Lock Time: Number of configuration clock cycles for the PLL to stabilize and lock, i.e., number of clock cycles from when the PLL reset pin is de-asserted to when the PLL has lock and is ready for use. This must correspond to a value that is equal to or more than 100us. Default value corresponds to 100us. |
| 15-13| Reserved     | Reset = 0x0
Reads return zeros.                                                                                                                             |
| 12-0 | tPLLRST      | Reset = 0x12C0
PLL Reset Time: Number of configuration clock cycles that the PLL must remain in reset mode, i.e., number of clock cycles from when PLL power-down pin is de-asserted and PLL reset pin is asserted to when PLL reset pin is de-asserted. This must correspond to a value that is equal to or more than 9 us. Default value corresponds to 9 us. |

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual
4.43 PHY Timing Register 2 (PTR2)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

![Figure 4-43. PHY Timing Register 2 (PTR2)](image-url)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-20| Reserved | Reset = 0x0
Reads return zeros. |
| 19-15| tWLDLYS  | Reset = 0x10
Write Leveling Delay Settling Time: Number of controller clock cycles from when a new value of the write leveling delay is applied to the LCDL to when to DQS high is driven high. This allows the delay to settle |
| 14-10| tCALH    | Reset = 0xF
Calibration Hold Time: Number of controller clock cycles from when the clock was disabled (cal_clk_en deasserted) to when calibration is enable (cal_en asserted). |
| 9-5  | tCALS    | Reset = 0xF
Calibration Setup Time: Number of controller clock cycles from when calibration is enabled (cal_en asserted) to when the calibration clock is asserted again (cal_clk_en asserted). |
| 4-0  | tCALON   | Reset = 0xF
Calibration On Time: Number of controller clock cycles that the calibration clock is enabled (cal_clk_en asserted). |
### 4.44 PHY Timing Register 3 (PTR3)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

#### Table 4-46. PHY Timing Register 3 (PTR3) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-29</td>
<td>Reserved</td>
<td>Reset = 0x0&lt;br&gt;Reads return zeros.</td>
</tr>
<tr>
<td>28-20</td>
<td>tDINIT1</td>
<td>Reset = 0x180&lt;br&gt;DRAM Initialization Time 1: DRAM initialization time in DRAM clock cycles corresponding to the following:&lt;br&gt;DDR3 = CKE high time to first command (tRFC + 10 ns or 5 tCK, whichever is bigger)&lt;br&gt;Default value corresponds to DDR3 tRFC of 360ns at 1066 MHz&lt;br&gt;tDINIT1 = (tCKE/tCK)-1</td>
</tr>
<tr>
<td>19-0</td>
<td>tDINIT0</td>
<td>Reset = 0x82536&lt;br&gt;DRAM Initialization Time 0: DRAM initialization time in DRAM clock cycles corresponding to the following:&lt;br&gt;DDR3 = CKE low time with power and clock stable (500 us)</td>
</tr>
</tbody>
</table>
4.45 PHY Timing Register 4 (PTR4)

PHY Timing Registers are used to program different timing parameters used by the PHY logic. All the default values shown in these tables are in decimal format and correspond to the highest speed the PHY can be compiled for, i.e. JEDEC DDR3-2133N speed grade. This corresponds to DRAM bit rate of 2133Mbps, DRAM clock frequency of 1066MHz, controller clock frequency of 533MHz, and configuration clock frequency of 533MHz. Configure these parameters assuming controller and configuration clocks of 533MHz. The clocks in which the timing numbers are measured are specified in the description of each parameter.

![Figure 4-45. PHY Timing Register 4 (PTR4)](image)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>Reserved</td>
<td>Reset = 0x0&lt;br&gt;Reads return zeros.</td>
</tr>
<tr>
<td>27-18</td>
<td>tDINIT3</td>
<td>Reset = 0x2AB&lt;br&gt;DRAM Initialization Time 3: DRAM initialization time in DRAM clock cycles corresponding to the following: &lt;br&gt;DDR3 = Time from ZQ initialization command to first command (1 us)&lt;br&gt;Default value corresponds to the DDR3 640ns at 1066 MHz.</td>
</tr>
<tr>
<td>17-0</td>
<td>tDINIT2</td>
<td>Reset = 0x34156&lt;br&gt;DRAM Initialization Time 2: DRAM initialization time in DRAM clock cycles corresponding to the following:&lt;br&gt;DDR3 = Reset low time (200 us on power-up or 100 ns after power-up)&lt;br&gt;Default value corresponds to DDR3 200 us at 1066 MHz.</td>
</tr>
</tbody>
</table>
The AC I/O Configuration Register is used to control the slew rate on the address/command lines.

**Figure 4-46. AC I/O Configuration Register (ACIOCR)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-30</td>
<td>ACSR</td>
<td>Reset = 0x0&lt;br&gt;Address/Command Slew Rate: Selects slew rate of the I/O for all address and command pins.&lt;br&gt;00 = very fast (use as default for DDR3 and DDR3L)&lt;br&gt;01 = fast&lt;br&gt;10 = medium&lt;br&gt;11 = slow</td>
</tr>
<tr>
<td>29-0</td>
<td>Reserved</td>
<td>Reset = 0x33C03812&lt;br&gt;Reserved.</td>
</tr>
</tbody>
</table>
4.47 DATX8 Common Configuration Register (DXCCR)

The DATX8 Common Configuration Register is used to control features that affect all DATX8 macros. These include on-die termination enables and power-down enables for SSTL I/Os for all SDRAM data, data mask and data strobe signals.

Figure 4-47. DATX8 Common Configuration Register (DXCCR)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>DDPDRCDO</td>
<td>Reset = 0x4 Dynamic Data Power Down Receiver Count Down Offset: Offset applied in calculating window of time where receiver is powered up</td>
</tr>
<tr>
<td>27-24</td>
<td>DDPDDCDO</td>
<td>Reset = 0x4 Dynamic Data Power Down Driver Count Down Offset: Offset applied in calculating window of time where driver is powered up</td>
</tr>
<tr>
<td>23</td>
<td>DYNDXPDR</td>
<td>Reset = 0x0 Data Power Down Receiver: Dynamically powers down, when set, the input receiver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDR and DXnGCR.DXPDR are not set to 1.</td>
</tr>
<tr>
<td>22</td>
<td>DYNDXPDD</td>
<td>Reset = 0x0 Dynamic Data Power Down Driver: Dynamically powers down, when set, the output driver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDD and DXnGCR.DXPDD are not set to 1.</td>
</tr>
<tr>
<td>21</td>
<td>UDQIOM</td>
<td>Reset = 0x0 Unused DQ I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>20</td>
<td>UDQPDR</td>
<td>Reset = 0x1 Unused DQ Power Down Receiver: Powers down, when set, the input receiver on the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>19</td>
<td>UDQPDD</td>
<td>Reset = 0x1 Unused DQ Power Down Driver: Powers down, when set, the output driver on the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>18</td>
<td>UDOQDT</td>
<td>Reset = 0x0 Unused DQ On-Die Termination: Enables, when set, the on-die termination on the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>17-15</td>
<td>MSBUDQ</td>
<td>Reset = 0x0 Most Significant Byte Unused DQs: Specifies the number of DQ bits that are not used in the most significant byte. The used (valid) bits for this byte are [8-MSBDQ- 1:0]. To disable the whole byte, use the DXnGCR.DXEN register.</td>
</tr>
<tr>
<td>14-13</td>
<td>DXSR</td>
<td>Reset = 0x0 Data Slew Rate: Selects slew rate of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. 00 = very fast (use as default for DDR3 and DDR3L) 01 = fast 10 = medium 11 = slow</td>
</tr>
<tr>
<td>12-9</td>
<td>DQSNRES</td>
<td>Reset = 0xC DQS# Resistor: Selects the on-die pull-up/pull-down resistor for DQS# pins. Same encoding as DQSRES.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-49. DATX8 Common Configuration Register (DXCCR) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>DDPDRCDO</td>
<td>Reset = 0x4 Dynamic Data Power Down Receiver Count Down Offset: Offset applied in calculating window of time where receiver is powered up</td>
</tr>
<tr>
<td>28</td>
<td>DDPDDCDO</td>
<td>Reset = 0x4 Dynamic Data Power Down Driver Count Down Offset: Offset applied in calculating window of time where driver is powered up</td>
</tr>
<tr>
<td>27</td>
<td>DYNDXPDR</td>
<td>Reset = 0x0 Data Power Down Receiver: Dynamically powers down, when set, the input receiver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDR and DXnGCR.DXPDR are not set to 1.</td>
</tr>
<tr>
<td>26</td>
<td>DYNDXPDD</td>
<td>Reset = 0x0 Dynamic Data Power Down Driver: Dynamically powers down, when set, the output driver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDD and DXnGCR.DXPDD are not set to 1.</td>
</tr>
<tr>
<td>25</td>
<td>UDQIOM</td>
<td>Reset = 0x0 Unused DQ I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>24</td>
<td>UDQPDR</td>
<td>Reset = 0x1 Unused DQ Power Down Receiver: Powers down, when set, the input receiver on the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>23</td>
<td>UDQPDD</td>
<td>Reset = 0x1 Unused DQ Power Down Driver: Powers down, when set, the output driver on the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>22</td>
<td>UDOQDT</td>
<td>Reset = 0x0 Unused DQ On-Die Termination: Enables, when set, the on-die termination on the I/O for unused DQ pins.</td>
</tr>
<tr>
<td>21</td>
<td>MSBUDQ</td>
<td>Reset = 0x0 Most Significant Byte Unused DQs: Specifies the number of DQ bits that are not used in the most significant byte. The used (valid) bits for this byte are [8-MSBDQ- 1:0]. To disable the whole byte, use the DXnGCR.DXEN register.</td>
</tr>
<tr>
<td>20</td>
<td>DXSR</td>
<td>Reset = 0x0 Data Slew Rate: Selects slew rate of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. 00 = very fast (use as default for DDR3 and DDR3L) 01 = fast 10 = medium 11 = slow</td>
</tr>
<tr>
<td>19</td>
<td>DQSNRES</td>
<td>Reset = 0xC DQS# Resistor: Selects the on-die pull-up/pull-down resistor for DQS# pins. Same encoding as DQSRES.</td>
</tr>
<tr>
<td>Bits</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>--------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 8-5  | DQSRES | Reset = 0x4  
DQS Resistor: Selects the on-die pull-down/pull-up resistor for DQS pins.  
DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1).  
DQSRES[2:0] selects the resistor value as follows:  
000 = Open: On-die resistor disconnected (use external resistor)  
001 = 688 ohms  
010 = 611 ohms  
011 = 550 ohms  
100 = 500 ohms  
101 = 458 ohms  
110 = 393 ohms  
111 = 344 ohms |
| 4    | DXPDR  | Reset = 0x0  
Data Power Down Receiver: Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDR configuration bit of the individual DATX8. |
| 3    | DXPDD  | Reset = 0x0  
Data Power Down Driver: Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDD configuration bit of the individual DATX8. |
| 2    | MDLEN  | Reset = 0x1  
Master Delay Line Enable: Enables, if set, all DATX8 master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or on when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high. This bit is ANDed with the MDLEN bit in the individual DATX8. |
| 1    | DXIOM  | Reset = 0x0  
Data I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the IOM configuration bit of the individual DATX8. |
| 0    | DXODT  | Reset = 0x0  
Data On-Die Termination: Enables, when set, the on-die termination on the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8. |
4.48 DRAM Configuration Register (DCR)

The DCR register is used to configure the DRAM system, and is described in the figure and table below.

Figure 4-48. DRAM Configuration Register (DCR)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-30</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>29</td>
<td>UDIMM</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>28</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>27</td>
<td>NOSRA</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>26-18</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>17-10</td>
<td>BYTEMASK</td>
<td>Reset = 0x1</td>
</tr>
<tr>
<td>9-8</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>7</td>
<td>MPRDQ</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>6-4</td>
<td>PDQ</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>3</td>
<td>DDR8BNK</td>
<td>Reset = 0x1</td>
</tr>
<tr>
<td>2-0</td>
<td>DDRMD</td>
<td>Reset = 0x3</td>
</tr>
</tbody>
</table>
4.49 **DRAM Timing Parameters Register 0 (DTPR0)**

DTPR0-2 are used to program timing parameters for different DDR3 speed grades. These timing parameters are in DRAM clock cycles and are derived from corresponding parameters in the SDRAM datasheet divided by the DRAM clock cycle time. Non-integer values should be rounded up to the next integer. All the default values correspond to the DDR3-2133 speed grade.

Figure 4-49. DRAM Timing Parameters Register 0 (DTPR0)

![Figure 4-49](image)

Table 4-51. DRAM Timing Parameters Register 0 (DTPR0) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-26 | IRC | Reset = 0x32  
Activate to activate command delay (same bank). Valid values are 2 to 63 |
| 25-22 | IRRD | Reset = 0x7  
Activate to activate command delay (different banks). Valid values are 1 to 15. |
| 21-16 | IRAS | Reset = 0x24  
Activate to precharge command delay. Valid values are 2 to 63 |
| 15-12 | IRCD | Reset = 0xE  
Activate to read or write delay. Minimum time from when an activate command is issued to when a read or write to the activated row can be issued. Valid values are 2 to 15. |
| 11-8  | IRP  | Reset = 0xE  
Precharge command period: The minimum time between a precharge command and any other command. Valid values are 2 to 15. |
| 7-4   | IWTR | Reset = 0x8  
Internal write to read command delay. Valid values are 1 to 15. |
| 3-0   | IRTP | Reset = 0x8  
Internal read to precharge command delay. Valid values are 2 to 15. |
4.50 DRAM Timing Parameters Register 1 (DTPR1)

DTPR0-2 are used to program timing parameters for different DDR3 speed grades. These timing parameters are in DRAM clock cycles and are derived from corresponding parameters in the SDRAM datasheet divided by the DRAM clock cycle time. Non-integer values should be rounded up to the next integer. All the default values correspond to the DDR3-2133 speed grade.

Figure 4-50. DRAM Timing Parameters Register 1 (DTPR1)

<table>
<thead>
<tr>
<th>Bit 31-30</th>
<th>Bit 29-26</th>
<th>Bit 25-20</th>
<th>Bit 19-11</th>
<th>Bit 10-5</th>
<th>Bit 4-2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>tWLO</td>
<td>tWLMRD</td>
<td>tRFC</td>
<td>tFAW</td>
<td>tMOD</td>
<td>tMRD</td>
</tr>
<tr>
<td>Reset = 0x0</td>
<td>RW = 0x8</td>
<td>RW = 0x28</td>
<td>RW = 0x176</td>
<td>RW = 0x26</td>
<td>RW = 0x4</td>
<td>RW = 0x2</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-52. DRAM Timing Parameters Register 1 (DTPR1) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-30</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>29-26</td>
<td>tWLO</td>
<td>Write leveling output delay: Number of clock cycles from when write leveling DQS is driven high by the PHY to when the results from the SDRAM on DQ is sampled by the PHY. This must include the SDRAM tWLO timing parameter plus the round trip delay from the DUT to SDRAM back to the DUT. TI recommends that this field always be programmed to 12 decimal.</td>
</tr>
<tr>
<td>25-20</td>
<td>tWLMRD</td>
<td>Minimum delay from when write leveling mode is programmed to the first DQS/DQS# rising edge</td>
</tr>
<tr>
<td>19-11</td>
<td>tRFC</td>
<td>Refresh-to-Refresh: Indicates the minimum time, in clock cycles, between two refresh commands or between a refresh and an active command. This is derived from the minimum refresh interval from the datasheet, tRFC(min), divided by the clock cycle time.</td>
</tr>
<tr>
<td>10-5</td>
<td>tFAW</td>
<td>4-bank activate period. No more than 4-bank activate commands may be issued in a given tFAW period. Valid values are 2 to 63.</td>
</tr>
<tr>
<td>4-2</td>
<td>tMOD</td>
<td>Load mode update delay. The minimum time between a load mode register command and a non-load mode register command. Valid values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 000 = 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 001 = 13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 010 = 14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 011 = 15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 100 = 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 101 = 17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 110 – 111 = Reserved</td>
</tr>
<tr>
<td>1-0</td>
<td>tMRD</td>
<td>Load mode cycle time: The minimum time between a load mode register command and any other command. For DDR3 this is the minimum time between two load mode register commands. The value used for tMRD is 4 plus the value programmed in these bits, i.e. tMRD ranges from 4 to 7.</td>
</tr>
</tbody>
</table>
4.51 DRAM Timing Parameters Register 2 (DTPR2)

DTPR0-2 are used to program timing parameters for different DDR3 speed grades. These timing parameters are in DRAM clock cycles and are derived from corresponding parameters in the SDRAM datasheet divided by the DRAM clock cycle time. Non-integer values should be rounded up to the next integer. All the default values correspond to the DDR3-2133 speed grade.

Figure 4-51. DRAM Timing Parameters Register 2 (DTPR2)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>tCCD</td>
<td>Reset = 0x0 Read to read and write to write command delay. Valid values are: • 0 = 4 DRAM clock cycles • 1 = 5 DRAM clock cycles</td>
</tr>
<tr>
<td>30</td>
<td>tRTW</td>
<td>Reset = 0x0 Read to Write command delay. This parameter is only used when the PHY issues commands during initialization and leveling. During normal operation, the controller issues commands to the SDRAM and uses the timing parameters programmed in the controller. TI recommends that this bit be always set to 1 to provide additional margin during PHY initiated initialization/leveling.</td>
</tr>
<tr>
<td>29</td>
<td>tRTODT</td>
<td>Reset = 0x0 Read to ODT delay. This parameter is only used when the PHY issues commands during initialization and leveling. During normal operation, the controller issues commands to the SDRAM and uses the timing parameters programmed in the controller. TI recommends that this bit be always set to 0.</td>
</tr>
<tr>
<td>28-19</td>
<td>tDLLK</td>
<td>Reset = 0x200 DLL locking time. Valid values are 2 to 1023.</td>
</tr>
<tr>
<td>18-15</td>
<td>tCKE</td>
<td>Reset = 0x6 CKE minimum pulse width. Also specifies the minimum time that the SDRAM must remain in power down or self refresh mode. This parameter must be set to the value of tCKESR which is usually bigger than the value of tCKE. Valid values are 2 to 15.</td>
</tr>
<tr>
<td>14-10</td>
<td>tXP</td>
<td>Reset = 0x1A Power down exit delay. The minimum time between a power down exit command and any other command. This parameter must be set to the maximum of the various minimum power down exit delay parameters specified in the SDRAM datasheet, i.e. max(tXP, tXPDLL). Valid values are 2 to 31.</td>
</tr>
<tr>
<td>9-0</td>
<td>tXS</td>
<td>Reset = 0x200 Self refresh exit delay. The minimum time between a self refresh exit command and any other command. This parameter must be set to the maximum of the various minimum self refresh exit delay parameters specified in the SDRAM datasheet, i.e. (tXS, tXSDLL) for DDR3. Valid values are 2 to 1023.</td>
</tr>
</tbody>
</table>
### 4.52 Mode Register 0 (MR0)

SDRAM definitions controlled by the Mode Register 0 (MR0) include, among other things, burst length, burst type, CAS latency, operating mode, DLL reset, write recovery and power-down modes.

**Figure 4-52. Mode Register 0 (MR0)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>Reserved</td>
<td>Reset = 0x0&lt;br&gt;Returns zeros on reads.</td>
</tr>
<tr>
<td>15-13</td>
<td>Reserved</td>
<td>Reset = 0x0&lt;br&gt;These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’.</td>
</tr>
<tr>
<td>12</td>
<td>PD</td>
<td>Reset = 0x0&lt;br&gt;Power-Down Control: Controls the exit time for power-down modes. This must always be set to 1.</td>
</tr>
</tbody>
</table>
| 11-9 | WR | Reset = 0x5<br>Write Recovery: This is the value of the write recovery in clock cycles. It is calculated by dividing the datasheet write recovery time, tWR (ns) by the datasheet clock cycle time, tCK (ns) and rounding up a non-integer value to the next integer.<br>Valid values are:  
  • 001 = 5  
  • 010 = 6  
  • 011 = 7  
  • 100 = 8  
  • 101 = 10  
  • 110 = 12  
  • 111 = 14  
  • 000 = 16  
  All other settings are reserved and should not be used. |
| 8 | DR | Reset = 0x0<br>DLL Reset: Writing a ‘1’ to this bit will reset the SDRAM DLL. This bit is self-clearing, i.e. it returns back to ‘0’ after the DLL reset has been issued. |
| 7 | TM | Reset = 0x0<br>Operating Mode: Always set to 0 for normal operating mode. |
| 6-4,2 | CL | Reset = 0xA<br>CAS Latency: The delay, in clock cycles, between when the SDRAM registers a read command to when data is available. Valid values are:  
  • 0010 = 5  
  • 0100 = 6  
  • 0110 = 7  
  • 1000 = 8  
  • 1010 = 9  
  • 1100 = 10  
  • 1110 = 11  
  • 0001 = 12  
  • 0011 = 13  
  • 0101 = 14  
  All other settings are reserved and should not be used. |
Table 4-54. Mode Register 0 (MR0) Field Descriptions (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3    | BT   | Reset = 0x0  
      |       | Burst type: Set to 0 for sequential burst (interleaved burst is not supported) |
| 1-0  | BL   | Reset = 0x0  
      |       | Burst Length: Determines the maximum number of column locations that can be accessed during a given read or write command. Set to 0 for a fixed burst length of 8 (other burst lengths are not supported) |
### Mode Register 1 (MR1)

SDRAM definitions controlled by the Mode register 1 (MR1) include, among other things, DLL enable/disable, drive strength, on-die termination (ODT) resistance, CAS additive latency, off-chip driver (OCD) impedance calibration and output enable.

**Figure 4-53. Mode Register 1 (MR1)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-16 | Reserved | Reset = 0x0  
Returns zeros on reads. |
| 15-13 | Reserved | Reset = 0x0  
These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’. |
| 12 | QOFF | Reset = 0x0  
Output Enable/Disable: Program to ‘0’ for all outputs to function as normal. |
| 11 | TDQS | Reset = 0x0  
Termination Data Strobe: This must always be set to 0. |
| 10 | Reserved | Reset = 0x0  
Reserved. This is a JEDEC reserved bit for DDR3 and is recommended by JEDEC to be programmed to ‘0’. |
| 9 | RTT | Reset = 0x0  
On Die Termination: Selects the effective resistance for SDRAM on die termination. Valid values are:  
• 000 = ODT disabled  
• 001 = RZQ/4  
• 010 = RZQ/2  
• 011 = RZQ/6  
• 100 = RZQ/12  
• 101 = RZQ/8  
All other settings are reserved and should not be used |
| 8 | Reserved | Reset = 0x0  
Reserved. This is a JEDEC reserved bit for DDR3 and is recommended by JEDEC to be programmed to ‘0’. |
| 7 | LEVEL | Reset = 0x0  
Write Leveling Enable: Enables write-leveling when set. |
| 6 | RTT | Reset = 0x0  
On Die Termination: Selects the effective resistance for SDRAM on die termination. Valid values are:  
• 000 = ODT disabled  
• 001 = RZQ/4  
• 010 = RZQ/2  
• 011 = RZQ/6  
• 100 = RZQ/12  
• 101 = RZQ/8  
All other settings are reserved and should not be used |
| 5 | DIC | Reset = 0x0  
Output Driver Impedance Control: Controls the output drive strength. Valid values are:  
• 00 = Reserved for RZQ/6  
• 01 = RZQ7  
• 10 = Reserved  
• 11 = Reserved |
Table 4-55. Mode Register 1 (MR1) Field Descriptions (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 4-3  | AL   | Reset = 0x0  
Posted CAS Additive Latency: the controller does not support this feature. This must always be set to 0. |
| 2    | RTT  | Reset = 0x0  
On Die Termination: Selects the effective resistance for SDRAM on die termination. Valid values are:  
• 000 = ODT disabled  
• 001 = RZQ/4  
• 010 = RZQ/2  
• 011 = RZQ/6  
• 100 = RZQ/12  
• 101 = RZQ/8  
All other settings are reserved and should not be used |
| 1    | DIC  | Reset = 0x0  
Output Driver Impedance Control: Controls the output drive strength. Valid values are:  
• 00 = Reserved for RZQ/6  
• 01 = RZQ7  
• 10 = Reserved  
• 11 = Reserved |
| 0    | DE   | Reset = 0x0  
DLL Enable/Disable: Enable (0) or disable (1) the DLL. DLL must be enabled for normal operation. |
4.54 Mode Register 2 (MR2)

Mode Register 2 controls (among other things) refresh related features of SDRAMs, and is described in the figure and table below.

**Figure 4-54. Mode Register 2 (MR2)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>31</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>3</th>
<th>2</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Reserved</td>
<td>RTTWR</td>
<td>Reserved</td>
<td>SRT</td>
<td>ASR</td>
<td>CWL</td>
<td>PASR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Description</td>
<td>R=0x0</td>
<td>RW=0x0</td>
<td>R=0x0</td>
<td>RW=0x0</td>
<td>RW=0x0</td>
<td>RW=0x0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual.

### Table 4-56. Mode Register 2 (MR2) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-16 | Reserved | Reset = 0x0  
Returns zeros on reads. |
| 15-11 | Reserved | Reset = 0x0  
These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’. |
| 10-9 | RTTWR | Reset = 0x0  
Dynamic ODT: Selects RTT for dynamic ODT. Valid values are:  
• 00 = Dynamic ODT off  
• 01 = RZQ/4  
• 10 = RZQ/2  
• 11 = Reserved |
| 8 | Reserved | Reset = 0x0  
These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’. |
| 7 | SRT | Reset = 0x0  
Self-Refresh Temperature Range: Selects either normal (‘0’) or extended (‘1’) operating temperature range during self-refresh. |
| 6 | ASR | Reset = 0x0  
Auto Self-Refresh: When enabled (‘1’), SDRAM automatically provides self-refresh power management functions for all supported operating temperature values. Otherwise the SRT bit must be programmed to indicate the temperature range. |
| 5-3 | CWL | Reset = 0x0  
CAS Write Latency: The delay, in clock cycles, between when the SDRAM registers a write command to when write data is available. Valid values are:  
• 000 = 5 (tCK > 2.5ns)  
• 001 = 6 (2.5ns > tCK > 1.875ns)  
• 010 = 7 (1.875ns > tCK > 1.5ns)  
• 011 = 8 (1.5ns > tCK > 1.25ns)  
• 100 = 9 (1.25ns > tCK > 1.07ns)  
• 101 = 10 (1.07ns > tCK > 0.935ns)  
• 110 = 11 (0.935ns > tCK > 0.833ns)  
• 111 = 12 (0.833ns > tCK > 0.75ns)  
All other settings are reserved and should not be used |
| 2-0 | PASR | Reset = 0x0  
Partial Array Self Refresh: Specifies that data located in areas of the array beyond the specified location will be lost if self refresh is entered.  
• 000 = Full Array  
• 001 = Half Array (BA[2:0] = 000, 001, 010 & 011)  
• 010 = Quarter Array (BA[2:0] = 000, 001)  
• 011 = 1/8 Array (BA[2:0] = 000)  
• 100 = 3/4 Array (BA[2:0] = 010, 011, 100, 101, 110 & 111)  
• 101 = Half Array (BA[2:0] = 100, 101, 110 & 111)  
• 110 = Quarter Array (BA[2:0] = 110 & 111)  
• 111 = 1/8 Array (BA[2:0] 111) |
4.55 Mode Register 3 (MR3)

Mode Register 3 controls (among other things) the multi-purpose register, and is described in the figure and table below.

**Figure 4-55. Mode Register 3 (MR3)**

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Reserved</td>
<td>MPR</td>
<td>MPRLOC</td>
<td></td>
</tr>
<tr>
<td>R=0x0</td>
<td>RW=0x0</td>
<td>RW=0x0</td>
<td></td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

**Table 4-57. Mode Register 3 (MR3) Field Descriptions**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-16 | Reserved | Reset = 0x0  
Returns zeros on reads. |
| 15-3  | Reserved | Reset = 0x0  
These are JEDEC reserved bits and are recommended by JEDEC to be programmed to ‘0’. |
| 2     | MPR   | Reset = 0x0  
Multi-Purpose Register Enable: Enables, if set, that read data should come from the Multi-Purpose Register. Otherwise read data come from the DRAM array. |
| 1-0   | MPRLOC| Reset = 0x0  
Multi-Purpose Register (MPR) Location: Selects MPR data location: Valid value are:  
• 00 = Predefined pattern for system calibration  
• All other settings are reserved and should not be used. |
4.56 ODT Configuration Register (ODTCR)

This register configures how ODT should be controlled on the different ranks when writing or reading a particular rank. This provides full flexibility on how the overall termination of the SDRAM system is set depending on how many ranks are used and whether the DIMM slots are occupied or not.

For example, assume the system is a 2-rank configuration and during Read commands the user wishes to always enable the ODT on the SDRAM which is not providing the Read data. In this case, the user would write “0010” to RDODT0 and “0001” to RDODT1.

Figure 4-56. ODT Configuration Register (ODTCR)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-28| WRODT3 | Reset = 0x8, 0x4, 0x2, 0x1 (WRODT3 - 0)  
Write ODT: Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a write command is sent to rank n. WRODT0, WRODT1, WRODT2, and WRODT3 specify ODT settings when a write is to rank 0, rank 1, rank 2, and rank 3, respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 3. Default is to enable ODT only on rank being written to |
| 27-4 | WRODT2 | See description for WRODT3. |
| 23-20| WRODT1 | See description for WRODT3. |
| 19-16| WRODT0 | See description for WRODT3. |
| 15-12| RDODT3 | Reset = All are 0x0  
Read ODT: Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a read command is sent to rank n. RDODT0, RDODT1, RDODT2, and RDODT3 specify ODT settings when a read is to rank 0, rank 1, rank 2, and rank 3, respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 3. Default is to disable ODT during reads. |
| 11-8 | RDODT2 | See description for RDODT3. |
| 7-4  | RDODT1 | See description for RDODT3. |
| 3-0  | RDODT0 | See description for RDODT3. |
4.57 Data Training Configuration Register (DTCR)

The DTCR register is used to set various configurations for data training, and is described in the figure and register below.

**Figure 4-57. Data Training Configuration Register (DTCR)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>RFSHDT</td>
<td>Refresh During Training: A non-zero value specifies that a burst of refreshes equal to the number specified in this field should be sent to the SDRAM after training each rank except the last rank.</td>
</tr>
<tr>
<td>27-24</td>
<td>RANKEN</td>
<td>Rank Enable: Specifies the ranks that are enabled for data-training. Bit 0 controls rank 0, bit 1 controls rank 1, bit 2 controls rank 2, and bit 3 controls rank 3. Setting the bit to 1 enables the rank, and setting it to 0 disable the rank.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>22</td>
<td>DTEXD</td>
<td>Data Training Extended Write DQS: Enables, if set, an extended write DQS whereby two additional pulses of DQS are added as post-amble to a burst of writes. Generally, this should only be enabled when running read bit deskew with the intention of performing read eye deskew prior to running write leveling adjustment.</td>
</tr>
<tr>
<td>21</td>
<td>DTDSTP</td>
<td>Data Training Debug Step: A write of 1 to this bit steps the data training algorithm through a single step. This bit is self-clearing.</td>
</tr>
<tr>
<td>20</td>
<td>DTDEN</td>
<td>Data Training Debug Enable: Enables, if set, the data training debug mode.</td>
</tr>
<tr>
<td>19-16</td>
<td>DTDBS</td>
<td>Data Training Debug Byte Select: Selects the byte during data training debug mod.</td>
</tr>
<tr>
<td>15-14</td>
<td>Reserved</td>
<td>Reset = 0x0</td>
</tr>
<tr>
<td>13</td>
<td>DTBDC</td>
<td>Data Training Bit Deskew Centering: Enables, if set, eye centering capability during write and read bit deskew training.</td>
</tr>
<tr>
<td>12</td>
<td>DTWBDDM</td>
<td>Data Training Write Bit Deskew Data Mask. If set it enables write bit deskew of the data mask.</td>
</tr>
<tr>
<td>11-8</td>
<td>DTWDQM</td>
<td>Training WDQ Margin: Defines how close to 0 or how close to 2*(wdq calibration_value) the WDQ lCdL can be moved during training. Basically defines how much timing margin.</td>
</tr>
<tr>
<td>7</td>
<td>DTCMPD</td>
<td>Data Training Compare Data: Specifies, if set, that DQS gate training should also check if the returning read data is correct. Otherwise data-training only checks if the correct number of DQS edges were returned.</td>
</tr>
<tr>
<td>6</td>
<td>DTMPR</td>
<td>Data Training Using MPR (DDR3 Only): Specifies, if set, that DQS gate training should use the SDRAM Multi-Purpose Register (MPR) register. Otherwise data training is performed by first writing to some locations in the SDRAM and then reading them back.</td>
</tr>
<tr>
<td>5-4</td>
<td>DTRANK</td>
<td>Data Training Rank: Selects the SDRAM rank to be used during data bit deskew and eye centering.</td>
</tr>
<tr>
<td>3-0</td>
<td>DTRPTN</td>
<td>Data Training Repeat Number: Repeat number used to confirm stability of DDR write or read.</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual.
4.58 Impedance Control Register 0 (ZQnCR0)

ZQnCR0-1 (n=0 to 3) registers are used for impedance control and calibration to enable the programmable and PVT compensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnCR0 register.

![Figure 4-58. Impedance Control Register 0 (ZQnCR0)](image)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31   | ZQPD     | Reset = 0x0
ZQ Power Down: Powers down, if set, the impedance control block. |
| 30   | ZCALEN   | Reset = 0x1
Impedance Calibration Enable: Enables if set the impedance calibration of the ZQn control block when impedance calibration is triggered using either the ZCAL bit of PIR register or the DFI update interface. |
| 29   | ZCALBYP  | Reset = 0x0
Impedance Calibration Bypass: Bypasses, if set, impedance calibration of the ZQn control block when impedance calibration is already in progress. Impedance calibration can be disabled prior to trigger by using the ZCALEN bit. |
| 28   | ZDEN     | Reset = 0x0
Impedance Over-ride Enable: When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZDATA field. Otherwise, the control is generated automatically by the impedance control logic |
| 27-0 | ZDATA    | Reset = 0x014A
Impedance Over-Ride Data: Data used to directly drive the impedance control. ZDATA field mapping is as follows:
- ZDATA[27:21] is used to select the pull-up on-die termination impedance
- ZDATA[20:14] is used to select the pull-down on-die termination impedance
- ZDATA[13:7] is used to select the pull-up output impedance
- ZDATA[6:0] is used to select the pull-down output impedance |

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-60. Impedance Control Register 0 (ZQnCR0) Field Descriptions
4.59 Impedance Control Register 1 (ZQnCR1)

ZQnCR0-1 (n=0 to 3) registers are used for impedance control and calibration to enable the programmable and PVTcompensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnCR1 register.

**Figure 4-59. Impedance Control Register 1 (ZQnCR1)**

<table>
<thead>
<tr>
<th>31</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>DFIPU0</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; \( \cdot n \) = value after reset

**Table 4-61. Impedance Control Register 1 (ZQnCR1) Field Descriptions**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-17| Reserved| Reset = 0x0  
Returns zeros on reads. |
| 16   | DFIPU0 | Impedance Calibration Enable: Setting to 1 enables the PHY to request periodic updates to compensate for VT drifts that might result in decreased timing margin. TI recommends this be set to 1. Note that this bit is supported only on K2H Rev2.0, K2K Rev 2.0 and all revisions of K2E and K2L families. It is not supported on K2H Rev 1.x or K2K Rev1.x. |
| 15-8 | Reserved| Reset = 0x0  
Returns zeros on reads. |
| 7-0  | ZPROG  | Impedance Divide Ratio: Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows:  
• ZPROG[7:4] = On-die termination divide select. Available values are:  
  – 2 decimal – 120 ohms  
  – 5 decimal – 60 ohms  
  – 8 decimal – 40 ohms  
• ZPROG[3:0] = Output impedance divide select. Available values are:  
  – 11 decimal – 40 ohms  
  – 13 decimal – 34 ohms |
4.60 Impedance Status Register 0 (ZQnSR0)

ZQnSR0-1 (n=0 to 3) registers are used to provide the status for impedance control and calibration to enable the programmable and PVT-compensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnSR0 register.

**Figure 4-60. Impedance Status Register 0 (ZQnSR0)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | ZDONE  | Reset = 0x0
Impedance Calibration Done: Indicates that impedance calibration has completed. |
| 30  | ZERR   | Reset = 0x0
Impedance Calibration Error: If set, indicates that there was an error during impedance calibration. |
| 29-28| Reserved | Reset = 0x0
Returns zeros on reads. |
| 27-0| ZCTRL  | Reset = 0x000014A
Impedance Control: Current value of impedance control. ZCTRL field mapping is as follows:
- ZCTRL[27:21] is used to select the pull-up on-die termination impedance
- ZCTRL[20:14] is used to select the pull-down on-die termination impedance
- ZCTRL[13:7] is used to select the pull-up output impedance
- ZCTRL[6:0] is used to select the pull-down output impedance |
4.61 Impedance Status Register 1 (ZQnSR1)

ZQnSR0-1 (n=0 to 3) registers are used to provide the status for impedance control and calibration to enable the programmable and PVT-compensated on-die termination (ODT) and output impedance of the functional SSTL cells. The following figure and table describe the bits of the ZQnSR1 register.

**Figure 4-61. Impedance Status Register 1 (ZQnSR1)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-8 | Reserved | Reset = 0x0  
| | | Returns zeros on reads. |
| 7-6 | OPU | Reset = 0x0  
| | | On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD. |
| 5-4 | OPD | Reset = 0x0  
| | | On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD. |
| 3-2 | ZPU | Reset = 0x0  
| | | Output impedance pull-up calibration status. Similar status encodings as ZPD. |
| 1-0 | ZPD | Reset = 0x0  
| | | Output impedance pull-down calibration status. Valid status encodings are:  
| | | • 00 = Completed with no errors  
| | | • 01 = Overflow error  
| | | • 10 = Underflow error  
| | | • 11 = Calibration in progress |

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual

**Table 4-63. Impedance Status Register 1 (ZQnSR1) Field Descriptions**
4.62 DATX8 General Configuration Register (DXnGCR)

This register is used for miscellaneous configurations specific to a particular instantiation of the DATX8 macro (n=0 to 8).

**Figure 4-62. DATX8 General Configuration Register (DXnGCR)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>CALBYP</td>
<td>Reset = 0x0 Calibration Bypass: Prevents, if set, period measurement calibration from automatically triggering after PHY initialization.</td>
</tr>
<tr>
<td>30</td>
<td>MDLEN</td>
<td>Reset = 0x1 Master Delay Line Enable: Enables, if set, the DATX8 master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high. This bit is ANDed with the common DATX8 MDL enable bit.</td>
</tr>
<tr>
<td>29-26</td>
<td>WLRNKEN</td>
<td>Reset = 0xF Write Level Rank Enable: Specifies the ranks that should be write leveled for this byte. Write leveling responses from ranks that are not enabled for write leveling for a particular byte are ignored and write leveling is flagged as done for these ranks. WLRKEN[0] enables rank 0, [1] enables rank 1, [2] enables rank 2, and [3] enables rank 3.</td>
</tr>
<tr>
<td>25-20</td>
<td>Reserved</td>
<td>Reset = 0x0 Reads return zeros.</td>
</tr>
<tr>
<td>19</td>
<td>PLLBYP</td>
<td>Reset = 0x0 PLL Bypass: Puts the byte PLL in bypass mode by driving the PLL bypass pin. This bit is not self-clearing and a '0' must be written to de-assert the bypass. This bit is ORed with the global BYP configuration bit in PLLCR.</td>
</tr>
<tr>
<td>18</td>
<td>GSHIFT</td>
<td>Reset = 0x0 Gear Shift: Enables, if set, rapid locking mode on the byte PLL.</td>
</tr>
<tr>
<td>17</td>
<td>PLLPD</td>
<td>Reset = 0x0 PLL Power Down: Puts the byte PLL in power down mode by driving the PLL power down pin. This bit is not self-clearing and a '0' must be written to de-assert the power-down. This bit is ORed with the global PLLPD configuration bit in PLLCR.</td>
</tr>
<tr>
<td>16</td>
<td>PLLRST</td>
<td>Reset = 0x0 PLL Rest: Resets the byte PLL by driving the PLL reset pin. This bit is not selfclearing and a '0' must be written to de-assert the reset. This bit is ORed with the global PLLRST configuration bit in PLLCR.</td>
</tr>
</tbody>
</table>
| 15-14| DXOEO    | Reset = 0x0 Data Byte Output Enable Override: Specifies whether the output I/O output enable for the byte lane should be set to a fixed value. Valid values are:  
• 00 = No override. Output enable is controlled by DFI transactions  
• 01 = Output enable is asserted (I/O is forced to output mode).  
• 10 = Output enable is de-asserted (I/O is forced to input mode)  
• 11 = Reserved |
| 13   | RTTOAL   | Reset = 0x0 RTT On Additive Latency: Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are:  
• 0 = ODT control is set to DQSO/DQODT almost two cycles before read data preamble  
• 1 = ODT control is set to DQSO/DQODT almost one cycle before read data preamble |

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual.
### Table 4-64. DATX8 General Configuration Register (DXnGCR) Field Descriptions (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 12-11 | RTTOH | Reset = 0x1  
RTT Output Hold: Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0') when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble. |
| 10   | DQRTT | Reset = 0x1  
DQ Dynamic RTT Control: Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0') during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT. |
| 9    | DQSRTT | Reset = 0x1  
DQS Dynamic RTT Control: Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0') during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field. |
| 8-7  | DSEN | Reset = 0x1  
Write DQS Enable: Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tri-stated. Valid settings are:  
• 00 = DQS disabled (Driven to constant 0)  
• 01 = DQS toggling with normal polarity (This should be the default setting)  
• 10 = DQS toggling with inverted polarity  
• 11 = DQS disabled (Driven to constant 1) |
| 6    | DQSRPD | Reset = 0x0  
DQSR Power Down: Powers down, if set, the PDQSR cell. |
| 5    | DXPDR | Reset = 0x0  
Data Power Down Receiver: Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. |
| 4    | DXPDD | Reset = 0x0  
Data Power Down Driver: Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. |
| 3    | DXIOM | Reset = 0x0  
Data I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. |
| 2    | DQODT | Reset = 0x0  
Data On-Die Termination: Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. |
| 1    | DQSODT | Reset = 0x0  
DQS On-Die Termination: Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte |
| 0    | DXEN | Reset = 0x1  
Data Byte Enable: Enables if set the data byte. Setting this bit to '0' disables the byte, i.e. the byte is not used in PHY initialization or training and is ignored during SDRAM read/write operations.  
Note: Software-initiated PHY initialization and leveling is only required after ECC has been enabled in the PHY by writing to DX8GCR.DXEN. Once ECC is enabled in the PHY and the PHY is initialized and leveled, the ECC enable bit in the controller (ECCCTL.ECC_EN) can be enabled or disabled without re-triggering PHY initialization and leveling.  

4.63 DATX8 General Status Register 0 (DXnGSR0)

DXnGSR0-2 are general status registers for the DATX8 (n=0 to 8). They indicate among other things whether write leveling or period measurement calibration is done. Note that WDQCAL, RDQSCAL, RDQSNCAL, GDQSCAL, and WLCAL are calibration measurement-done flags that should be used for debug purposes if the global calibration done flag (PGSR0[CAL]) is not asserted. These flags will typically assert for a minimum of two configuration clock cycles and then de-assert when all measurement done flags are asserted.

Figure 4-63. DATX8 General Status Register 0 (DXnGSR0)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-29</td>
<td>Reserved</td>
<td>Reset = 0x0; Reads return zeros.</td>
</tr>
<tr>
<td>28</td>
<td>WLDQ</td>
<td>Reset = 0x0; Write Leveling DQ Status: Captures the write leveling DQ status from the DRAM during software write leveling</td>
</tr>
<tr>
<td>27-24</td>
<td>QSGERR</td>
<td>Reset = 0x0; DQS Gate Training Error: Indicates if set that there is an error in DQS gate training. One bit for each of the up to 4 ranks</td>
</tr>
<tr>
<td>23-16</td>
<td>GDQSPRD</td>
<td>Reset = 0x0; Read DQS gating Period: Returns the DDR clock period measured by the read DQS gating LCDL during calibration. This value is PVT compensated</td>
</tr>
<tr>
<td>15</td>
<td>DPLOCK</td>
<td>Reset = 0x0; DATX8 PLL Lock: Indicates, if set, that the DATX8 PLL has locked.</td>
</tr>
<tr>
<td>14-7</td>
<td>WLPRD</td>
<td>Reset = 0x0; Write Leveling Period: Returns the DDR clock period measured by the write leveling LCDL during calibration. The measured period is used to generate the control of the write leveling pipeline which is a function of the write-leveling delay and the clock period. This value is PVT compensated</td>
</tr>
<tr>
<td>6</td>
<td>WLERR</td>
<td>Reset = 0x0; Write Leveling Error: Indicates, if set, that there is a write leveling error in the DATX8.</td>
</tr>
<tr>
<td>5</td>
<td>WLDONE</td>
<td>Reset = 0x0; Write Leveling Done: Indicates, if set, that the DATX8 has completed write leveling.</td>
</tr>
<tr>
<td>4</td>
<td>WLCAL</td>
<td>Reset = 0x0; Write Leveling Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the write leveling slave delay line</td>
</tr>
<tr>
<td>3</td>
<td>GDQSCAL</td>
<td>Reset = 0x0; Read DQS gating Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the read DQS gating LCDL.</td>
</tr>
<tr>
<td>2</td>
<td>RDQSNCAL</td>
<td>Reset = 0x0; Read DQS# Calibration (Type B/B1 PHY Only): Indicates, if set, that the DATX8 has finished doing period measurement calibration for the read DQS# LCDL</td>
</tr>
<tr>
<td>1</td>
<td>RDQSCAL</td>
<td>Reset = 0x0; Read DQS Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the read DQS LCDL</td>
</tr>
<tr>
<td>0</td>
<td>WDQCAL</td>
<td>Reset = 0x0; Write DQ Calibration: Indicates, if set, that the DATX8 has finished doing period measurement calibration for the write DQ LCDL</td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual.
4.64 DATX8 General Status Register 2 (DXnGSR2)

DATX8 General Status Register 2 (DXnGSR2) are general status registers for the DATX8 (n=0 to 8). They indicate among other things whether write leveling or period measurement calibration is done. Note that WDQCAL, RDQSCAL, RDQSNCAL, GDQSCAL, and WLCAL are calibration measurement-done flags that should be used for debug purposes if the global calibration done flag (PGSR0[CAL]) is not asserted. These flags will typically assert for a minimum of two configuration clock cycles and then de-assert when all measurement done flags are asserted.

Figure 4-64. DATX8 General Status Register 2 (DXnGSR2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-12</td>
<td>Reserved</td>
<td>Reset = 0x0; Reads return zeros.</td>
</tr>
<tr>
<td>11-8</td>
<td>ESTAT</td>
<td>Reset = 0x0; Error Status: If an error occurred for this lane as indicated by RDERR, WDERR, REERR or WEERR the error status code can provide additional information regard when the error occurred during the algorithm execution.</td>
</tr>
<tr>
<td>7</td>
<td>WEWN</td>
<td>Reset = 0x0; Write Eye Centering Warning: Indicates, if set, that the byte lane n has encountered a warning during execution of the write eye centering training.</td>
</tr>
<tr>
<td>6</td>
<td>WEERR</td>
<td>Reset = 0x0; Write Eye Centering Error: Indicates, if set, that the byte lane n has encountered an error during execution of the write eye centering training.</td>
</tr>
<tr>
<td>5</td>
<td>REWN</td>
<td>Reset = 0x0; Read Eye Centering Warning: Indicates, if set, that the byte lane n has encountered a warning during execution of the read eye centering training.</td>
</tr>
<tr>
<td>4</td>
<td>REERR</td>
<td>Reset = 0x0; Read Eye Centering Error: Indicates, if set, that the byte lane n has encountered an error during execution of the read eye centering training.</td>
</tr>
<tr>
<td>3</td>
<td>WDWN</td>
<td>Reset = 0x0; Write Bit Deskew Warning: Indicates, if set, that the byte lane n has encountered a warning during execution of the write bit deskew training.</td>
</tr>
<tr>
<td>2</td>
<td>WDERR</td>
<td>Reset = 0x0; Write Bit Deskew Error: Indicates, if set, that the byte lane n has encountered an error during execution of the write bit deskew training.</td>
</tr>
<tr>
<td>1</td>
<td>RDWN</td>
<td>Reset = 0x0; Read Bit Deskew Warning: Indicates, if set, that the byte lane n has encountered a warning during execution of the read bit deskew training.</td>
</tr>
<tr>
<td>0</td>
<td>RDERR</td>
<td>Reset = 0x0; Read Bit Deskew Error: Indicates, if set, that the byte lane n has encountered an error during execution of the read bit deskew training.</td>
</tr>
</tbody>
</table>
DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0)

The DATX8 local calibrated delay line registers 0-2 (n=0 to 8) are used to select the delay value on the LCDLs used in the DATX8 macros. A single LCDL field in the LCDLR register connects to a corresponding LCDL. The following tables describe the bits of the DATX8 LCDLR registers. The write data delay (WDQD) and the read DQS delay (RDQSD) are automatically derived from the measured period during calibration. WDQD and RDQSD correspond to a 90 degrees phase shift for DQ during writes and DQS during reads, respectively. The 90 degrees phase shift is used to centre DQS into the write and read data eyes. A 90 degrees phase shift is equivalent to half the DDR clock period. After calibration WDQD and RDQSD fields will contain a value that corresponds to half the DDR clock period (or a quarter of the SDRAM clock period). The write leveling delay (RnWLD) and read DQS gating delay DQSGD are derived from the write leveling and DQS training algorithms. These are normally run automatically by the PHY control block or they can be executed in software by the user. After calibration RnWLD field will contain a value that corresponds to the DDR clock period (or half of the SDRAM clock period), while RnDQSGD field will contain a value that corresponds to half the DDR clock period (or a quarter of the SDRAM clock period).

After the initial setting, all LCDL register fields are automatically updated by the VT compensation logic to track drifts due to voltage and temperature. The user can however override these values by writing to the respective fields of the register and/or optionally disabling the automatic drift compensation.

### Figure 4-65. DATX8 Local Calibrated Delay Line Register 0 (DXnLCDLR0)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>R3WLD</td>
<td>Reset = 0x0&lt;br&gt;Rank 3 Write Leveling Delay: Rank 3 delay select for the write leveling (WL) LCDL</td>
</tr>
<tr>
<td>23-16</td>
<td>R2WLD</td>
<td>Reset = 0x0&lt;br&gt;Rank 2 Write Leveling Delay: Rank 2 delay select for the write leveling (WL) LCDL</td>
</tr>
<tr>
<td>15-8</td>
<td>R1WLD</td>
<td>Reset = 0x0&lt;br&gt;Rank 1 Write Leveling Delay: Rank 1 delay select for the write leveling (WL) LCDL</td>
</tr>
<tr>
<td>7-0</td>
<td>R0WLD</td>
<td>Reset = 0x0&lt;br&gt;Rank 0 Write Leveling Delay: Rank 0 delay select for the write leveling (WL) LCDL</td>
</tr>
</tbody>
</table>
The DXnLCDLR1 register is described in the figure and table below.

**Figure 4-66. DATX8 Local Calibrated Delay Line Register 1 (DXnLCDLR1)**

<table>
<thead>
<tr>
<th>Bit Section</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-24       | Reserved | Reset = 0x0
 |              |          | Reads return zeros                                    |
| 23-16       | RDQSND  | Reset = 0x0
 |              |          | Read DQSN Delay: Delay select for the read DQSN (RDQS) LCDL |
| 15-8        | RDQSD   | Reset = 0x0
 |              |          | Read DQS Delay: Delay select for the read DQS (RDQS) LCDL |
| 7-0         | WDQD    | Reset = 0x0
 |              |          | Write Data Delay: Delay select for the write data (WDQ) LCDL |
4.67 DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2)

The DXnLCDLR2 register is described in the figure and table below.

Figure 4-67. DATX8 Local Calibrated Delay Line Register 2 (DXnLCDLR2)

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-24        | R3DQSGD  | Reset = 0x0
|              |          | Rank 3 Read DQS Gating Delay: Rank 3 delay select for the read DQS gating (DQSG) LCDL. |
| 23-16        | R2DQSGD  | Reset = 0x0
|              |          | Rank 2 Read DQS Gating Delay: Rank 2 delay select for the read DQS gating (DQSG) LCDL. |
| 15-8         | R1DQSGD  | Reset = 0x0
|              |          | Rank 1 Read DQS Gating Delay: Rank 1 delay select for the read DQS gating (DQSG) LCDL. |
| 7-0          | R0DQSGD  | Reset = 0x0
|              |          | Rank 0 Read DQS Gating Delay: Rank 0 delay select for the read DQS gating (DQSG) LCDL. |

Legend: R = Read only; W = Write only; -n = value after reset; -x, value is indeterminate — see the device-specific data manual
4.68 DATX8 Master Delay Line Register (DXnMDLR)

The DATX8 Master Delay Line Registers return different period values measured by the master delay lines in the DATX8 macros. In the default normal operating conditions, the value of the DXnMDLR registers change based on ongoing calibration and measurements.

Figure 4-68. DATX8 Master Delay Line Register (DXnMDLR)

<table>
<thead>
<tr>
<th>31</th>
<th>24</th>
<th>23</th>
<th>16</th>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>MDLD</td>
<td>TPRD</td>
<td>IPRD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R=0x0</td>
<td>RW=0x0</td>
<td>RW=0x0</td>
<td>RW=0x0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: R = Read only; W = Write only; - n = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-70. DATX8 Master Delay Line Register (DXnMDLR) Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31-24 | Reserved | Reset = 0x0  
Reads return zeros |
| 23-16 | MDLD | Reset = 0x0  
MDL Delay: Delay select for the LCDL for the Master Delay Line. |
| 15-8 | TPRD | Reset = 0x0  
Target Period: Target period measured by the master delay line calibration for VT drift compensation. This is the current measured value of the period and is continuously updated if the MDL is enabled to do so. |
| 7-0 | IPRD | Reset = 0x0  
Initial Period: Initial period measured by the master delay line calibration for VT drift compensation. This value is used as the denominator when calculating the ratios of updates during VT compensation. |
**DATX8 General Timing Register (DXnGTR)**

This register is used to control various timing settings of the byte lane, including DQS gating system latency and write leveling system latency.

**Figure 4-69. DATX8 General Timing Register (DXnGTR)**

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-20</td>
<td>Reserved</td>
<td>Reset = 0x0, Reads return zeros</td>
</tr>
<tr>
<td>19-18</td>
<td>R3WLSL</td>
<td>Reset = All 0x1, Rank n Write Leveling System Latency: Adjust write latency</td>
</tr>
<tr>
<td></td>
<td></td>
<td>after write leveling. Power-up default is 01 (i.e. no extra clock cycles</td>
</tr>
<tr>
<td></td>
<td></td>
<td>required). The SL fields are initially set by the PUB during automatic</td>
</tr>
<tr>
<td></td>
<td></td>
<td>write leveling but these values can be overwritten by a direct write to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>this register. Every two bits of this register control the latency of</td>
</tr>
<tr>
<td></td>
<td></td>
<td>each of the (up to) four ranks. R0WLSL controls the latency of rank 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R1WLSL controls rank 1, and so on. Valid values:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 00 = Write latency = WL - 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 01 = Write latency = WL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 10 = Write latency = WL + 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 11 = Reserved</td>
</tr>
<tr>
<td>17-16</td>
<td>R2WLSL</td>
<td>See description for R3WLSL.</td>
</tr>
<tr>
<td>15-14</td>
<td>R1WLSL</td>
<td>See description for R3WLSL.</td>
</tr>
<tr>
<td>13-12</td>
<td>R0WLSL</td>
<td>See description for R3WLSL.</td>
</tr>
<tr>
<td>11-9</td>
<td>R3DGSL</td>
<td>Reset = All 0x0, Rank n DQS Gating System Latency: Increase number of</td>
</tr>
<tr>
<td></td>
<td></td>
<td>clock cycles to expect valid DDR read data by up to seven extra clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cycles. This is used to compensate for board delays and other system</td>
</tr>
<tr>
<td></td>
<td></td>
<td>delays. Power-up default is 000 (i.e. no extra clock cycles required).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The SL fields are initially set by the PHY during automatic DQS data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>training but these values can be overwritten by a direct write to this</td>
</tr>
<tr>
<td></td>
<td></td>
<td>register. Every three bits of this register control the latency of each</td>
</tr>
<tr>
<td></td>
<td></td>
<td>of the (up to) four ranks. R0DGSL controls the latency of rank 0, R1DGSL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>controls rank 1, and so on. Valid values are 0 to 7:</td>
</tr>
<tr>
<td>8-6</td>
<td>R2DGSL</td>
<td>See description for R3DGSL.</td>
</tr>
<tr>
<td>5-3</td>
<td>R1DGSL</td>
<td>See description for R3DGSL.</td>
</tr>
<tr>
<td>2-0</td>
<td>R0DGSL</td>
<td>See description for R3DGSL.</td>
</tr>
</tbody>
</table>
## Revision History

### Changes from January 21, 2015 to March 27, 2015

<table>
<thead>
<tr>
<th>Change</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added RDIMM is not supported to Features</td>
<td>12</td>
</tr>
<tr>
<td>Changed RDIMMINIT bit in PHY Initialization Register to Reserved</td>
<td>85</td>
</tr>
<tr>
<td>Changed PARERR bit in PHY General Status Register to Reserved</td>
<td>94</td>
</tr>
</tbody>
</table>

### (From Revision B to C)

### Revision History

### Changes from A Revision (May 2014) to B Revision

<table>
<thead>
<tr>
<th>Change</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated Self-Refresh Mode section</td>
<td>26</td>
</tr>
<tr>
<td>Changed SDTIM2 offset from 18h to 1Ch.</td>
<td>46</td>
</tr>
<tr>
<td>Updated SDRAM Timing 3 (SDTIM3) Register</td>
<td>57</td>
</tr>
<tr>
<td>Updated SDRAM Timing 4 (SDTIM4) Register</td>
<td>58</td>
</tr>
<tr>
<td>Updated PHY General Configuration Register 0 (PGCR0)</td>
<td>87</td>
</tr>
<tr>
<td>Updated PHY General Configuration Register 1 (PGCR1)</td>
<td>89</td>
</tr>
<tr>
<td>Updated PHY General Configuration Register 2 (PGCR2)</td>
<td>91</td>
</tr>
<tr>
<td>Updated PLL Control Register (PLLCR)</td>
<td>95</td>
</tr>
<tr>
<td>Updated PHY Timing Register 0 (PTR0)</td>
<td>96</td>
</tr>
<tr>
<td>Updated PHY Timing Register 3 (PTR3)</td>
<td>99</td>
</tr>
<tr>
<td>Updated DRAM Configuration Register (DCR)</td>
<td>104</td>
</tr>
<tr>
<td>Updated DRAM Configuration Register (DCR)</td>
<td>104</td>
</tr>
<tr>
<td>Updated DRAM Timing Parameters Register 1 (DTPR1)</td>
<td>106</td>
</tr>
<tr>
<td>Updated DRAM Timing Parameters Register 2 (DTPR2)</td>
<td>107</td>
</tr>
<tr>
<td>Updated Mode Register 0 (MR0)</td>
<td>108</td>
</tr>
<tr>
<td>Updated Mode Register 1 (MR1)</td>
<td>110</td>
</tr>
<tr>
<td>Added DFIPU0 bit to Impedance Control Register 1 (ZQnCR1)</td>
<td>117</td>
</tr>
<tr>
<td>Updated Impedance Control Register 1 (ZQnCR1)</td>
<td>117</td>
</tr>
<tr>
<td>Updated DATX8 General Configuration Register (DXnGCR)</td>
<td>121</td>
</tr>
<tr>
<td>Added DXxGSR2 registers to PHY Register table</td>
<td>123</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio</td>
<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
</tr>
<tr>
<td>Amplifiers</td>
<td><a href="http://www.amplifier.ti.com">www.amplifier.ti.com</a></td>
</tr>
<tr>
<td>Data Converters</td>
<td><a href="http://www.dataconverter.ti.com">www.dataconverter.ti.com</a></td>
</tr>
<tr>
<td>DLP® Products</td>
<td><a href="http://www.dlp.com">www.dlp.com</a></td>
</tr>
<tr>
<td>DSP</td>
<td>dsp.ti.com</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td><a href="http://www.ti.com/clocks">www.ti.com/clocks</a></td>
</tr>
<tr>
<td>Interface</td>
<td>interface.ti.com</td>
</tr>
<tr>
<td>Logic</td>
<td><a href="http://www.logic.ti.com">www.logic.ti.com</a></td>
</tr>
<tr>
<td>Power Mgmt</td>
<td><a href="http://www.power.ti.com">www.power.ti.com</a></td>
</tr>
<tr>
<td>Microcontrollers</td>
<td><a href="http://www.microcontroller.ti.com">www.microcontroller.ti.com</a></td>
</tr>
<tr>
<td>RFID</td>
<td><a href="http://www.ti-rfid.com">www.ti-rfid.com</a></td>
</tr>
<tr>
<td>OMAP Applications Processors</td>
<td><a href="http://www.ti.com/omap">www.ti.com/omap</a></td>
</tr>
<tr>
<td>Wireless Connectivity</td>
<td><a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a></td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2015, Texas Instruments Incorporated