1.1 Stackup

The PCB Layout designer needs to balance many different requirements when starting a PCB layout. The first is the board stackup. The 66AK2Gxx device has a 21 mm × 21 mm package which has a 0.80mm pitch ball array of 25 × 25. To minimize cost, this ball grid is nearly a solid array. Due to the number of rows of signal balls around the periphery, designs will need to have 2 routing layers not counting the top and bottom layers which can also contain some signal routes. Also, due to the number of power supply rails, there will need to be 2 layers dedicated for power planes. Ground planes will need to be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. Therefore, designs that route out all of the signal balls will need a 10-layer stackup similar to the following:

A 10-layer stack-up like the one discussed above will be needed for relatively dense PCBs. Alternately, the layer count can be reduced assuming one or more of the following exist:

- The PCB is not crowded around the 66AK2Gxx device. This allows for more routing away from the device on the top and bottom layers which can reduce layer congestion.
- Many of the signal balls are unused. Many designs will not use all of the interfaces resulting in unused signal balls. This also reduces routing congestion.
- The PCB layout team has time to carefully place the routes. Note that this can be very time consuming.

It is not acceptable to violate routing rules simply to save money on reduced PCB layers or due to limited routing time. All requirements must still be met. Also, creative routing will increase design validation time - both in simulation and bench testing. This can be minimized if the layout is similar to one of the 66AK2Gxx EVM design.

The 66AK2Gxx EVM is implemented in a 10-layer stack-up similar to the one described above. This design has nearly every signal ball routed to circuitry or a connector. This drives the requirement for the full number of layers. Additionally, this board is designed for optimum signal integrity on the high speed interfaces while limiting the board size. The 66AK2G02 EVM is implemented without an HDI (High Density Interconnect) board using micro vias on both the top 2 and bottom 2 layers. All vias on the 66AK2Gxx EVM pass completely through the board. This complicates the escape from the BGA.
1.2 Floorplan Component Placement

Optimum trace routing will have routes as short as possible with a minimum of cross-over. This requires careful placement of the components around the 66AK2Gxx device. The figure below shows the default arrangement of the signal balls as well as the power and ground balls. (It is understood that some of the interfaces can move to other locations due to pin multiplex choices and that there are other interfaces not listed that are exposed through pin multiplex choices.) The PCB layout team will need to analyze the locations of the interfaces used and the associated components and connectors.

Figure 1-1. Interface Positions
1.3 Critical Interfaces Impact Placement

Placement of the 66AK2Gxx device and some of the component and connectors will also be dictated by some of the highest performance interfaces. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

1.4 Route Critical Interfaces First

As indicated above, critical interfaces will affect component placement options. Then when routing begins, these critical interfaces must be routed first. The design team needs to establish a priority for the different interfaces. Those with higher priority must be completed before implementing those of lower priority. PCB layout teams often waste considerable effort ripping up and re-routing traces for lower priority interfaces when deficiencies are found in the routing of more critical interfaces. Always complete routing for the critical interfaces first.

The table below lists a recommended priority order for interfaces contained on the 66AK2Gxx family of devices. Individual design requirements may cause this list to change somewhat but this provides a good baseline.

<table>
<thead>
<tr>
<th>Interface</th>
<th>Routing Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe</td>
<td>10 (Highest Priority)</td>
</tr>
<tr>
<td>DDR3</td>
<td>9</td>
</tr>
<tr>
<td>USB2</td>
<td>8</td>
</tr>
<tr>
<td>Power distribution</td>
<td>7</td>
</tr>
<tr>
<td>RGMII</td>
<td>6</td>
</tr>
<tr>
<td>QSPI</td>
<td>6</td>
</tr>
<tr>
<td>Parallel Video</td>
<td>5</td>
</tr>
<tr>
<td>eMMC</td>
<td>5</td>
</tr>
<tr>
<td>Clocks</td>
<td>5</td>
</tr>
<tr>
<td>MII / RMII</td>
<td>4</td>
</tr>
<tr>
<td>SPI</td>
<td>4</td>
</tr>
<tr>
<td>Motor control</td>
<td>4</td>
</tr>
<tr>
<td>Analog audio</td>
<td>3</td>
</tr>
<tr>
<td>GPMC</td>
<td>2</td>
</tr>
<tr>
<td>GPIO</td>
<td>1</td>
</tr>
<tr>
<td>UART</td>
<td>1</td>
</tr>
<tr>
<td>I2C</td>
<td>1 (Lowest Priority)</td>
</tr>
</tbody>
</table>

The placement of most of these should appear obvious. The multi-gigabit SERDES interfaces are the most critical due to their data rate and loss concerns. PCIe is at the top since it is very sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the PCIe connector and the 66AK2Gxx device. PCIe signals are found on the outside layer of the BGA footprint allowing the traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution. It is often left to last. This then results in poor decoupling performance and current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling needs to be allocated before routing the middle and low priority interfaces.**
1.5 Route SERDES Interfaces First

The previous section highlighted priorities for the PCB routing. The BGA ball map is also arranged to support routing the highest priority interfaces first. You will notice that most of the PCIe SERDES interface is located on the outer row to allow these to route away from the device without requiring vias. See below for the routing of the PCIe Lane 0 signals on the 66AK2Gxx EVM on the top layer.

![SERDES Signal Escape Routing](image)

**Figure 1-2. SERDES Signal Escape Routing**

1.6 Route DDR3 Signals Next

The DDR3 signals need to be routed next. See the 66AK2Gxx data sheets for detailed recommendations for DDR3 routing. The images below show the BGA breakout for the DDR3 on the 66AK2Gxx GP EVM.

The DDR3 SDRAM memory devices should be arranged so that the data group balls are closest to the 66AK2Gxx device. This will allow the data group nets to have the shortest possible routing. The Address, Command and Control signals operate at half the bandwidth of the data so they are expected to be longer.

1.6.1 Data Group Routes

The DDR3 signals need to be routed next. See the 66AK2Gxx data sheets for detailed recommendations for DDR3 routing. The images below show the BGA breakout for the DDR3 on the 66AK2Gxx GP EVM.

The DDR3 SDRAM memory devices should be arranged so that the data group balls are closest to the 66AK2Gxx device. This will allow the data group nets to have the shortest possible routing. The Address, Command and Control signals operate at half the bandwidth of the data so they are expected to be longer.
Figure 1-3. DDR3 Data Group Routing

Point-to-point data bus routing
The following image shows escape of the signals on the top layer of the board. Note that most of the routing is not on the top layer. Signals will travel through traces routed on the top and bottom layer will travel at different speed then traces routed on internal layers. This difference must be included in the length matching calculations. Ideally, all DDR3 signals should be routed on internal layers.

The following image shows escape of the signals on the top layer of the board. Note that most of the routing is not on the top layer. Signals will travel through traces routed on the top and bottom layer will travel at different speed then traces routed on internal layers. This difference must be included in the length matching calculations. Ideally, all DDR3 signals should be routed on internal layers.

Data byte routing
Top layer

Figure 1-4. DDR3 Data Group Top Layer Escape

The following image shows the routing under the BGA on layer 3. Ideally the odd lanes should be routed on the same layer. The area between the vias for the even lanes can be used to escape signals that are in rows closer to the center. The EVM used layer 3 to escape most of byte lane 1 and all of byte lane 3. Some of the signals from byte lane 2 are also present on this layer.

Data byte routing
Layer 3
Most of Byte lanes 1 & 3
Byte lane 0 – Red
Byte lane 1 – Blue
Byte lane 2 - Yellow
Byte lane 3 – Green
Check Byte - Violet

Figure 1-5. DDR3 Data Group Layer 3 Escape
The following image shows the routing under the BGA on layer 8. Ideally the even lanes should be routed on the same layer. The area between the vias for the odd lanes can be used to escape signals that are in rows closer to the center. The EVM used layer 8 to escape most of byte lane 2 and all of byte lane 0 as well as the check byte signals. Some of the signals from byte lane 1 are also present on this layer.

Data byte routing
Layer 8
Most of Byte lanes 0, 2 & CB
Byte lane 0 – Red
Byte lane 1 – Blue
Byte lane 2 - Yellow
Byte lane 3 – Green
Check Byte - Violet

Figure 1-6. DDR3 Data Group Layer 8 Escape

1.6.2 Address, Command, Control and Clock Group Routes

The address, command and clock signals are routed in flyby starting with the check byte memory and moving up to byte lane 0. The VTT termination resistors are placed at the end of the trace past the byte 0 memory device.
Figure 1-7. DDR3 Address/Command Group Flyby Routing
The layers 3, 8 and 10 are used to escape and route the address and command signals. The signals must be length matched to ensure that the signals arrive at each memory at the same time. Length matching must be from the SoC to each memory individually including the stub to the memory pad. Simply matching the length of each trace from beginning to end is not sufficient. The speed difference between the signals routed on the bottom layer and the internal layers must also be taken into account.

The escapes of the address and command signals for these three layers are shown below.
Figure 1-8. DDR3 Address/Command Group Escape
1.6.3 **Complete Power Decoupling Next**

The middle priority interfaces and the power distribution planes and pours would be routed next after the SERDES and DDR3 interfaces. It is strongly encouraged to complete all SERDES and DDR3 routing before continuing with other interfaces. Note that the power distribution planes and pours and all of the decoupling will need to be placed before PCB simulations are executed for the SERDES and DDR3 routes. The highest speed source-synchronous interfaces like RGMII and QSPI may also require simulation so these may need to be completed at this time as well.

1.6.4 **Route Lowest Priority Interfaces Last**

Once the length matching and simulations have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and then the lower priority interfaces.
## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>Changes from Original (April 2017) to A Revision</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed 66AK2G02 to 66AK2Gxx.</td>
<td>2</td>
</tr>
</tbody>
</table>

---

**Submit Documentation Feedback**

Copyright © 2017, Texas Instruments Incorporated
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT. AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated