TI Designs

Thunderbolt™ Single Port Design Outline
## Contents

1. **Introduction**  
   3

2. **High Level Design Information**  
   4
   2.1 Design Block Diagram  
   4
   2.2 TPS65980 Thunderbolt Bus Power Management Unit  
   5

3. **Design Details & Schematic**  
   6
   3.1 Schematic Net Description  
   6
   3.2 Schematic: TPS65980 Block  
   7
   3.3 Schematic: TPS22920L for Thunderbolt_Active_Rail  
   9
   3.4 Schematic: TPS22920L for Thunderbolt_High_Speed_Core_Rail  
   9
   3.5 Schematic: Bus Power or Self Power Configuration  
   10
   3.6 Schematic: Thunderbolt Connector & Control Signals  
   11

## List of Figures

1. Design Block Diagram  
   4
2. TPS65980 Power Diagram  
   5
3. TPS65980 Control Signal Diagram  
   5
4. TPS65980 Schematic  
   7
5. TPS65980 Layout Example  
   8
6. TPS22920L Schematic for Thunderbolt_Active_Rail  
   9
7. TPS22920L Schematic for Thunderbolt_High_Speed_Core_Rail  
   9
8. Bus or Self Power Input  
   10
9. External Supply Present Schematic  
   10
10. PCIe_12V Control from External Power  
    10
11. Thunderbolt Connector  
    11
12. PCIe Connector and PCIe Reset Schematic  
    11
1 Introduction

This design guide will help a developer get started with a Thunderbolt™ single port design. For more information on Thunderbolt please refer to www.ti.com/thunderbolt

Single port Thunderbolt devices can come in two different forms. Self powered devices have an external supply to provide power to the device or bus powered device which use the available 10W provided. This design can be configured for both self or bus powered applications. Thunderbolt certification and testing has been completed for this design.

For licensed Thunderbolt developers, please contact thunderbolt_support@list.ti.com. For information on obtaining a Thunderbolt license please refer to https://thunderbolttechnology.net/contact/thunderbolt-developer.

Thunderbolt and the Thunderbolt logo are trademarks of Intel Corporation in the U.S. and/or other countries.
2 High Level Design Information

2.1 Design Block Diagram

A Thunderbolt single port design consists of two main blocks, Thunderbolt data and power blocks. The Thunderbolt data block consists of a Thunderbolt controller and support system with various control signals. The Thunderbolt power block consists of all the needed supplies for a Thunderbolt system. There are three main power supplies in present in the system; main Thunderbolt power which powers the Thunderbolt controller and support system, Thunderbolt cable power which is needed to power the active Thunderbolt cable, and PCIe supply for PCIe bridge devices. Please check the block diagram below.

![Design Block Diagram](image-url)

Figure 1. Design Block Diagram
2.2 TPS65980 Thunderbolt Bus Power Management Unit

The TPS65980 is the first fully integrated Thunderbolt Bus PMU which provides the needed power supplies (Thunderbolt main supply, Thunderbolt Cable supply, and PCIe supply) while meeting all of the power sequencing requirements of Thunderbolt. The TPS65980 also provides the needed control signals that interface between the Thunderbolt power and data blocks. The TPS65980 integrates many discrete subsystems which saves significantly on BOM cost, solution size, and reduces the design complexity. Find more information at http://www.ti.com/product/tps65980.
# 3 Design Details & Schematic

## 3.1 Schematic Net Description

<table>
<thead>
<tr>
<th>Net</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Rails</strong></td>
<td></td>
</tr>
<tr>
<td>Main_Thunderbolt_Rail</td>
<td>Main 3.3V power rail that powers the Thunderbolt Controller and must remain constant during all operations of the systems</td>
</tr>
<tr>
<td>Cable_Power</td>
<td>3.3V current limited power rail that is sent back down the Thunderbolt cable to provide power to the active cable circuitry</td>
</tr>
<tr>
<td>PCIe_Aux_Supply</td>
<td>3.3V rail controlled by Thunderbolt controller to power PCIe bridge functions</td>
</tr>
<tr>
<td>Thunderbolt_Power_In</td>
<td>Thunderbolt bus power input from Thunderbolt connector</td>
</tr>
<tr>
<td>External_12V</td>
<td>External supply for self powered systems</td>
</tr>
<tr>
<td>TBT_IN</td>
<td>External_12V &amp; Thunderbolt_Power_In diode-or for TPS65980 power input</td>
</tr>
<tr>
<td>Thunderbolt_High_Speed_Rail</td>
<td>Thunderbolt controller generated low voltage</td>
</tr>
<tr>
<td>Thunderbolt_High_Speed_Core_Rail</td>
<td>Thunderbolt controller input core voltage (TPS22920L)</td>
</tr>
<tr>
<td>Thunderbolt_Active_Rail</td>
<td>3.3V power rail for Thunderbolt active link (TPS22920L)</td>
</tr>
<tr>
<td>PCIe_12V</td>
<td>12V PCIe connector supply for self powered systems</td>
</tr>
<tr>
<td><strong>Signal Nets</strong></td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Wake_EN</td>
<td>Thunderbolt controller generated signal to power up Thunderbolt_Active_Rail, and signal Thunderbolt link</td>
</tr>
<tr>
<td>External_Supply_Present</td>
<td>TPS3700 generated signal to indicated that external 12V supply is present in the system</td>
</tr>
<tr>
<td>PCIe_Aux_Supply_EN</td>
<td>Thunderbolt controller generated signal to control PCIe_Aux_Supply from TPS65980 (DEV_OUT)</td>
</tr>
<tr>
<td>RESET_N</td>
<td>TPS65980 generated signal to indicate to the Thunderbolt controller that Main_Thunderbolt_Rail is active</td>
</tr>
<tr>
<td>PCIe_Connector_Reset</td>
<td>Buffered PCIe reset signal from Thunderbolt controller</td>
</tr>
<tr>
<td>Thunderbolt_Controller_PCIE_Reset</td>
<td>Thunderbolt controller generated signal for PCIe reset</td>
</tr>
<tr>
<td>Thunderbolt_Data_R_0_P</td>
<td>Thunderbolt high speed data lines</td>
</tr>
<tr>
<td>Thunderbolt_Data_R_0_N</td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Data_R_1_P</td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Data_R_1_N</td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Data_D_1_P</td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Data_D_1_N</td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Data_D_0_P</td>
<td></td>
</tr>
<tr>
<td>Thunderbolt_Data_D_0_N</td>
<td></td>
</tr>
<tr>
<td>LSTX</td>
<td>Low speed RX and TX data lines</td>
</tr>
<tr>
<td>LSRX</td>
<td></td>
</tr>
<tr>
<td>Buffer_LSRX</td>
<td></td>
</tr>
<tr>
<td>Config_1</td>
<td>Thunderbolt configuration pins</td>
</tr>
<tr>
<td>Config_2</td>
<td></td>
</tr>
</tbody>
</table>
3.2 Schematic: TPS65980 Block

Check the figure below for the TPS65980 schematic. The schematic for TPS65980 uses 20uF (C44, C56, C49) for TBT_IN and may be increased to 52uF, the maximum allowed bus power capacitance. The TBT_OUT capacitance for the TPS65980 is limited to 68uF. C43, 64, C50 are the output capacitance for the TPS65980 and C65, C66, C67, C68 are the input capacitance to the Thunderbolt controller which is supplied through TBT_OUT. Careful consideration of inductor current rating and capacitor de-rating is recommended, as it is in every system. For a quick start the TPS65980EVM schematic can be used as a reference.

![Figure 4. TPS65980 Schematic](image)
When doing layout for the TPS65980 it is best to follow the Figure 5. below. Most of the components are placed on the top side of the board with the exception of the DEV_OUT cap which is placed on the bottom side. DEV_OUT is best routed to the bottom layer of the board to allow for closer placement of the inductor. When sufficient top side ground and vias from the PowerPad to ground plane are used the best thermal performance is achieved. Placing the TBT_IN capacitors close to the device and allowing the PGND and GND from TBT_IN capacitors to share the top plane will limit the amount of noise generated by the TPS65980 power stage. The TBT_OUT capacitor(s) should be placed close to the TPS65980 and right after the inductor.

Figure 5. TPS65980 Layout Example
3.3 Schematic: TPS22920L for Thunderbolt_Active_Rail

![Schematic: TPS22920L for Thunderbolt_Active_Rail](image)

Rail Powered during Thunderbolt data transmission

Figure 6. TPS22920L Schematic for Thunderbolt_Active_Rail

3.4 Schematic: TPS22920L for Thunderbolt_High_Speed_Core_Rail

![Schematic: TPS22920L for Thunderbolt_High_Speed_Core_Rail](image)

Low Voltage for Thunderbolt Controller

Figure 7. TPS22920L Schematic for Thunderbolt_High_Speed_Core_Rail
3.5 Schematic: Bus Power or Self Power Configuration

The design covered can be configured as a bus or self powered system. For bus powered systems, the self powered components maybe removed from the design and the vice-a-versa for a self powered system. When used in a bus power configuration, J2 power jack, DB2 & DB3 “diode or”, U13 TPS3700, and Q2 & Q3 with passives should be removed. Self powered applications should include all of the components in the design.

![Diagram of bus or self power input](image8)

**Figure 8. Bus or Self Power Input**

![Diagram of external supply present](image9)

**Figure 9. External Supply Present Schematic**

![Diagram of PCIe_12V control from external power](image10)

**Figure 10. PCIe_12V Control from External Power**
3.6 Schematic: Thunderbolt Connector & Control Signals

Figure 11. Thunderbolt Connector

Figure 12. PCIe Connector and PCIe Reset Schematic
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated (“TI”) reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design. TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED “AS IS”. TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN, IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer’s risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated