TI Designs Ultra-Small, Flexible LED Expansion Reference Design

U TEXAS INSTRUMENTS

Description

This document focuses on two reference designs using the SN74HC595B 8-bit shift register with three state output registers and the SN74LVC244A octal buffer with three-state outputs in the ultra-small X1QFN package to expand a limited number of general purpose outputs to a larger number of general purpose outputs. The *Seven Segment Driver Reference Design* (Section 2.1) focuses on individually controlling the eight LEDs in a seven-segment display with hardware that fits underneath the seven segment. The *8x8 LED Matrix Reference Design* (Section 2.2) focuses on driving 64 LEDs arranged as an 8x8 matrix display, which can be panelized to create larger displays.

Resources

TIDA-01233 SN74HC595B SN74LVC244A Design Folder Product Folder Product Folder



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Features

- Wide-Voltage Supply Range of 2 V to 3.6 V
- Expands Three General Purpose Output Pins to 64+ Outputs
- Adaptable to Wide Range of Output Expansion
 Applications
- Simple Cost-Effective Solution
- Allows Custom Character Displays on Seven Segments
- Indefinitely expandable to additional Seven Segments
- Drive 8×8 Light-Emitting Diode (LED) Matrix With Only Three General Purpose Output Pins
- Compatible With 2.5-V and 3.3-V Standard Logic Outputs

Applications

- White Goods
- Microwave Ovens
- Home Automation
- Controllable Electronic Displays
- Industrial Readouts









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1 System Overview

1.1 System Description

The Ultra-Small Flexible Output Expansion Reference Design demonstrates the compactness of the X1QFN package in a common application. By easily fitting the control circuitry behind the elements that they drive, board space requirements are significantly reduced from a traditional solution. The shift registers used can be controlled from any voltage-compatible controller, enabling use of this design across a broad variety of end equipments.

The test board shown on the first page has four instances of the *Seven-Segment Driver Reference Design* (Section 2.1) serially linked. Any number of digits can be serially connected and function almost identically. That board also contains one instance of the *8x8 LED Matrix Reference Design* (Section 2.2). A larger or smaller matrix is easy to build using the same design techniques.

1.2 Key System Specifications

PARAMETER	SPECIFICATIONS
Recommended V _{cc}	3.3 V
Absolute maximum V _{CC}	2 V to 3.6 V
Recommended input and output voltage	0 V to 5.5 V
Absolute maximum input and output voltage	–0.5 V to 6.5 V
Typical LED current consumption of an LED in the LED matrix	2 mA
Typical current consumption of one of the segments in the seven segment	8 mA

Table 1. Key System Specifications



1.3 Block Diagram



Figure 1. Block Diagram for Seven-Segment Driver Reference Design



Figure 2. Block Diagram for 8x8 LED Matrix Reference Design

1.4 Highlighted Products

1.4.1 SN74HC595B

The SN74HC595B devices (see Figure 3) contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel three-state outputs. Separate clocks are provided for both the shift register and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (\overline{OE}) input is high, then all outputs are in the high-impedance state except Q_H.



Figure 3. Logic Diagram for SN74HC595B

1.4.1.1 SN74HC595B Features

- 8-bit serial-in, parallel-out shift registers
- Available in ultra-small logic QFN package (0.5-mm maximum height)
- Overvoltage tolerant on inputs independent of V_{cc}
- Wide-operating voltage range of 2 V to 6 V
- High-current three-state outputs can drive up to 15 LSTTL loads
- Low power consumption: 80-µA (maximum) ICC
- $t_{pd} = 13 \text{ ns}$ (typical)

- ±6-mA output drive at 5 V
- Low input current: 1 μA (maximum)
- -55°C to 125°C operating temperature

1.4.2 SN74LVC244A

The SN74LVC244A is an octal bus buffer designed for 1.65-V to 3.6-V V_{cc} operation (see Figure 4). The SN74LVC244A devices are designed for asynchronous communication between data buses.

System Overview



Figure 4. Logic Diagram for SN74LVC244A

1.4.2.1 SN74LVC244A Features

- Operates from 1.65 V to 3.6 V
- Inputs accept voltages to 5.5 V
- Maximum t_{pd} of 5.9 ns at 3.3 V
- Supports mixed-mode signal operation on all ports (5-V input or output voltage with 3.3-V VCC)
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Available in ultra-small logic QFN package (0.5-mm maximum height)
- t_{pd} = 13 ns (typical)
- Latch-up performance exceeds 250 mA per JESD 17



2 System Design Theory

Both reference designs shown here are for the use of output expansion, specifically to drive large numbers of LEDs from a small number of general purpose input/ouput (GPIO) pins. Each design takes a different approach, so they have been separated into two sections.

2.1 Seven-Segment Driver Reference Design

2.1.1 Concept

Each seven-segment display requires eight LEDs to be controlled (seven LEDs for the digit plus one for the decimal point). Directly controlling so many LEDs from an MCU quickly becomes impractical because of a lack of available digital output pins. By utilizing a serial shift register, the number of output pins drops from 32 for four displays down to only 3. The SN74HC595B device is ideal for this application because it includes both a standard shift register and a D-type register for the outputs, which allows the shift register to load new data while the device outputs continue to display the last loaded data in the output registers.

NOTE: An important feature to note is that the same three output pins can be used almost indefinitely to expand the outputs by just continually adding serial-in, parallel-out shift registers to the end of the chain. The primary limitation is the amount of time required to load all of the serial devices. For a display application, it is preferable to keep the refresh rate faster than 30 frames per second, which equates to a loading time of about 33.3 ms. At a relatively slow clock speed of 10 kHz, over 40 serial devices (that is, 320+ outputs) can be updated in that time.

The SN74LVC244A device contains eight digital buffers which are used to increase the drive current of the eight channels coming out of the SN74HC595B device. Channels can be paralleled for increased current in higher current applications. For low current applications, the SN74LVC244A is often not required.

Two pins (SER and SRCLK) are required to load the data serially into the shift register, then one pin (RCLK) is used to save that data to the output registers. These three pins allow for complete control of the seven-segment display. Any individual LED can be turned ON or OFF as is required by the controller.

2.1.2 Schematic

The V_{CC} rail goes to 3.3 V. The four lines labeled \overline{OE} , SER, SRCLK, and RCLK are the only lines used to control the seven-segment driver (see Figure 5).



Figure 5. Seven-Segment Driver Reference Design Schematic

2.1.3 Component Selection

The SN74HC595B is the chosen shift register and was selected for its extremely small size. The SN74HC595B is available in the X1QFN (extra-small quad-flatpack without leads), which allows it to be used in extremely space-constrained designs. In this case, the SN74HC595B device is placed between the leads of the chosen seven-segment display on the back of the board. Essentially, the size requirement for the seven-segment display board only requires that it be large enough to include the seven-segment display elements and a connector for the control and power lines (five total wires). Additionally, the SN74HC595B device can be linked serially, creating a long chain of seven-segment display digits without the requirement for additional control lines.

The SN74HC595B can only source 70 mA total for all eight output channels; however, this design requires 80 mA, so a second driver chip is required. The SN74LVC244A device contains eight digital buffers capable of driving up to a total of 100 mA (12.5 mA per channel). This reference design uses one of these devices per seven-segment display to drive the LEDs. Each LED in the display is specified to operate at 10 mA and is driven from a single channel of the SN74LVC244A device. Note that it is possible to parallel channels of the SN74LVC244A device to increase drive current if required.

The seven-segment module was selected for color, size, cost, and through-hole design. The module was specifically chosen to be through-hole to show how small the X1QFN packages really are; because the pins go all the way through the board, the pins frame the control circuitry on the back. As Figure 7 shows, all control circuitry required to drive the seven-segment display fits between the pins on the back of the board, which includes all passive and active components.



Each segment LED has a series resistor to limit the current going through it. The resistor value (R_s) was calculated from the required current for the LED (i_f), the forward voltage for the LED (V_f), and the output voltage of the SN74LVC244A (V_{OH}). The following Equation 1 used is:

$$\mathsf{R}_{\mathsf{s}} = \frac{\mathsf{V}_{\mathsf{OH}} - \mathsf{V}_{\mathsf{f}}}{\mathsf{i}_{\mathsf{f}}} \tag{1}$$

The required LED current is 10 mA, the forward voltage of the LED is 2.1 V, and V_{OH} can be assumed very close to V_{CC} because of the supplied current being significantly below the data sheet specified value for V_{OH} at 24 mA. Inputting those values results in Equation 2:

$$\frac{3.3 \text{ V} - 2.1 \text{ V}}{10 \text{ mA}} = 120 \Omega$$

(2)

2.1.4 Timing and Control Requirements

Each string of an SN74HC595B device requires three control lines: serial data (SER), serial clock (SRCLK), and register clock (RCLK). This reference design includes a fourth line to allow for dimming the display ,which is tied to the output enable pin of the SN74LVC244A device. By applying a PWM signal to the OE input, the display brightness can be precisely controlled.

To load data into the shift register, first SRCLK and RCLK must be in the LOW state. SER is set to the first desired bit value, then SRCLK is pulsed to clock that value into the shift register. This process is repeated for all 8 bits of the shift register. As soon as the data has been loaded into the shift register, RCLK is pulsed to push the data from the internal register to the outputs of the device. The output registers continue to hold the values shifted into them until either another RCLK is received or the device has been powered off.

Figure 6 shows the timing diagram for the SN74HC595B.



NOTE: XXXXXXXX implies that the output is in 3-State mode.

Figure 6. Timing Diagram for the SN74HC595B



2.1.5 Layout

The channels used on the SN74LVC244A have been selected such that they were aligned with the pins of the seven-segment. Resistors and capacitors are in the 0402 package and the SN74HC595B and SN74LVC244A are in the X1QFN package. In this example, the $Q_{H'}$ signal from this device continues on to the neighboring seven-segment. An MCU on a separate board is connected through a header (not shown) to the \overline{OE} line of the SN74LVC244A device and the SER, SRCLK, and RCLK lines of the SN74HC595B device.

System Design Theory

Because of the low current requirements of this circuit, the traces can be extremely small. The size is limited by the manufacturer and not the actual current requirement of the trace. In this case, the manufacturer required 5-mil minimum traces and the traces shown are 5mil wide (see Figure 7).



Figure 7. Seven-Segment Driver Reference Design Hardware Layout Example From BOOSTXL-SHIFTLED BoosterPack™ Plug-in Module (Left: Board Back, Right: Board Front)



2.2 8×8 LED Matrix Reference Design

2.2.1 Concept

64 digital outputs are the number of outputs required to individually control all the LEDs in an 8×8 matrix display. Directly controlling so many LEDs from an MCU quickly becomes impractical because of a lack of available digital output pins. By utilizing a serial shift register, the number of output pins drops from 64 to only 3. The SN74HC595B is ideal for this application because it includes both a standard shift register and a D-type register for the outputs, which allows the shift register to have new data loaded while the device outputs continue to display the last loaded data in the output registers.

Individually controlling all of the LEDs in an 8×8 matrix is possible using shift registers, which would require eight 8-bit shift registers and still only require three control lines. By only turning on one column at a time and scanning across the columns at a high speed, controlling all 64 LEDs is possible with only two shift registers, which is the method chosen for this reference design. One shift register is used to control the active LEDs of the selected column, while a second shift register is used to select which column is active. These two devices are in series to reduce the number of pins required at the MCU.

The selected LEDs use 2 mA each. Because each column can require up to 16 mA total current to operate, a higher current device than the SN74HC595B is required for the column selector.

The SN74LVC244A contains eight digital buffers which are used to increase the sink current of the eight channels coming out of the SN74HC595B device. Channels can be paralleled for increased current in higher current applications.

Two pins (SER and SRCLK) are required to load the data serially into the shift register, then one pin (RCLK) is used to save that data to the output registers. These three pins allow for complete control of the 8×8 matrix display. The scan rate of the columns change the apparent brightness of the LEDs; at slower scan rates, the LEDs appear brighter and at faster scan rates, they appear dimmer. TI recommends to avoid scanning slower than 30 frames per second ($4.1\overline{6}$ ms per column), as this starts to generate obvious flicker to the human eye.

2.2.2 Schematic

The V_{cc} rail goes to 3.3 V. All resistor values are 750 Ω and all diodes are from the Rohm company part number SML-311UTT86. Red components and wires indicate row control and blue components and wires indicate column control. The three lines labeled SER, SRCLK, and RCLK are the only lines used to control the 8x8 matrix (see Figure 8).

System Design Theory



Figure 8. 8×8 LED Matrix Reference Design Schematic

2.2.3 Component Selection

Small, low current LEDs have been chosen for this display. The individual LEDs have been selected for color, size, cost, and current requirement. Each LED requires 2 mA of forward current to operate. Each LED has a series resistor to limit the current going through it. The resistor value (R_s) was calculated from the required current for the LED (i_f), the forward voltage for the LED (V_f), the output voltage of the SN74HC595B (V_{OH}), and the output voltage of the SN74LVC244A (V_{OL}). The following equation used is Equation 3:

$$\mathsf{R}_{\mathsf{s}} = \frac{\mathsf{V}_{\mathsf{OH}} - \mathsf{V}_{\mathsf{OL}} - \mathsf{V}_{\mathsf{f}}}{\mathsf{i}_{\mathsf{f}}}$$

 $(V_{OH} - V_f - V_{OL})/(i_f) = R_s$. The required LED current is 2 mA, the forward voltage of the LED is 1.8 V, and V_{OH} can be assumed to be very close to V_{CC} because of the supplied current appearing significantly below the data sheet specified value for V_{OH} , and similarly the V_{OL} for SN74LVC244A can be assumed to be very close to 0 V. Inputting those values results in Equation 4:

$$\frac{3.3 \text{ V} - 0 \text{ V} - 1.8 \text{ V}}{2 \text{ mA}} = 750 \Omega \tag{4}$$

The SN74HC595B is the chosen shift register and has been selected for its extremely small size. The SN74HC595B is available in the X1QFN (extra-small quad-flatpack without leads), which allows it to be used in extremely space-constrained designs. In this case, the SN74HC595B device is placed near the 8x8 matrix display; however it can also be incorporated behind the display with some minor changes to the layout. Essentially, the final board must only be slightly larger than the LED matrix which it houses. Additionally, the SN74HC595B device can be linked serially, creating a long chain of matrix displays without the requirement for additional control lines.

The SN74HC595B has limited current sink capability for each channel; however, this design requires 16 mA, which means a second driver chip is required. The SN74LVC244A contains eight digital buffers capable of sinking up to 24 mA per channel at 3 V V_{cc}. This reference design uses one of these devices per 8×8 matrix display. Each LED in the matrix display is specified to operate at 2 mA and is driven from a single channel of the SN74HC595B device, while each column of eight LEDs sink into a single channel of the SN74HC595B device, while each column of the SN74LVC244A device to increase drive current, if required.

Also note that it is possible to sink more current into the SN74LVC244A device with this design than its absolute maximums allows. If all LEDs were turned on simultaneously, 128 mA of total current would be sunk into the SN74LVC244A device. To avoid this situation, only one column must be active at any time and multiplexing must be used to create the illusion that all columns are turned ON.

2.2.4 Timing and Control Requirements

Each string of SN74HC595B devices require three control lines: serial data (SER), serial clock (SRCLK), and register clock (RCLK).

To load data into the shift register, first ensure that SRCLK and RCLK are in the LOW state. SER is set to the first desired bit value, then SRCLK is pulsed to clock that value into the shift register. This process is repeated for all 8 bits of the shift register. As soon as the data has been loaded into the shift register, RCLK is pulsed to push the data from the internal register to the outputs of the device. The output registers continue to hold the values shifted into them until either another RCLK is received or the device has been powered off.

The software to control the 8×8 matrix display is relatively complex. First, each image must be broken down into columns, then each column is loaded into the shift registers: first a byte of what is to be displayed (also called the 'row byte'), then a byte to indicate which column is to display it (also called the 'column byte'). A soon as both bytes have loaded, RCLK is pulsed to push the data to the LEDs. When this process completes, the next column can be loaded and RCLK can wait to pulse until the desired time is elapsed (as previously mentioned, at least 4.16 ms later). This process is repeated for each frame that is to be displayed.

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(3)



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Figure 9 shows the timing diagram for the SN74HC595B.	
SER	
SRCLR	
OE	
Q _A	
Q _B	
QC	
Q _D	
Q _E	
Q _F	
Q _G	
а _н	
а _н ,	

NOTE: XXXXXXX implies that the output is in 3-State mode.

Figure 9. Timing Diagram for SN74HC595B



2.2.5 Layout

The two SN74HC595B devices are placed on the front of the board alongside the 8x8 LED matrix while the SN74LVC244A device is placed on the back of the board. which were choices made out of convenience. Each LED has a limiting resistor directly behind it in this design. Especially in scenarios with large displays, the resistors can be placed on the front of the board. The large pours connecting the resistors and LEDs into columns and rows were not required, but were convenient in this arrangement. Because this board had a large amount of space, each device has been separated out; however, the devices can be condensed to a very small space if necessary for a design.



Figure 10. 8×8 LED Matrix Reference Design Hardware Layout Example From BOOSTXL-SHIFTLED BoosterPack[™] Plug-in Module (Top: Board Front, Bottom: Board Back)



2.2.6 Software Flowchart

The flowchart in Figure 11 shows a generic method for outputting a single frame to the hardware of the *8x8 matrix display reference design*. There are three loops here: The first loop uses "j" as an iterator and indicates which column is being output and has the other two loops nested within it. The second loop uses "i" as an iterator and loads the row byte into the shift registers (indicating which LEDs in the column are ON or OFF). The third loop also uses i as an iterator and loads the column byte into the shift registers (indicating which column is to be displayed). After all values have been loaded into the shift registers, RCLK is pulsed to push those values to the outputs and activate the display. The column is then left on for an eighth of the indicated frame time (4 ms is a good value for this delay), and the process is repeated for the remaining seven columns.

System Design Theory



Figure 11. 8×8 Matrix Display Single-Frame Output Flow Chart



3 Testing and Results

These reference designs were used in the design of the BOOSTXL-SHIFTLED BoosterPack[™] Plug-in Module (not yet released). A prototype board for this BoosterPack was used for testing the reference designs. The board is shown on the first page of this reference design.

3.1 Seven-Segment Driver Reference Design Testing

The primary concerns for this design relate to power consumption and thermal dissipation. In spaceconstrained designs, there is little space for heat sinks, so the capability of devices operating in close proximity without heat sinks is important.

3.1.1 Current Testing

The purpose of this test was to determine the actual current requirement of the seven-segment display while all segments are active (see Table 2). The current was measured at the power supply to the BOOSTXL-SHIFTLED BoosterPack board. All unused circuitry was either depopulated or disconnected.

TEST	TEST CONDITIONS	RESULT	UNITS
Standby current	V_{CC} = 2 V; all LEDs turned off	< 100 ⁽¹⁾	nA
	V_{CC} = 3.6 V; all LEDs turned off	< 100 ⁽¹⁾	nA
Maximum current	V _{CC} = 2 V; all segments turned on for one seven-segment display	82.40	mA
	V _{CC} = 3.6 V; all segments turned on for one seven-segment display	99.57	mA

Table 2. Current Test Results

⁽¹⁾ The device used to measure this value could not accurately measure less than 100 nA.

3.1.2 Thermal Testing

The purpose of this test was to determine the thermal increase while all segments are active. A thermal camera was used to capture the temperature increase.

Thermal images were taken after one minute at maximum current at $V_{CC} = 2 V$ (see Figure 12), and at $V_{CC} = 3.6 V$ (see Figure 13).









The maximum temperature variations observed were recorded in Table 3.

TEST	TEST CONDITIONS	RESULT	UNITS
Maximum temperature – change	T_A = 25°C; V_{CC} = 2 V; all segments turned on for one seven segment display	5	°C
	$T_{\rm A}$ = 25°C; $V_{\rm CC}$ = 3.6 V; all segments turned on for one seven segment display	9	°C

Table 3. Thermal Test Results

3.2 8×8 LED Matrix Reference Design Testing

The primary concerns for this design relate to power consumption and thermal dissipation. In spaceconstrained designs, there is little space for heat sinks, so the capability of devices operating in close proximity without heat sinks is important.

3.2.1 Current Testing

The purpose of this test was to determine the actual current requirement of the 8×8 LED matrix (see Table 4). Current was measured at the power supply to the BOOSTXL-SHIFTLED BoosterPack board. All unused circuitry was either depopulated or disconnected.

Table 4. Current Test Results

TEST	TEST CONDITIONS	RESULT	UNITS
Standby current	V_{CC} = 2 V; all LEDs turned off	<100 ⁽¹⁾	nA
	V_{CC} = 3.6 V; all LEDs turned off	<100 ⁽¹⁾	nA
Single column Maximum current	V _{cc} = 2 V; all LEDs turned on for one column	2.47	mA
	V _{cc} = 3.6 V; all LEDs turned on for one column	16.08	mA
Maximum current	V_{CC} = 2 V; all LEDs turned on	12.37 ⁽²⁾	mA
	V_{CC} = 3.6 V; All LEDs turned on	84.97 ⁽²⁾	mA

⁽¹⁾ The device used to measure this value could not accurately measure less than 100 nA.

⁽²⁾ The absolute maximum rating of the SN74LVC244A is 100 mA at $V_{CC} = 5.5$ V. Although this design can violate that maximum when all LEDs are turned on (depending on the V_f for the specific seven segment used), the device is still operating below the absolute maximum power.



3.2.2 Thermal Testing

The purpose of this test was to determine the thermal increase when all segments are active. A thermal camera was used to capture the temperature increase (see and Figure 13).



Figure 14. Thermal image—8×8 LED Matrix Reference Design Operating at Max Current: V_{cc} = 2 V

The thermal results are summarized in Table 5.



Figure 15. Thermal Image—8×8 LED Matrix Reference Design Operating at Max Current: V_{cc} = 3.6 V

Table 5. Thermal Test Results

TEST	TEST CONDITIONS	RESULT	UNITS
Maximum temperature change	$T_A = 25^{\circ}C$; $V_{CC} = 2$ V; all LEDs turned on	4	°C
	$T_A = 25^{\circ}$ C; $V_{CC} = 3.6$ V; all LEDs turned on	7	°C



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01233.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01233.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01233.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01233.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01233.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01233.

5 Software Files

To download the software files, see the design files at TIDA-01233.

6 Terminology

Daisy-chained— Devices connected together in series. For shift registers, this means that the bit that was in the 8th slot will be set as an input for the SER pin of the next shift register.

Pulse width modulation—Changing the duty cycle of a square wave based on how bright the LED should be.

6.1 Trademarks

All trademarks are the property of their respective owners.

7 About the Author

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