NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P12V" represents connection to the +12V power plane.
2. The netname "P3P3V" represents connection to the +3.3V power plane.
3. The netname "P1P8V" represents connection to the +1.8V digital power plane.
4. The netname "P1P1V" represents connection to the +1.1V power plane.
5. The netname "P1P8V_ITEA" represents connection to the +1.8V ITE6535 analog supply power plane.
6. The netname "F_VCCIO" represents connection to the +3V FPGA Vccio power plane.
7. The netname "P2P5V_FAUXPLL" represents connection to the +2.5V FPGA aux/pll power plane.
8. The netname "P1P8V_A" represents connection to the +1.8V controller analog supply power plane.
9. The netname "GND" represents connection to the ground plane.
10. A "Z" suffix on a signal name indicates an active low signal.
11. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2137507: Initial Release	11/1/2013	NG
B	ECO 2140137: Updated to rev B	2/18/2014	NG
C	ECO 2141055: Updated to rev C	4/8/2014	NG
D	ECO 2142175: Updated to rev D	5/28/2014	NG
E	ECO 2144118: Updated to rev E	8/8/2014	NG
F	Updated to rev F	11/7/2019	DH
G	Updated to rev G	5/11/2020	DH

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		SYST	TITLE: ESD, DLPLCR900DEVM DLP043
		PRJ L. Harvey 8/8/2014	
2513535	0314PO	QA	A3 DRAWING NO 2513534 REV G
NEXT ASSY	USED ON		SCALE SHEET 1 of 29
APPLICATION		SW Cadence 16.6	

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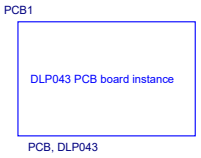

Boot_Hold Shunt
60900213421

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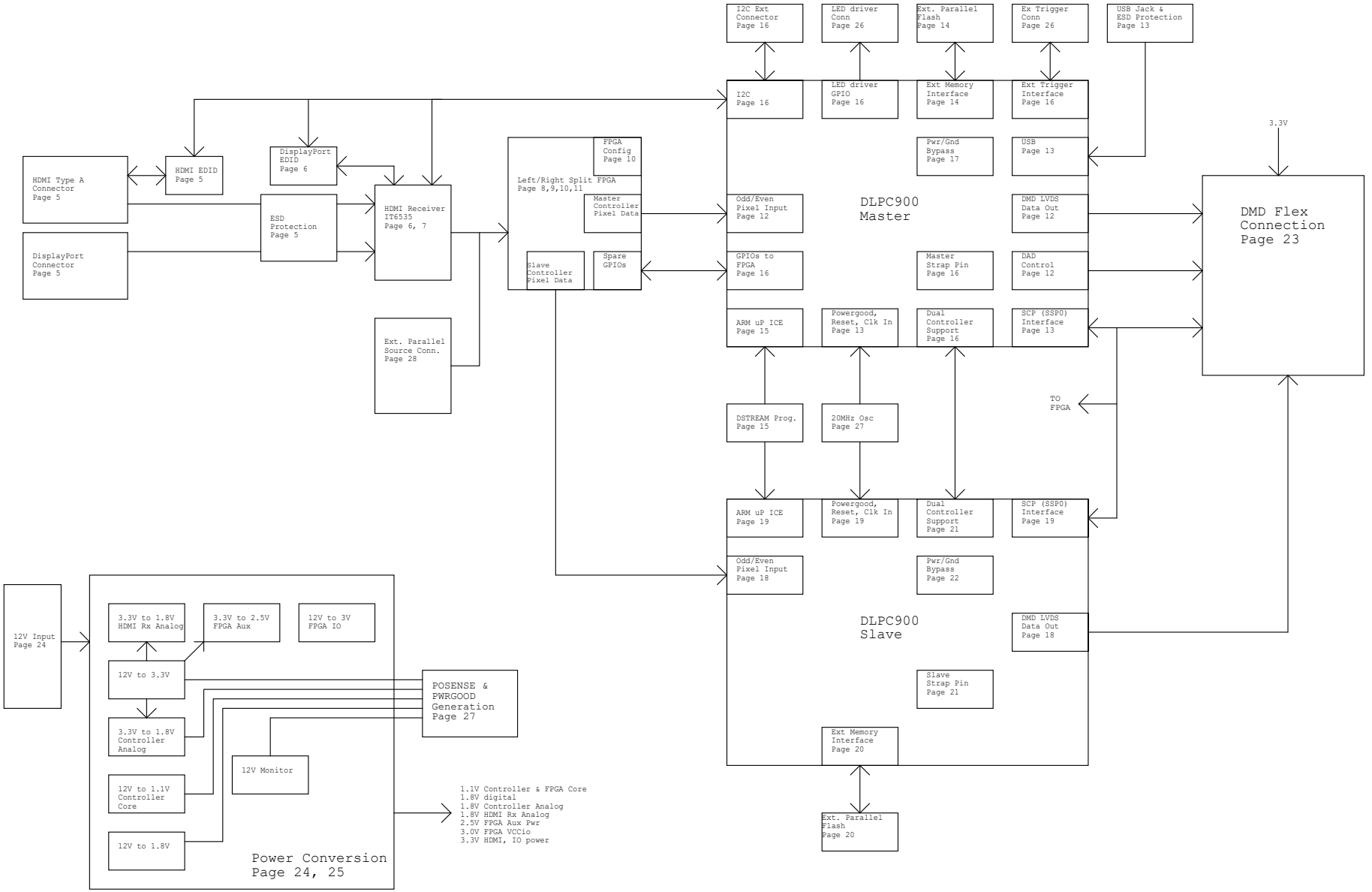

Block Diagram

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
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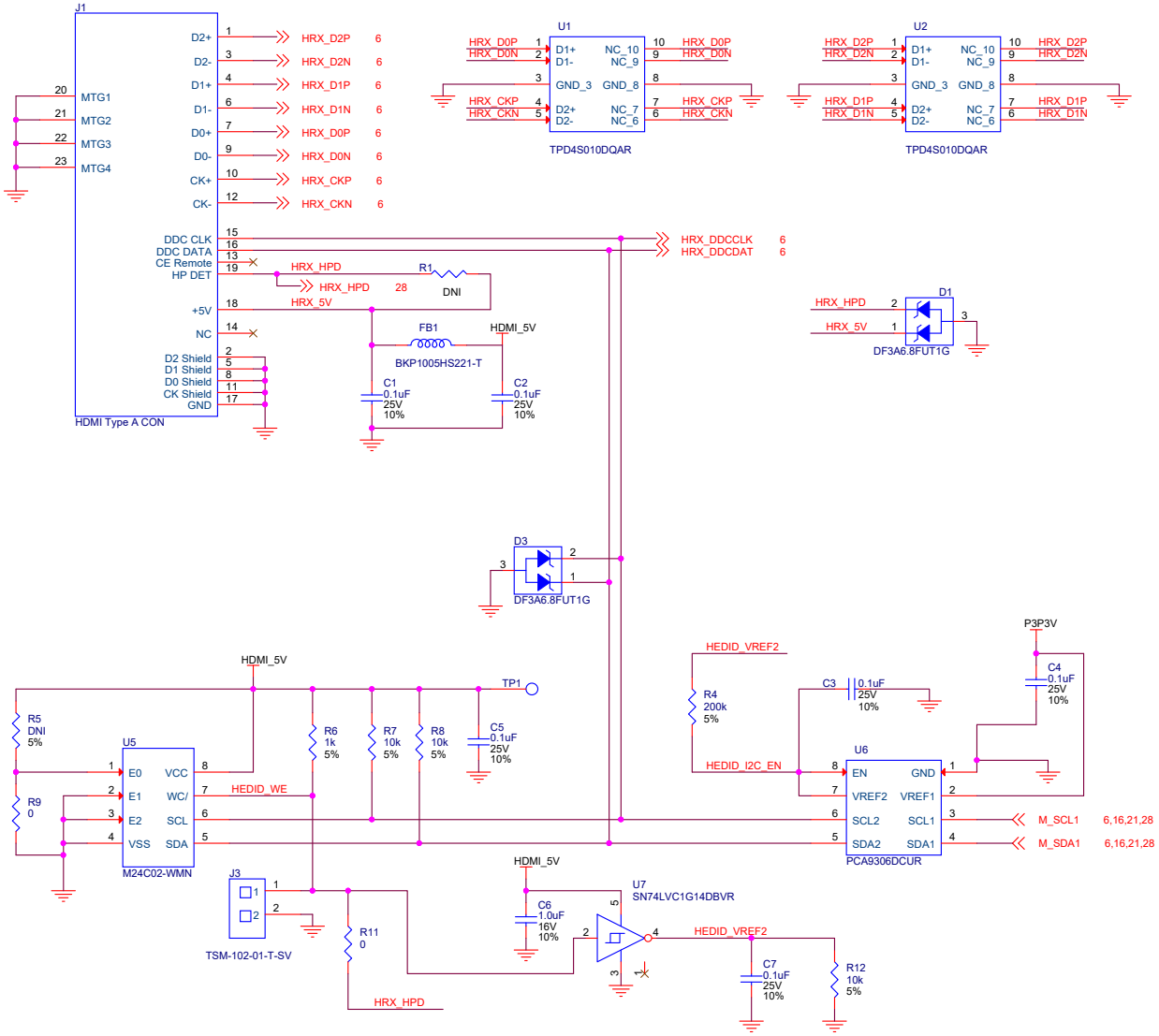
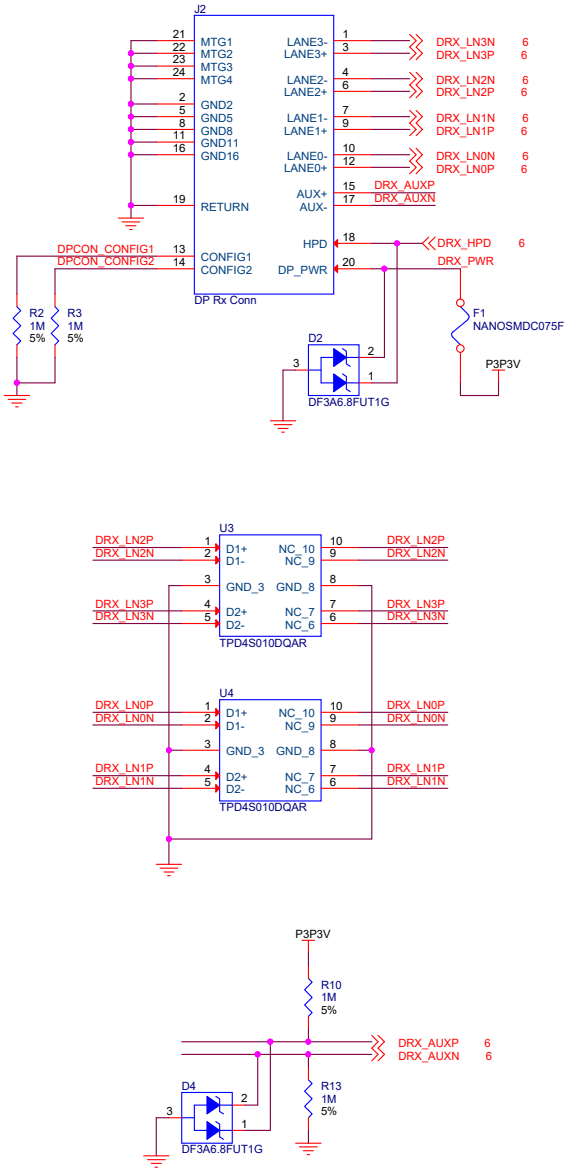


To program HDMI EDID
- install jumper to enable PROM write and disable hot plug detect
- connect HDMI cable to supply 5V
- use TI control program to update EDID

HDMI TypeA Rx Conn, ESD, and EDID



DisplayPort Rx Conn, ESD

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
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Apply a crystal input
even audio function
is not used per ITE
recommandation

I2C address select
low = 0xB0
high = 0xB2

Must connect I2C and interrupt
to controller for register setup

HDMI receiver input/output

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TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
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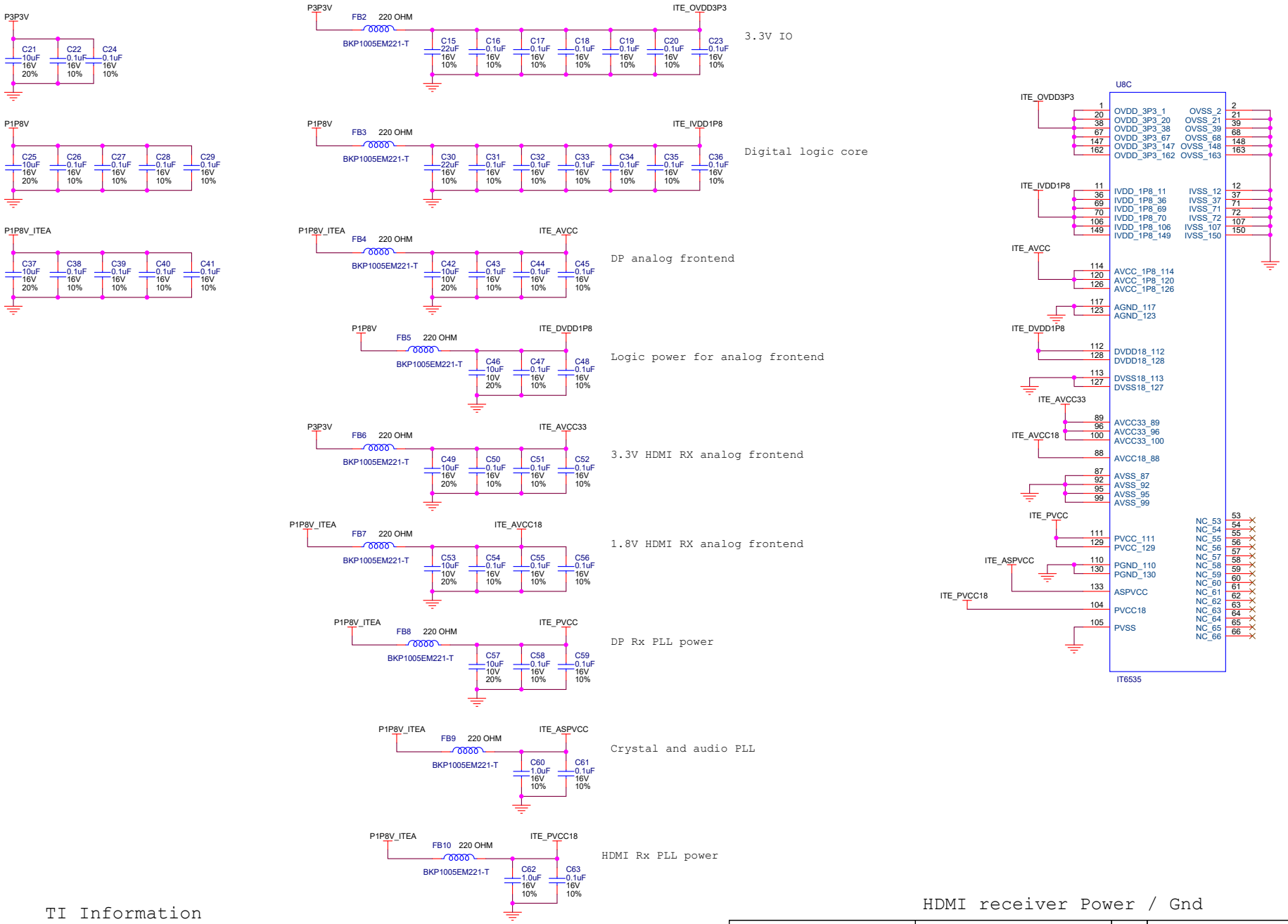

HDMI receiver Power / Gnd

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
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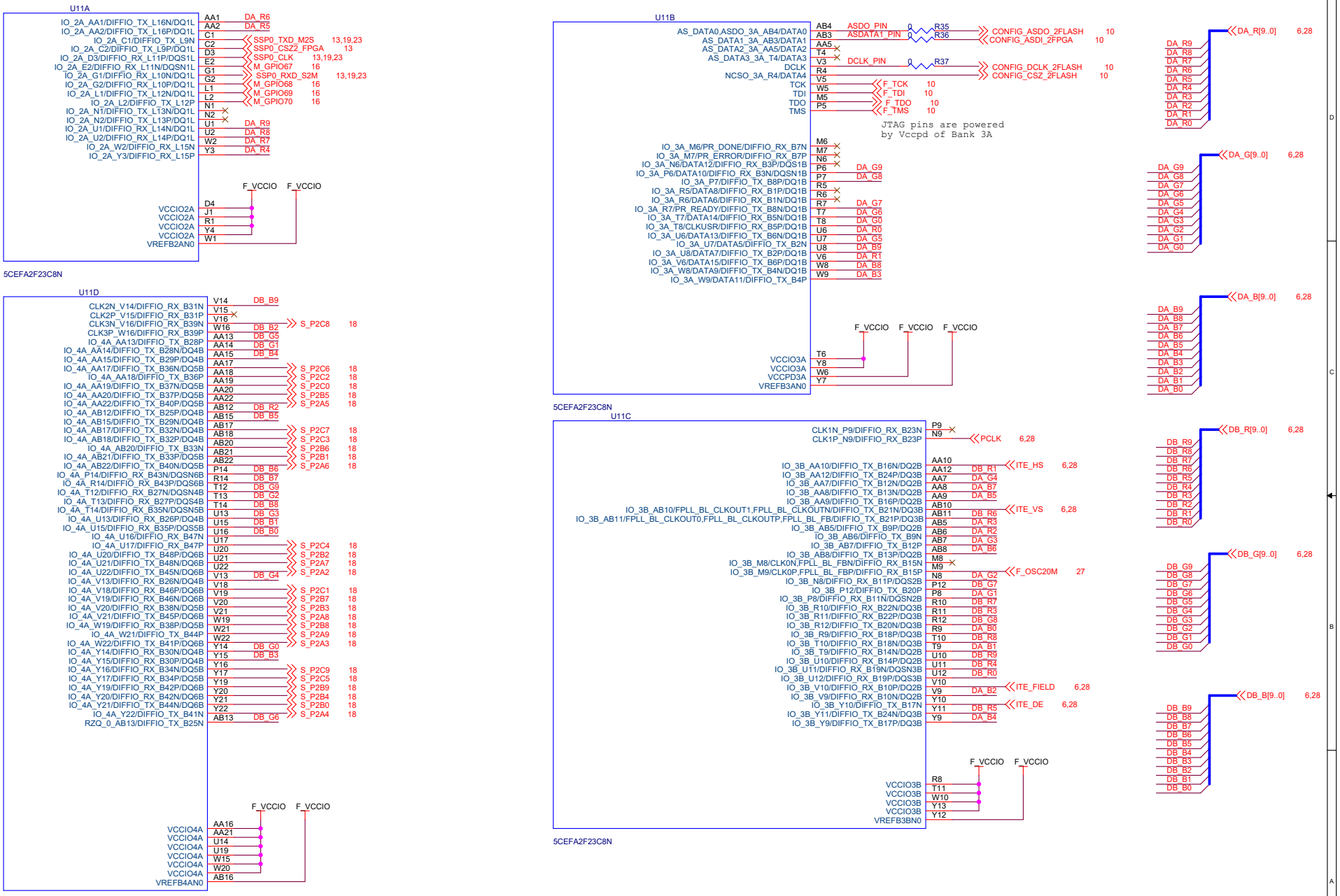

Left/Right Split FPGA Bank 2A, 3A, 3B, 4A

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
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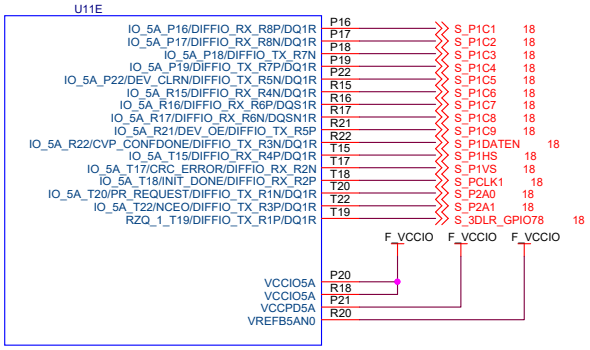

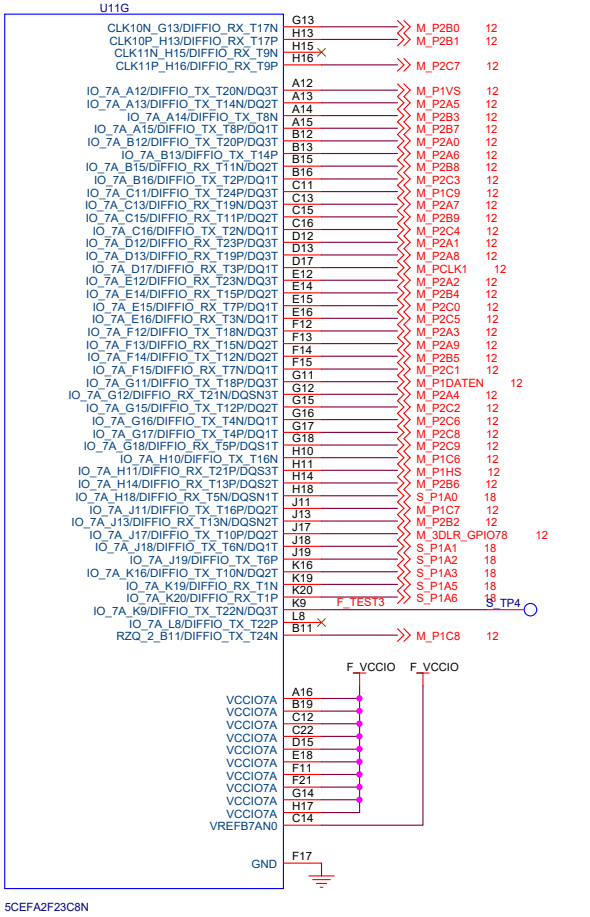

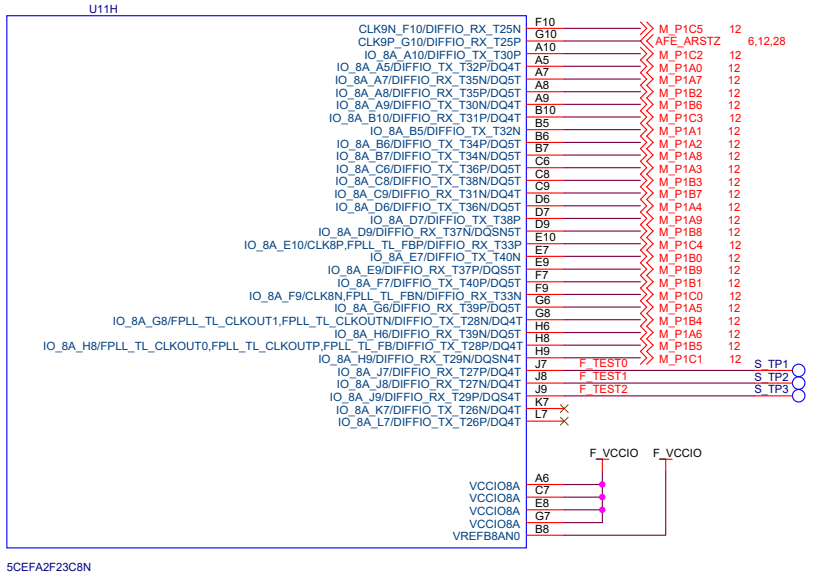

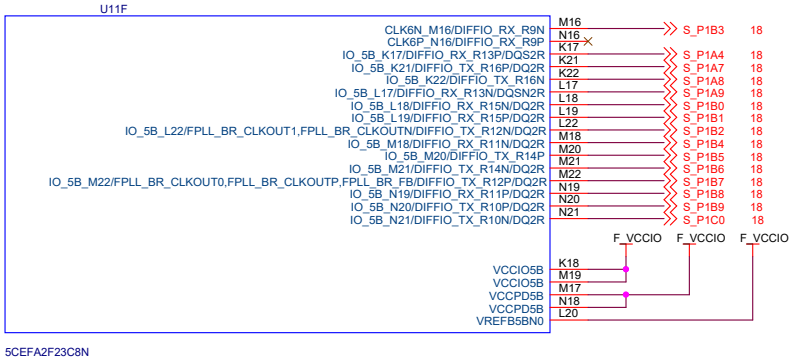

Left/Right Split FPGA Bank 5A, 5B, 7A, 8A

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
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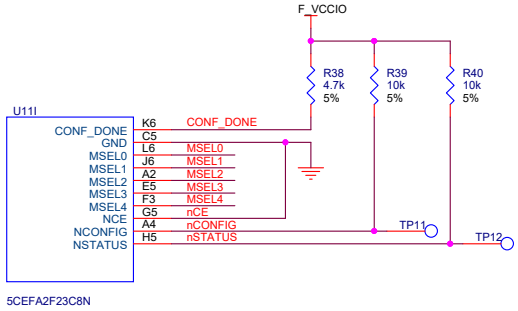
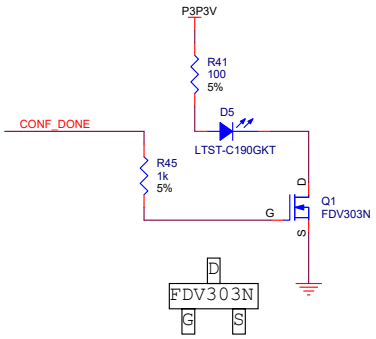
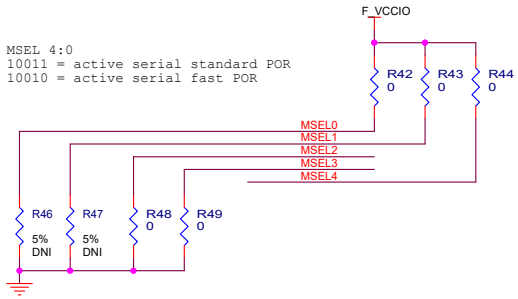
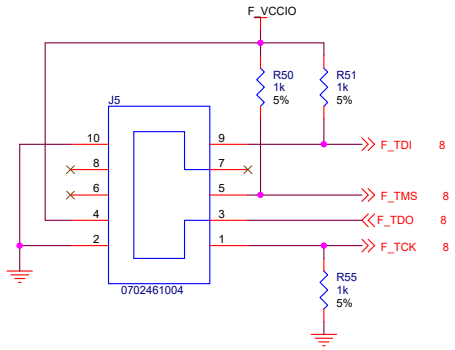
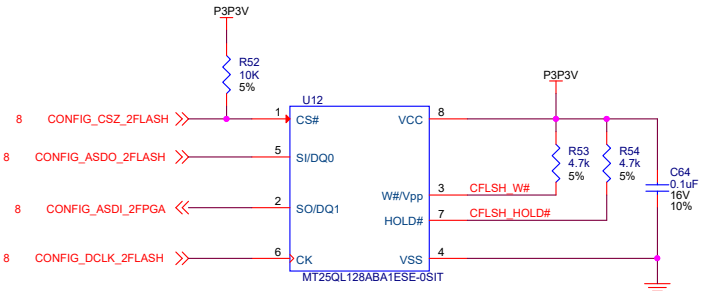








Altera's USB ByteBlaster Connector



Use Altera's "Serial loader" option to update flash
thru the FPGA JTAG port with Byteblaster cable

Left/Right Split FPGA Configuration

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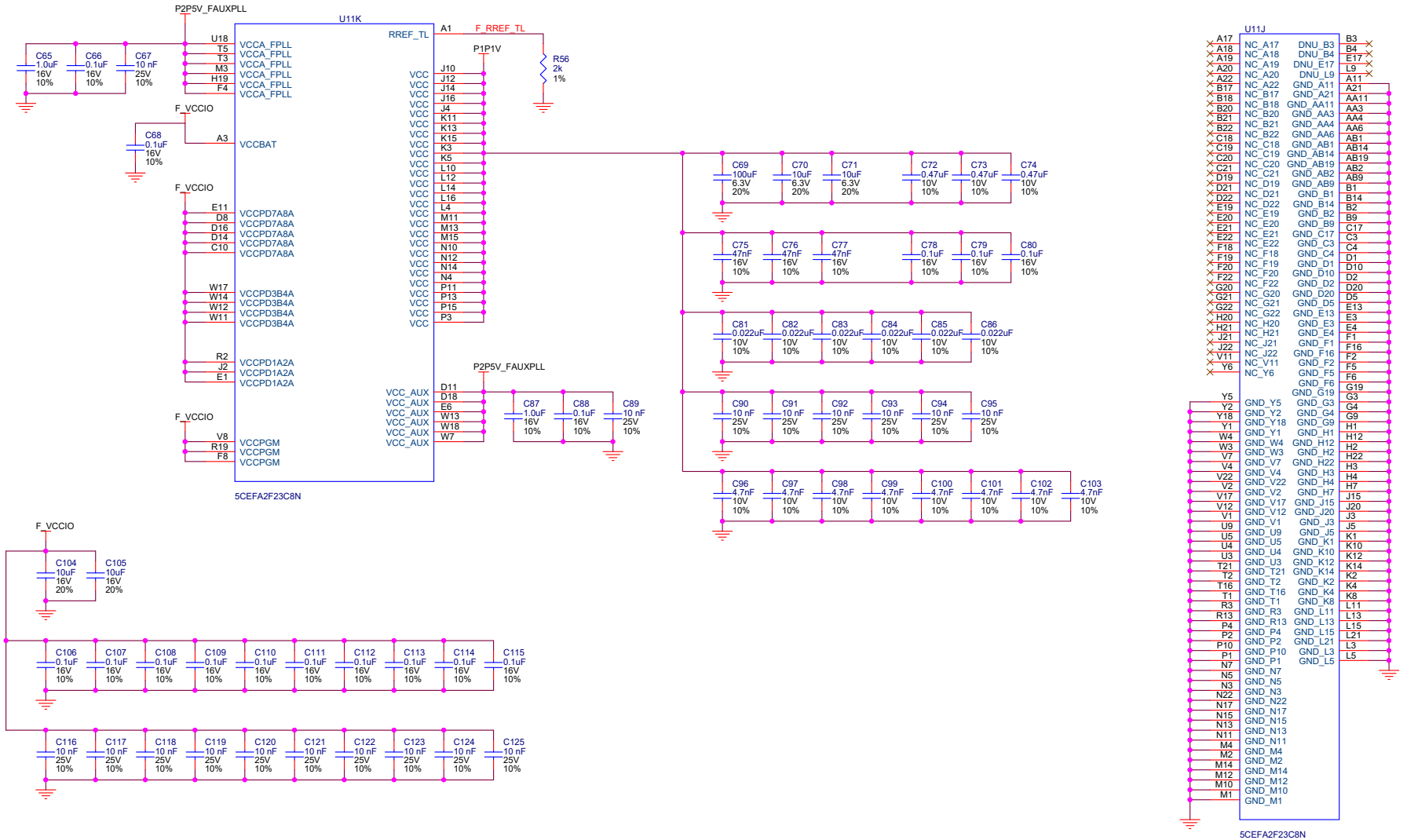

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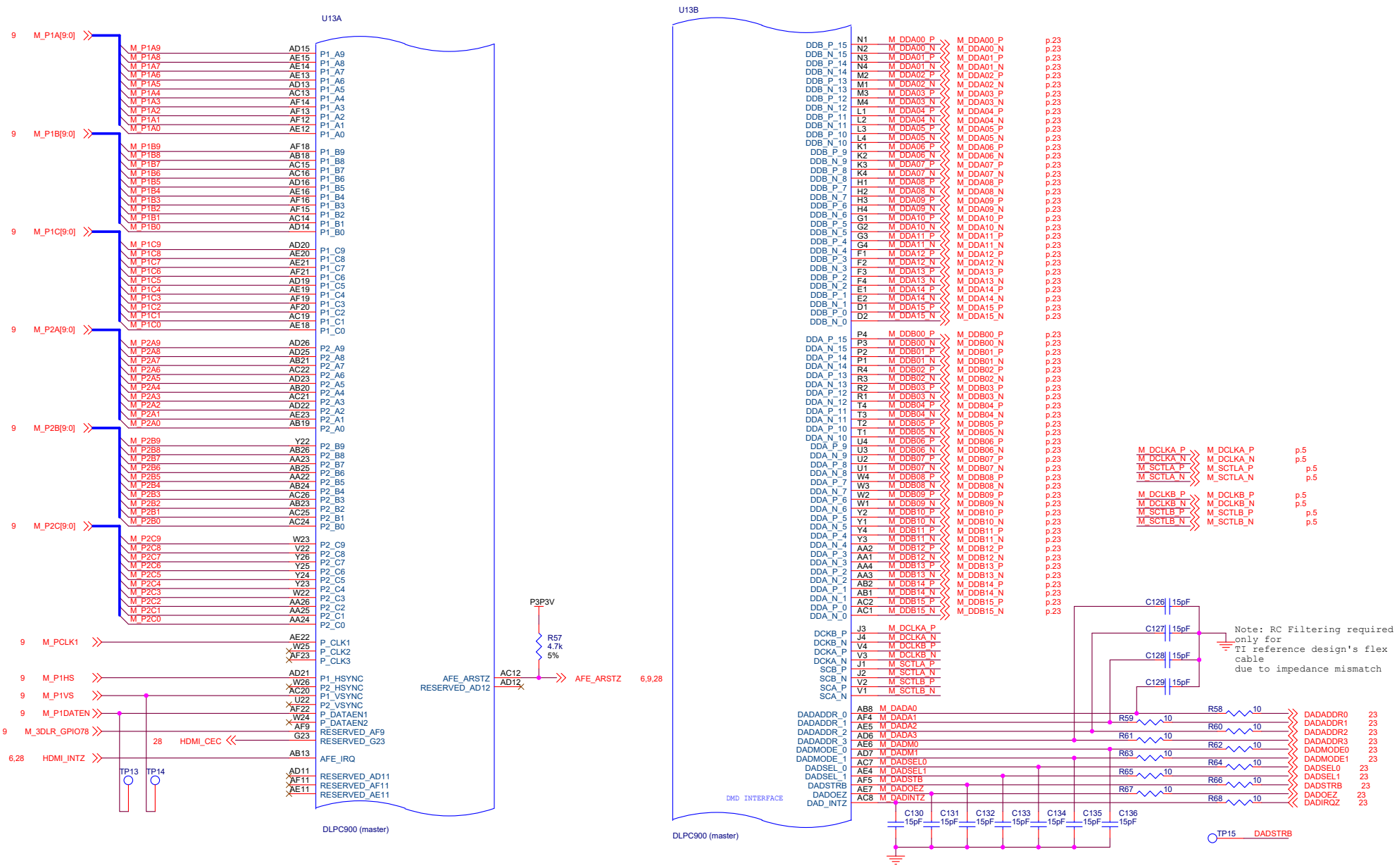

Master Controller Video Input, DMD & DAD Output

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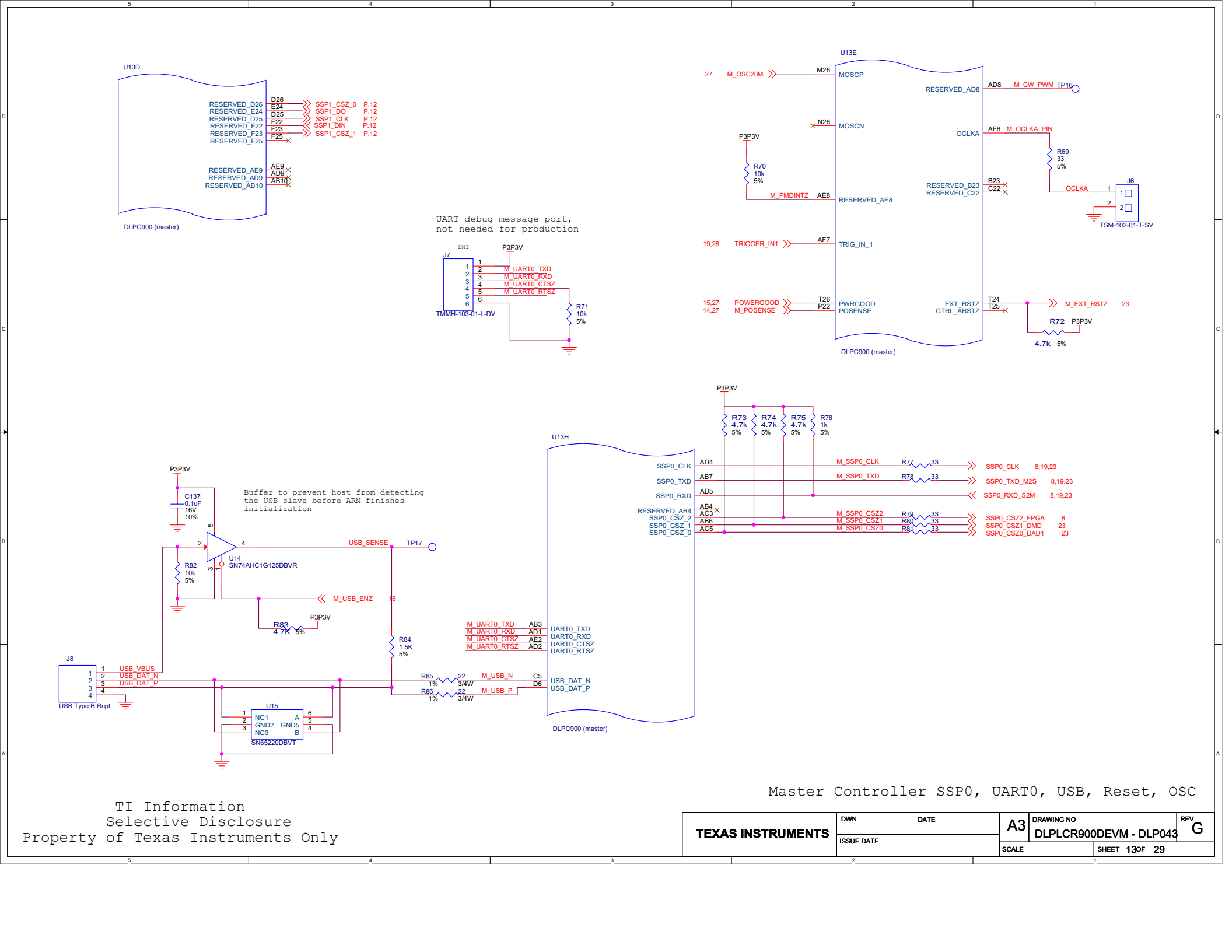
U13D
RESERVED_D26
RESERVED_E24
RESERVED_D25
RESERVED_F22
RESERVED_F23
RESERVED_F25
SSP1_CSZ_0 P.12
SSP1_DO P.12
SSP1_CLK P.12
SSP1_DIN P.12
SSP1_CSZ_1 P.12
RESERVED_AE9
RESERVED_AD9
RESERVED_AB10
DLPC900 (master)
UART debug message port,
not needed for production
J7
DNI
TMMH-103-01-L-DV
M_UART0_TXD
M_UART0_RXD
M_UART0_CTSZ
M_UART0_RTSZ
R71
10k
5%
U13E
M_OSC20M
MOSCP
MOSCN
R70
10k
5%
M_PMDINTZ
RESERVED_AE8
TRIGGER_IN1
TRIG_IN_1
POWERGOOD
M_POSENSE
PWRGOOD
POSENSE
RESERVED_AD8
M_CW_PWM TP16
OCLKA
R69
33
5%
RESERVED_B23
RESERVED_C22
J6
TSM-102-01-T-SV
EXT_RSTZ
CTRL_ARSTZ
M_EXT_RSTZ
R72
4.7k
5%
DLPC900 (master)
P3P3V
C137
0.1uF
16V
10%
Buffer to prevent host from detecting
the USB slave before ARM finishes
initialization
U14
SN74AHC1G125DBVR
R82
10k
5%
USB_SENSE
TP17
M_USB_ENZ
R83
4.7K
5%
R84
1.5K
5%
J8
USB Type B Rcpt
USB_VBUS
USB_DAT_N
USB_DAT_P
R85
R86
22
3/4W
1%
M_USB_N
M_USB_P
U15
SN65220DBVT
U13H
SSP0_CLK
SSP0_TXD
SSP0_RXD
RESERVED_AB4
SSP0_CSZ_2
SSP0_CSZ_1
SSP0_CSZ_0
R73
4.7k
5%
R74
4.7k
5%
R75
4.7k
5%
R76
1k
5%
R77
R78
R79
R80
R81
33
M_SSP0_CLK
M_SSP0_TXD
M_SSP0_CSZ2
M_SSP0_CSZ1
M_SSP0_CSZ0
SSP0_CLK 8,19,23
SSP0_TXD_M2S 8,19,23
SSP0_RXD_S2M 8,19,23
SSP0_CSZ2_FPGA 8
SSP0_CSZ1_DMD 23
SSP0_CSZ0_DAD1 23
UART0_TXD
UART0_RXD
UART0_CTSZ
UART0_RTSZ
USB_DAT_N
USB_DAT_P
DLPC900 (master)
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Master Controller SSP0, UART0, USB, Reset, OSC
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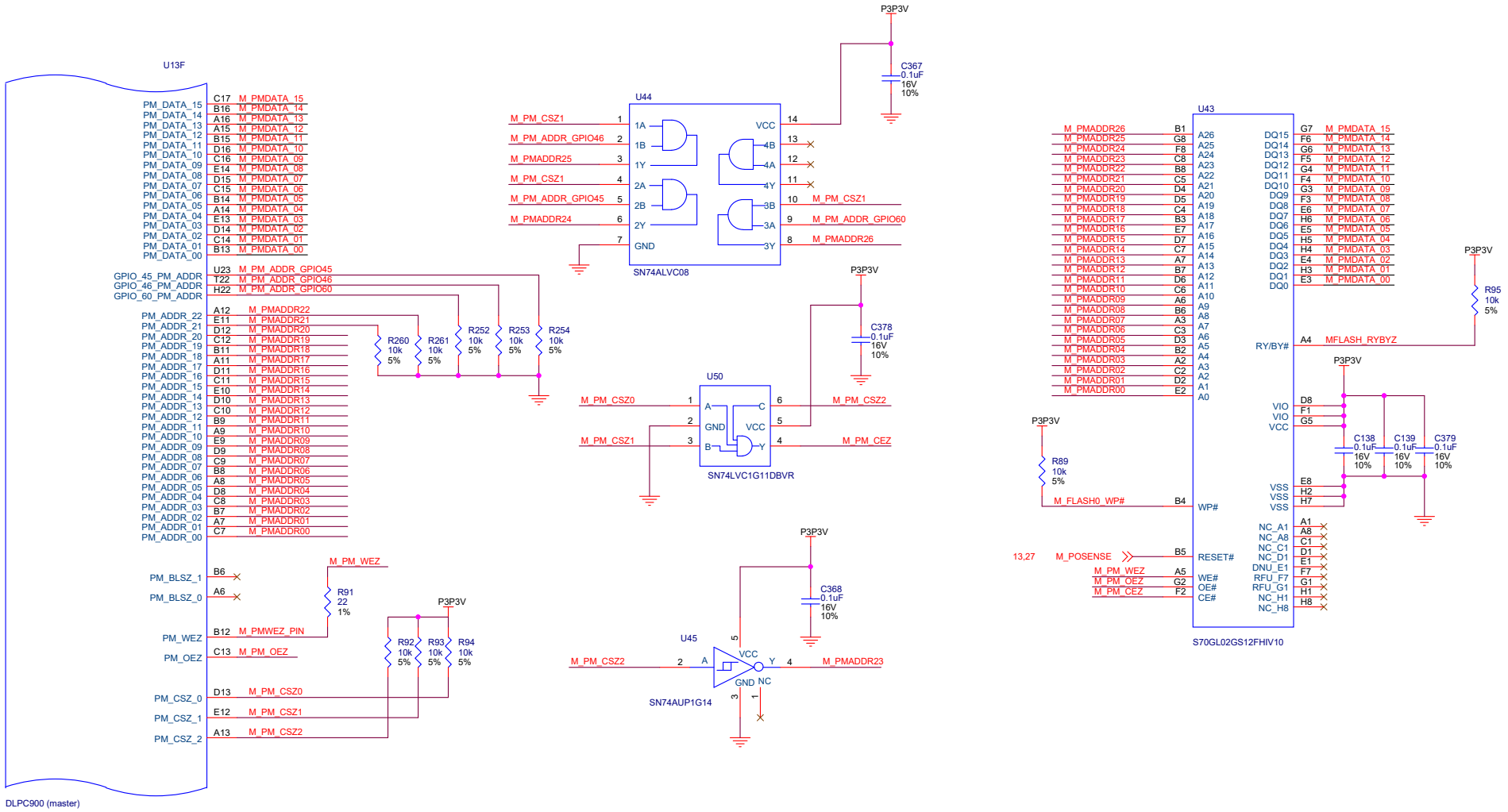

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Master Controller Flash Interface

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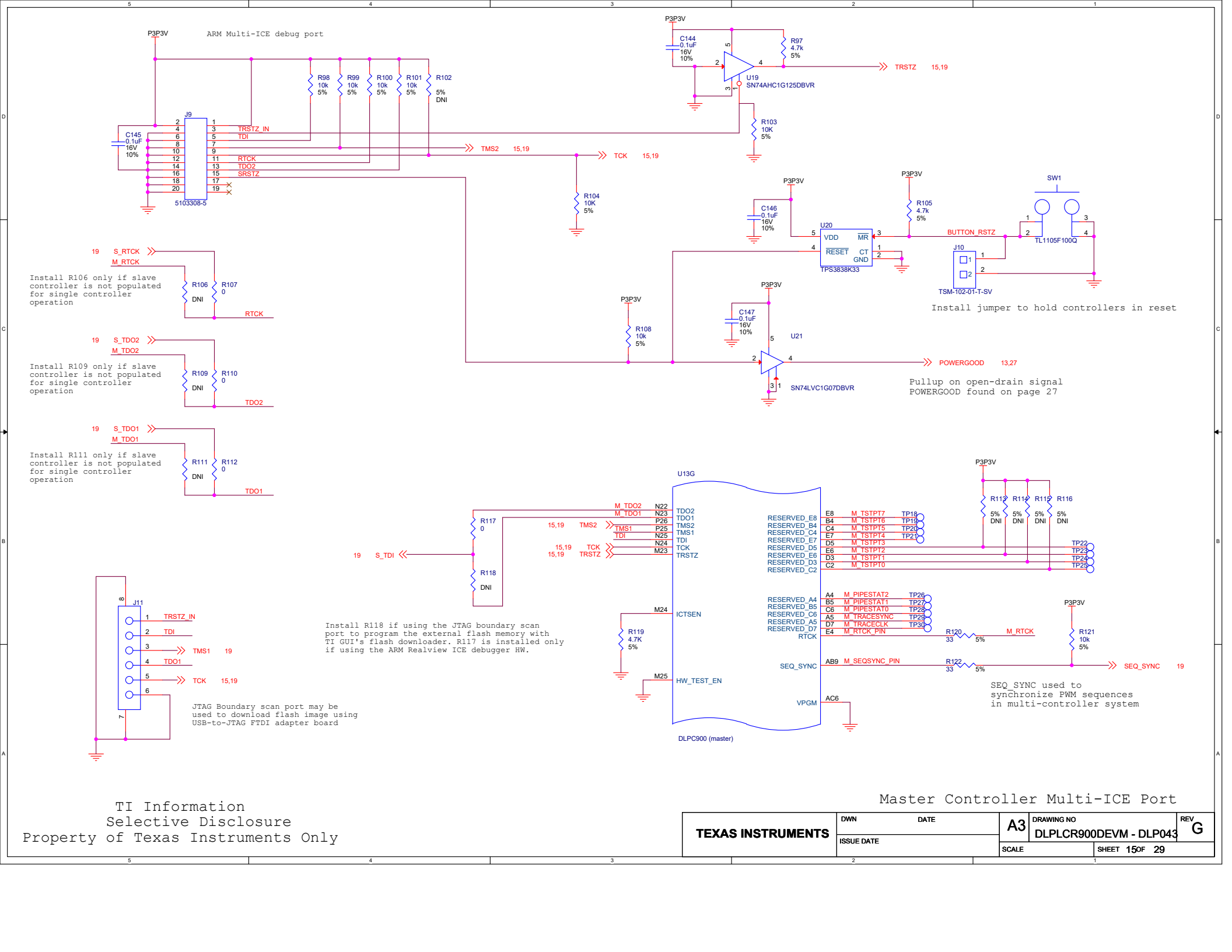

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Master Controller Multi-ICE Port

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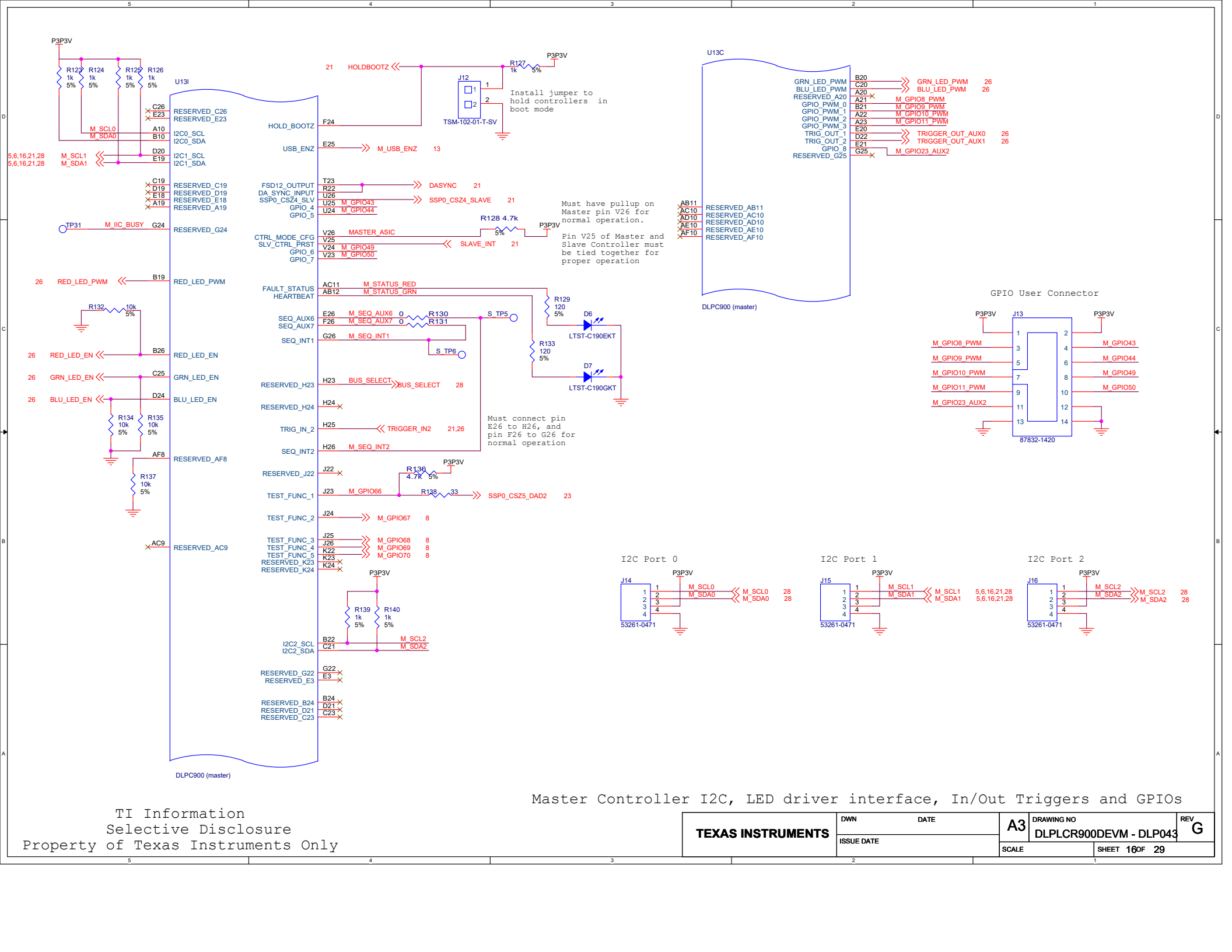
U13I
DLPC900 (master)
U13C
DLPC900 (master)
HOLDBOOTZ
HOLD_BOOTZ
USB_ENZ
M_USB_ENZ
TSM-102-01-T-SV
Install jumper to hold controllers in boot mode
DASYNC
SSP0_CSZ4_SLAVE
SLAVE_INT
MASTER_ASIC
Must have pullup on Master pin V26 for normal operation.
Pin V25 of Master and Slave Controller must be tied together for proper operation
M_STATUS_RED
M_STATUS_GRN
LTST-C190EKT
LTST-C190GKT
S_TP5
S_TP6
BUS_SELECT
TRIGGER_IN2
M_SEQ_INT2
Must connect pin E26 to H26, and pin F26 to G26 for normal operation
M_GPIO66
SSP0_CSZ5_DAD2
M_GPIO67
M_GPIO68
M_GPIO69
M_GPIO70
M_SCL2
M_SDA2
M_IIC_BUSY
RED_LED_PWM
RED_LED_EN
GRN_LED_EN
BLU_LED_EN
GRN_LED_PWM
BLU_LED_PWM
M_GPIO8_PWM
M_GPIO9_PWM
M_GPIO10_PWM
M_GPIO11_PWM
M_GPIO23_AUX2
TRIGGER_OUT_AUX0
TRIGGER_OUT_AUX1
GPIO User Connector
87832-1420
I2C Port 0
I2C Port 1
I2C Port 2
53261-0471
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Master Controller I2C, LED driver interface, In/Out Triggers and GPIOs
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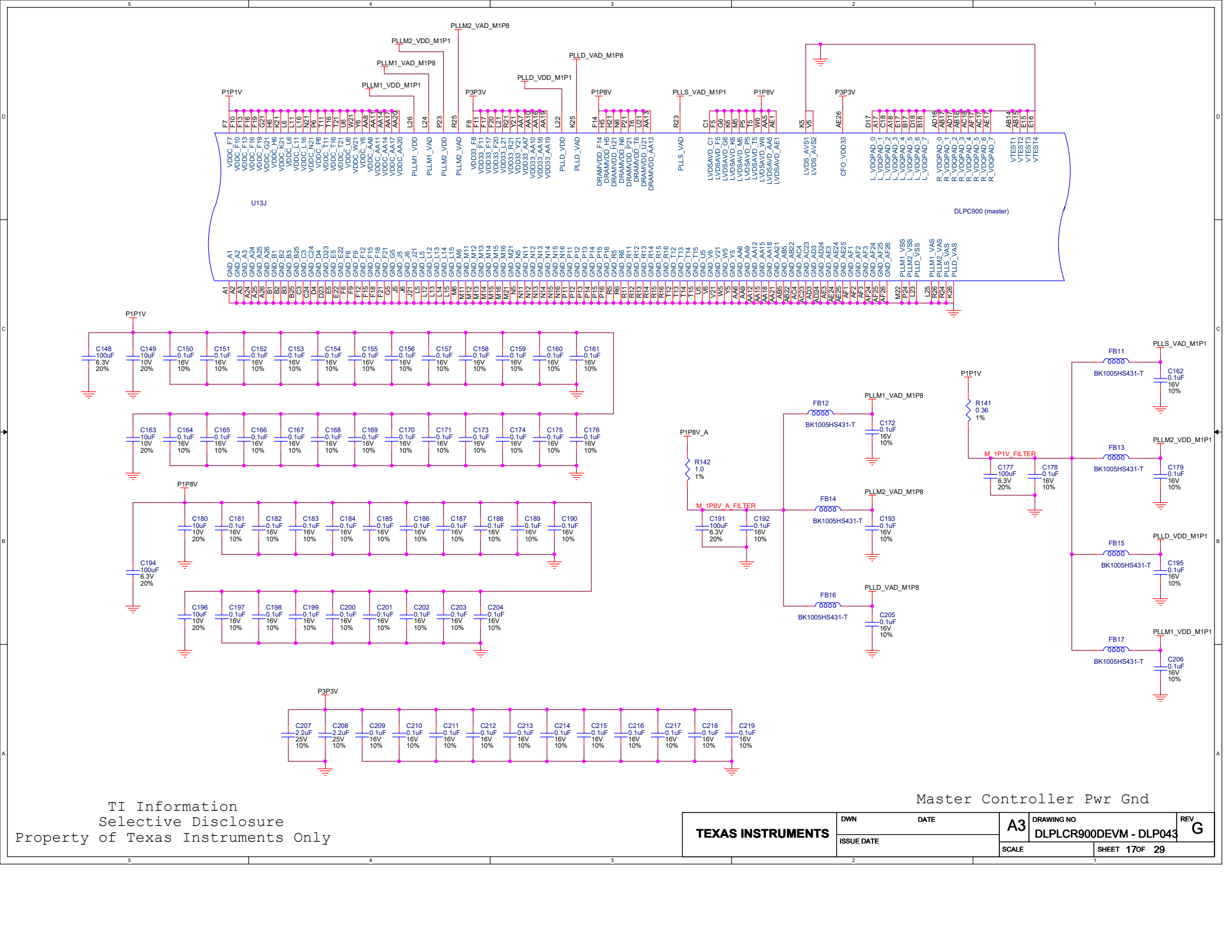

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Master Controller Pwr Gnd

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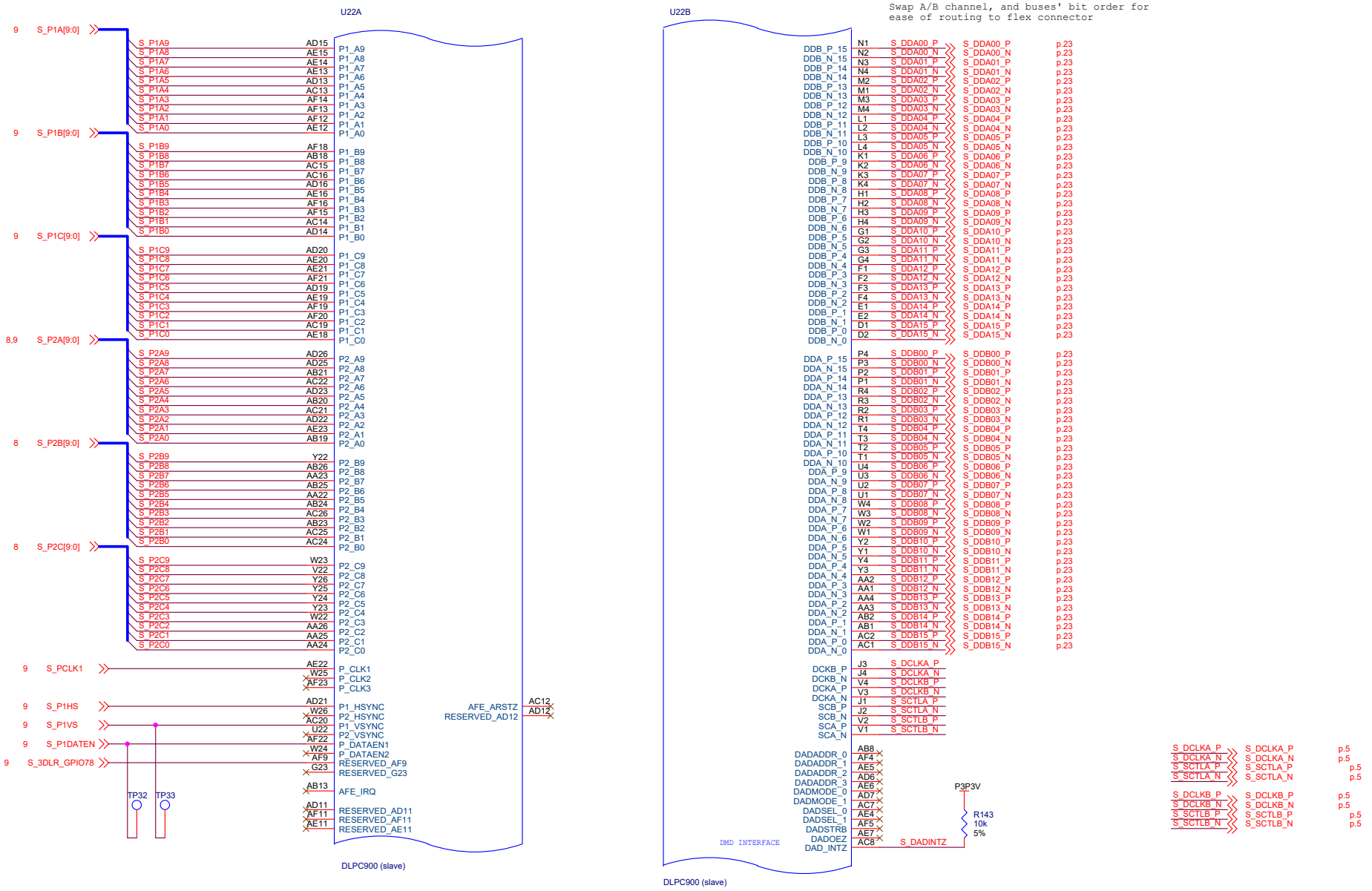

Slave Controller Video Input, DMD Output

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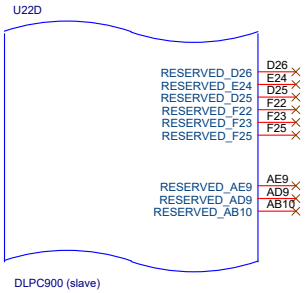
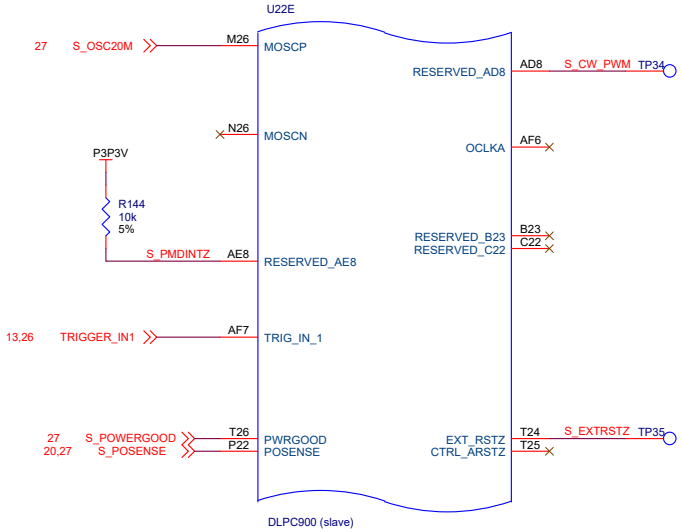
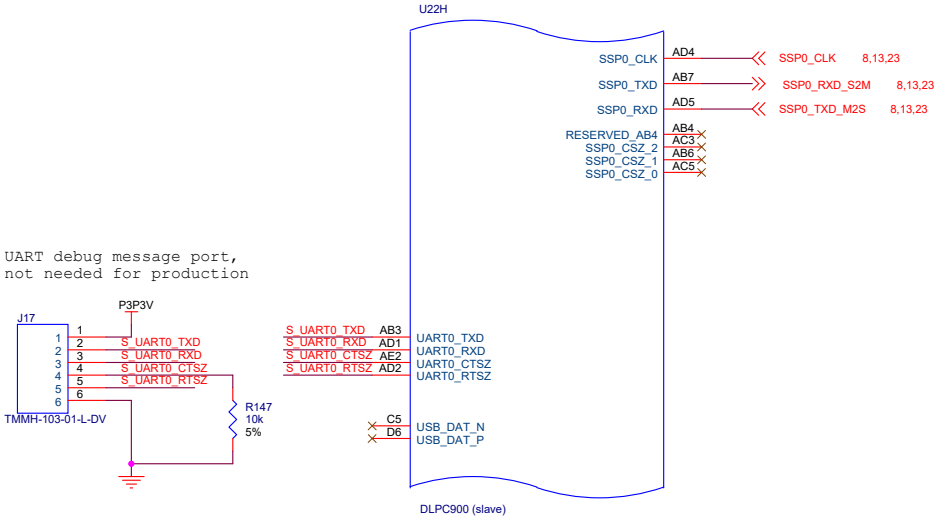
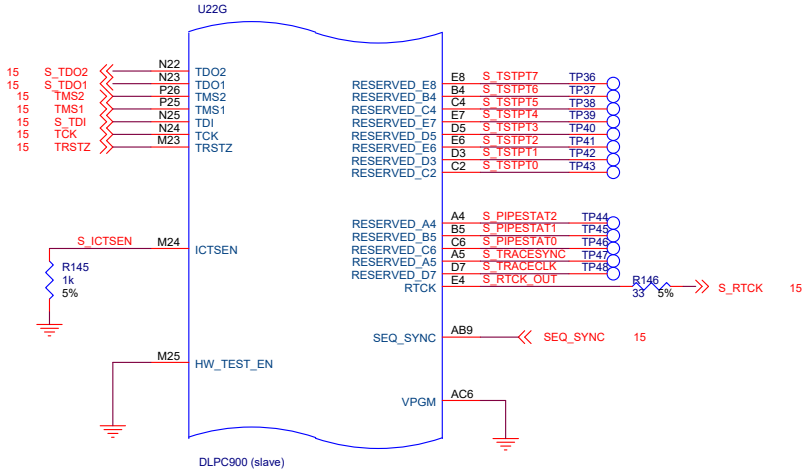


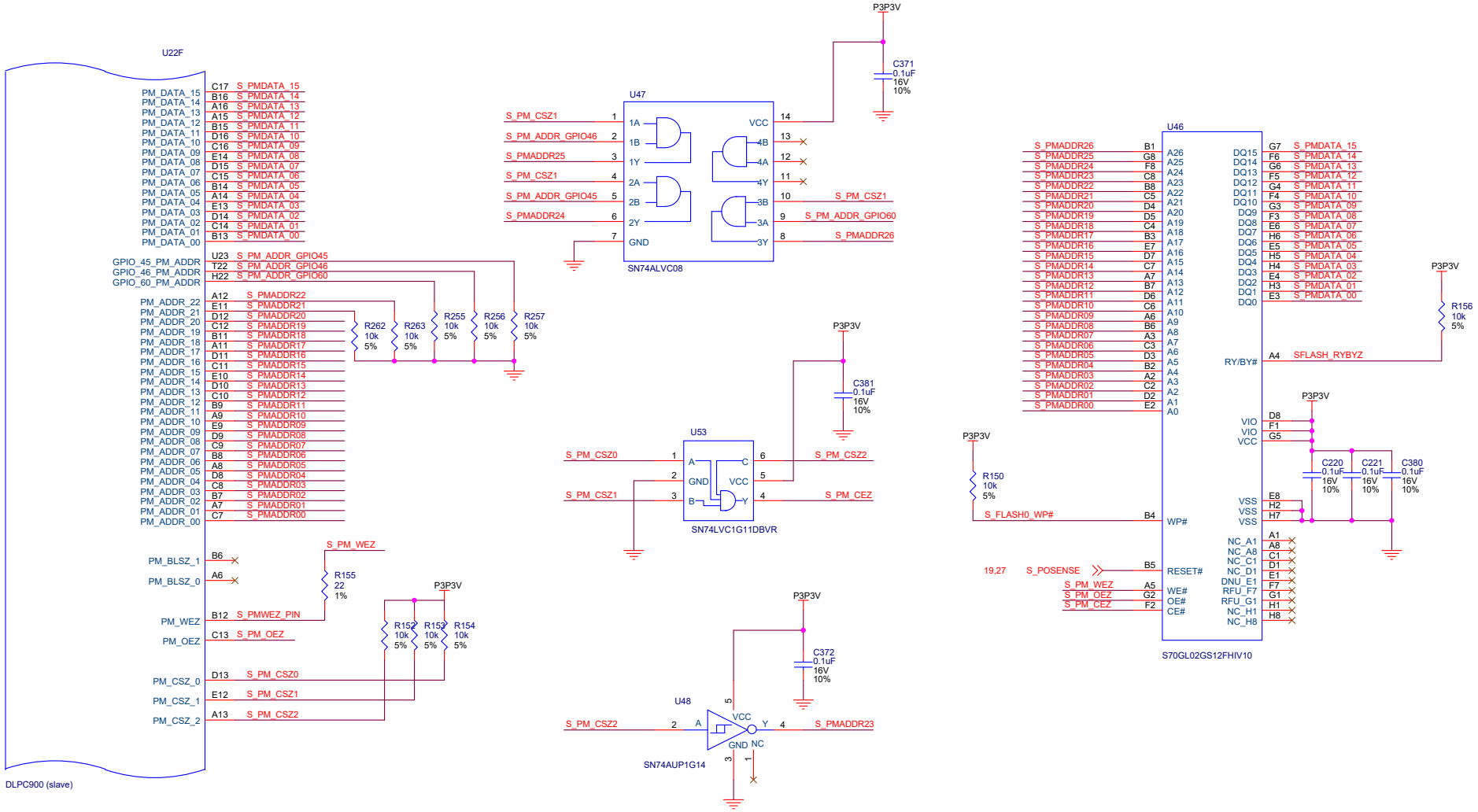






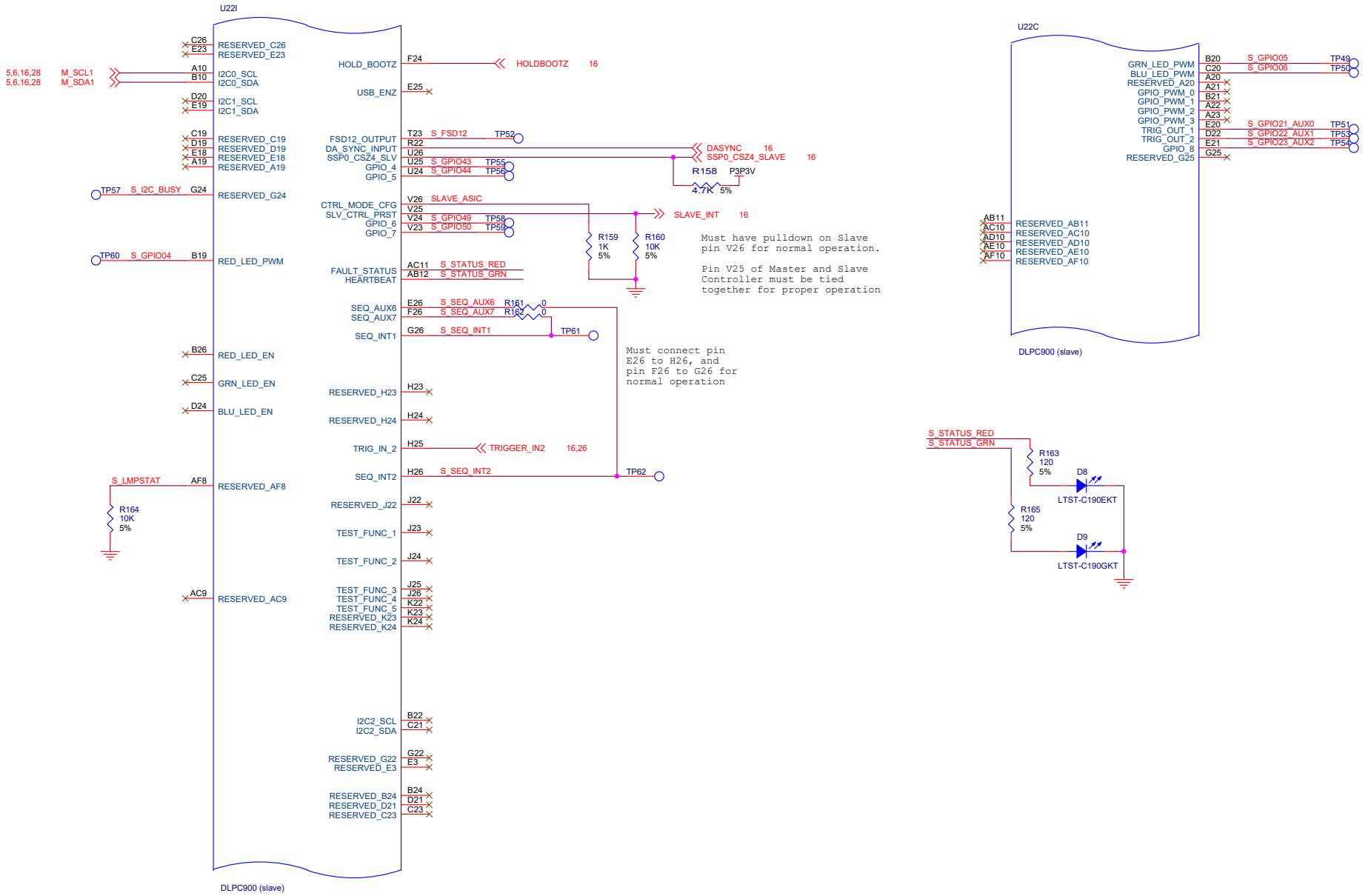
Slave Controller Reset, OSC, JTAG, UART0, SSP Port

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043	REV G
	ISSUE DATE		SCALE	SHEET 19 OF 29



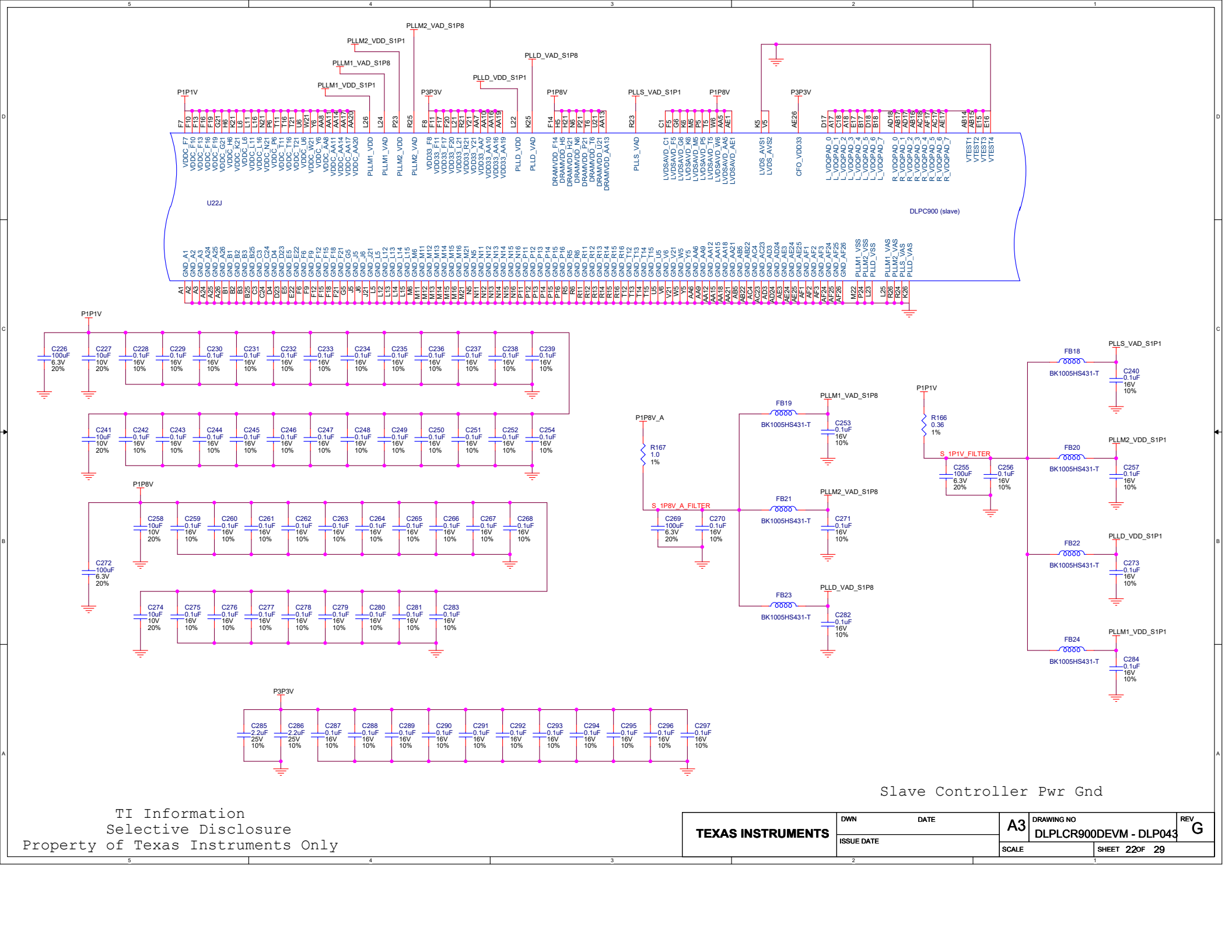
Slave Controller Flash Interface

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE			SCALE: SHEET 20 OF 29



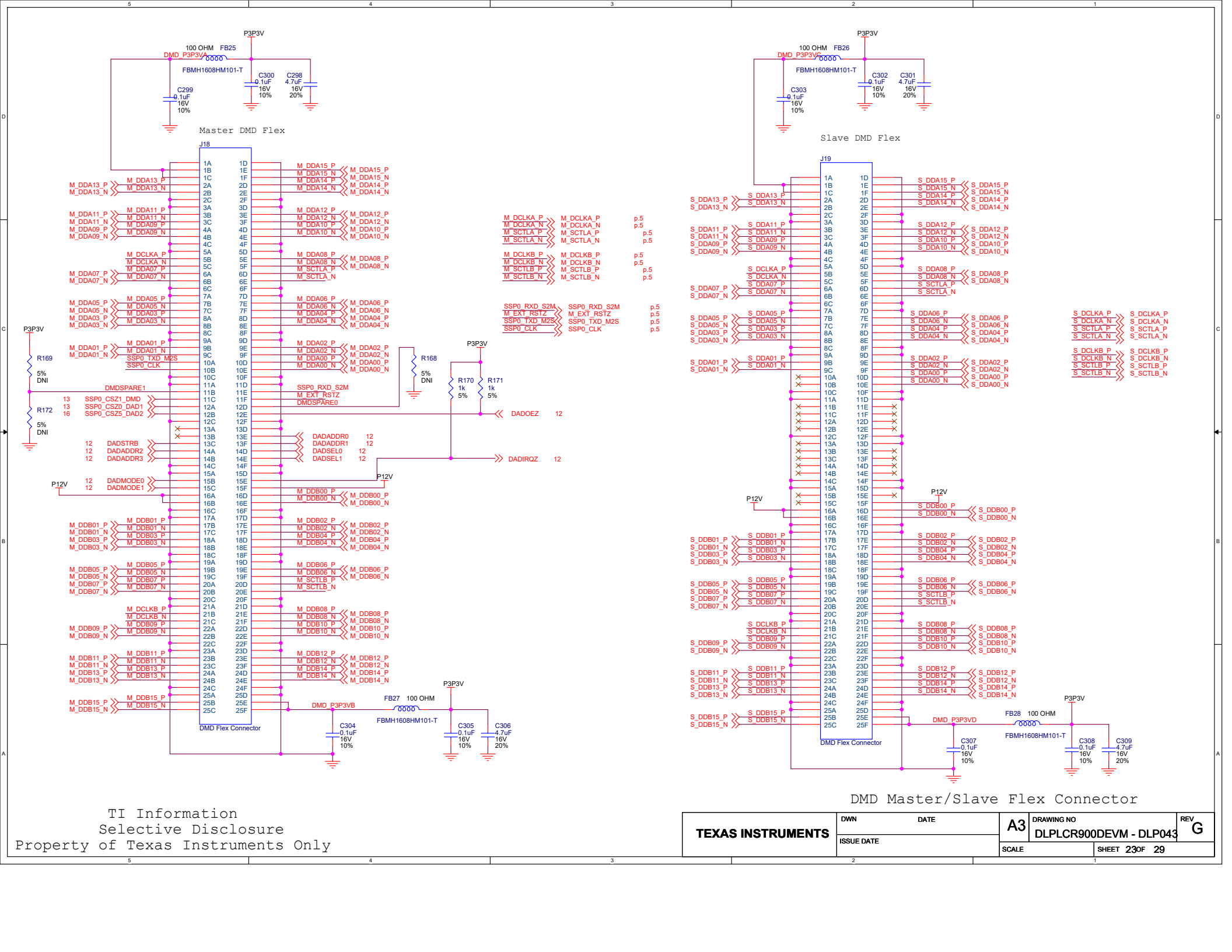
Slave Controller I2C, GPIOs

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE	SHEET 21 OF 29



Slave Controller Pwr Gnd

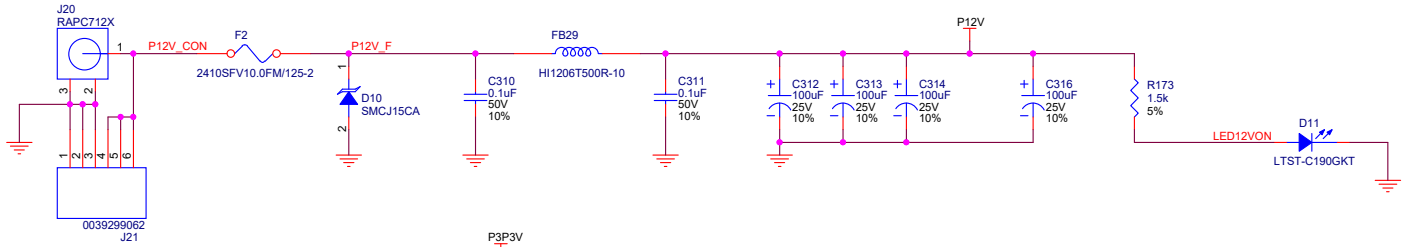
TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE		SCALE	SHEET 22 OF 29

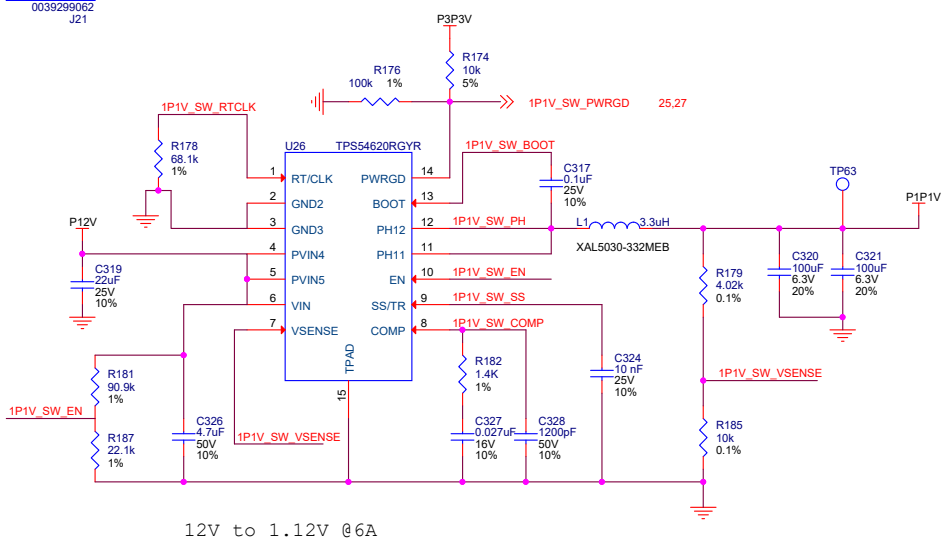


DMD Master/Slave Flex Connector

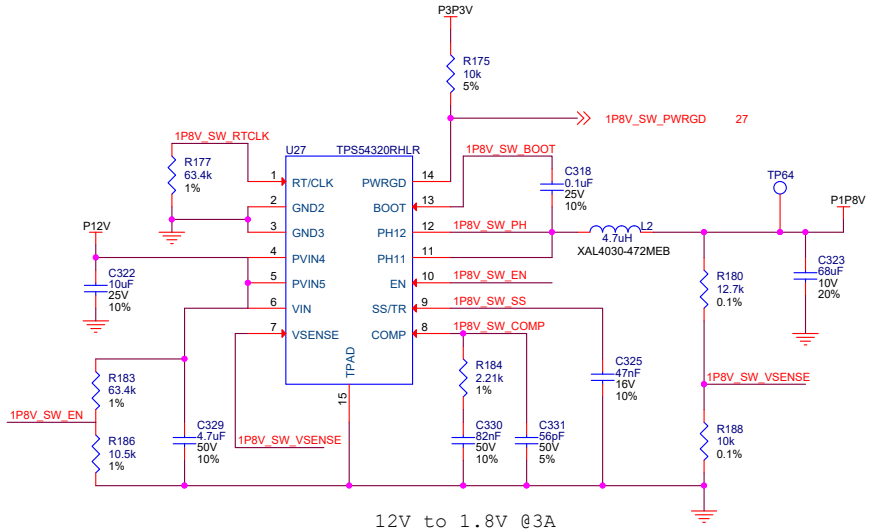
TI Information
Selective Disclosure
Property of Texas Instruments Only

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE	SHEET 23 OF 29

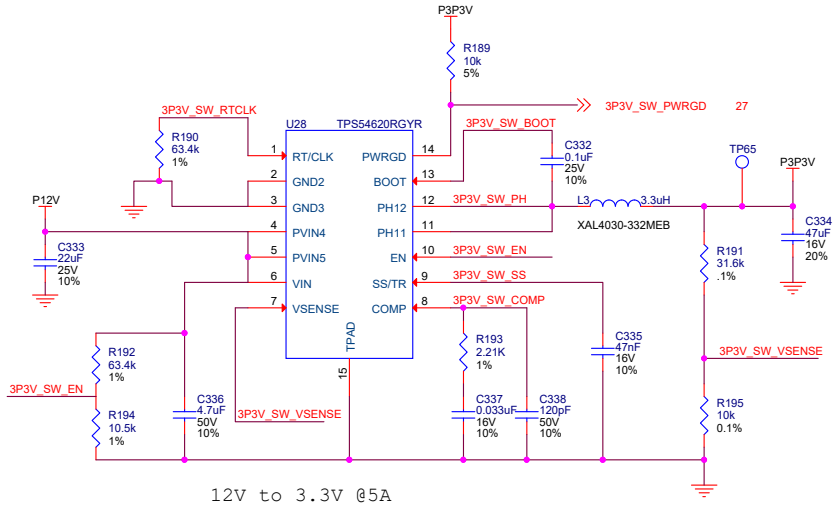




12V to 1.12V @6A
Switching Freq ~ 700KHz
Vstart/stop ~ 6.08V/5.57V
SS ~ 3.5ms



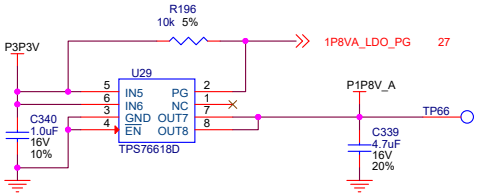
12V to 1.8V @3A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms



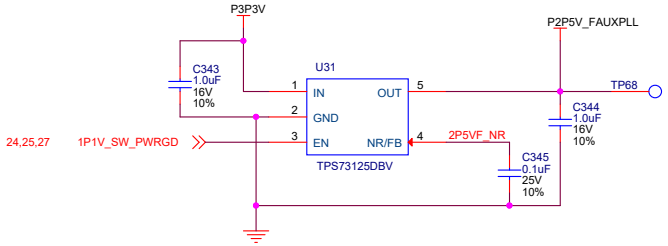
12V to 3.3V @5A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms

Power Generation 1.1V, 1.8V and 3.3V

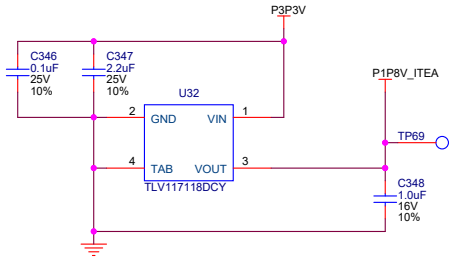
TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE		SCALE	SHEET 24 OF 29



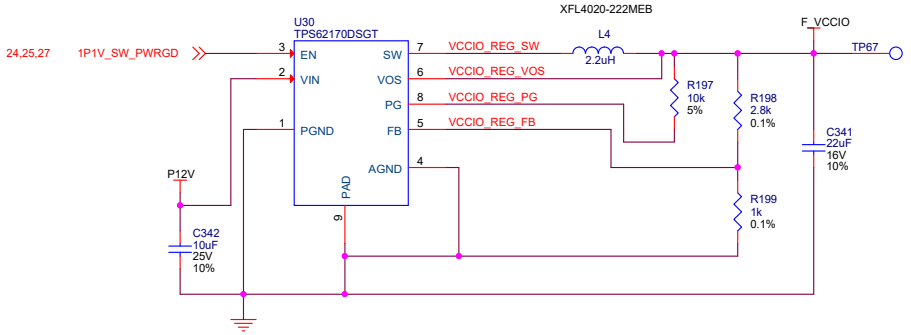
3.3V to 1.8V @250mA LDO
for controller 1.8V analog



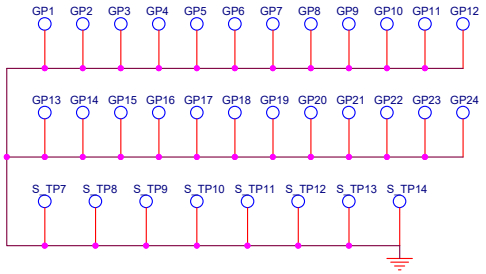
3.3V to 2.5V @150mA LDO
for FPGA 2.5V AUX/PLL power



3.3V to 1.8V @1A LDO
for HDMI Rx 1.8V analog



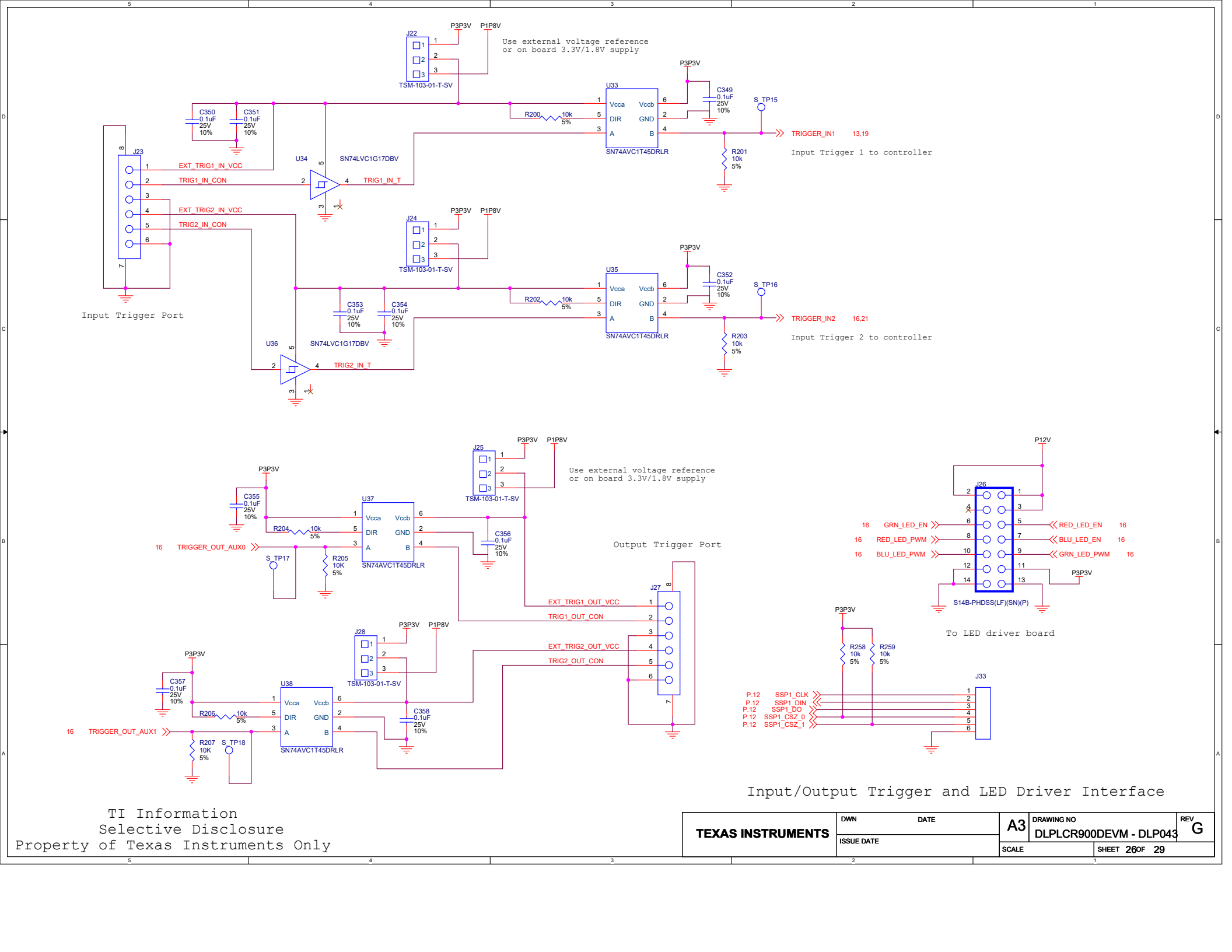
12V to 3V @500mA
for FPGA Vccio



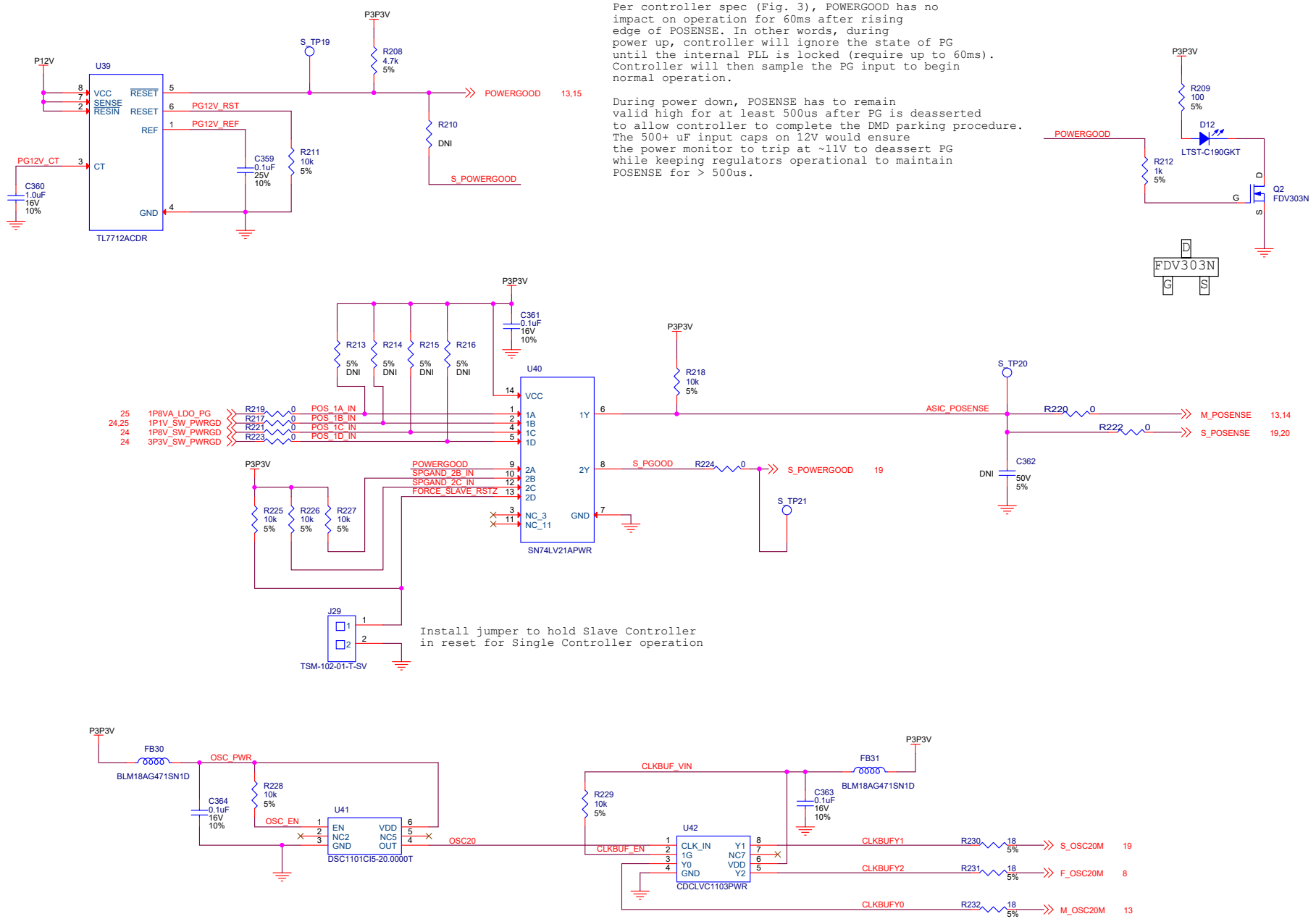
Distribute ground vias around PCB

Left/Right Split FPGA Power Generation VCCIO, 1.8V & 2.5V LDOs

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043
	ISSUE DATE		SCALE	REV: G
			SHEET 25 OF 29	

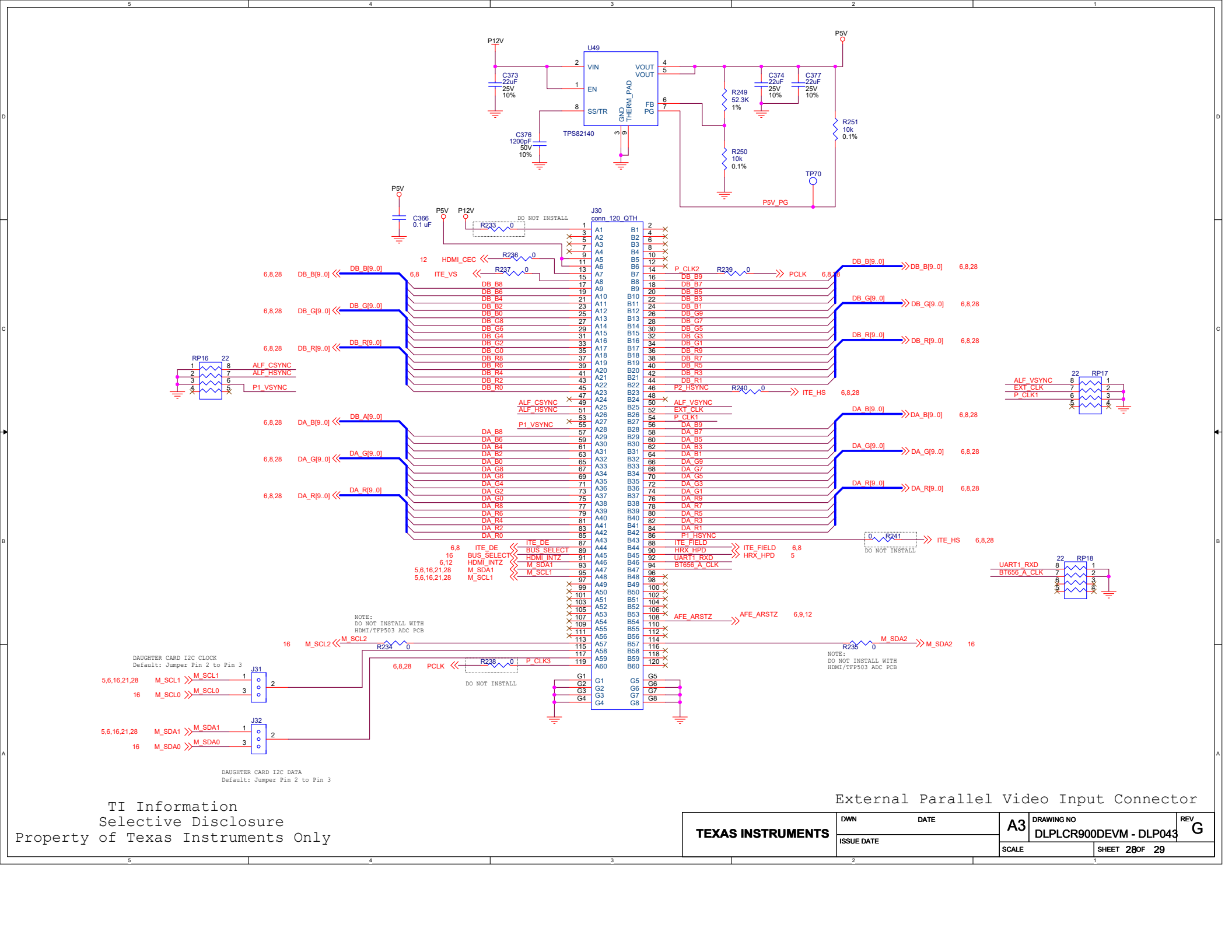


TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE		SCALE	SHEET 26 OF 29



Powergood, POSENSE, Conroller Clocks

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE	SHEET 27 OF 29



External Parallel Video Input Connector

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE		SCALE	SHEET 28 OF 29

REVISION HISTORY

Rev A

PAGES - ALL

- initial rev

Rev B

PAGE 27

- new part for C360

PAGE 26

- relocated S_TP17 and S_TP18

PAGE 24

- new part for R179
- removed C315, bulk cap not needed

PAGE 25

- new part for L4

PAGE 10

- new part for U12

Rev C

PAGES for U13 & U22

- update pin name to match datasheet

PAGE 15

- add comments for usage of R117 & R118

Rev D

Remove references to DLPC910

Rev E

Updated U7

Rev F

Added External Parallel Video Connector and 5V source

Sheet 12:
Added net HDMI_CEC to U13A,G23

Sheet 28:
Inserted Parallel Video Connector as Sheet 28. Revisions page moved to Sheet 29.
Added U49
Added J30, J31, J32
Added R233, R234, R235, R236, R237, R238, R239, R240, R241, R249, R250, R251
Added RP16, RP17, RP18
Added C366, C373, C374, C376, C377

Increased External Flash Memory to 128 MByte

Sheet 14:
Added net M_PM_ADDR_GPIO45 to U13F,U23
Added net M_PM_ADDR_GPIO46 to U13F,T22
Added net M_PM_ADDR_GPIO60 to U13F, H22
Added net BUS_SELECT to U13I,H23

Sheet 20:
Added net S_PM_ADDR_GPIO45 to U22F,U23
Added net S_PM_ADDR_GPIO45 to U22F,T22
Added net S_PM_ADDR_GPIO60 to U22F, H22

Sheet 14:
Removed U16, U17, U18
Removed R87, R88, R90, R96
Removed C140, C141, C142, C143
Added U43, U44, U45, U50
Added C367, C368, C378, C379
Added R252, R253, R254

Sheet 20:
Removed U23, U24, U25
Removed R148, R149, R151, R157
Removed C222, C223, C224, C225
Added U46, U47, U48, U53
Added C371, C372, C380, C381
Added R255, R256, R257

Addeded Connector for SSP1 Bus
Added J33, R258, R259

Rev G

Sheet 5
- Changed J2 footprint to SMT

Sheet 10
- U12 changed to Micron MT25QL128ABA1ESE-0SIT

Sheet 14
- Added R260 and R261
- Changed net connected to U44 pin 5 to M_PM_ADDR_GPIO45

Sheet 20
- Added R262 and R263
- Changed net connected to U48 pin 2 to S_PM_CSZ2

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043	REV G
	ISSUE DATE		SCALE	SHEET 29 OF 29