COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2137507: Initial Release	11/1/2013	NG
B	ECO 2140137: Updated to rev B	2/18/2014	NG
C	ECO 2141055: Updated to rev C	4/8/2014	NG
D	ECO 2142175: Updated to rev D	5/28/2014	NG
E	ECO 2144118: Updated to rev E	8/8/2014	NG
F	Updated to rev F	11/7/2019	DH
G	Updated to rev G	5/11/2020	DH

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P12V" represents connection to the +12V power plane.
2. The netname "P3P3V" represents connection to the +3.3V power plane.
3. The netname "P1P8V" represents connection to the +1.8V digital power plane.
4. The netname "P1P1V" represents connection to the +1.1V power plane.
5. The netname "P1P8V_ITEA" represents connection to the +1.8V ITE6535 analog supply power plane.
6. The netname "F_VCCIO" represents connection to the +3V FPGA Vccio power plane.
7. The netname "P2P5V_FAUXPLL" represents connection to the +2.5V FPGA aux/pll power plane.
8. The netname "P1P8V_A" represents connection to the +1.8V controller analog supply power plane.
9. The netname "GND" represents connection to the ground plane.
10. A "Z" suffix on a signal name indicates an active low signal.
11. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.

DLP®

TEXAS INSTRUMENTS

NOTE:

THIS IS A PRELIMINARY SCHEMATIC AND HAS NOT BEEN FULLY VALIDATED

		DWN A. NG DATE 8/8/2014	TEXAS INSTRUMENTS
		ENGR A. NG 8/8/2014	(C) COPYRIGHT 2018 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		SYST	TITLE: ESD, DLPLCR900DEVM DLP043
		PRJ L. Harvey 8/8/2014	
2513535	0314PO	QA	
NEXT ASSY	USED ON		A3 DRAWING NO 2513534 REV G
APPLICATION		SW Cadence 16.6	SCALE SHEET 1 of 29

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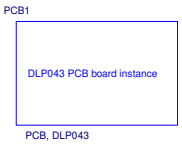

Boot_Hold Shunt
60900213421

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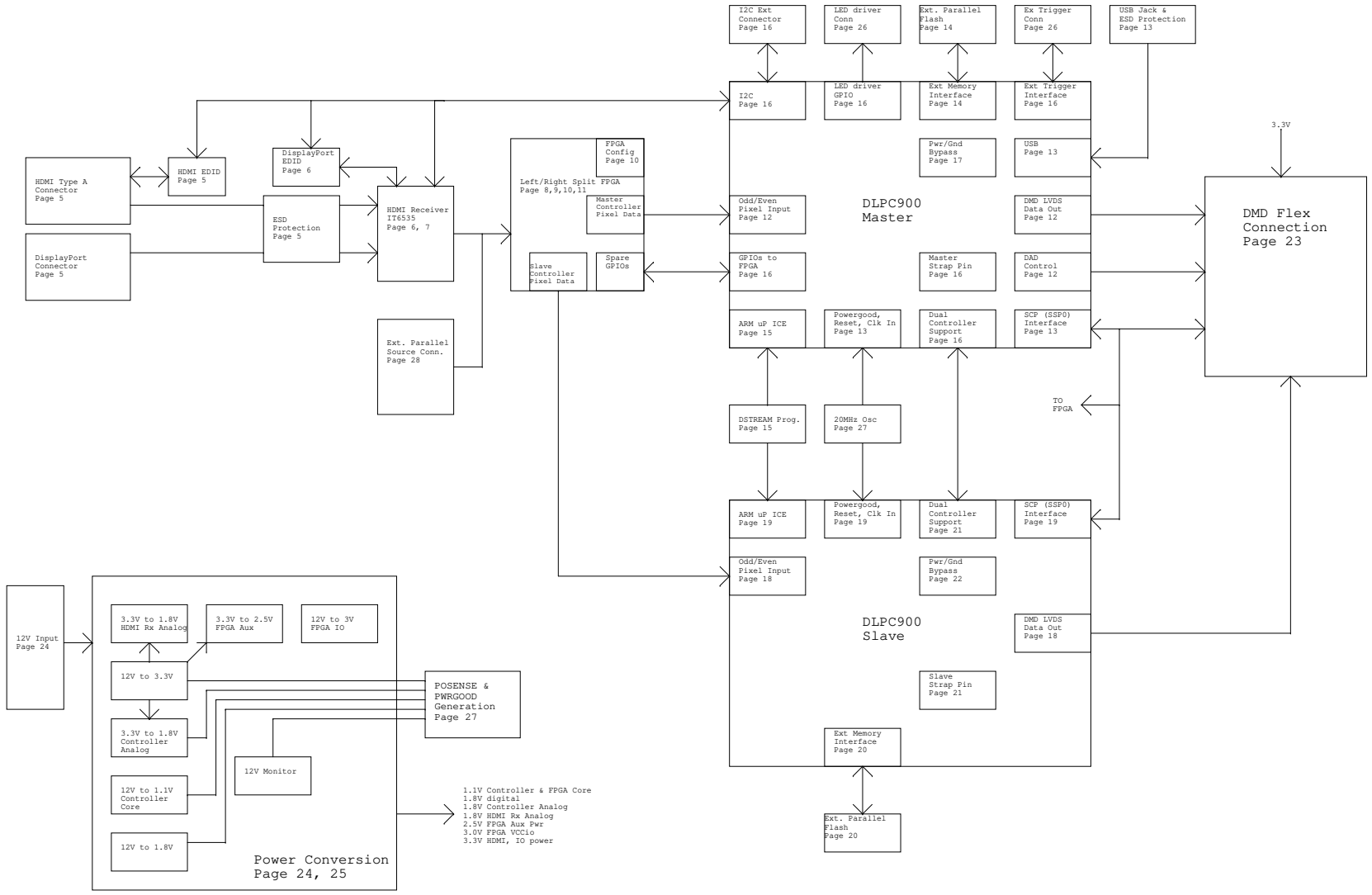

Block Diagram

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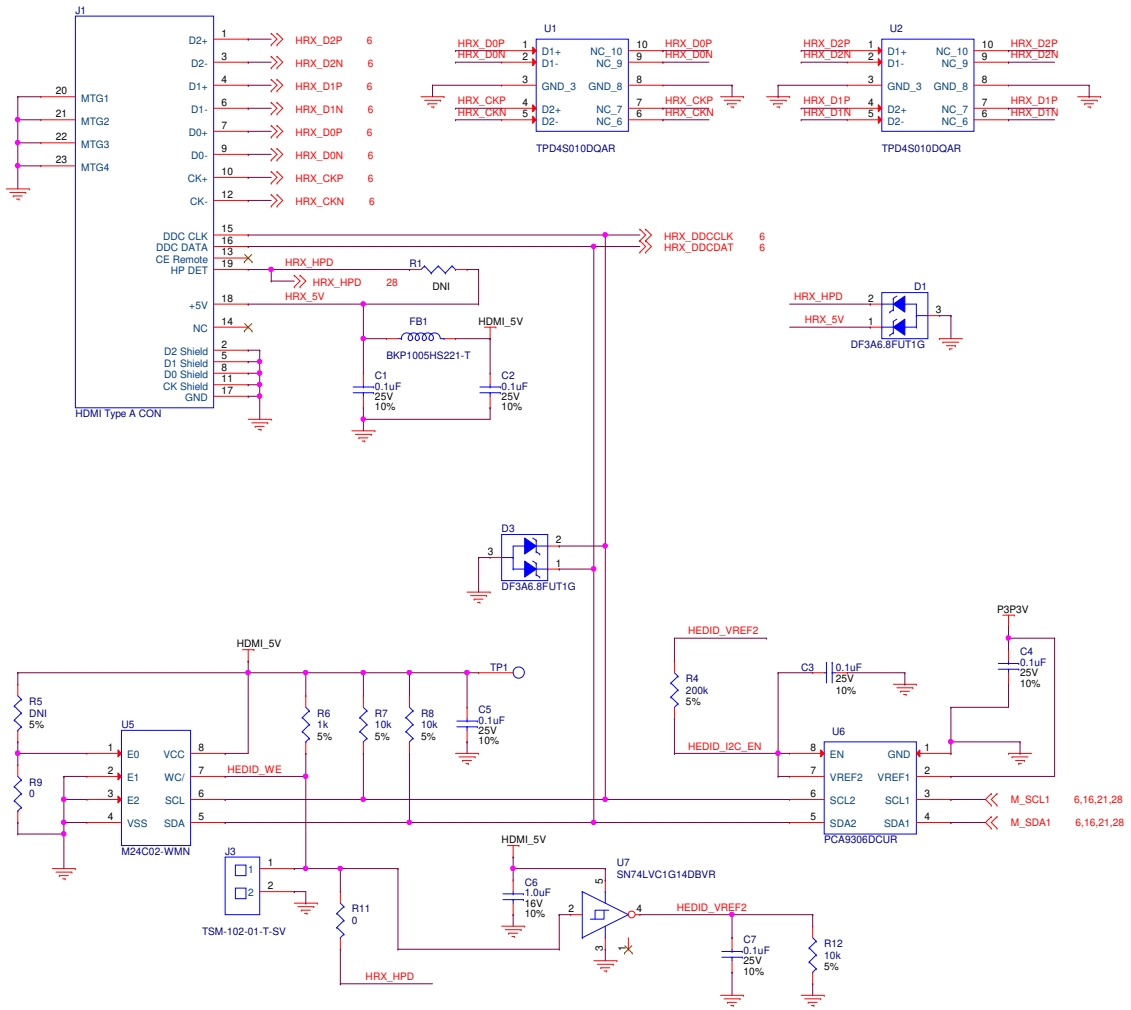

To program HDMI EDID
- install jumper to enable PROM write and disable hot plug detect
- connect HDMI cable to supply 5V
- use TI control program to update EDID

HDMI TypeA Rx Conn, ESD, and EDID

DisplayPort Rx Conn, ESD

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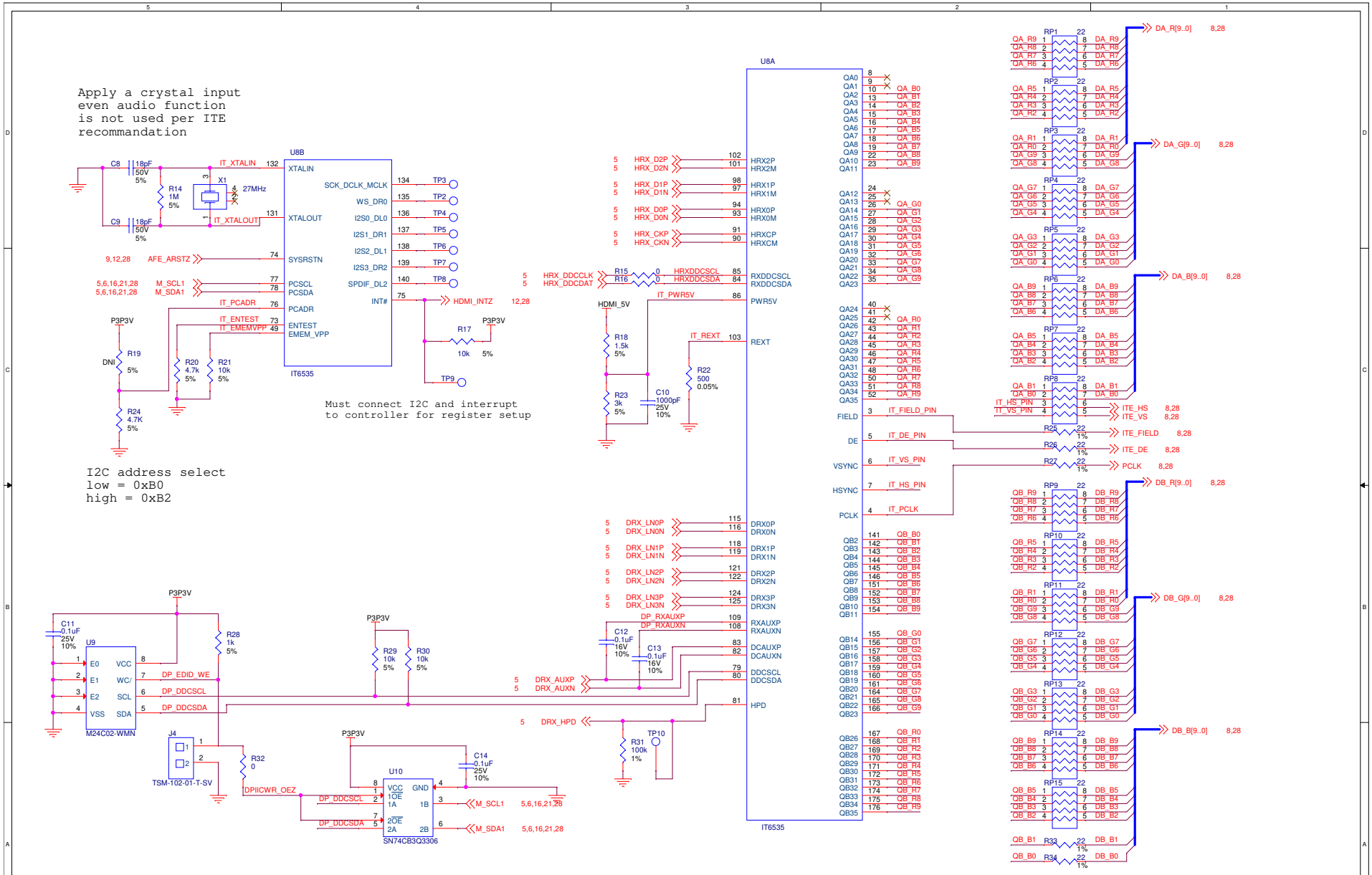
Apply a crystal input
even audio function
is not used per ITE
recommandation
U8B
IT6535
Must connect I2C and interrupt
to controller for register setup
I2C address select
low = 0xB0
high = 0xB2
U8A
IT6535
M24C02-WMN
TSM-102-01-T-SV
U10
SN74CB3Q3306
HDMI receiver input/output
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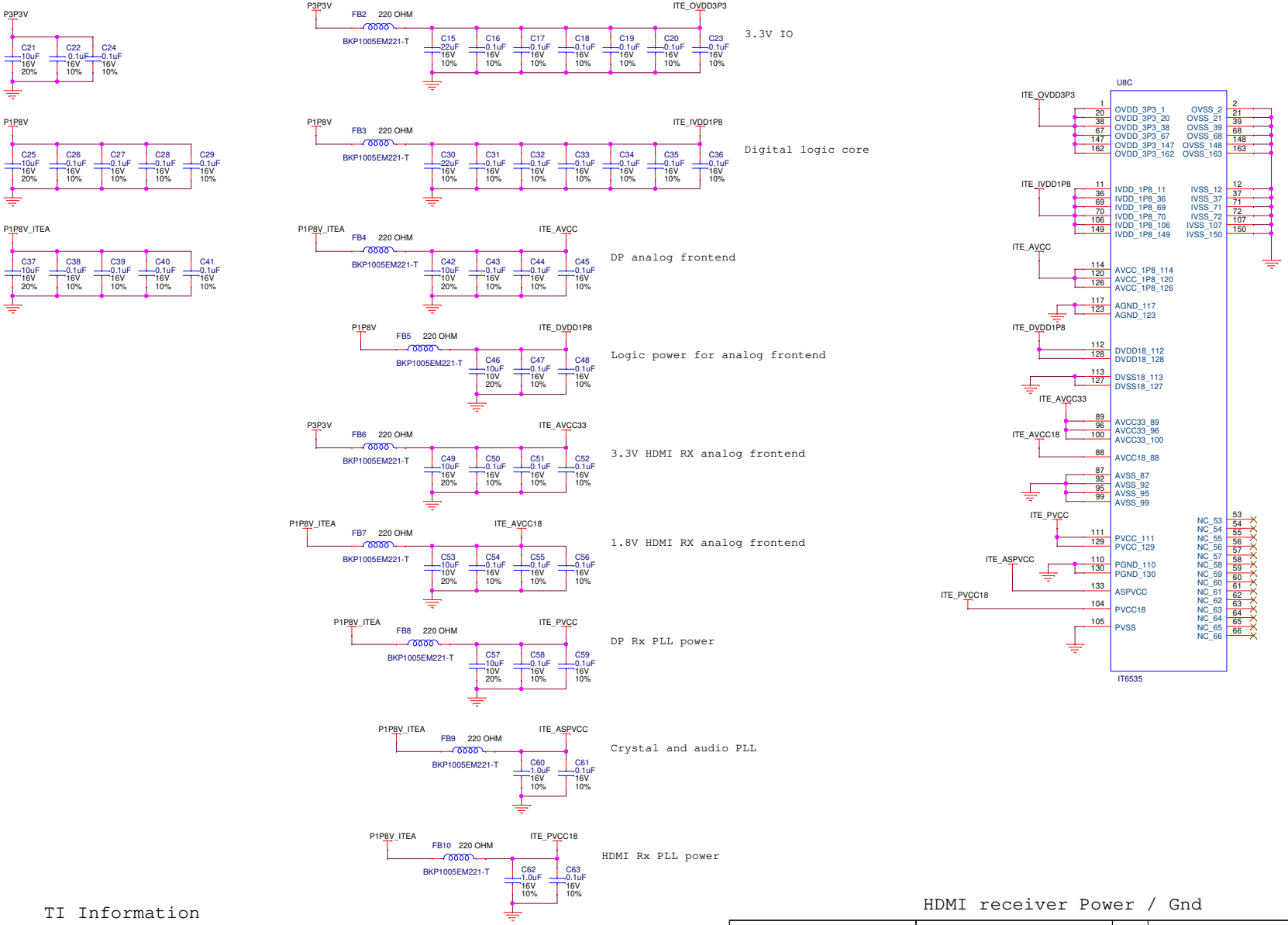

HDMI receiver Power / Gnd

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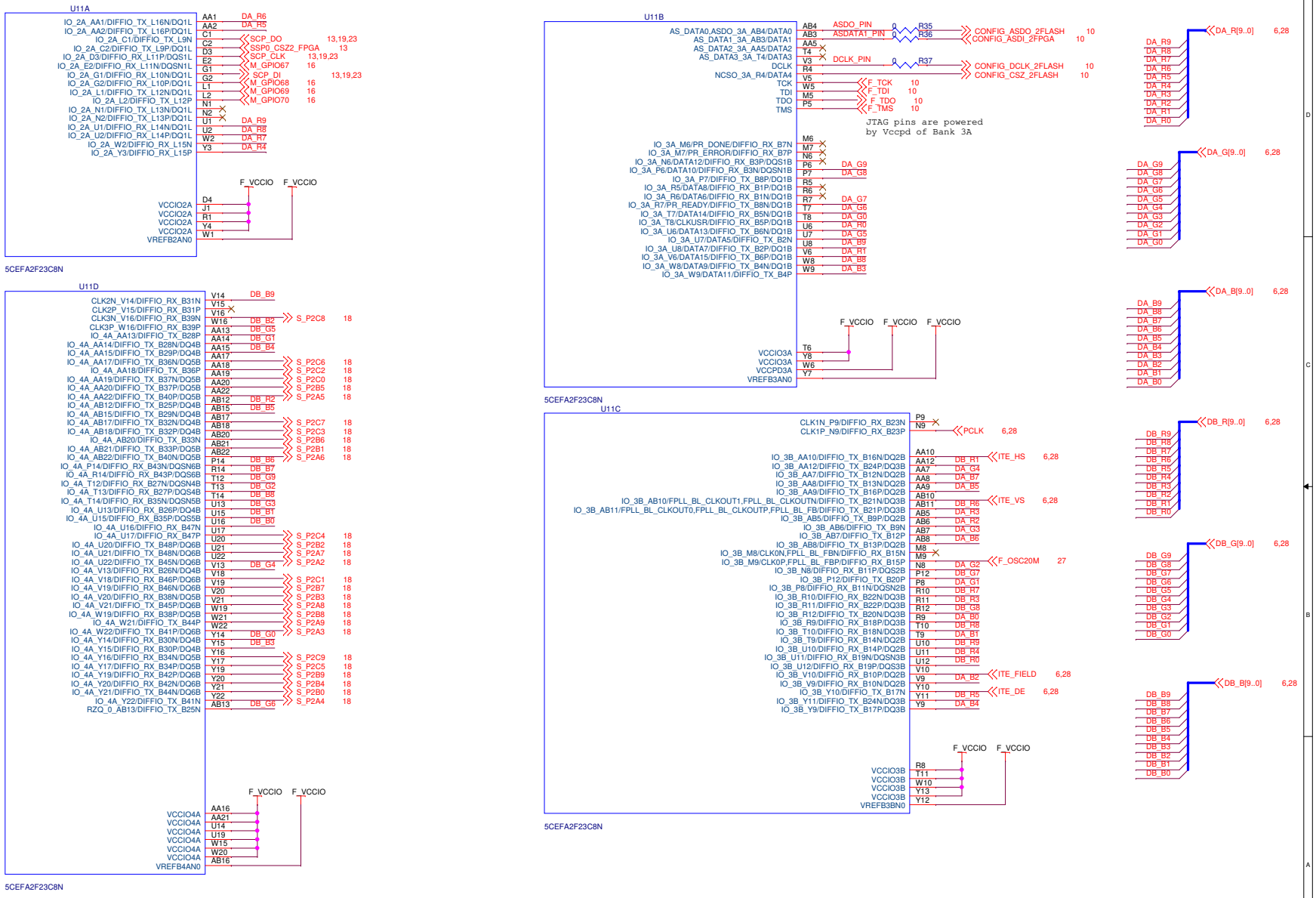

Left/Right Split FPGA Bank 2A, 3A, 3B, 4A

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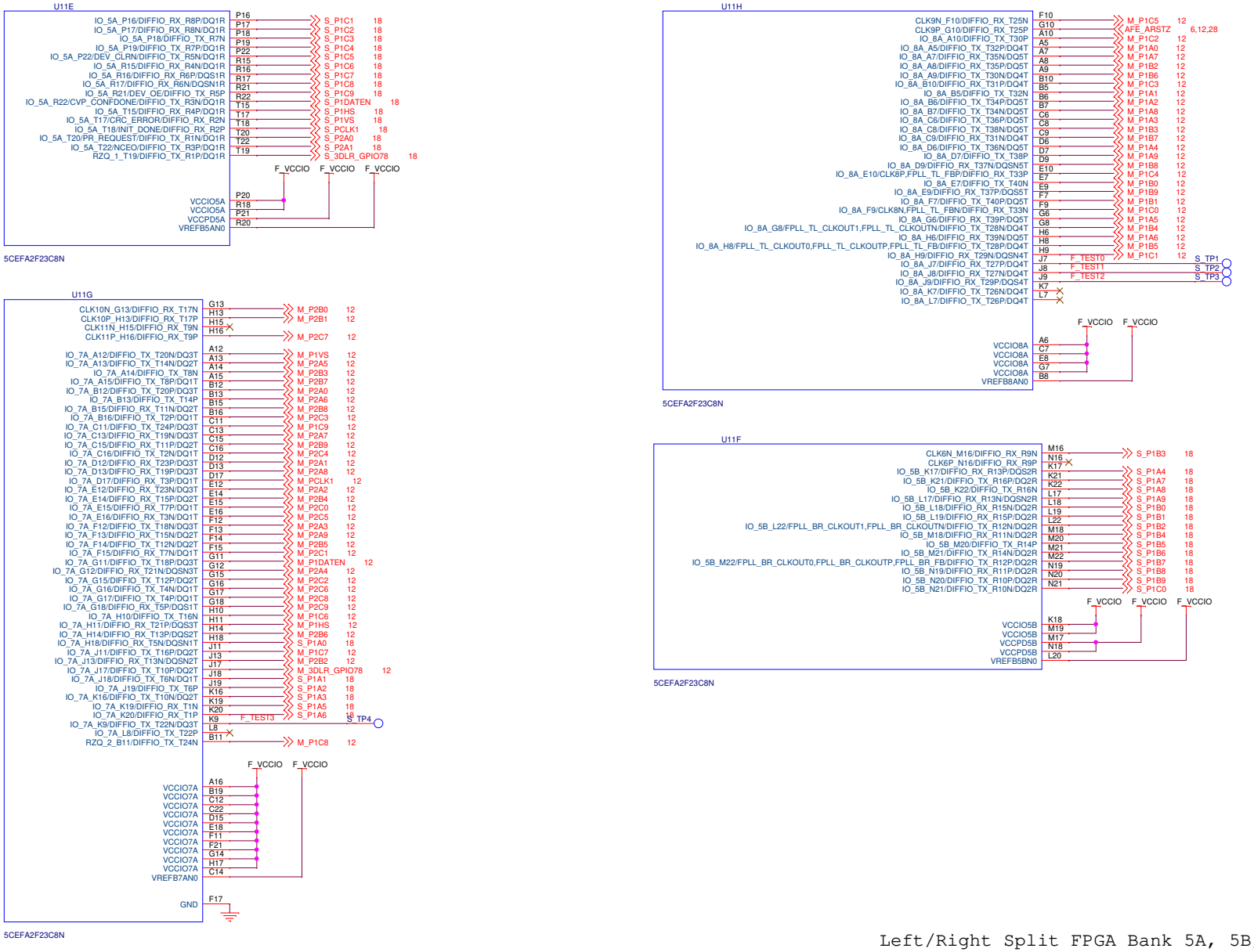
U11E
IO_5A_P16/DIFFIO_RX_R8P/DQ1R
IO_5A_P17/DIFFIO_RX_R8N/DQ1R
IO_5A_P18/DIFFIO_TX_R7N
IO_5A_P19/DIFFIO_TX_R7P/DQ1R
IO_5A_P22/DEV_CLRN/DIFFIO_TX_R5N/DQ1R
IO_5A_R15/DIFFIO_RX_R4N/DQ1R
IO_5A_R16/DIFFIO_RX_R6P/DQS1R
IO_5A_R17/DIFFIO_RX_R6N/DQSN1R
IO_5A_R21/DEV_OE/DIFFIO_TX_R5P
IO_5A_R22/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R
IO_5A_T15/DIFFIO_RX_R4P/DQ1R
IO_5A_T17/CRC_ERROR/DIFFIO_RX_R2N
IO_5A_T18/INIT_DONE/DIFFIO_RX_R2P
IO_5A_T20/PR_REQUEST/DIFFIO_TX_R1N/DQ1R
IO_5A_T22/NCEO/DIFFIO_TX_R3P/DQ1R
RZQ_1_T19/DIFFIO_TX_R1P/DQ1R
P16
P17
P18
P19
P22
R15
R16
R17
R21
R22
T15
T17
T18
T20
T22
T19
S_P1C1 18
S_P1C2 18
S_P1C3 18
S_P1C4 18
S_P1C5 18
S_P1C6 18
S_P1C7 18
S_P1C8 18
S_P1C9 18
S_P1DATEN 18
S_P1HS 18
S_P1VS 18
S_PCLK1 18
S_P2A0 18
S_P2A1 18
S_3DLR_GPIO78 18
F_VCCIO F_VCCIO F_VCCIO
VCCIO5A
VCCIO5A
VCCPD5A
VREFB5AN0
P20
R18
P21
R20
5CEFA2F23C8N
U11G
CLK10N_G13/DIFFIO_RX_T17N
CLK10P_H13/DIFFIO_RX_T17P
CLK11N_H15/DIFFIO_RX_T9N
CLK11P_H16/DIFFIO_RX_T9P
IO_7A_A12/DIFFIO_TX_T20N/DQ3T
IO_7A_A13/DIFFIO_TX_T14N/DQ2T
IO_7A_A14/DIFFIO_TX_T8N
IO_7A_A15/DIFFIO_TX_T8P/DQ1T
IO_7A_B12/DIFFIO_TX_T20P/DQ3T
IO_7A_B13/DIFFIO_TX_T14P
IO_7A_B15/DIFFIO_RX_T11N/DQ2T
IO_7A_B16/DIFFIO_TX_T2P/DQ1T
IO_7A_C11/DIFFIO_TX_T24P/DQ3T
IO_7A_C13/DIFFIO_RX_T19N/DQ3T
IO_7A_C15/DIFFIO_RX_T11P/DQ2T
IO_7A_C16/DIFFIO_TX_T2N/DQ1T
IO_7A_D12/DIFFIO_RX_T23P/DQ3T
IO_7A_D13/DIFFIO_RX_T19P/DQ3T
IO_7A_D17/DIFFIO_RX_T3P/DQ1T
IO_7A_E12/DIFFIO_RX_T23N/DQ3T
IO_7A_E14/DIFFIO_RX_T15P/DQ2T
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IO_7A_F13/DIFFIO_RX_T15N/DQ2T
IO_7A_F14/DIFFIO_TX_T12N/DQ2T
IO_7A_F15/DIFFIO_RX_T7N/DQ1T
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IO_7A_G12/DIFFIO_RX_T21N/DQSN3T
IO_7A_G15/DIFFIO_TX_T12P/DQ2T
IO_7A_G16/DIFFIO_TX_T4N/DQ1T
IO_7A_G17/DIFFIO_TX_T4P/DQ1T
IO_7A_G18/DIFFIO_RX_T5P/DQS1T
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IO_7A_J19/DIFFIO_TX_T6P
IO_7A_K16/DIFFIO_TX_T10N/DQ2T
IO_7A_K19/DIFFIO_RX_T1N
IO_7A_K20/DIFFIO_RX_T1P
IO_7A_K9/DIFFIO_TX_T22N/DQ3T
IO_7A_L8/DIFFIO_TX_T22P
RZQ_2_B11/DIFFIO_TX_T24N
G13
H13
H15
H16
A12
A13
A14
A15
B12
B13
B15
B16
C11
C13
C15
C16
D12
D13
D17
E12
E14
E15
E16
F12
F13
F14
F15
G11
G12
G15
G16
G17
G18
H10
H11
H14
H18
J11
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K19
K20
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VCCIO7A
VCCIO7A
VCCIO7A
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C22
D15
E18
F11
F21
G14
H17
C14
GND
F17
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IO_8A_B5/DIFFIO_TX_T32N
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A5
A7
A8
A9
B10
B5
B6
B7
C6
C8
C9
D6
D7
D9
E10
E7
E9
F7
F9
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H9
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J9
K7
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K21
K22
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L18
L19
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M21
M22
N19
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N21
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S_P1A9 18
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S_P1B1 18
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S_P1B6 18
S_P1B7 18
S_P1B8 18
S_P1B9 18
S_P1C0 18
F_VCCIO F_VCCIO F_VCCIO
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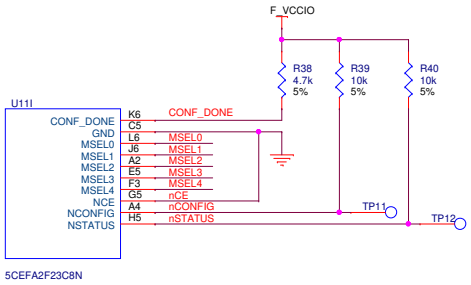
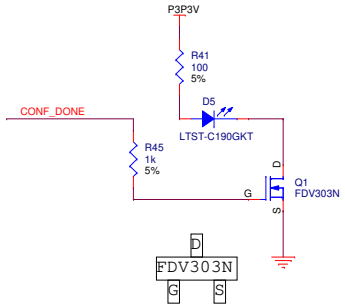
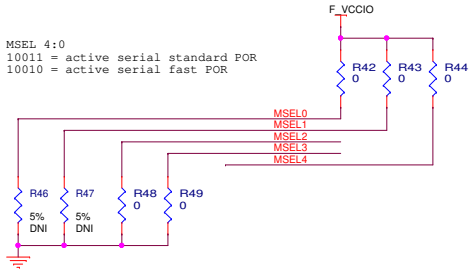
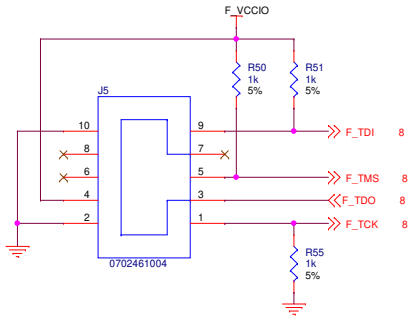
SHEET 9 OF 29

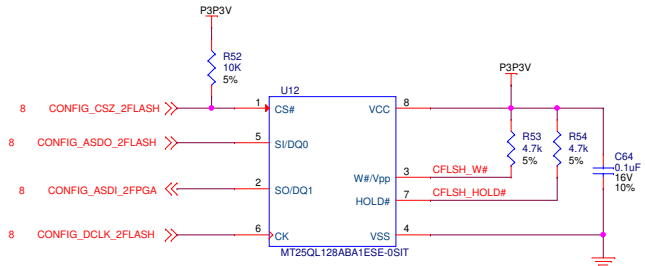








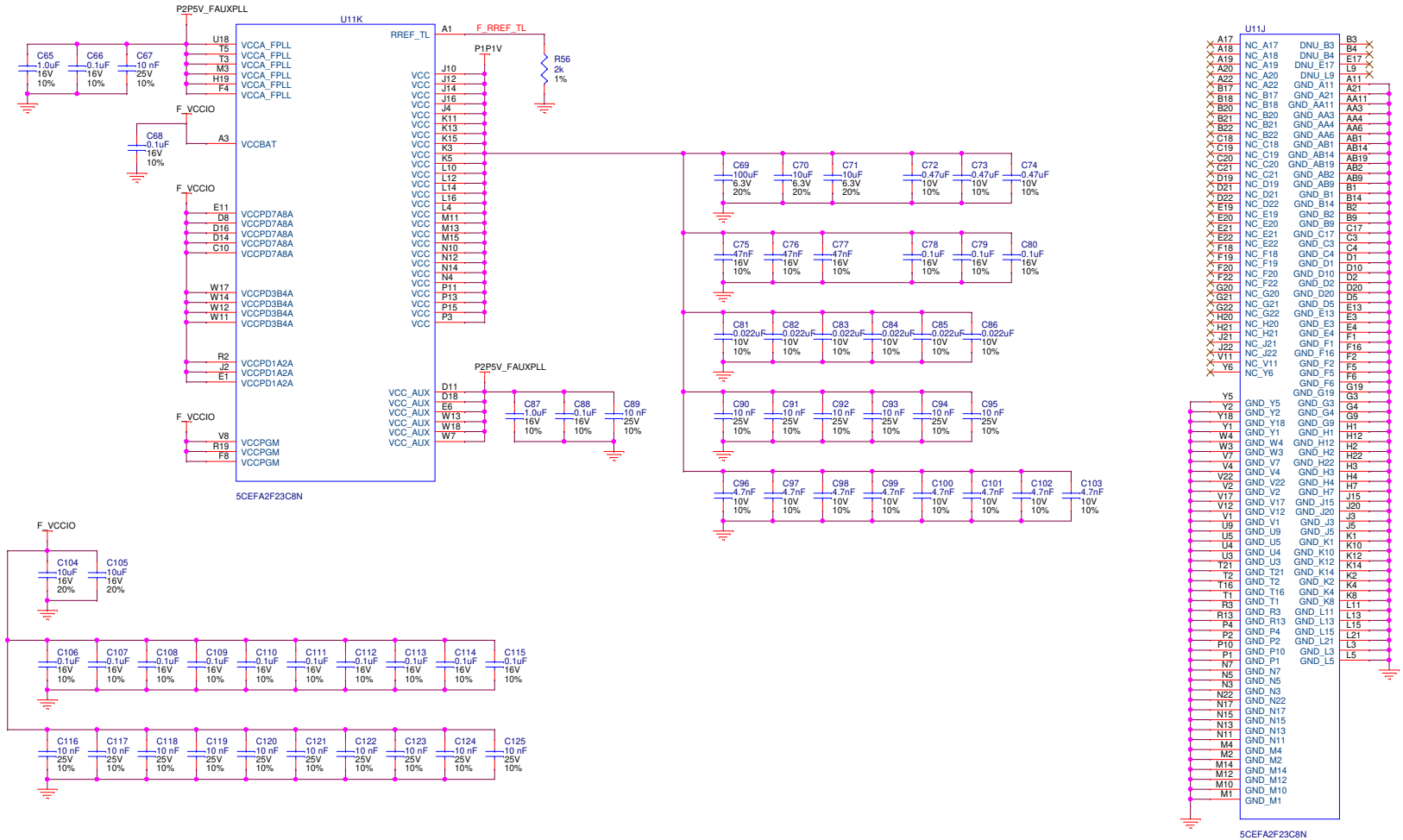
Altera's USB ByteBlaster Connector



Use Altera's "Serial loader" option to update flash
thru the FPGA JTAG port with Byteblaster cable

Left/Right Split FPGA Configuration

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE SHEET 10 OF 29



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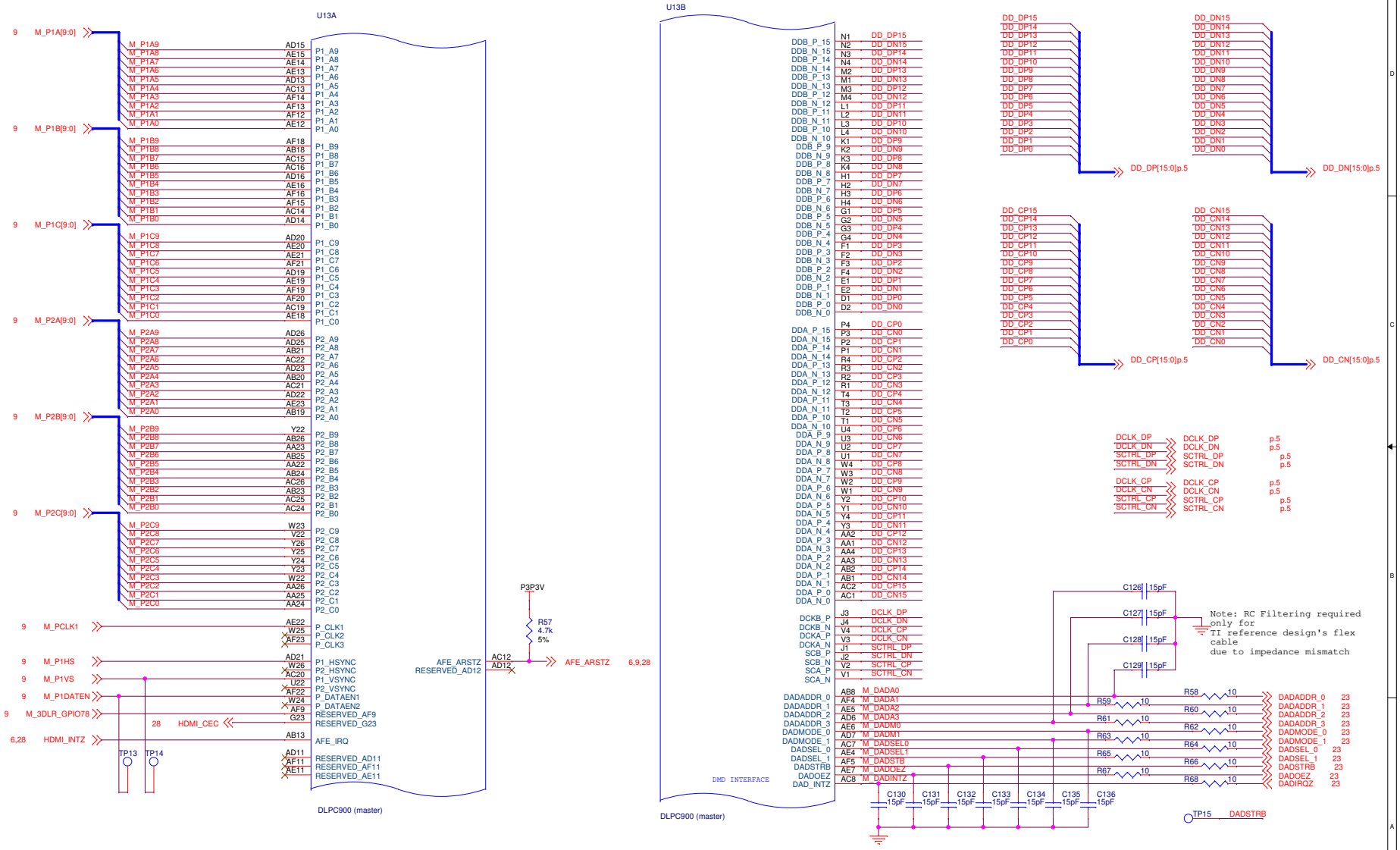
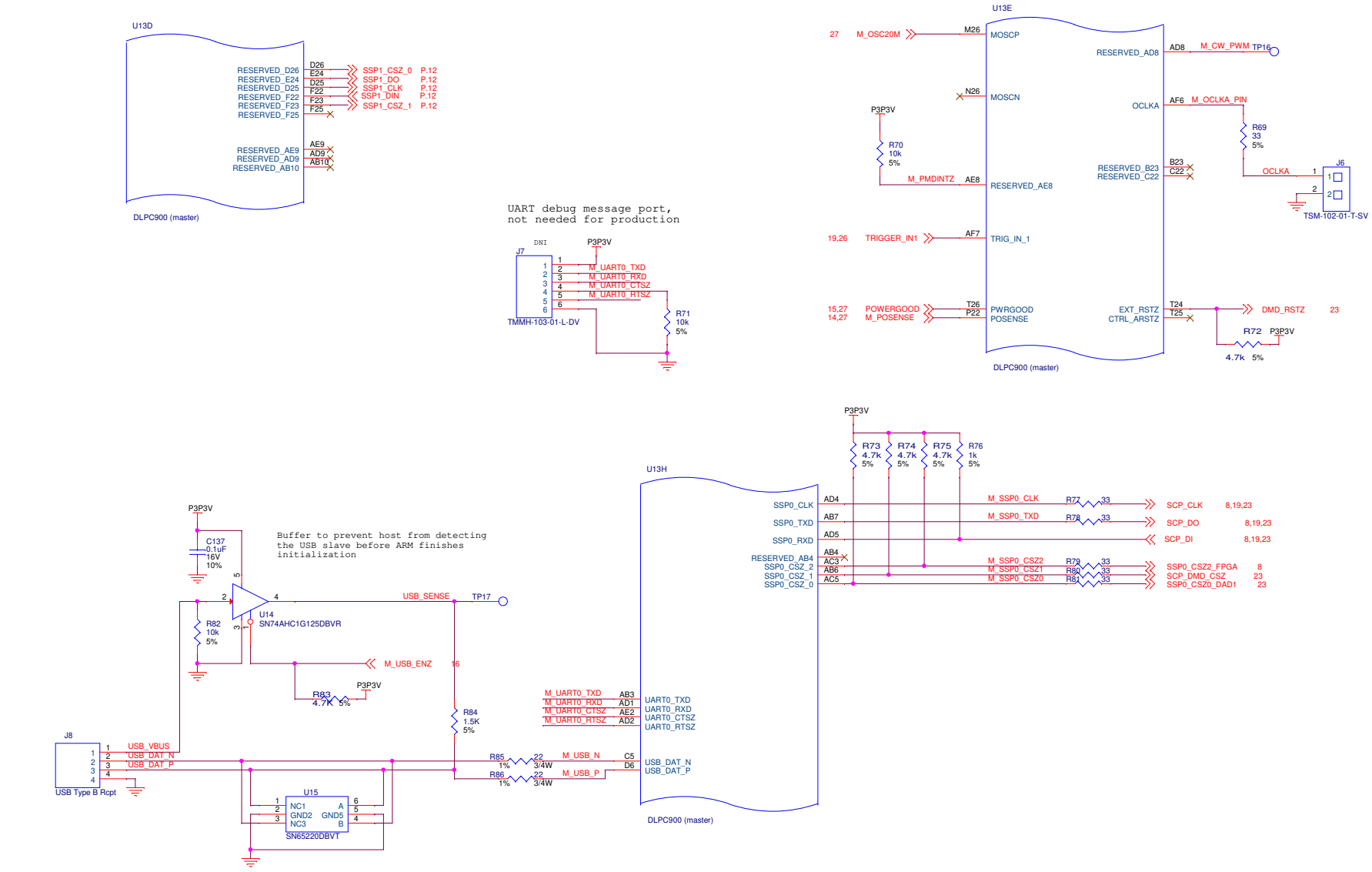
Left/Right Split FPGA Pwr/Gnd

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE	SHEET 11 OF 29



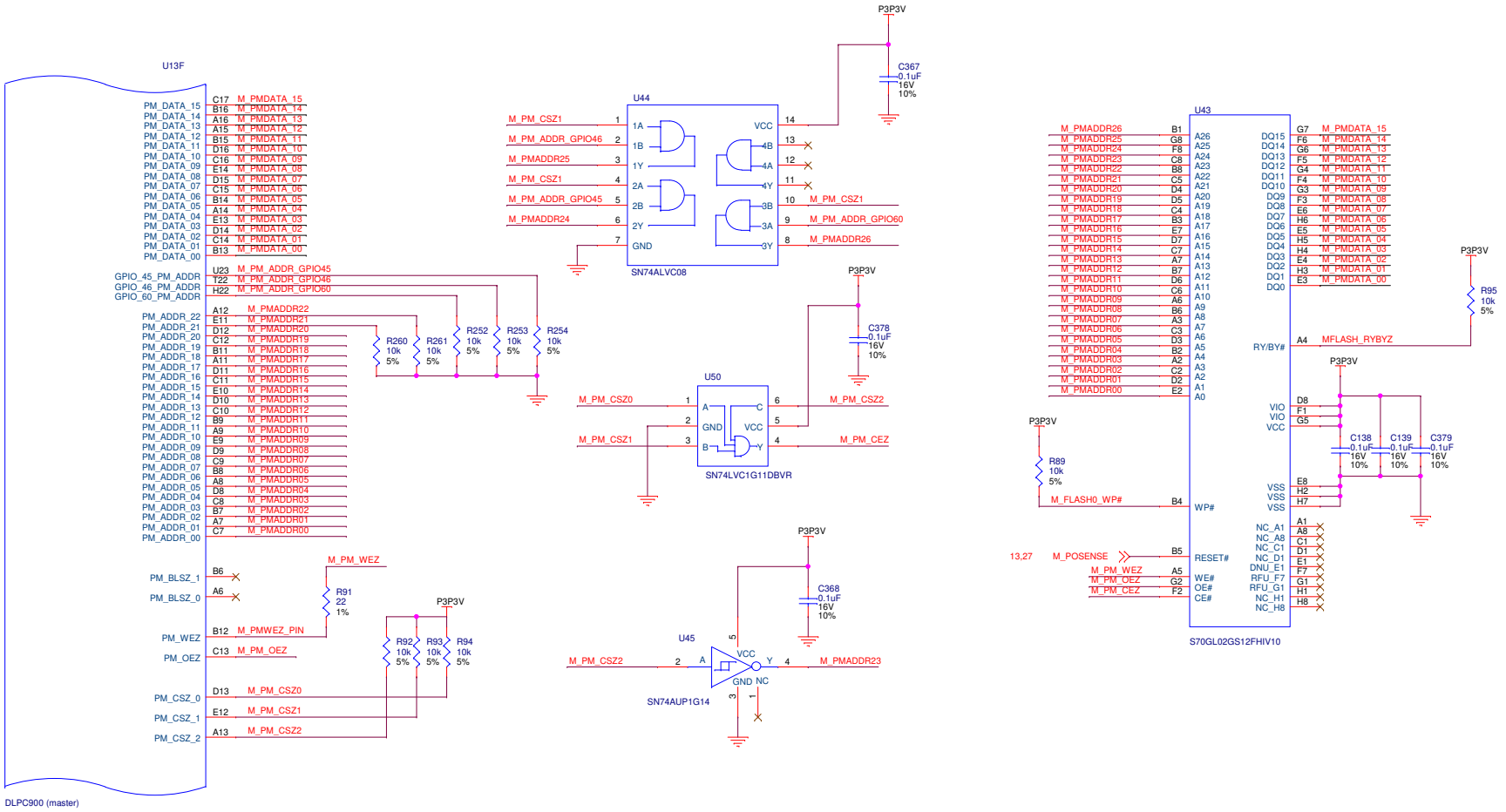
Master Controller Video Input, DMD & DAD Output

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043
	ISSUE DATE		SCALE	SHEET 12 OF 29
				REV G



Master Controller SSP0, UART0, USB, Reset, OSC

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043	REV G
	ISSUE DATE		SCALE	SHEET 13 OF 29



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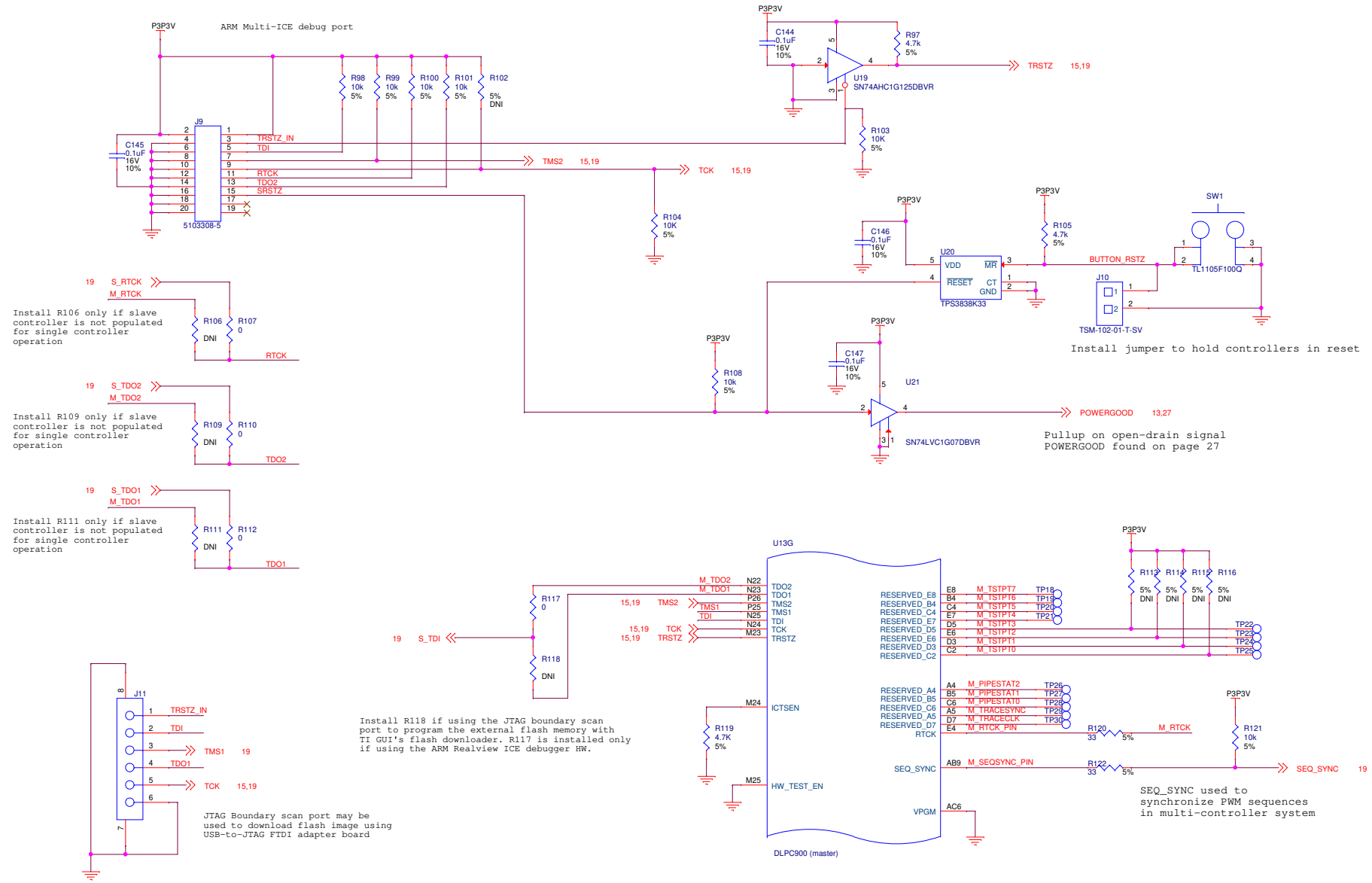
Master Controller Flash Interface

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE		SCALE	SHEET 14 OF 29



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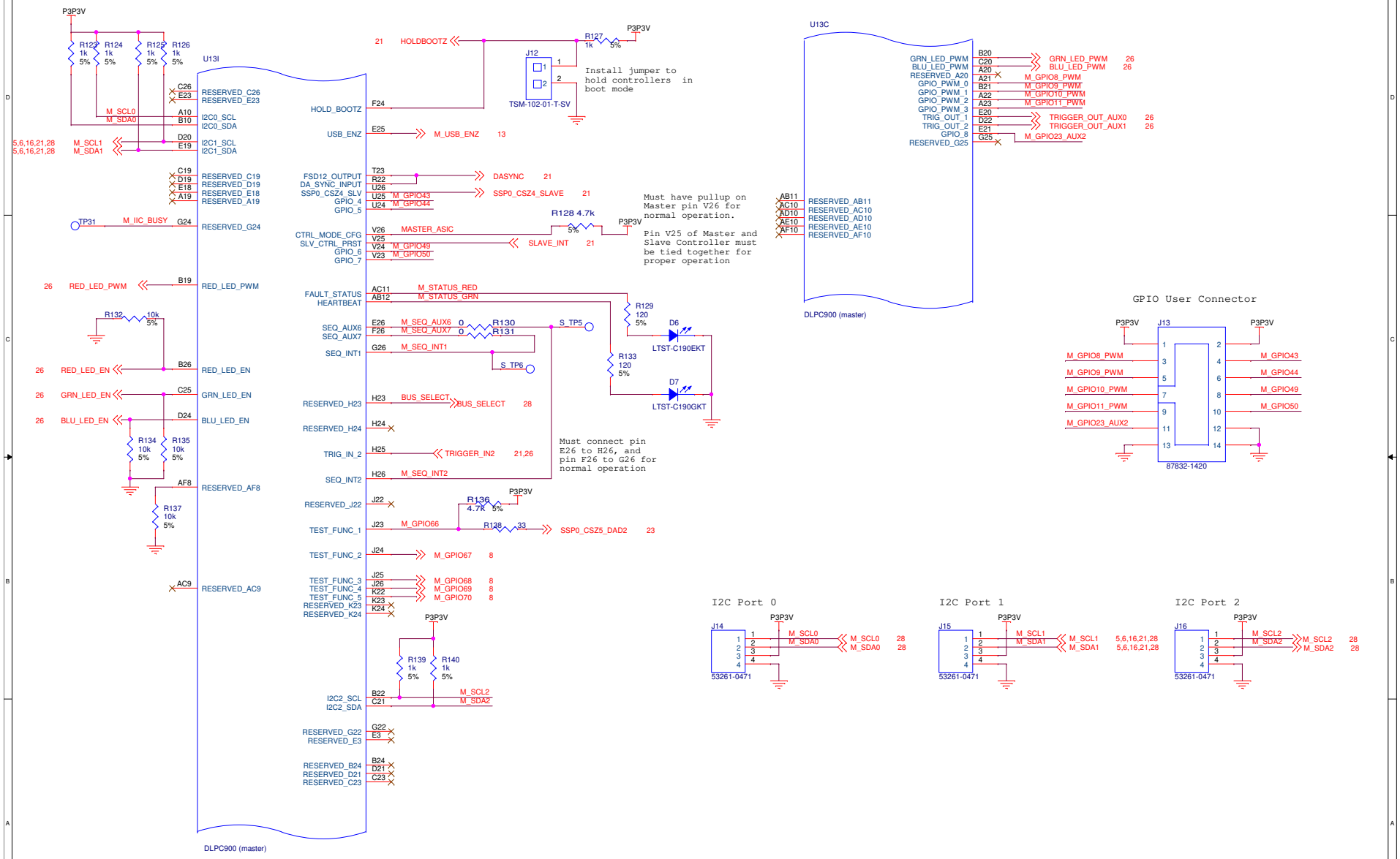
Master Controller Multi-ICE Port

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE SHEET 15 OF 29



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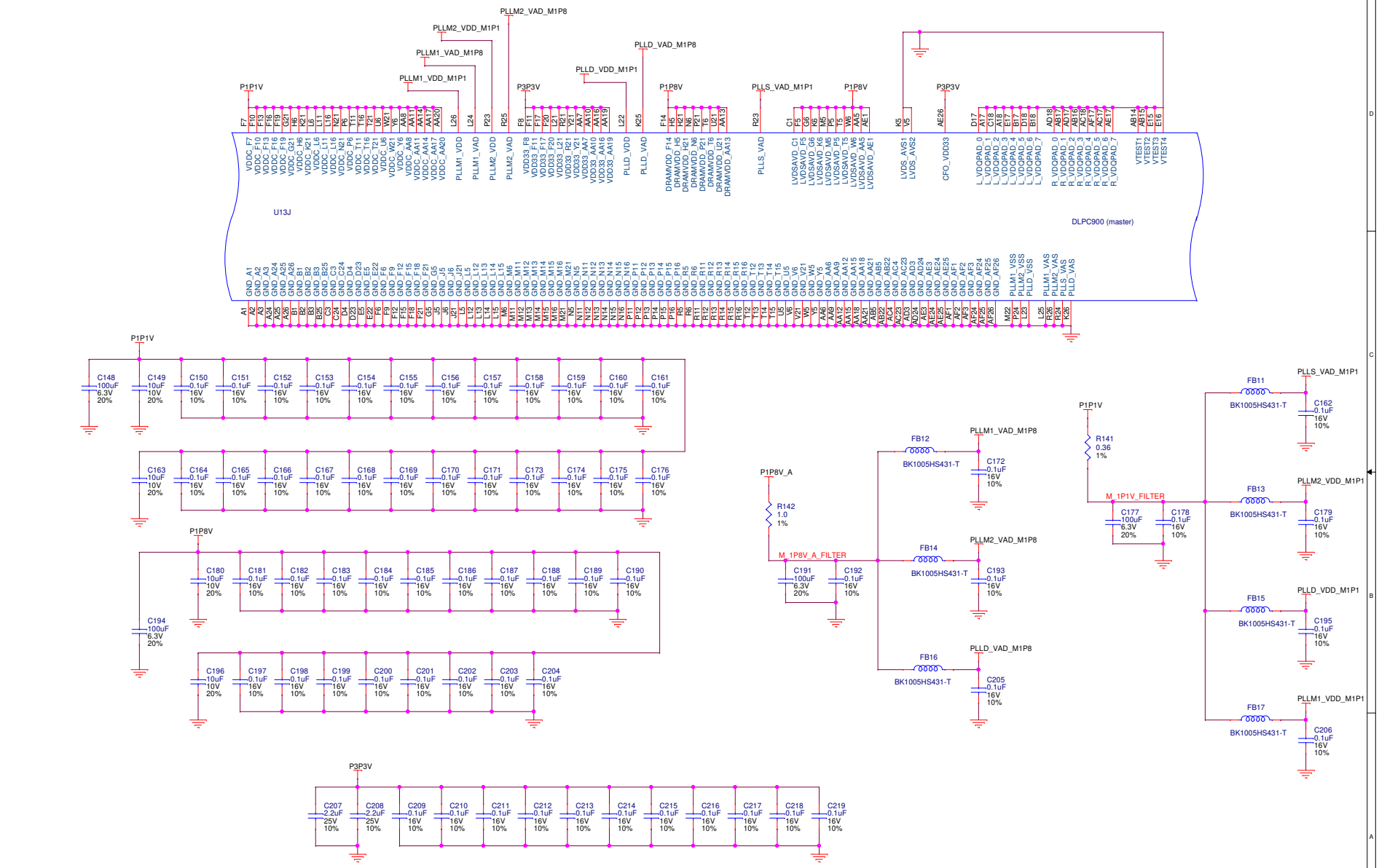
Master Controller I2C, LED driver interface, In/Out Triggers and GPIOs

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE		SCALE	SHEET 16 OF 29



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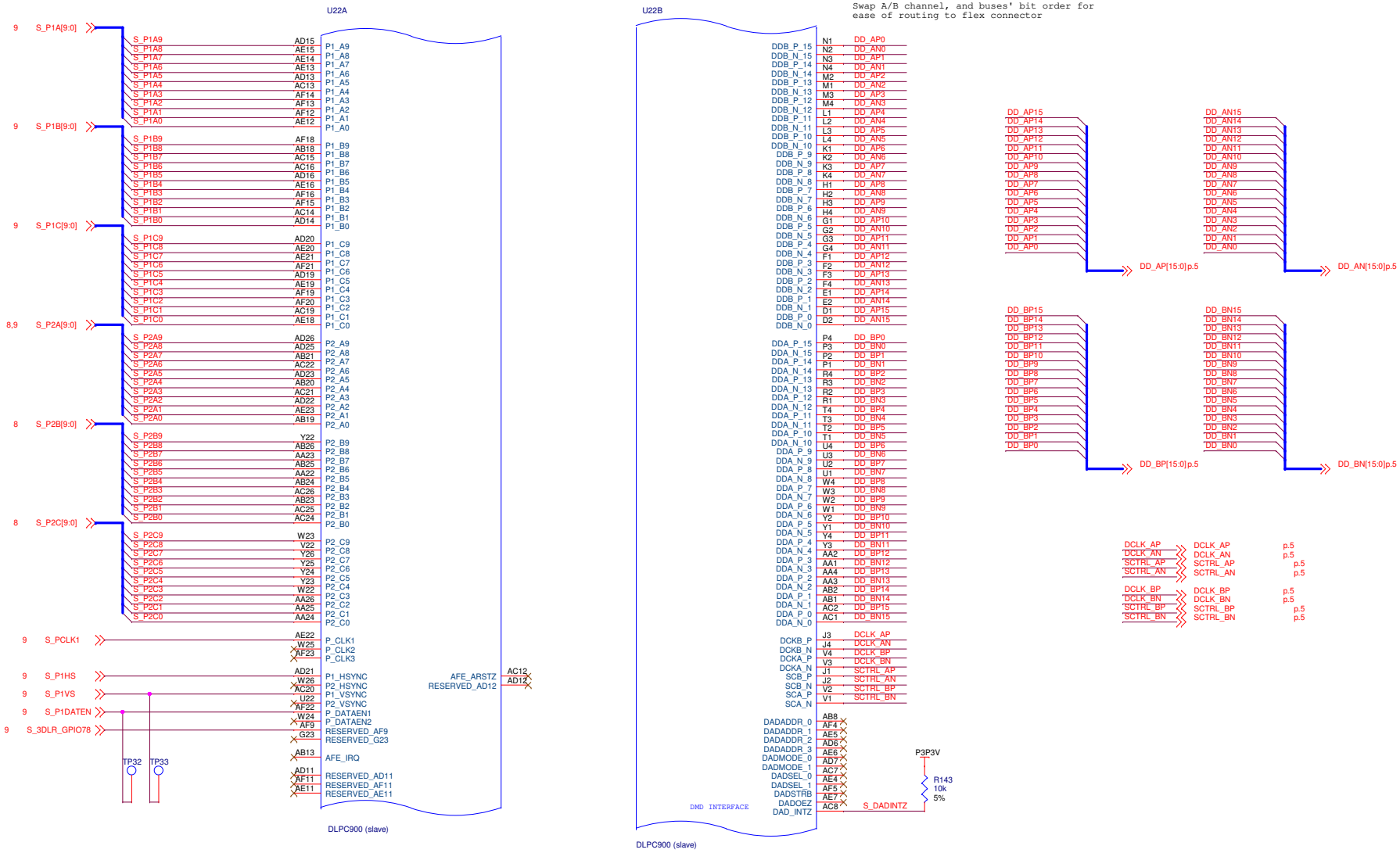
Master Controller Pwr Gnd

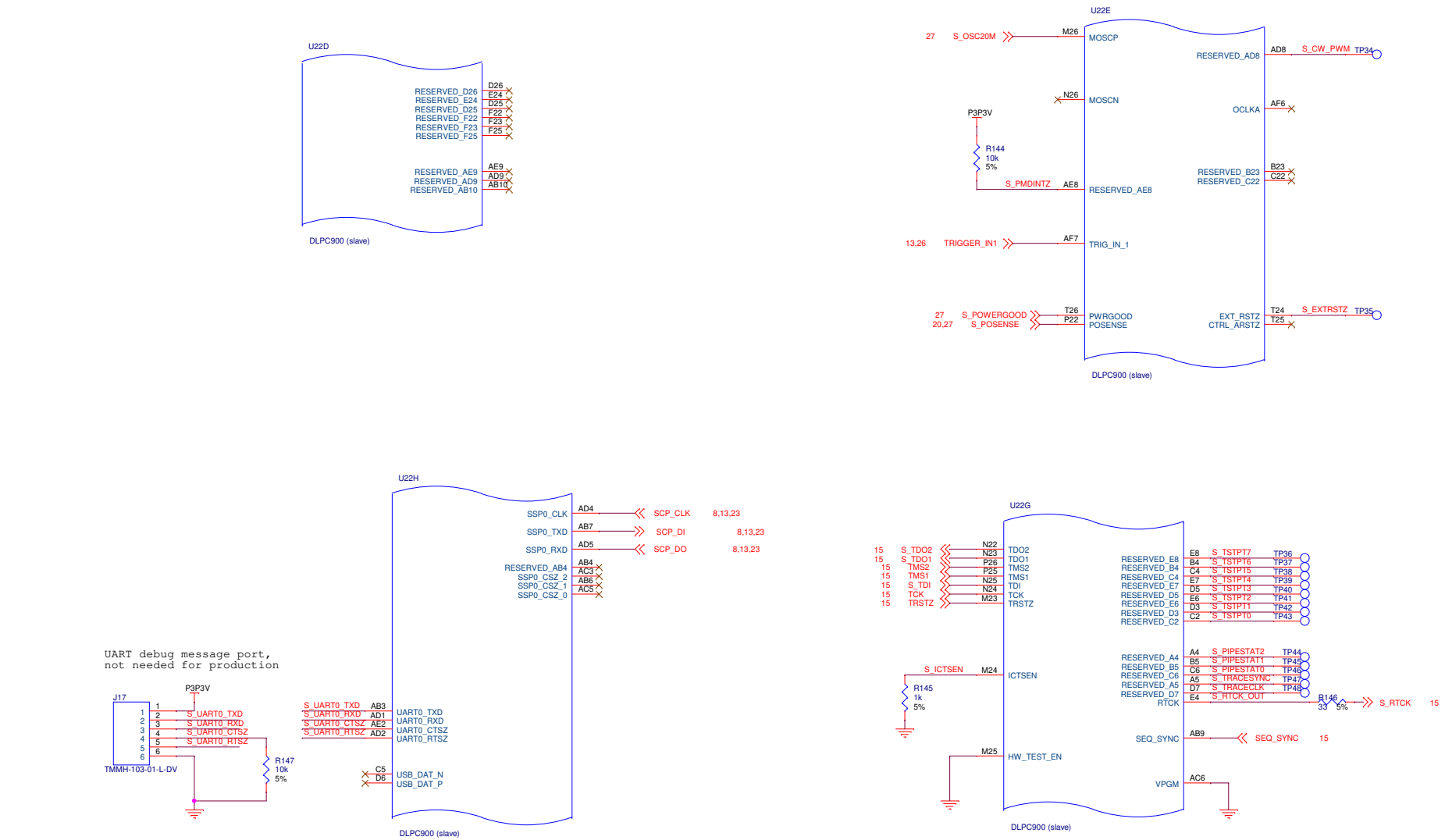
TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043
	ISSUE DATE		SCALE	SHEET 17 OF 29

REV G



Slave Controller Video Input, DMD Output

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE SHEET 18 OF 29



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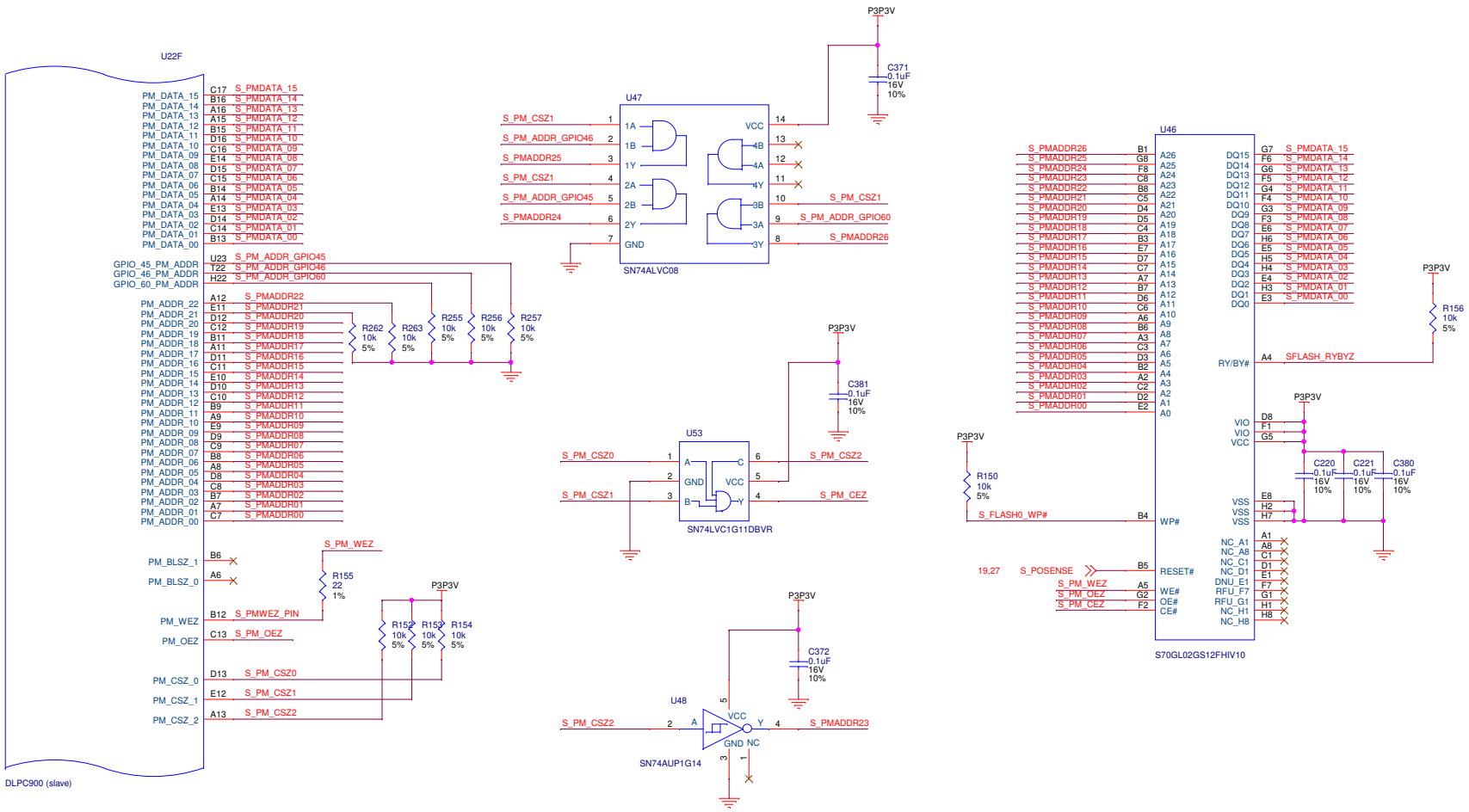
Slave Controller Reset, OSC, JTAG, UART0, SSP Port

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE			SCALE: SHEET 19 OF 29



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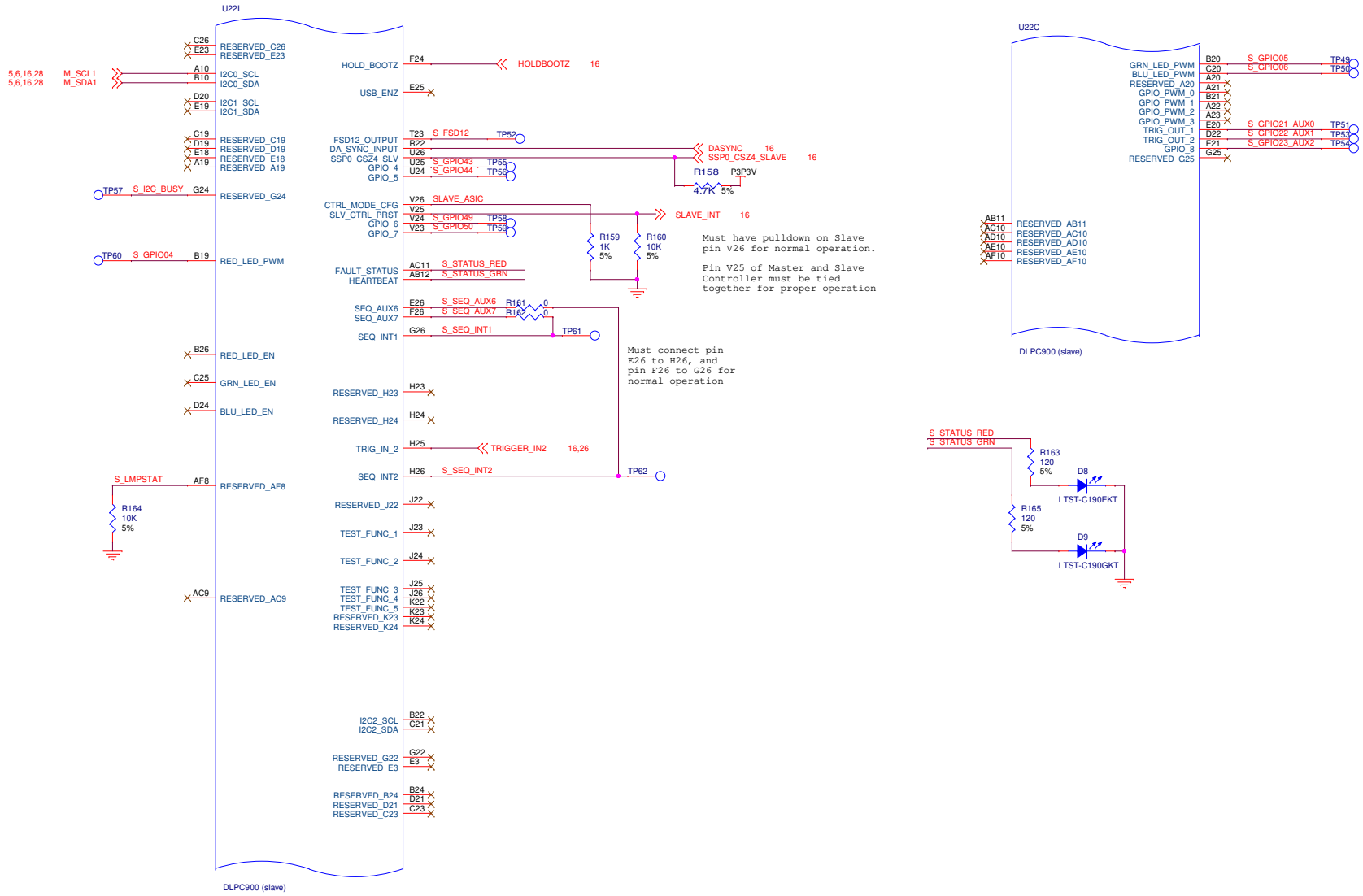
Slave Controller Flash Interface

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043
	ISSUE DATE		SCALE	SHEET 20 OF 29

REV G



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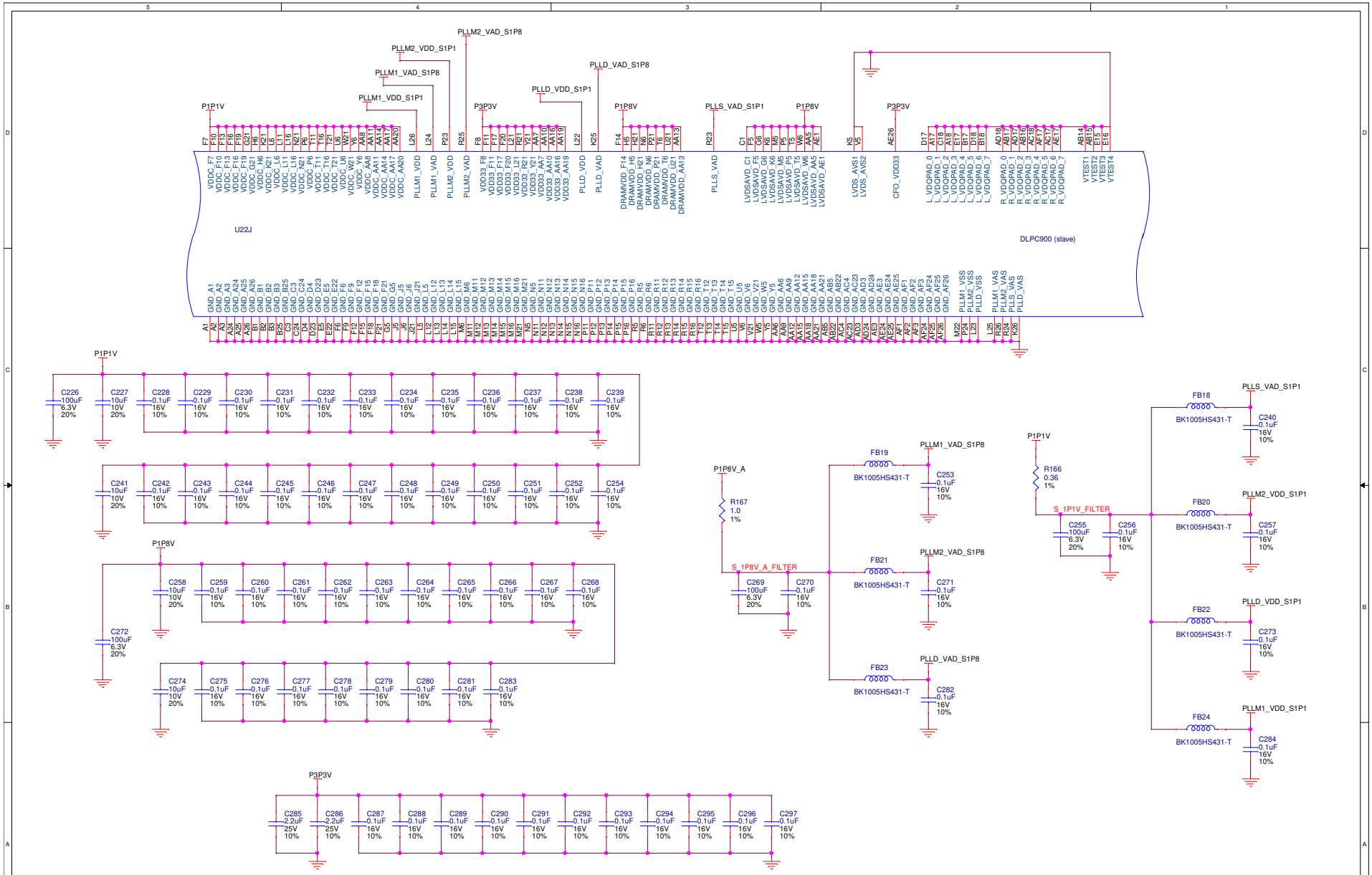
Slave Controller I2C, GPIOs

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE	SHEET 21 OF 29


PLLM2_VAD_S1P8
PLLM2_VDD_S1P1
PLLM1_VAD_S1P8
PLLM1_VDD_S1P1
PLLD_VAD_S1P8
PLLD_VDD_S1P1
P1P1V
P3P3V
P1P8V
PLLS_VAD_S1P1
U22J
DLPC900 (slave)
P1P8V_A
R167
1.0
1%
S_1P8V_A_FILTER
R166
0.36
1%
S_1P1V_FILTER
FB18
FB19
FB20
FB21
FB22
FB23
FB24
BK1005HS431-T
PLLS_VAD_S1P1
PLLM2_VDD_S1P1
PLLD_VDD_S1P1
PLLM1_VDD_S1P1
PLLM1_VAD_S1P8
PLLM2_VAD_S1P8
PLLD_VAD_S1P8
Slave Controller Pwr Gnd
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TEXAS INSTRUMENTS
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ISSUE DATE
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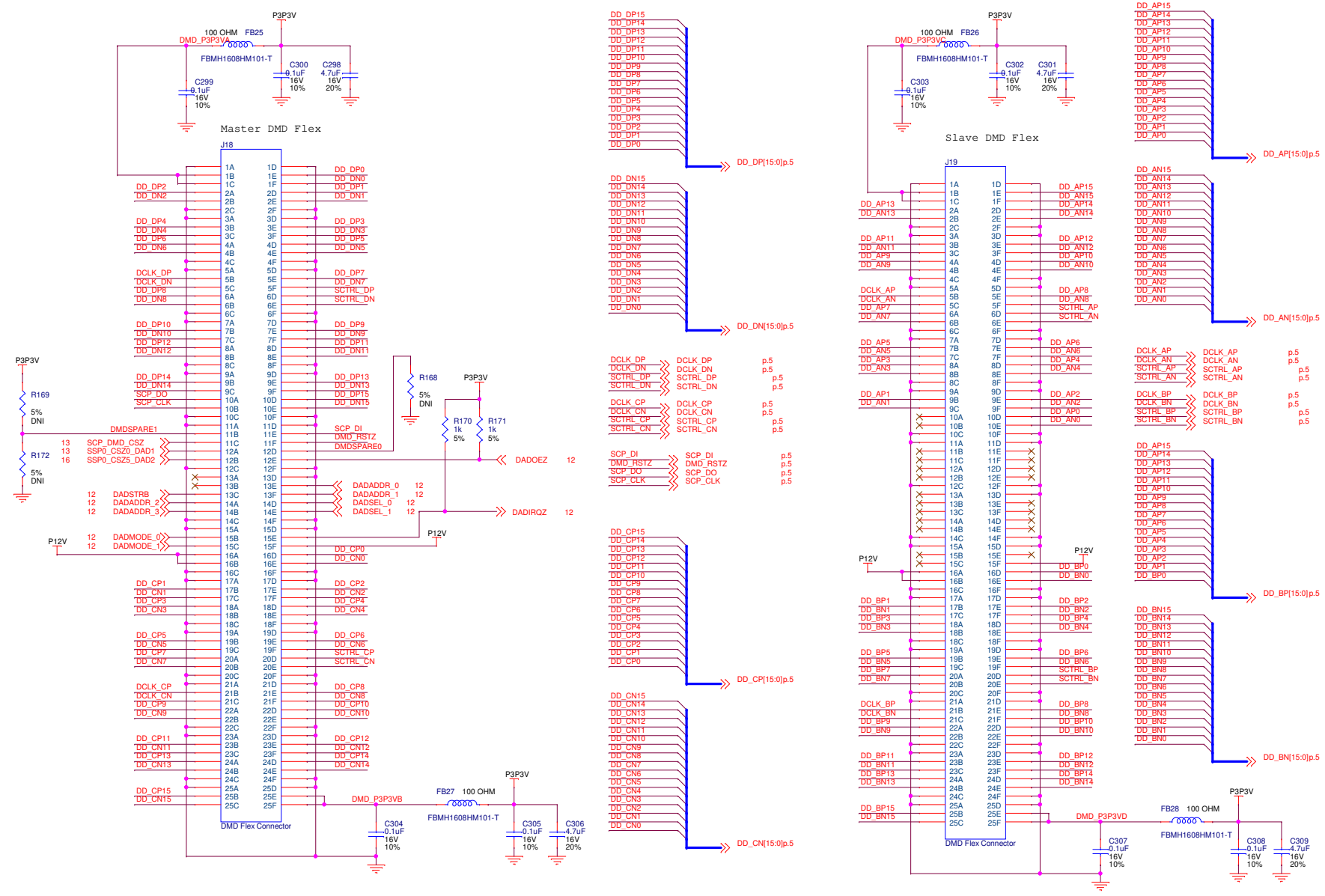

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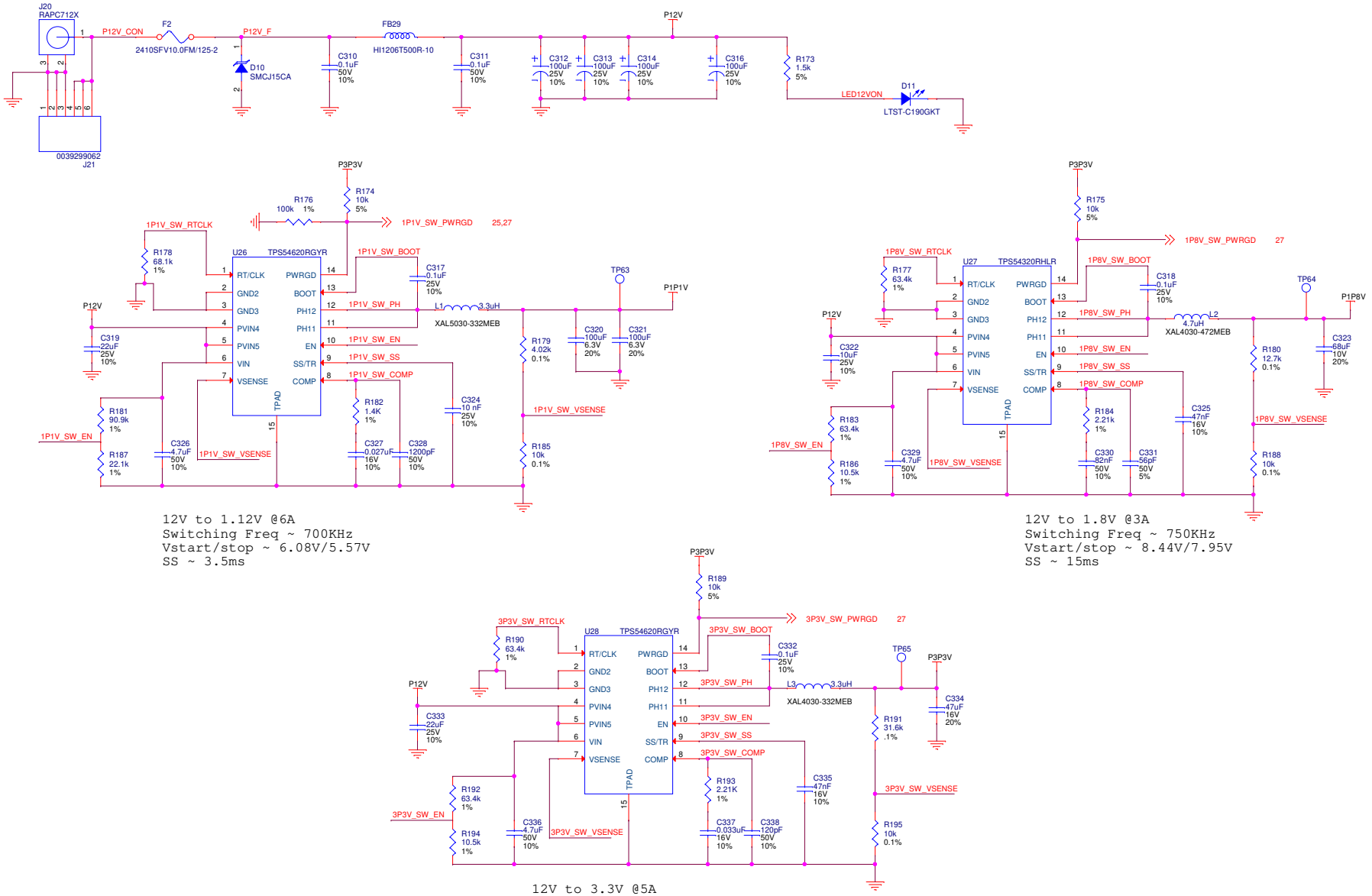
TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043 REV G
	ISSUE DATE		SCALE	SHEET 23 OF 29


J20
RAPC712X
P12V_CON
F2
2410SFV10.0FM/125-2
P12V_F
D10
SMCJ15CA
FB29
HI1206T500R-10
C310
0.1uF
50V
10%
C311
0.1uF
50V
10%
C312
100uF
25V
10%
C313
100uF
25V
10%
C314
100uF
25V
10%
C316
100uF
25V
10%
P12V
R173
1.5k
5%
LED12VON
D11
LTST-C190GKT
0039299062
J21
P3P3V
R176
100k 1%
R174
10k
5%
1P1V_SW_PWRGD 25,27
1P1V_SW_RTCLK
R178
68.1k
1%
U26
TPS54620RGYR
RT/CLK
GND2
GND3
PVIN4
PVIN5
VIN
VSENSE
PWRGD
BOOT
PH12
PH11
EN
SS/TR
COMP
TPAD
1P1V_SW_BOOT
C317
0.1uF
25V
10%
1P1V_SW_PH
L1
3.3uH
XAL5030-332MEB
1P1V_SW_EN
1P1V_SW_SS
1P1V_SW_COMP
TP63
P1P1V
C319
22uF
25V
10%
R181
90.9k
1%
R187
22.1k
1%
C326
4.7uF
50V
10%
1P1V_SW_VSENSE
R182
1.4K
1%
C327
0.027uF
16V
10%
C328
1200pF
50V
10%
C324
10 nF
25V
10%
R179
4.02k
0.1%
C320
100uF
6.3V
20%
C321
100uF
6.3V
20%
R185
10k
0.1%
12V to 1.12V @6A
Switching Freq ~ 700KHz
Vstart/stop ~ 6.08V/5.57V
SS ~ 3.5ms
P3P3V
R175
10k
5%
1P8V_SW_PWRGD 27
1P8V_SW_RTCLK
R177
63.4k
1%
U27
TPS54320RHLR
1P8V_SW_BOOT
C318
0.1uF
25V
10%
1P8V_SW_PH
L2
4.7uH
XAL4030-472MEB
TP64
P1P8V
1P8V_SW_EN
1P8V_SW_SS
1P8V_SW_COMP
C322
10uF
25V
10%
R183
63.4k
1%
R186
10.5k
1%
C329
4.7uF
50V
10%
1P8V_SW_VSENSE
R184
2.21k
1%
C330
82nF
50V
10%
C331
56pF
50V
5%
C325
47nF
16V
10%
R180
12.7k
0.1%
C323
68uF
10V
20%
R188
10k
0.1%
12V to 1.8V @3A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms
P3P3V
R189
10k
5%
3P3V_SW_PWRGD 27
3P3V_SW_RTCLK
R190
63.4k
1%
U28
TPS54620RGYR
3P3V_SW_BOOT
C332
0.1uF
25V
10%
TP65
3P3V_SW_PH
L3
3.3uH
XAL4030-332MEB
C333
22uF
25V
10%
3P3V_SW_EN
3P3V_SW_SS
3P3V_SW_COMP
C334
47uF
16V
20%
R191
31.6k
.1%
R192
63.4k
1%
R194
10.5k
1%
C336
4.7uF
50V
10%
3P3V_SW_VSENSE
R193
2.21K
1%
C337
0.033uF
16V
10%
C338
120pF
50V
10%
C335
47nF
16V
10%
R195
10k
0.1%
12V to 3.3V @5A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms
Power Generation 1.1V, 1.8V and 3.3V
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TEXAS INSTRUMENTS
DWN
DATE
ISSUE DATE
A3
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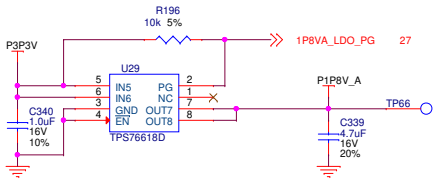
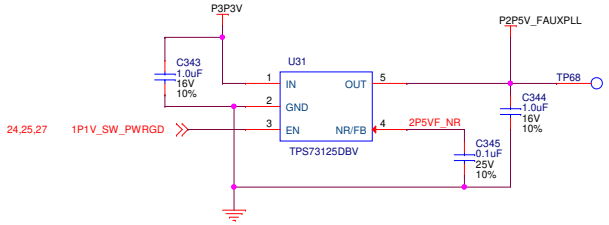
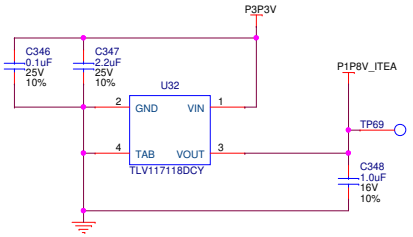
SHEET 24 OF 29



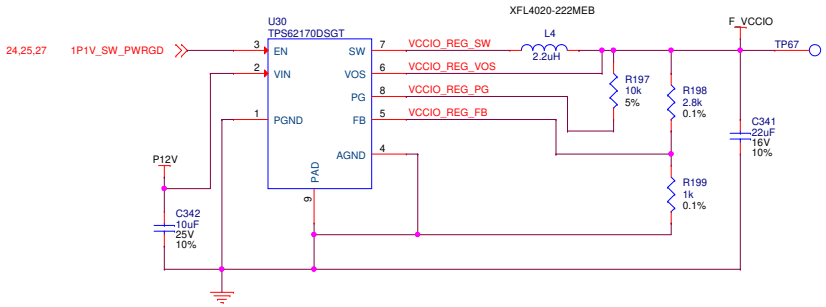
3.3V to 1.8V @250mA LDO
for controller 1.8V analog



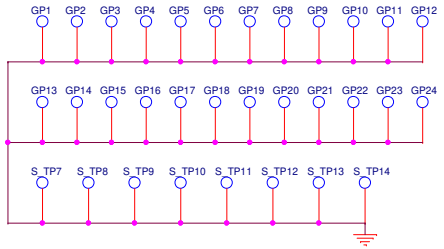
3.3V to 2.5V @150mA LDO
for FPGA 2.5V AUX/PLL power



3.3V to 1.8V @1A LDO
for HDMI Rx 1.8V analog



12V to 3V @500mA
for FPGA Vccio



Distribute ground vias around PCB

Left/Right Split FPGA Power Generation VCCIO, 1.8V & 2.5V LDOs

TEXAS INSTRUMENTS	DWN DATE	A3	DRAWING NO DLPLCR900DEVM - DLP043	REV G
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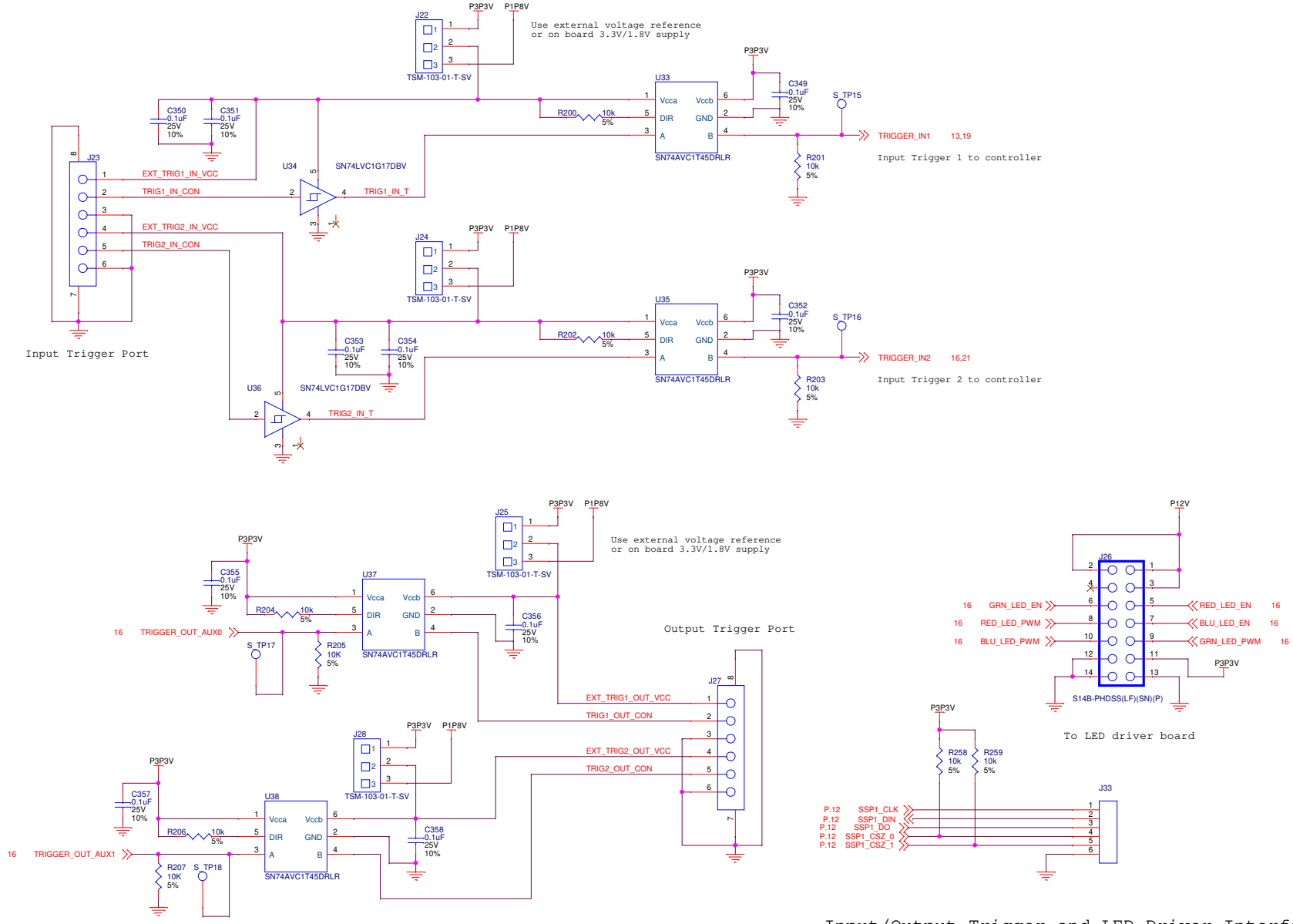
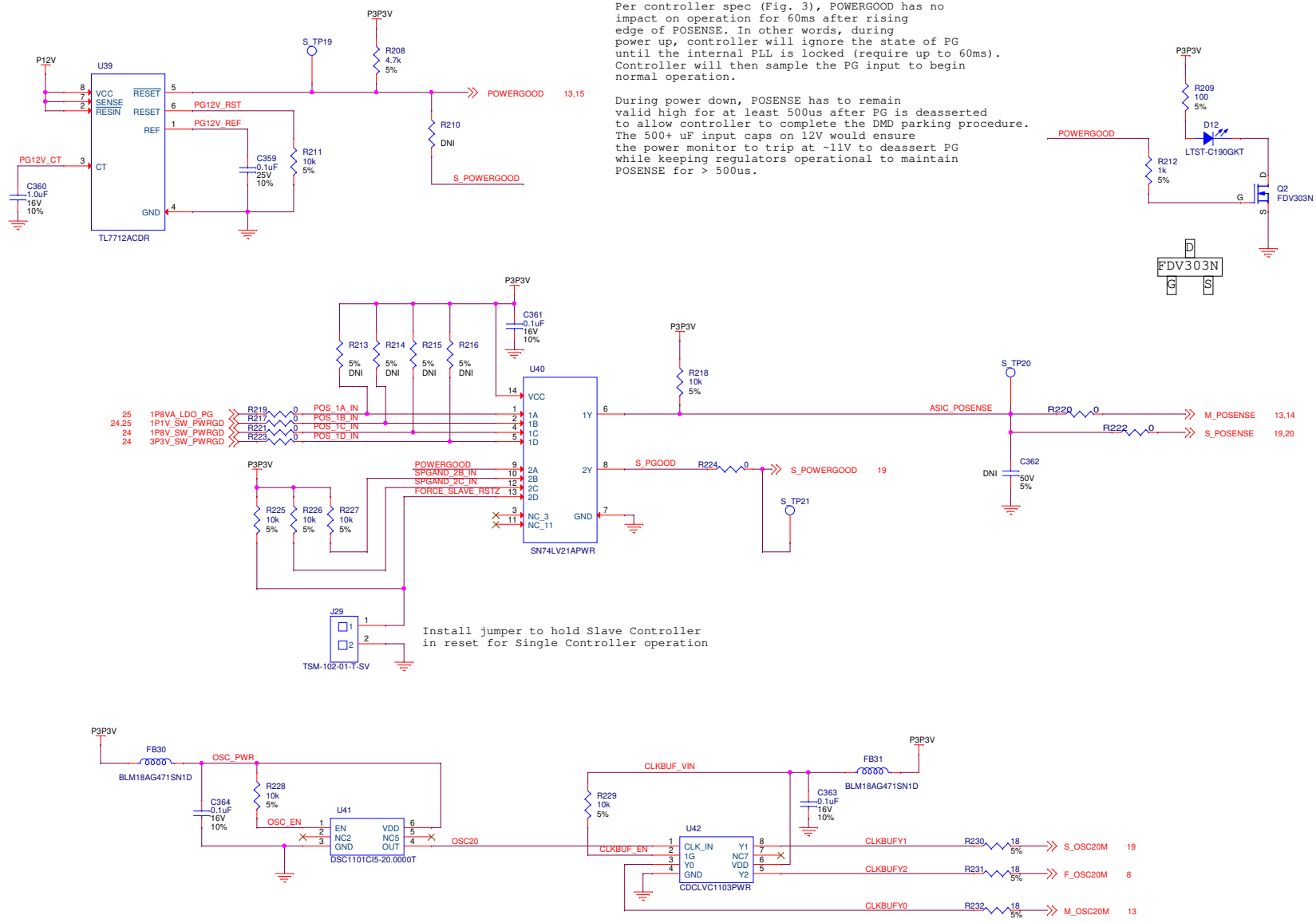


Input/Output Trigger and LED Driver Interface

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043 REV: G
	ISSUE DATE			SCALE: SHEET 26 OF 29



Powergood, POSENSE, Conroller Clocks

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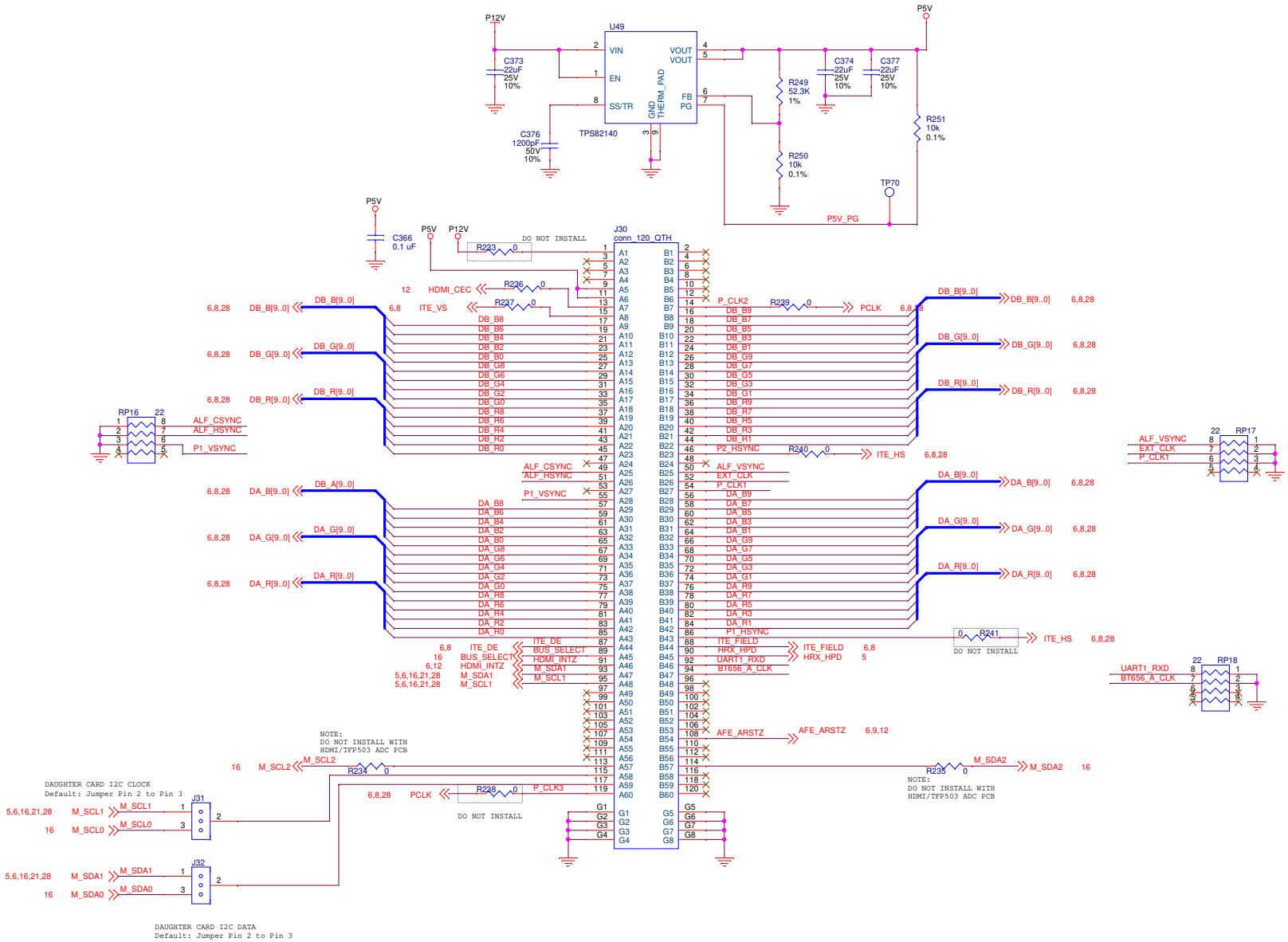
	ISSUE DATE		SCALE SHEET 27 OF 29



External Parallel Video Input Connector

TEXAS INSTRUMENTS	DWN	DATE	A3	DRAWING NO: DLPLCR900DEVM - DLP043
	ISSUE DATE			REV: G
			SCALE	SHEET 28 OF 29

REVISION HISTORY

Rev A

PAGES - ALL

- initial rev

Rev B

PAGE 27

- new part for C360

PAGE 26

- relocated S_TP17 and S_TP18

PAGE 24

- new part for R179
- removed C315, bulk cap not needed

PAGE 25

- new part for L4

PAGE 10

- new part for U12

Rev C

PAGES for U13 & U22

- update pin name to match datasheet

PAGE 15

- add comments for usage of R117 & R118

Rev D

Remove references to DLPC910

Rev E

Updated U7

Rev F

Added External Parallel Video Connector and 5V source

Sheet 12:
- Added net HDMI_CEC to U13A,G23

Sheet 28:
- Inserted Parallel Video Connector as Sheet 28. Revisions page moved to Sheet 29.
- Added U49
- Added J30, J31, J32
- Added R233, R234, R235, R236, R237, R238, R239, R240, R241, R249, R250, R251
- Added RP16, RP17, RP18
- Added C366, C373, C374, C376, C377

Increased External Flash Memory to 128 MByte

Sheet 14:
- Added net M_PM_ADDR_GPIO45 to U13F,U23
- Added net M_PM_ADDR_GPIO46 to U13F,T22
- Added net M_PM_ADDR_GPIO60 to U13F, H22
- Added net BUS_SELECT to U13I,H23

Sheet 20:
- Added net S_PM_ADDR_GPIO45 to U22F,U23
- Added net S_PM_ADDR_GPIO45 to U22F,T22
- Added net S_PM_ADDR_GPIO60 to U22F, H22

Sheet 14:
- Removed U16, U17, U18
- Removed R87, R88, R90, R96
- Removed C140, C141, C142, C143
- Added U43, U44, U45, U50
- Added C367, C368, C378, C379
- Added R252, R253, R254

Sheet 20:
- Removed U23, U24, U25
- Removed R148, R149, R151, R157
- Removed C222, C223, C224, C225
- Added U46, U47, U48, U53
- Added C371, C372, C380, C381
- Added R255, R256, R257

Addeded Connector for SSP1 Bus
- Added J33, R258, R259

Rev G

Sheet 5
- Changed J2 footprint to SMT

Sheet 10
- U12 changed to Micron MT25QL128ABA1ESE-0SIT

Sheet 14
- Added R260 and R261
- Changed net connected to U44 pin 5 to M_PM_ADDR_GPIO45

Sheet 20
- Added R262 and R263
- Changed net connected to U48 pin 2 to S_PM_CSZ2

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