TEXAS INSTRUMENTS

IBIS QUALITY REPORT

Design ID: MLVD202A
Part Technology Type: MLVD
Marketing part Number: SN65MLVD202A
IBIS Zip File Name: sn65mlvd202a_2p2_ibis.zip
IBIS File Name: mlvd202a.ibs
Available package types: 14D SOIC Package
Date: 11/13/2008
Datasheet Link: http://focus.ti.com/lit/ds/symlink/sn65mlvd202a.pdf

Contact IBIS modeling Support at elab_ibis@list.ti.com for questions

IBIS MODEL QUALITY CHECKLIST

Included IBIS quality summary information in quality report. For more information on IBIS Quality specification visit http://www.vhdl.org/pub/ibis/quality_wip/

```
**********************************************************************
                          IBIS Quality Summary
**********************************************************************
|IQ Over all Quality of IBIS model of component:  Level 2
|
|IQ Level 0 – 0 errors 0 warnings
|
IQ Level1 – All Level1 checks are done for completeness and correctness; they are either          OK or NA
|
|IQ Level2 – V-T IBIS data compared to TISPICE models. TISPICE used for IBIS model generation
|
IQ Level2b – C_comp Laboratory and TISPICE Correlation
|
|IQ BEGIN IBIS Quality Checklist
|IQ File: mlvd202a.ibs   IQ Level: 1
|IQ COMPONENT: SN65MLVD202AD   Level:1
|IQ MODEL: RECEIVER_IN              Level:2
|IQ MODEL: RECEIVER_OUT             Level:2
|IQ END IBIS Quality Checklist
```

TEXAS INSTRUMENTS

IBIS MODEL CORRELATION

Datasheet Correlation

1. For Output model include IBIS vs. Datasheet spec for IOH and IOL data.
   a. IBIS IOH vs. Datasheet IOH
   Not Available
   b. IBIS IOL vs. Datasheet IOL
   Not Available

2. Compare c_comp with datasheet's input capacitance spec. Table provides data comparing c_comp for all models and all package combinations

   Component Name: **SN65MLVD202A**

		IBIS			Datasheet
		typ	min	max	typ
	C_comp	2.975pF	2.868pF	3.108pF	NA
Input A &B	C_package	0.3705pF	0.964pF	0.377pF	NA
	C_total	**3.346pF**	**3.832pF**	**3.485pF**	**3pF**
	C_comp	2.787pF	2.766pF	2.964pF	NA
Output Y&Z	C_package	0.424pF	0.372pF	0.476pF	NA
	C_total	**3.211pF**	**3.138pF**	**3.44pF**	**3pF**

Note: Datasheet spec and IBIS typical IOCAP are close. Once measurements obtained for this part, quality report and datasheet may be updated as required.

IBIS vs. TISPICE Correlation

1. For all Outputs correlate V-T transient simulations using IBIS(B-element) and TISPICE netlist to ensure correlation

   Case a: RECEIVER_IN at 50MHz. Used below setupin **Figure (iii)** and node naming conventions for IBIS and TISPICE deck file(*.sp file).

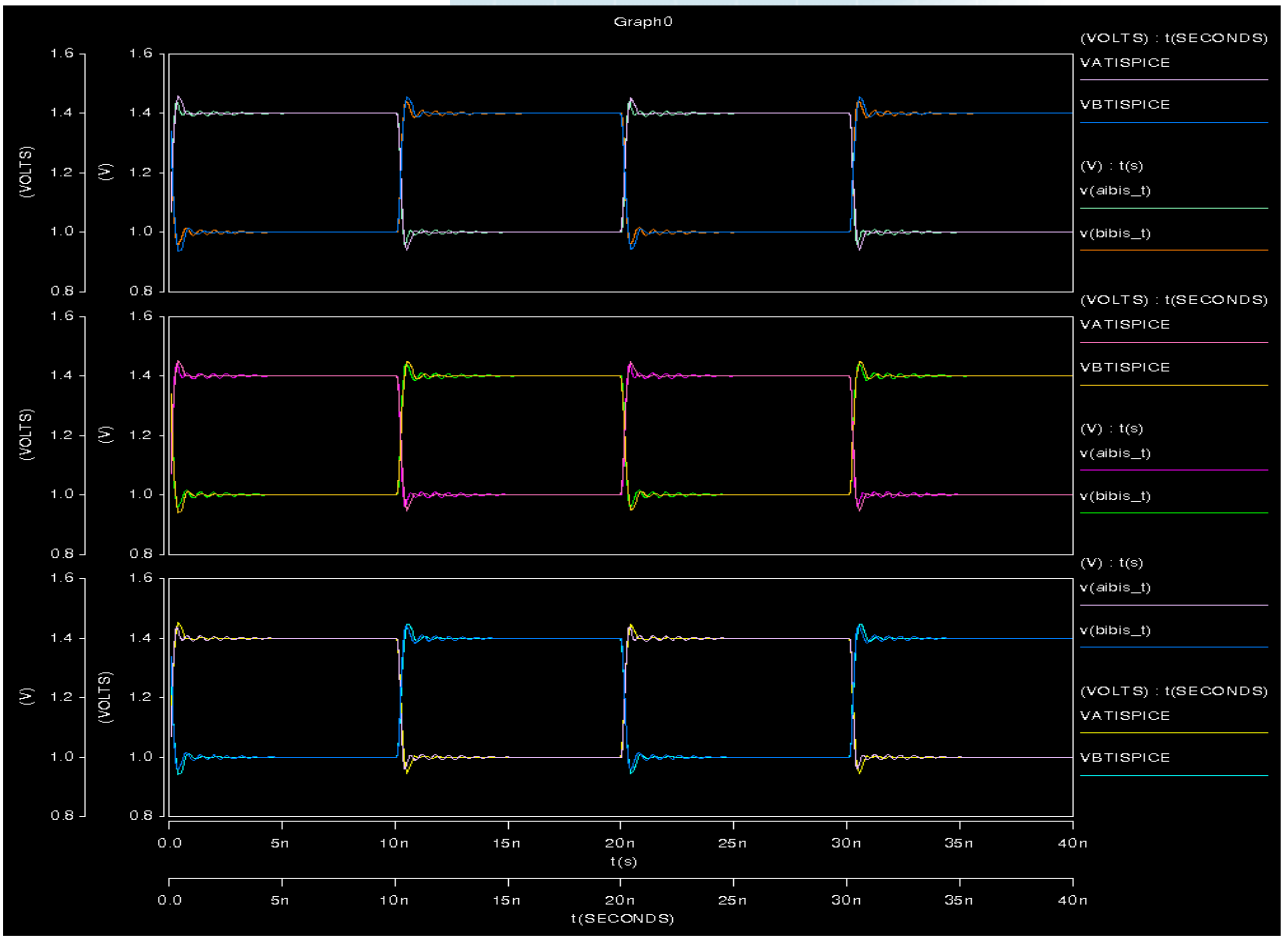

Figure (i)

Caseb: DRIVER_OUT at 50MHz. Used below setup in **Figure (v)** and node naming conventions for IBIS and TISPICE deck file(*.sp file). Set up in **Figure(iv)** yields the same result. **Please use either setup in Figure(iv) or Figure(v) as needed for correct results. Refer to comments below in "Revision History and Comments" section.**

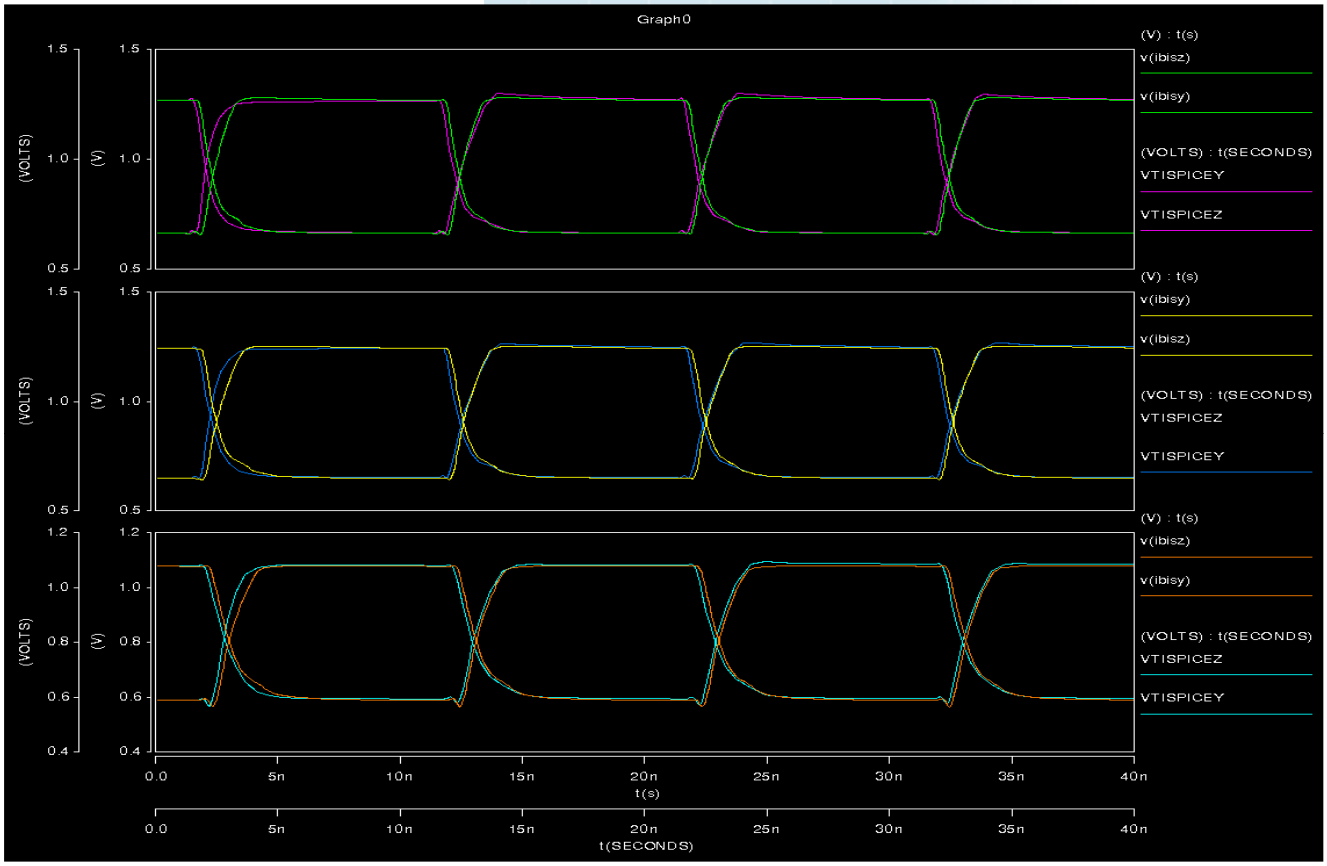

Figure (ii)

Schematics used for Correlation:

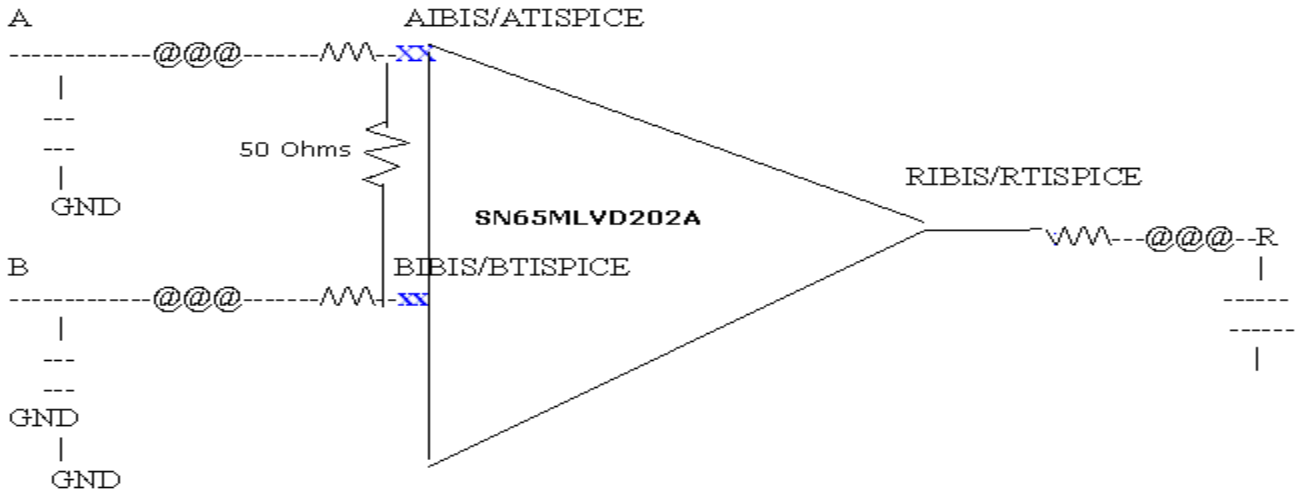

Figure (iii)

Note: **"xx"** indicate nodes at which results are shown in the waveforms.

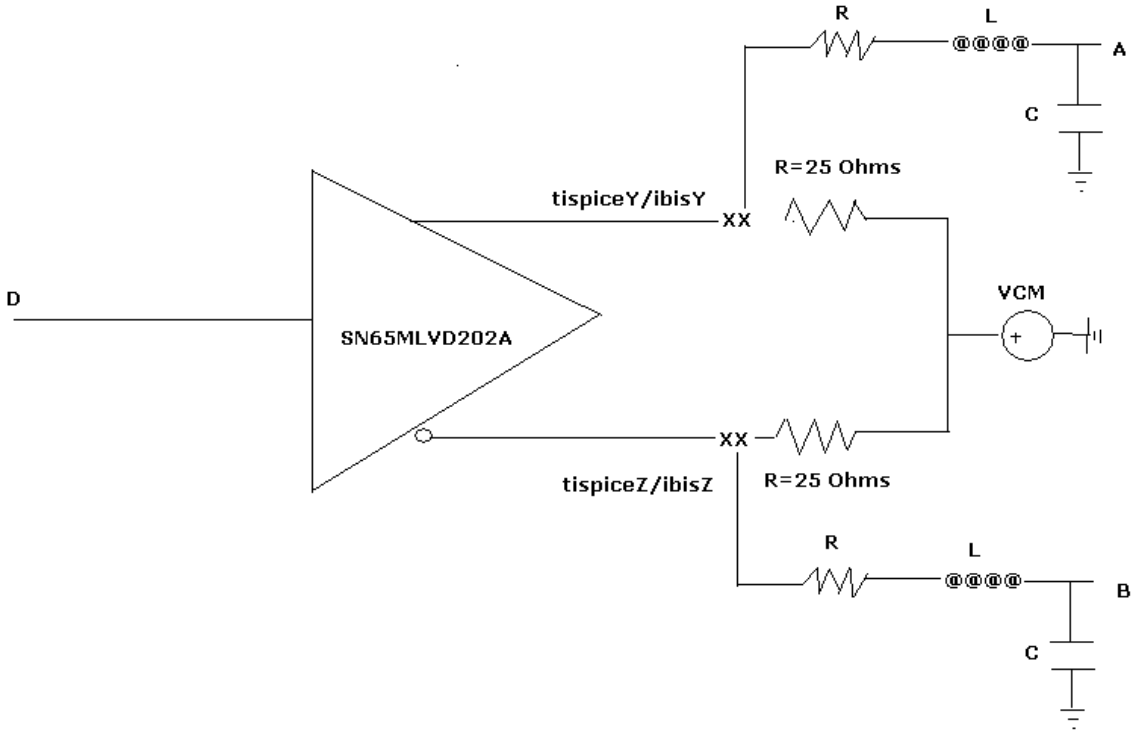

Figure (iv)

Note: **"xx"** indicate nodes at which results are shown in the waveforms.

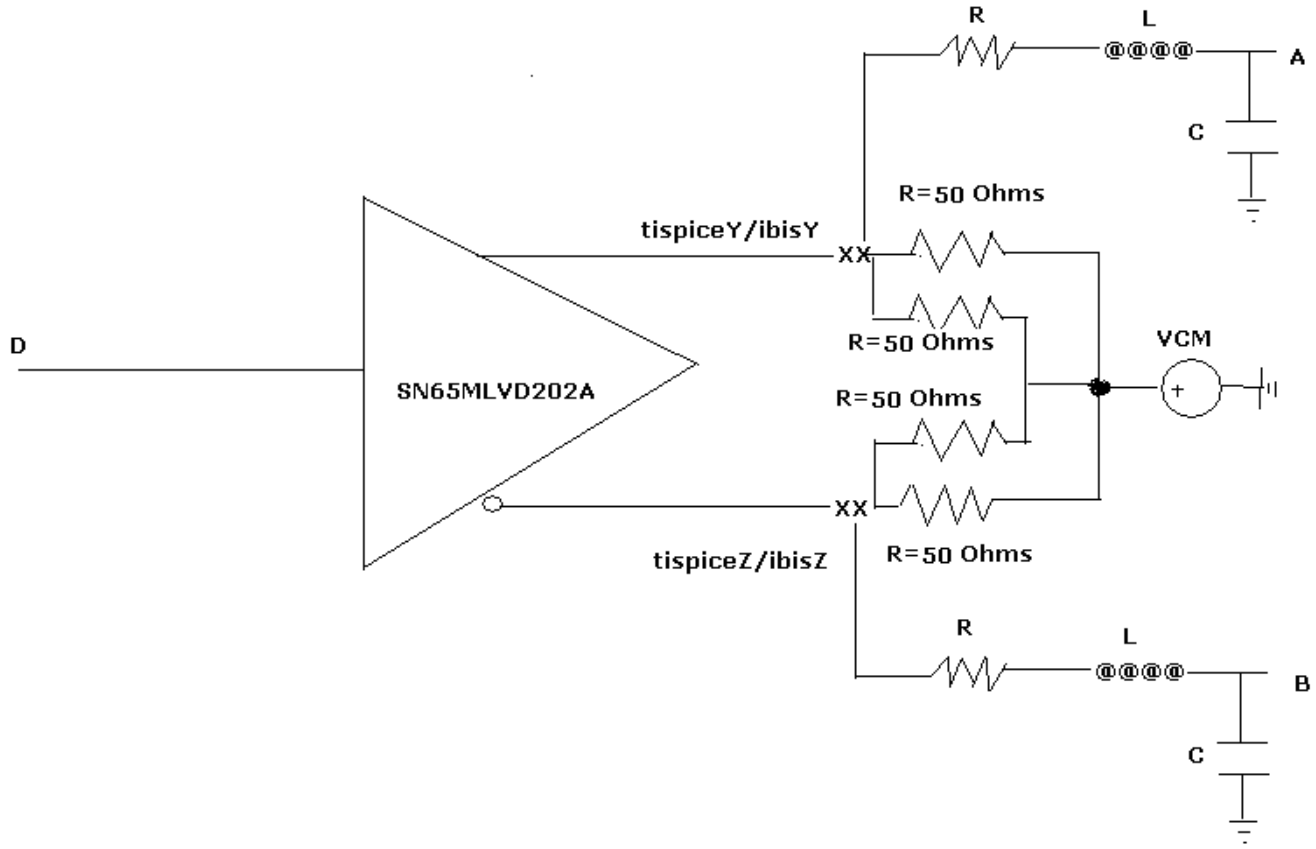

Figure (v)

Note: **"xx"** indicate nodes at which results are shown in the waveforms.

Revision History and Comments;

Rev 1.0: 11/13/2008

- **Quality report for mvld202a.ibs, only valid fro RECEIVER_IN and DRIVER_OUT buffer models. IBIS version file v2.2**
- **Please note that the DRIVER_OUT model is a common-mode model, hence termination of 50Ohms should be split into 25Ohms and mid-point should be connected to common mode voltage(VCM) of 0.936V, 0.814V and 0.995V for TYP, MIN and MAX corners respectively. If two parallel 100Ohms are to be used instead between Y and Z, then split each of them into two series 50Ohms resistors and terminate each of their midpoints to VCM.**