ADS922x Dual, Simultaneous-Sampling, 16-Bit, 10-MSPS SAR ADCs With Fully Differential ADC Input Driver

1 Features

- High-speed sampling rate: 10 MSPS/ch
  - ADS9228 (preview): 10 MSPS/ch
  - ADS9227: 5 MSPS/ch
- 2-channel, simultaneous sampling
- Feature integration:
  - Integrated ADC driver
  - Integrated precision reference
  - Common-mode voltage output buffer
- High-performance
  - 16-bit no-missing-codes
  - INL: ±0.3 LSB, DNL: ±0.3 LSB
  - SNR: 93.5 dB, THD: –120 dB at f_{IN} = 2 kHz
- Wide input bandwidth:
  - ADS9228: 90 MHz (–3 dB)
  - ADS9227: 45 MHz (–3 dB)
- Low-power 141 mW/ch at 10 MSPS/ch
- Serial LVDS interface:
  - SDR and DDR output modes
  - Synchronous clock and data output
- Extended operating range: –40°C to 125°C
- 6 mm × 6 mm VQFN package

2 Applications

- Power analyzers
- Source measurement units (SMU)
- Marine equipment
- Servo drive position feedback
- DC power supplies, AC sources, electronic loads

3 Description

The ADS922x is a family of 16-bit, high-speed, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated driver for the ADC inputs. The integrated ADC driver simplifies external signal-chain that can be optimized for low-power and high-precision. The ADC consumes only 141 mW/ch at 10 MSPS/ch and the power consumption scales with lower sampling rates.

The ADS922x uses a serial LVDS (SLVDS) data interface that enables high-speed digital interface while minimizing digital switching noise. The dual-channel ADC data can be read using separate SLVDS outputs per ADC channel or one SLVDS output for both ADC channels.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS922x	RHA (VQFN, 40)	6 mm × 6 mm
ADS9228(3)	RHA (VQFN, 40)	6 mm × 6 mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Preview device (not Production Data).

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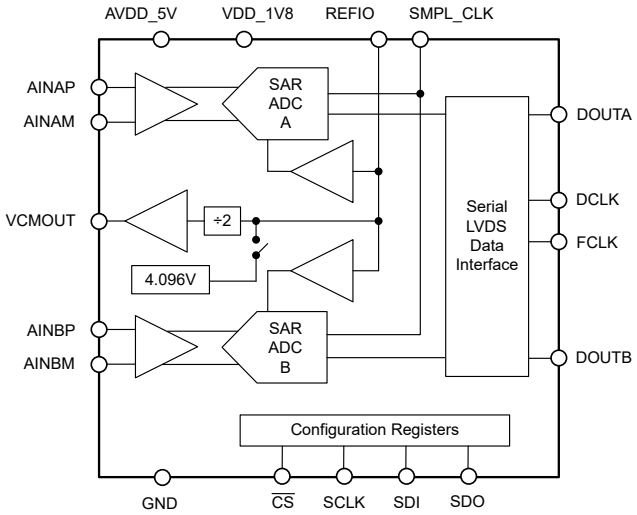

Device Block Diagram

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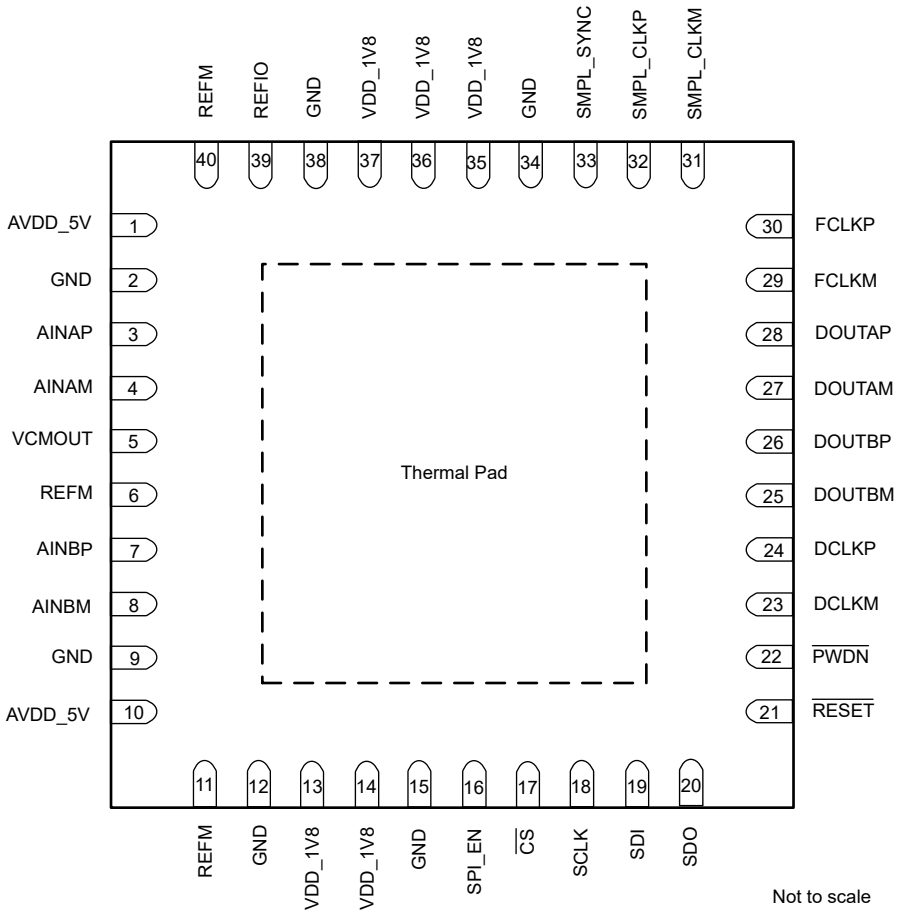

Figure 4-1. RHA Package, 6-mm × 6-mm, 40-Pin VQFN (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AINAM	4	I	Negative analog input for ADC A.
AINAP	3	I	Positive analog input for ADC A.
AINBM	8	I	Negative analog input for ADC B.
AINBP	7	I	Positive analog input for ADC B.
AVDD_5V	1, 10	P	5-V analog power-supply pin.
$\overline{CS}$	17	I	Chip-select input pin for the configuration interface; active low.
DCLKM	23	O	Negative differential data clock output. Connect a 100-Ω resistor between DCLKP and DCLKM close to the receiver.
DCLKP	24	O	Positive differential data clock output. Connect a 100-Ω resistor between DCLKP and DCLKM close to the receiver.
DOUTAM	27	O	Negative differential data output. Connect a 100-Ω resistor between DOUTAP and DOUTAM close to the receiver. Transmits ADC A data in 2-lane mode. Transmits ADC A and ADC B data in 1-lane mode.
DOUTAP	28	O	Positive differential data output corresponding to ADC A. Connect a 100-Ω resistor between DOUTAP and DOUTAM close to the receiver. Transmits ADC A data in 2-lane mode. Transmits ADC A and ADC B data in 1-lane mode.

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Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DOUTBM	25	O	Negative differential data output corresponding to ADC B in 2-lane mode. Connect a 100-Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode.
DOUTBP	26	O	Positive differential data output corresponding to ADC B in 2-lane mode. Connect a 100-Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode.
FCLKM	29	O	Negative differential data frame clock output. Connect a 100-Ω resistor between FCLKP and FCLKM close to the receiver.
FCLKP	30	O	Positive differential data frame clock output. Connect a 100-Ω resistor between FCLKP and FCLKM close to the receiver.
GND	2, 9, 12, 15, 34, 38	P	Ground.
$\overline{\text{PWDN}}$	22	I	Power-down control; active low. Connect to VDD_1V8 if unused.
REFIO	39	I/O	Internal reference voltage output. External reference voltage input. Connect a 10-µF decoupling capacitor to REFM.
REFM	6, 11, 40	P	Reference ground. Connect to GND.
$\overline{\text{RESET}}$	21	I	Reset input; active low. Connect to VDD_1V8 if unused.
SCLK	18	I	Serial clock input for the configuration interface.
SDI	19	I	Serial data input for the configuration interface.
SDO	20	O	Serial data output for the configuration interface.
SMPL_CLKM	31	I	ADC sampling clock input. Negative differential input for the LVDS sampling clock. Connect this pin to GND for the CMOS sampling clock.
SMPL_CLKP	32	I	ADC sampling clock input. Positive differential input for the LVDS sampling clock. Clock input for the CMOS sampling clock.
SMPL_SYNC	33	I	Synchronization input for internal averaging filter. Connect to GND if unused.
SPI_EN	16	I	Control to enable configuration of the SPI interface; active high. Connect a pullup resistor to VDD_1V8 to keep the configuration interface enabled. Connect to GND if SPI configuration is unused.
Thermal Pad	—	P	Exposed thermal pad. Connect to GND.
VCMOUT	5	O	Common-mode voltage output. Use VCMOUT to set the common-mode voltage at the ADC inputs. Connect a 1-µF decoupling capacitor to GND.
VDD_1V8	13, 14, 35, 36, 37	P	1.8-V power-supply. Connect 1-µF and 0.1-µF decoupling capacitors to GND.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD_1V8 to GND	–0.3	2.1	V
AVDD_5V to GND	–0.3	5.5	V
AINAP, AINAM, AINBP, and AINBM to GND	GND – 0.3	AVDD_5V + 0.3	V
REFIO to REFM	REFM – 0.3	AVDD_5V + 0.3	V
Digital inputs to GND	GND – 0.3	VDD_1V8 + 0.3	V
REFM to GND	–0.3	0.3	V
Input current to any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pin current must be limited to 10 mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, analog input pins AINAP, AINAM, AINBP, and AINBM(1)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±1000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		ADS922x RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply	AVDD_5V to GND	4.75	5	5.25	V
VDD_1V8	Power supply	VDD_1V8 to GND	1.75	1.8	1.85	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.076	4.096	4.116	V
ANALOG INPUTS						
V_{IN}	Absolute input voltage	AINx(1) to GND	0.7		4.1	V
FSR	Full-scale input range	(AINAP – AINAM) and (AINBP – AINBM)	–3.2		3.2	V
V_{CM}	Common-mode input range	(AINAP – AINAM) / 2 and (AINBP – AINBM) / 2	V_{CMOUT} – 0.025		V_{CMOUT} + 0.025	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AINAP, AINAM, AINBP, and AINBM.

5.5 Electrical Characteristics

at AVDD_5V = 4.75 V to 5.25 V for ADS9228 and ADS9229, AVDD_5V = 4.5 V to 5.5 V for ADS9227 VDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_B	Input bias current			0.5	TBD	µA
	Input bias current thermal drift			1		nA/°C
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity		–0.5	±0.3	0.5	LSB
INL	Integral nonlinearity		–0.75	±0.3	0.75	LSB
$V_{(OS)}$	Input offset error			±2	TBD	LSB
dV_{OS}/dT	Input offset error thermal drift			±0.3	TBD	ppm/°C
G_E	Gain error(1)		–0.05	±0.01	0.05	%FSR
dG_E/dT	Gain error thermal drift			±0.5	TBD	ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2 kHz	TBD	93.4		dB
		f_{IN} = 1 MHz		90.4		
SNR	Signal-to-noise ratio	f_{IN} = 2 kHz	TBD	93.5		dBFS
		f_{IN} = 1 MHz		90.5		
THD	Total harmonic distortion	f_{IN} = 2 kHz		–120		dB
		f_{IN} = 1 MHz		–104		
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		120		dB
		f_{IN} = 1 MHz		104		
	Isolation crosstalk	f_{IN} = 2 kHz		TBD		dB
SAMPLING DYNAMICS						

5.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75 V to 5.25 V for ADS9228 and ADS9229, AVDD_5V = 4.5 V to 5.5 V for ADS9227 VDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Input-bandwidth	ADS9228		90		MHz
		ADS9227		45		
COMMON-MODE OUTPUT BUFFER						
V_{CMOUT}	Common-mode output voltage			2.4		V
	Output current drive		0		5	µA
LVDS RECEIVER (SMPL_CLK)						
V_{TH}	High-level input voltage				100	mV
V_{TL}	Low-level input voltage		–100			mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.4	V
LVDS OUTPUT (CLKOUT, DOUTA, and DOUTB)						
V_{ODIFF}	Differential output voltage	R_L = 100 Ω	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_L = 100 Ω	1.08	1.1	1.32	V
CMOS INPUTS ($\overline{CS}$, SCLK, and SDI)						
V_{IL}	Input low logic level		–0.1		0.5	V
V_{IH}	Input high logic level		1.3		VDD_1V8	V
CMOS OUTPUT (SDO)						
V_{OL}	Output low logic level	I_{OL} = 200-µA sink	0		0.4	V
V_{OH}	Output high logic level	I_{OH} = 200-µA source	1.4		VDD_1V8	V
POWER SUPPLY						
I_{AVDD_5V}	Supply current from AVDD_5V	At 10 MSPS throughput (ADS9228)		30	40	mA
		At 5 MSPS throughput (ADS9227)		18	24	
		Power-down			2	
I_{VDD_1V8}	Supply current from VDD_1V8	At 10 MSPS throughput (ADS9228)		68	89	mA
		At 5 MSPS throughput (ADS9227)		51	66	
		Power-down			2	

(1) These specifications include full temperature range variation but not the error contribution from internal reference.

5.6 Timing Requirements

at AVDD_5V = 4.75 V to 5.25 V for ADS9228 and ADS9229, AVDD_5V = 4.5 V to 5.5 V for ADS9227 VDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values at T_A = 25°C.

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{CYCLE}	Sampling-frequency	ADS9228	3.6	10	MHz
		ADS9227	3.6	5	
t_{CYCLE}	ADC cycle-time period		1 / f_{CYCLE}		s
$t_{PL\_SMPLCLK}$	Sample clock low time		0.48	0.52	t_{CYCLE}
$t_{PH\_SMPLCLK}$	Sample clock high time		0.48	0.52	t_{CYCLE}
f_{CLK}	Maximum SCLK frequency			10	MHz
t_{CLK}	Minimum SCLK time period		100		ns
SPI TIMINGS					
t_{hi_CSZ}	Pulse duration: $\overline{CS}$ high		220		ns
t_{PH_CK}	SCLK high time		0.48	0.52	t_{CLK}

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at AVDD_5V = 4.75 V to 5.25 V for ADS9228 and ADS9229, AVDD_5V = 4.5 V to 5.5 V for ADS9227 VDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values at T_A = 25°C.

		MIN	MAX	UNIT
t_{PL_CK}	SCLK low time	0.48	0.52	t_{CLK}
t_{d_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK rising edge	20		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge	10		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI	5		ns
t_{d_CKCS}	Delay time: last SCLK falling edge to $\overline{CS}$ rising	5		ns

5.7 Switching Characteristics

at AVDD_5V = 4.75 V to 5.25 V for ADS9228 and ADS9229, AVDD_5V = 4.5 V to 5.5 V for ADS9227 VDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			25	ms
LVDS DATA INTERFACE					
t_{RT}	Rise time	With 50-Ω transmission line of length = 20 mm, differential R_L = 100 Ω, and C_L = 1 pF		600	ps
t_{FT}	Fall time			600	ps
t_{CYCLE}	Sampling clock period	ADS9228	100		ns
		ADS9227	200		
t_{DCLK}	Clock output		4.167		ns
	Clock duty cycle		45	55	%
t_{d_DCLKDO}	Time delay: DCLKP rising to corresponding data valid	At 5Msps, SDR mode	–0.8	0.8	ns
$t_{off\_DCLKDO\_r}$	Time offset: DCLKP rising to corresponding data valid	At 5Msps, DDR mode	t_{DCLK} / 4 – 0.8	t_{DCLK} / 4 + 0.8	ns
$t_{off\_DCLKDO\_f}$	Time offset: DCLKP falling to corresponding data valid	At 5Msps, DDR mode	t_{DCLK} / 4 – 0.8	t_{DCLK} / 4 + 0.8	ns
t_{PD}	Time delay: SMPL_CLK falling to DCLKP rising			t_{DCLK}	ns
$t_{PU\_SMPL\_CLK}$	Time delay: free running clock connected to SMPL_CLK to ADC data valid			100	µs
SPI TIMINGS					
t_{den_CKDO}	Time delay: 8th SCLK rising edge to SDO enable			30	ns
t_{dz_CKDO}	Time delay: 24th SCLK rising edge to SDO going Hi-Z			30	ns
t_{d_CKDO}	Time delay: SCLK launch edge to corresponding data valid on SDO			20	ns
t_{ht_CKDO}	Hold time: SCLK launch edge to previous data valid on SDO		2		ns

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5.8 Timing Diagrams

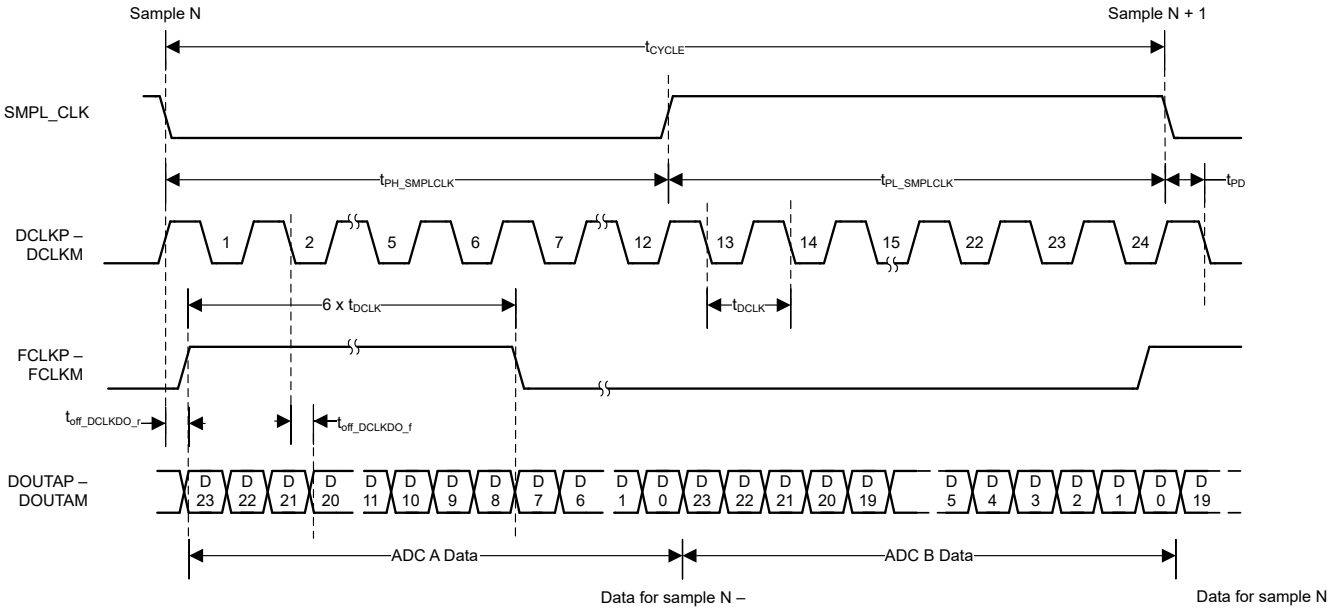

Figure 5-1. LVDS Data Interface: 1-Lane DDR

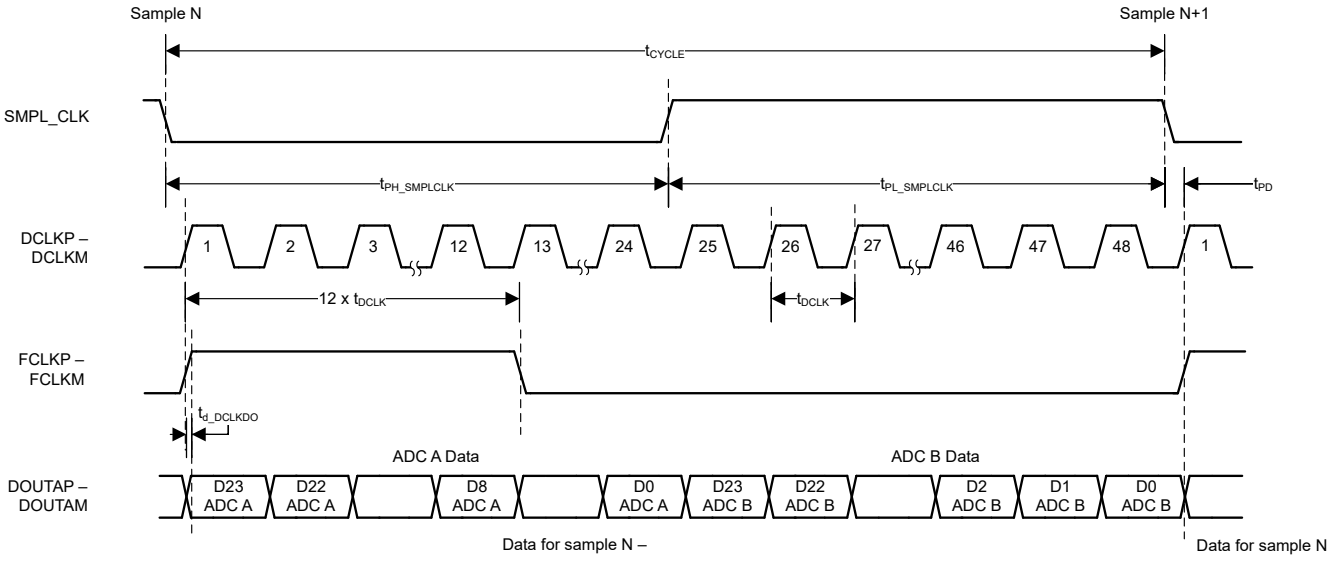

Figure 5-2. LVDS Data Interface: 1-Lane SDR

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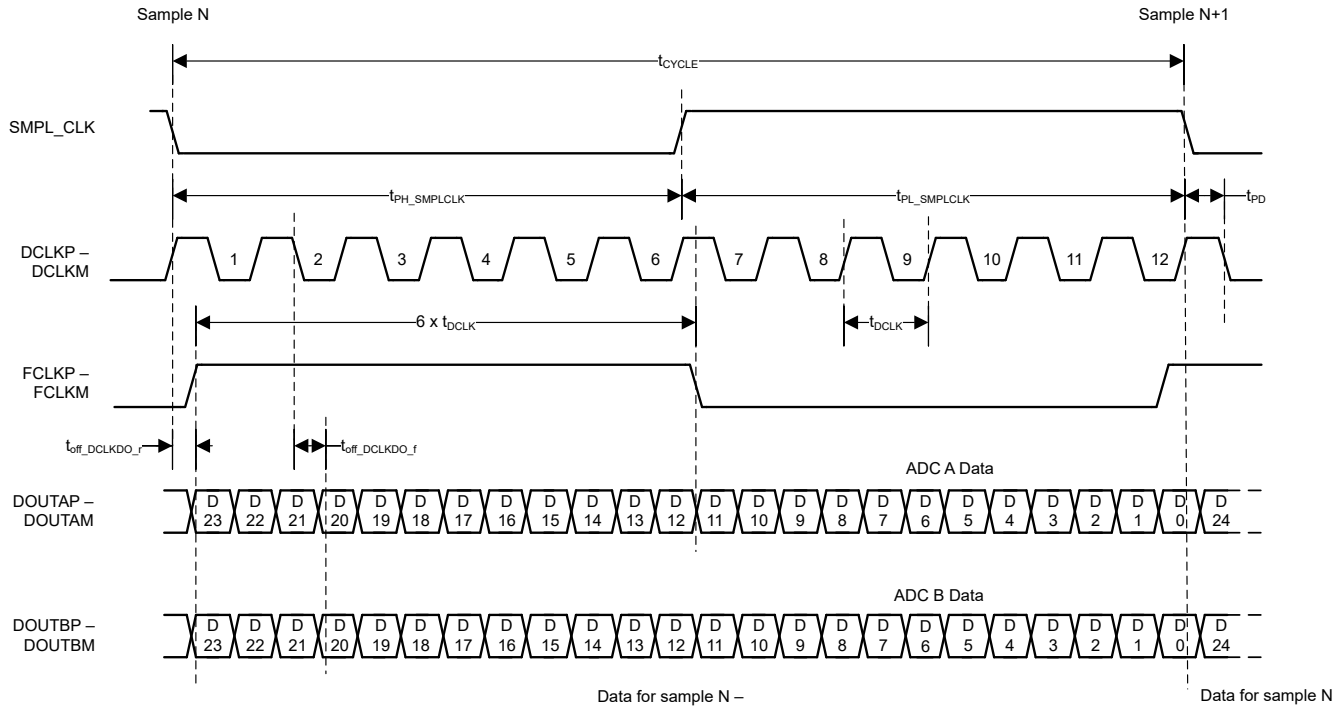

Figure 5-3. LVDS Data Interface: 2-Lane DDR

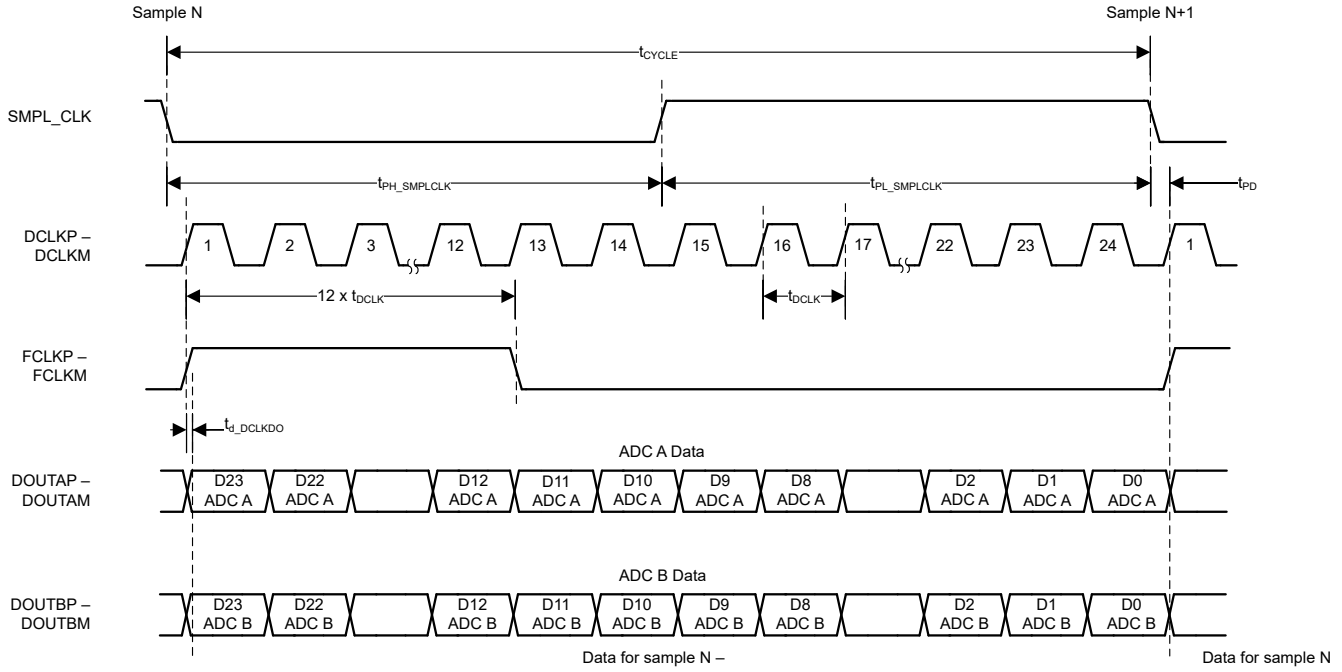

Figure 5-4. LVDS Data Interface: 2-Lane SDR

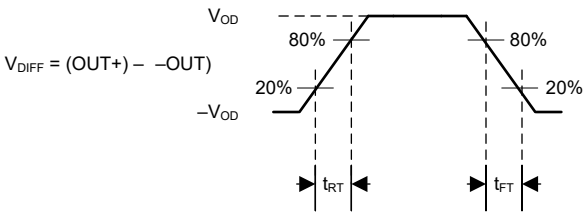

Figure 5-5. LVDS Output Transition Times

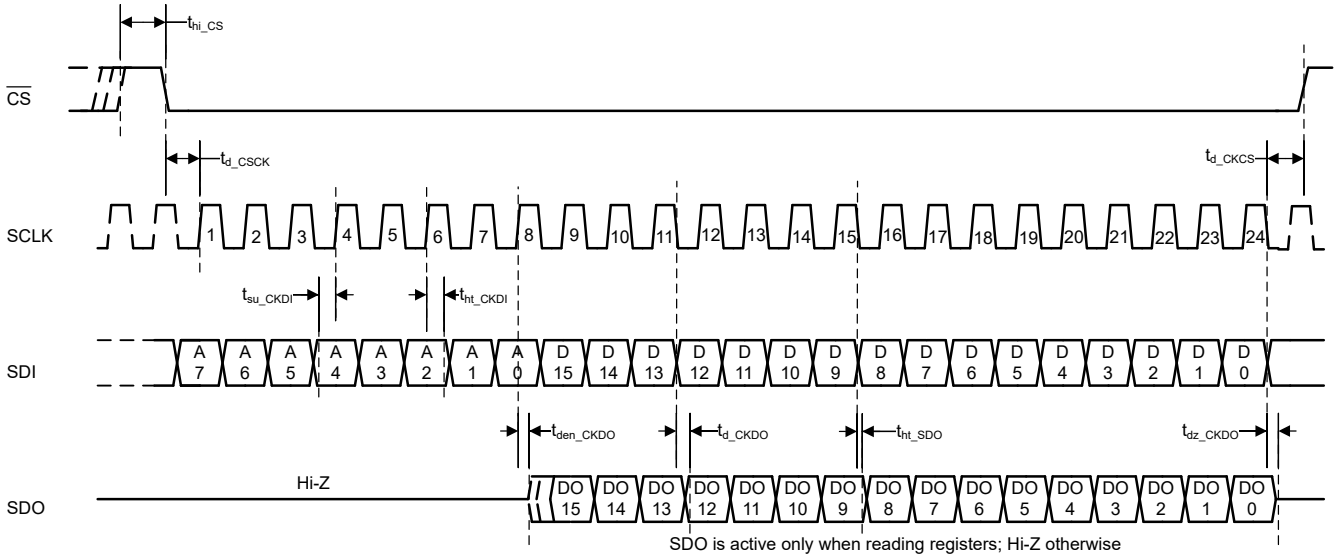

Figure 5-6. Configuration SPI

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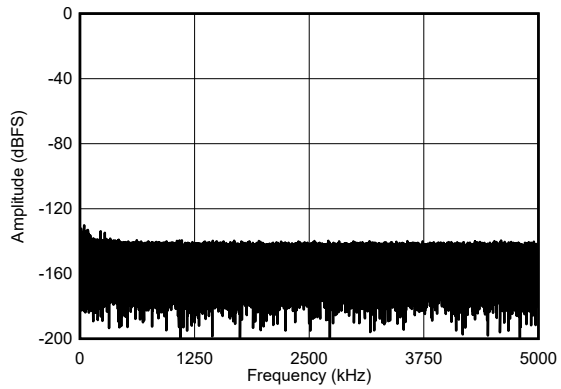
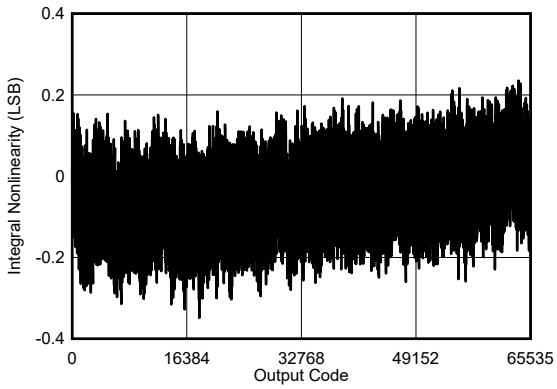
5.9 Typical Characteristics: ADS9228

at T_A = 25°C, AVDD_5V = 5 V, AVDD_1V8 = 1.8 V, DVDD_1V8 = 1.8 V, internal V_{REF} = 4.096 V, and maximum throughput (unless otherwise noted)



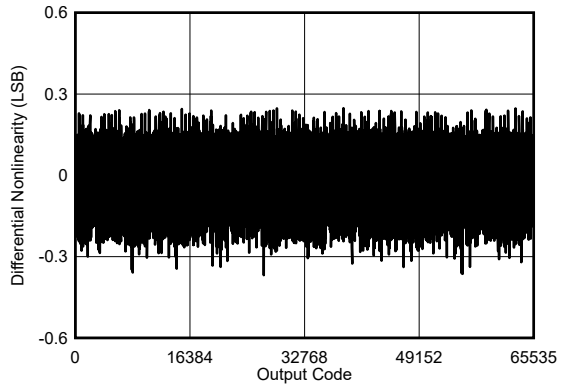
f_{IN} = 2 kHz, SNR = 94.4 dB, THD = –115 dB

Figure 5-7. Typical FFT



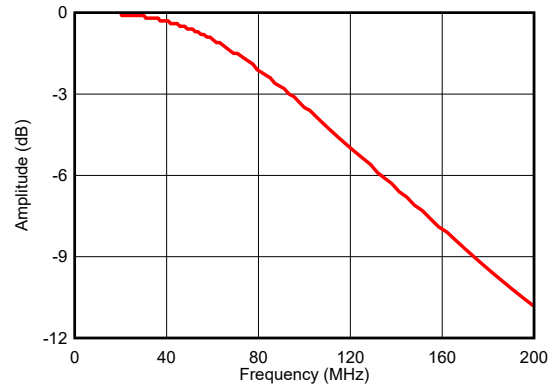
Typical INL = ±0.3 LSB

Figure 5-8. Typical INL



Typical DNL = ±0.3 LSB

Figure 5-9. Typical DNL

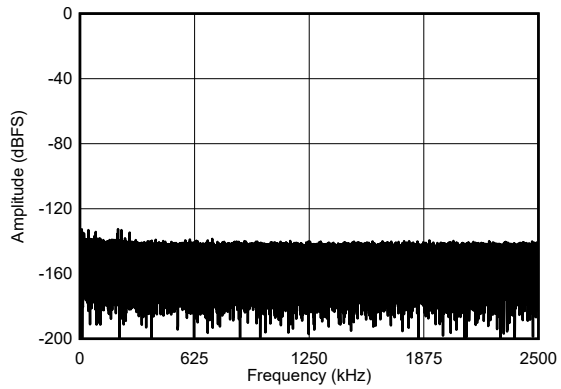


Typical BW (–3 dB) = 90 MHz

Figure 5-10. Typical Analog Input Bandwidth

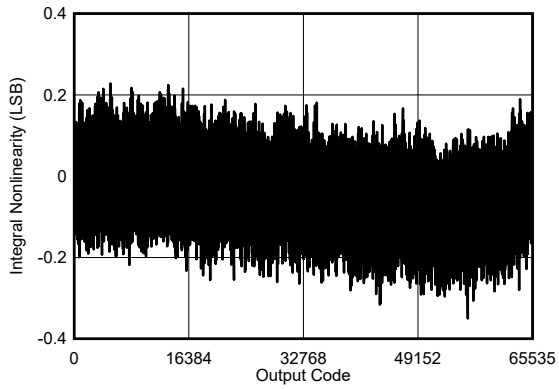
5.10 Typical Characteristics: ADS9227

at T_A = 25°C, AVDD_5V = 5 V, AVDD_1V8 = 1.8 V, DVDD_1V8 = 1.8 V, internal V_{REF} = 4.096 V, and maximum throughput (unless otherwise noted)



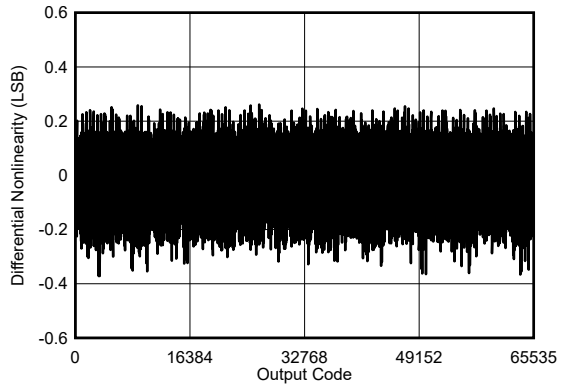
f_{IN} = 2 kHz, SNR = 94.4 dB, THD = –115 dB

Figure 5-11. Typical FFT



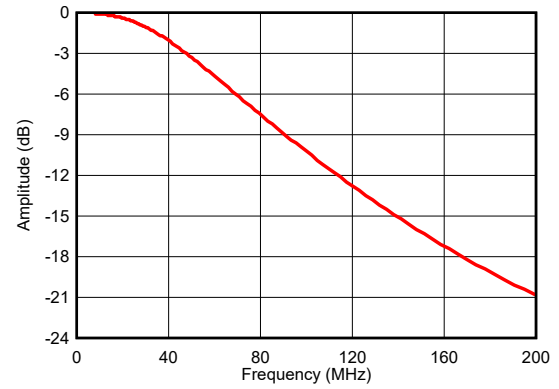
Typical INL = ±0.3 LSB

Figure 5-12. Typical INL



Typical DNL = ±0.3 LSB

Figure 5-13. Typical DNL



Typical BW (–3 dB) = 45 MHz

Figure 5-14. Typical Analog Input Bandwidth

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6 Detailed Description

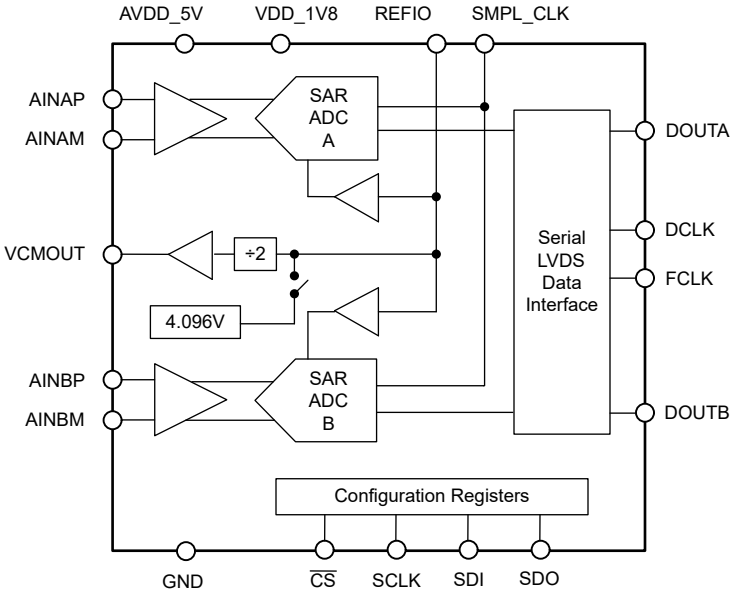
6.1 Overview

The ADS922x is a 16-bit, 20-MSPS/ch, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC). The ADS922x integrates a high-impedance buffer at the ADC inputs, voltage reference, reference buffer, and common-mode voltage output buffer. The ADS9228 supports unipolar differential analog input signals. The buffer at the ADC inputs is optimized for low-distortion and low-power operation.

For DC level shifting of the analog input signals, the device has a common-mode voltage output buffer. The common-mode voltage is derived from the output of the integrated reference buffer. When a conversion is initiated, the differential input between the (AINAP – AINAM) and (AINBP – AINBM) pins is sampled. The ADS922x uses a clock input on the SMPL_CLKP pin to initiate conversions.

The ADS922x consumes only 141 mW/ch of power when operating at 10 MSPS/ch, which includes the power dissipation of the buffer at the ADC inputs. The serial LVDS (SLVDS) digital interface simplifies board layout, timing, firmware, and supports full throughput at lower clock speeds.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Analog Inputs

The ADS922x supports both AC-coupled and DC-coupled differential analog inputs. The input common-mode voltage of the analog inputs must match the voltage level on the VCMOUT pin. Figure 6-1 shows the equivalent input network diagram of the device.

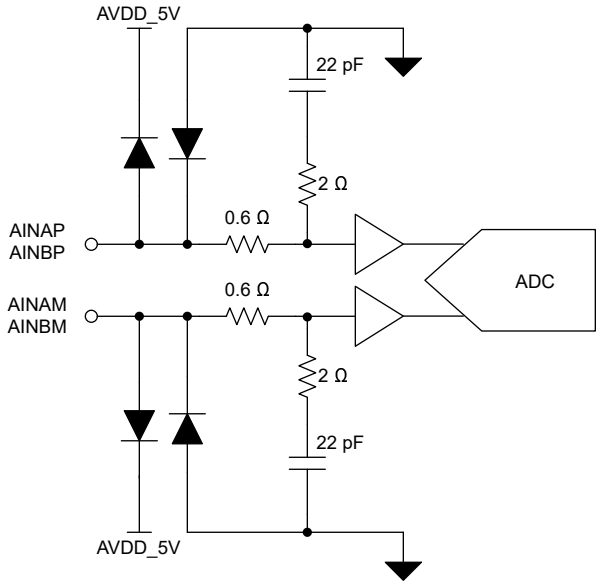

Figure 6-1. Equivalent Input Network

6.3.2 Analog Input Bandwidth

Figure 5-10 illustrates the analog full-power input bandwidth of the ADS922x device family. The –3-dB bandwidth is 135 MHz, 90 MHz, and 45 MHz for the ADS9228 and ADS9227, respectively.

6.3.3 ADC Transfer Function

The ADS922x supports a ±3.2-V differential input range. The device outputs 16-bit conversion data in either straight-binary or binary 2's-complement formats. As shown in Table 6-1, the format for the output codes is the same across all analog channels. The format for the output codes can be configured using the DATA_FORMAT field in register address 0x0D. The least significant bit (LSB) for the ADC is given by 1 LSB = 6.4 V / 2^{16} .

Table 6-1. Transfer Characteristics

INPUT VOLTAGE	DESCRIPTION	ADC OUTPUT IN 2's-COMPLEMENT FORMAT	ADC OUTPUT IN STRAIGHT-BINARY FORMAT
≤ –3.2 V + 1 LSB	Negative full-scale code	0x8000 0x80000	0x0000 0x00000
0 V + 1 LSB	Mid-code	0x0000 0x00000	0x7FFF 0x1FFFF
≥ 3.2 V – 1 LSB	Positive full-scale code	0x7FFF 0x1FFFF	0xFFFF 0x3FFFF

6.3.4 Reference

The ADS922x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 10-µF ceramic bypass capacitor to the REFIO pin. An external reference can also be connected at the REFIO pin with the internal reference voltage disabled by writing to PD_REF field in register address 0xC1.

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6.3.4.1 Internal Reference Voltage

The ADS922x features an internal reference voltage with a nominal output voltage of 4.096 V. On power-up, the internal reference is enabled by default. Place a minimum 10-µF decoupling capacitor between the REFIO and REFM pins. Figure 6-2 shows a block diagram of the internal reference voltage.

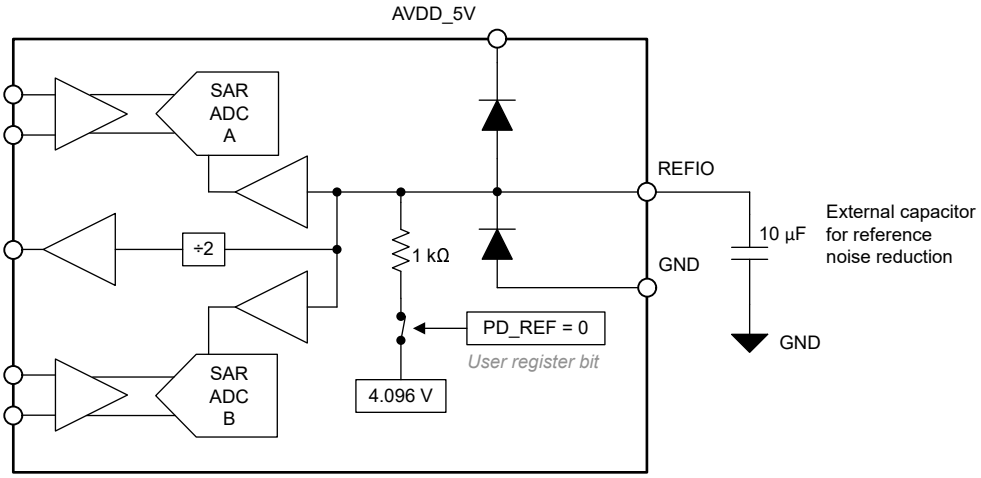

Figure 6-2. Internal Reference Voltage

6.3.4.2 External Reference Voltage

An external 4.096-V reference voltage can be connected at the REFIO pin with an appropriate decoupling capacitor placed between the REFIO and REFM pins. For improved thermal drift performance, the REF7040 is recommended. To disable the internal reference, set PD_REF = 1b in address 0xC1 in register bank 1. The REFIO pin has electrostatic discharge (ESD) protection diodes connected to the AVDD_5V and REFM pins. Figure 6-3 shows an external reference diagram.

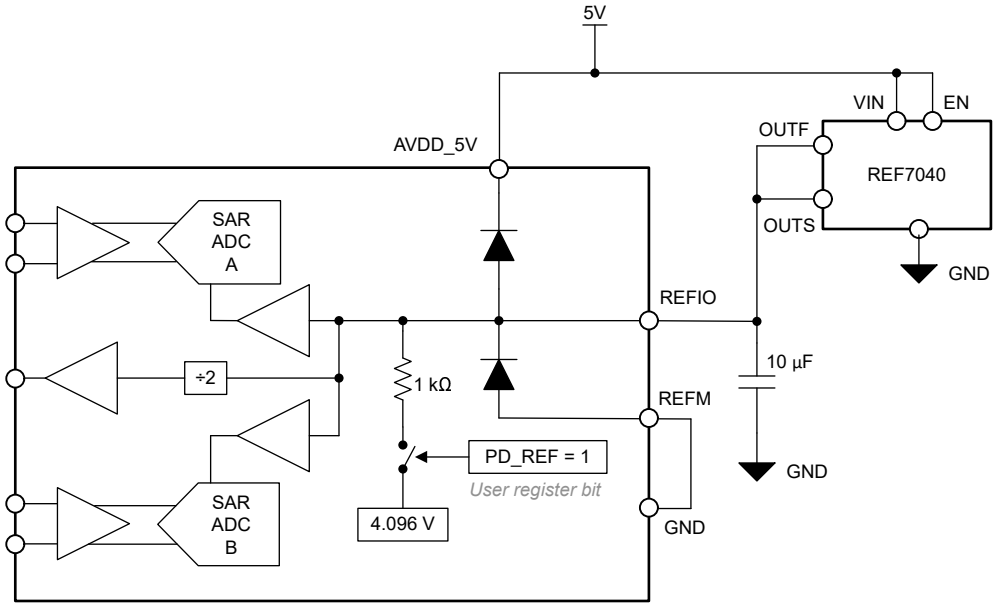

Figure 6-3. External Reference Voltage

6.3.5 Data Averaging

The ADS922x features built in data averaging that decimates the conversions results from the ADC. The output data-rate is reduced with higher data averaging. Table 6-2 shows the register settings corresponding to oversampling ratios supported by the ADS9228 and ADS9227.

Table 6-2. Register Map Settings for OSR

OSR	REGISTER	VALUE
OSR Initialization	CLK3 (0xC5[9])	1
	OSR_INIT1 (0xC0[11:10])	0 for DATA_LANES = 5 or 7 1 for DATA_LANES = 0 or 2
	OSR_INIT2 (0xC4[5:4])	2
	OSR_INIT3 (0xC4[1])	1
	OSR_EN (0x0D[6])	1
2	OSR (0x0D[5:2])	0
	OSR_CLK (0xC0[9:7])	0
4	OSR (0x0D[5:2])	1
	OSR_CLK (0xC0[9:7])	4
8	OSR (0x0D[5:2])	2
	OSR_CLK (0xC0[9:7])	5
16	OSR (0x0D[5:2])	3
	OSR_CLK (0xC0[9:7])	6

6.3.6 Data Interface

The ADS922x features a high-speed serial LVDS data interface with 2-lane and 1-lane options for data output. The host can configure the output data frame width to 20 bits or 24 bits with the single-data rate (SDR) and double-data rate (DDR) modes as shown in Table 6-4

The ADS922x generates a data clock DCLK that is a multiple of the ADC sampling clock SMPL_CLK. The data clock frequency depends on the number of data output lanes (1 or 2), data frame width (20 bit or 24 bit) and data rate (SDR or DDR). Equation 1 calculates the DCLK speed. Table 6-3 lists the possible values for the output data clock frequency.

$$\text{DCLK speed} = \frac{2\ \text{ADC channels} \times \text{Data Frame Width (24 bit or 20 bit)}}{\text{Data Lanes (1 or 2)} \times \text{Data Rate(SDR} = 1,\ \text{DDR} = 2)} \times \text{SMPL\_CLK} \quad (1)$$

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Table 6-3. Data Clock (DCLK) Speed[1]

ADC CHANNELS	DATA FRAME WIDTH (Bits)	DATA RATE (1 = SDR, 2 = DDR)	OUTPUT LANES	SMPL_CLK MULTIPLIER	DCLK (SMPL_CLK = 5 MHz)	DCLK (SMPL_CLK = 10 MHz)
2	24	1	1	48	240 MHz	480 MHz
			2	24	120 MHz	240 MHz
		2	1	24	120 MHz	240 MHz
			2	12	60 MHz	120 MHz
	20	1	1	40	200 MHz	400 MHz
			2	20	100 MHz	200 MHz
		2	1	20	100 MHz	200 MHz
			2	10	50 MHz	100 MHz

(1) The LVDS output data and clock are specified up to 600 MHz. Faster speeds are not supported.

Table 6-4. Register Map Settings for Output Data Interface

DATA FRAME WIDTH (Bits)	DATA RATE	OUTPUT LANES	DATA_LANES 0x12[2:0]	DATA_RATE 0xC1[8]	CLK1 0xC0[12]	CLK2 0xC1[0]	CLK3 0xC5[9]
20	SDR	1	5	1	1	1	1
20	SDR	2	0	1	0	1	0
20	DDR	1	5	0	1	1	1
20	DDR	2	0	0	0	1	0
24	SDR	1	7	1	1	0	1
24	SDR	2	2	1	0	0	0
24	DDR	1	7	0	1	0	1
24	DDR	2	2	0	0	0	0

6.3.6.1 Data Frame Width

As shown in Figure 6-4, the ADS922x supports 24-bit and 20-bit data frame width options. Configure the DATA_WIDTH field in address 0x12 to select the data frame width. The default output data frame width is 24 bits. The ADC resolution is 18 bits, represented by 20 bits. The two extra lower bits in the 20-bit data can be ignored.

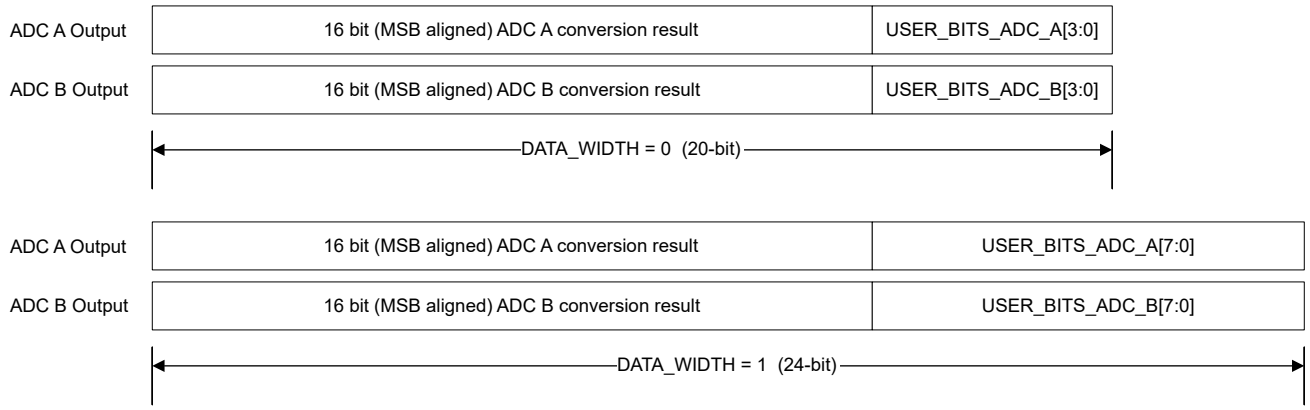

Figure 6-4. Data Frame Width Composition

6.3.6.2 Test Patterns for Data Interface

The ADS922x features test patterns that can be used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. The test patterns can be enabled by configuring the corresponding register addresses 0x13 through 0x1B in bank 1.

The ADS922x supports the following test patterns:

- User-defined output: User-defined, 24-bit pattern. Separate patterns for ADC A and ADC B; see the *User-defined Test Pattern* section.
- Ramp output: Digital ramp output with a user-defined increment between two steps. There are separate ramp outputs for ADC A and ADC B; see the *Ramp Test Pattern* section.
- Alternate output: User-defined, 24-bit outputs that alternate between two user-defined patterns; see the *User-defined Alternating Test Pattern* section.

To disable the test patterns, set TEST_PAT_EN_CHA and TEST_PAT_EN_CHB to 0b.

6.3.6.2.1 User-defined Test Pattern

The user-defined test pattern allows the host to specify a fixed 24-bit value that is output by the ADS922x. Configure the registers in bank 1 to enable the user-defined test pattern:

- Configure the test patterns in TEST_PAT0_ADC_A (address = 0x15 MSB, 0x14 LSB) and TEST_PAT0_ADC_B (address = 0x1A MSB, 0x19 LSB)
- Set TEST_PAT_EN_ADC_A = 1, TEST_PAT_MODE_ADC_A = 0 (address = 0x13) and TEST PAT_EN_ADC_B = 1, TEST_PAT_MODE_ADC_B = 0 (address = 0x18)

The ADS922x outputs the TEST_PAT0_ADC_A (address 0x15 [7:0], address 0x14 [15:0]) and TEST_PAT0_ADC_B (address 0x1A [7:0], address 0x19 [15:0]) register values in place of ADC A and ADC B data, respectively.

6.3.6.2.2 User-defined Alternating Test Pattern

The user-defined alternating test pattern allows the host to specify two fixed 24-bit values that are output by the ADS922x alternately. Configure the registers in bank 1 to enable the user-defined alternating test pattern:

- Configure the test patterns in TEST_PAT0_CHA (address = 0x14, 0x15), TEST_PAT1_CHA (address = 0x15, 0x16) and TEST_PAT0_CHB (address = 0x19, 0x1A), TEST_PAT1_CHB (address = 0x1A, 0x1B)
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 3 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 3 (address = 0x18)

The ADS922x outputs the TEST_PAT0_CHA and TEST_PAT0_CHB register values in place of the ADC A and ADC B data, respectively, in one output frame and the TEST_PAT1_CHA and TEST_PAT1_CHB register values in the next frame.

6.3.6.2.3 Ramp Test Pattern

The ramp test pattern allows the host to specify a digital ramp that is output by the ADS922x. Configure the registers in bank 1 to enable the ramp test pattern:

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC_CHA (address = 0x13) and RAMP_INC_CHB (address = 0x18) registers, respectively. The digital ramp increments by N + 1, where N is the value configured in these registers.
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 2 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 2 (address = 0x18).

The ADS922x outputs digital ramp values in place of the ADC A and ADC B data, respectively.

6.3.7 ADC Sampling Clock Input

Use a low-jitter external clock with a high slew rate to maximize SNR performance. The ADS922x can be operated with a differential or a single-ended clock input. Clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, provide a clock signal with fast slew rates that maximizes swing between IOVDD and GND levels.

The sampling clock must be a free-running continuous clock. The ADC generates a valid output data, data clock, and frame clock $t_{PU\_SMPL\_CLK}$, as specified in the *Switching Characteristics* after a free-running sampling clock is applied. The ADC output data, data clock, and frame clock are invalid when the sampling clock is stopped.

Figure 6-5 shows a diagram of the differential sampling clock input. For this configuration, connect the differential sampling clock input to the SMPL_CLKP and SMPL_CLKM pins. Figure 6-6 shows a diagram of the single-

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ended sampling clock input. In this configuration, connect the single-ended sampling clock to SMPL_CLKP and connect SMPL_CLKM to ground.

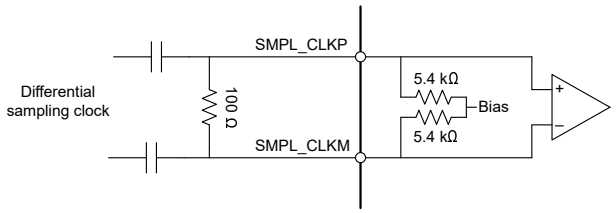

Figure 6-5. AC-coupled Differential Sampling Clock

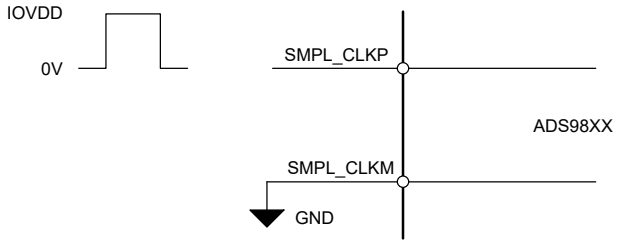

Figure 6-6. Single-ended Sampling Clock

6.4 Device Functional Modes

6.4.1 Reset

The ADS922x can be powered down by either a logic 0 on the $\overline{\text{RESET}}$ pin or by writing 1b to the RESET field in address 0x00 in register bank 0. The device registers are initialized to the default values after reset and the device must be initialized with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.2 Power-down Options

The ADS922x can be powered down by either a logic 0 on the $\overline{\text{PWDN}}$ pin or by writing 11b to the PD_CH field in address 0xC0 in register bank 1. The device registers are initialized to the default values after power-up and the device must be initialized with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.3 Normal Operation

In normal operating mode, the ADS922x is powered-up and digitizes the analog inputs at the falling edge of the sampling clock. The ADC outputs the data clock, frame clock, and MSB-aligned, 16-bit conversion result.

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6.4.4 Initialization Sequence

As shown in Table 6-5, the ADS922x must be initialized by a sequence of register writes after device power-up or reset. A free-running sampling clock must be connected to the ADC before executing the initialization sequence. The ADS922x registers are initialized with the default value after the initialization sequence is complete.

Table 6-5. ADS922x Initialization Sequence

STEP NUMBER	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	0	0x03	0x0002	Select register bank 1
2	1	0xF6	0x0002	INIT_2 = 1
3	0	0x04	0x000B	INIT_1 = 1011b
4	0	0x03	0x0010	Select register bank 2
5	2	0x12	0x0040	INIT_3 = 1
6	2	0x13	0x8000	INIT_4 = 1
7	2	0x0A	0x4000	INIT_5 = 1
8	Wait 10 µs (min)			
9	2	0x0A	0x0000	INIT_5 = 0
10	0	0x03	0x0002	Select register bank 1
11	1	0xF6	0x0000	INIT_2 = 0
12	0	0x03	0x0010	Select register bank 2
13	2	0x13	0x0000	INIT_5 = 0
14	2	0x12	0x0000	INIT_4 = 0
15	0	0x04	0x0000	INIT_1 = 0
16	0	0x03	0x0002	Select register bank 1
17	1	0x33	0x0030	Write INIT_KEY
18	1	0xF4	0x0000	INIT = 0
19	1	0xF4	0x0002	INIT = 1
20	Wait 1 ms (min)			
21	1	0xF4	0x0000	INIT = 0
22	Wait 1 ms (min)			
23	1	0x33	0x0000	INIT_KEY = 0
24	1	0x0D	<user-defined>	Enable gain error calibration and select ADC output data format
25	1	0x33	0x2040	Enable gain error calibration

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6.5 Programming

6.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Register bank 1 and register bank 2 can be selected for read or write operation by configuring the PAGE_SEL0 and PAGE_SEL1 bits, respectively. Registers in bank 0 are always accessible, irrespective of the PAGE_SELx bits because the register addresses in bank 0 are unique and are not used in register banks 1 and 2.

As shown in Figure 6-7, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to a register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

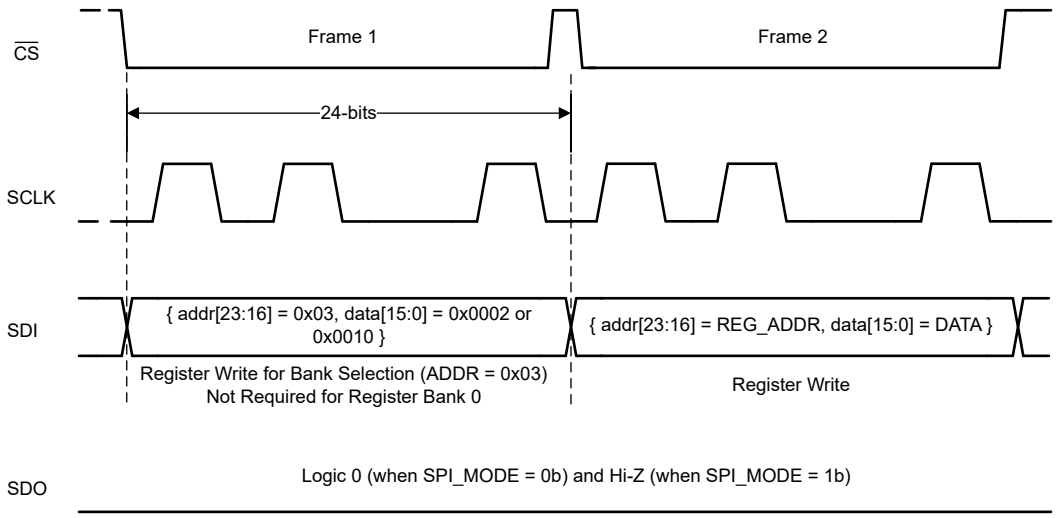

Figure 6-7. Register Write

6.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Register read access is enabled by setting SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0. As illustrated in Figure 6-8, registers can be read using two 24-bit SPI frames after SPI_RD_EN and SPI_MODE are set. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in Figure 6-8, steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank 0 for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register reads and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.

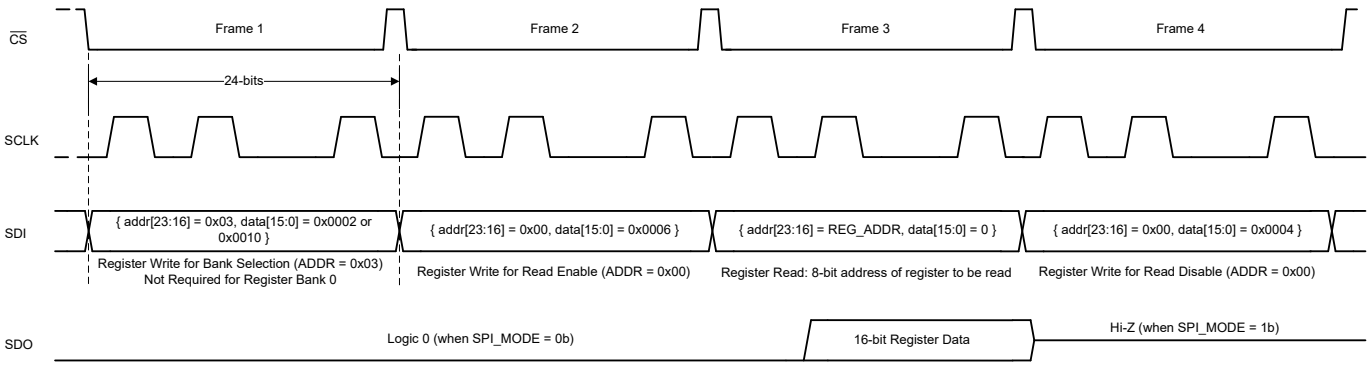

Figure 6-8. Register Read

6.5.3 Multiple Devices: Daisy-Chain Topology for SPI Configuration

Figure 6-9 shows a typical connection diagram showing multiple devices in a daisy-chain topology.

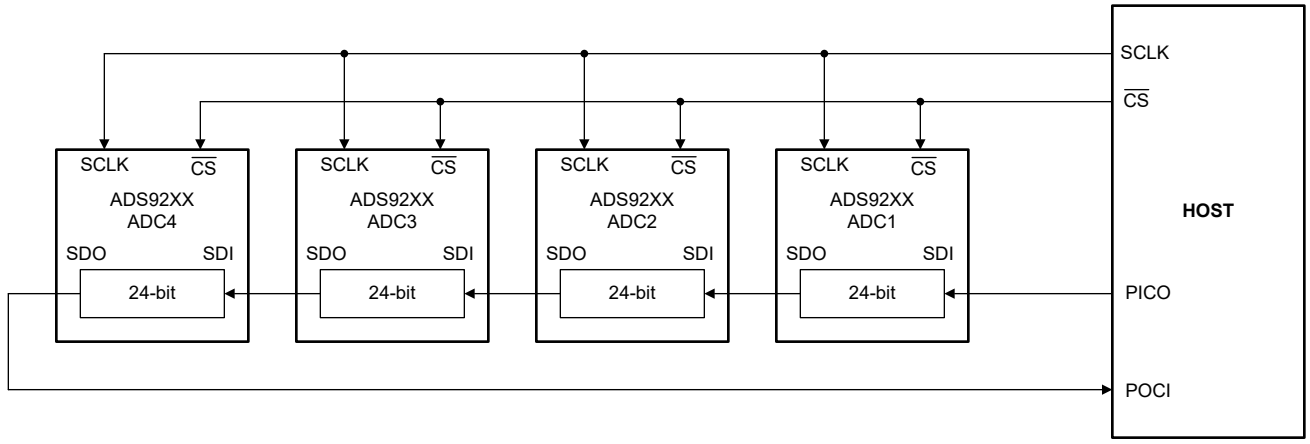

Figure 6-9. Daisy-Chain Connections for SPI Configuration

The $\overline{CS}$ and SCLK inputs of all ADCs are connected together and are controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller, the SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{CS}$ is active.

The daisy-chain mode must be enabled after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LENGTH register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain, excluding ADC1. In Figure 6-9, the DAISY_CHAIN_LENGTH is 3.

6.5.3.1 Register Write With Daisy-Chain

Writing to registers in daisy-chain configuration requires N × 24 SCLKs in one SPI frame. Register writes in a daisy-chain configuration containing four ADCs, as illustrated in Figure 6-9, requires 96 SCLKs.

The daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LENGTH field to enable daisy-chain mode. The waveform in Figure 6-10 must be repeated N times, where N is the number of ADCs in the daisy-chain. Figure 6-11 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

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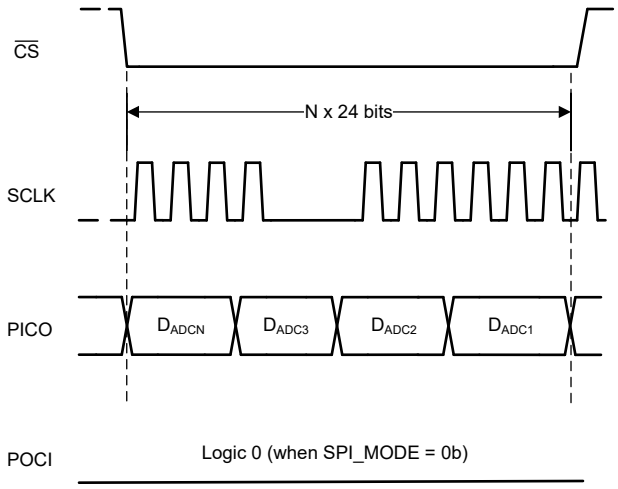

Figure 6-10. Register Write With Daisy-Chain

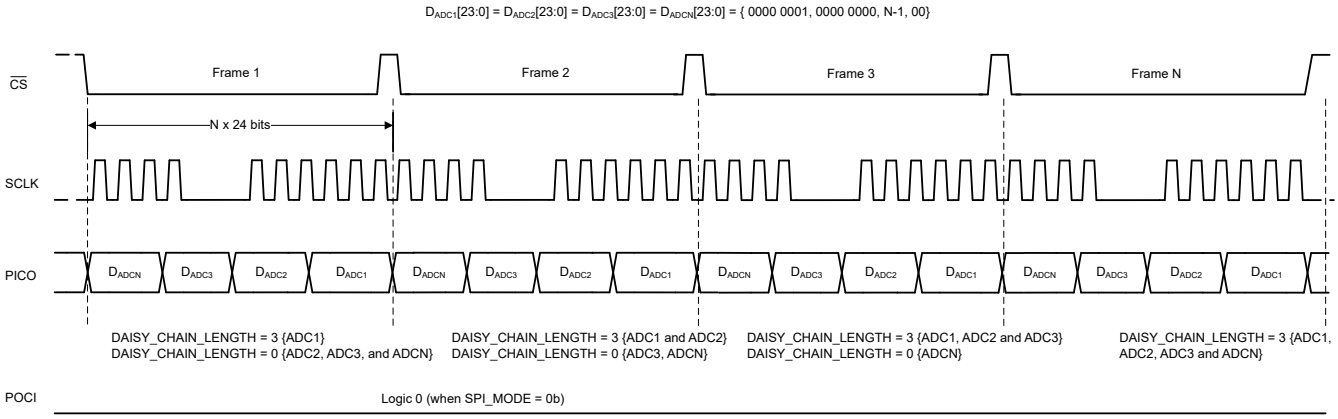

Figure 6-11. Register Write to Configure Daisy-Chain Length

6.5.3.2 Register Read With Daisy-Chain

Figure 6-12 illustrates an SPI waveform for reading registers in daisy-chain configuration. Steps for reading registers from N ADCs connected in daisy-chain are:

1. Register read is enabled by writing to the following registers:
   a. Write to PAGE_SEL to select the desired register bank
   b. Enable register reads by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller can read register data by:
   a. N × 24-bit SPI frame containing the 8-bit register address to be read: N times (0xFE, 0x00, 8-bit register address)
   b. N × 24-bit SPI frame to read out register data: N times (0xFF, 0xFF, 0xFF)

The 0xFE in step 2a configures the ADC for register read from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.

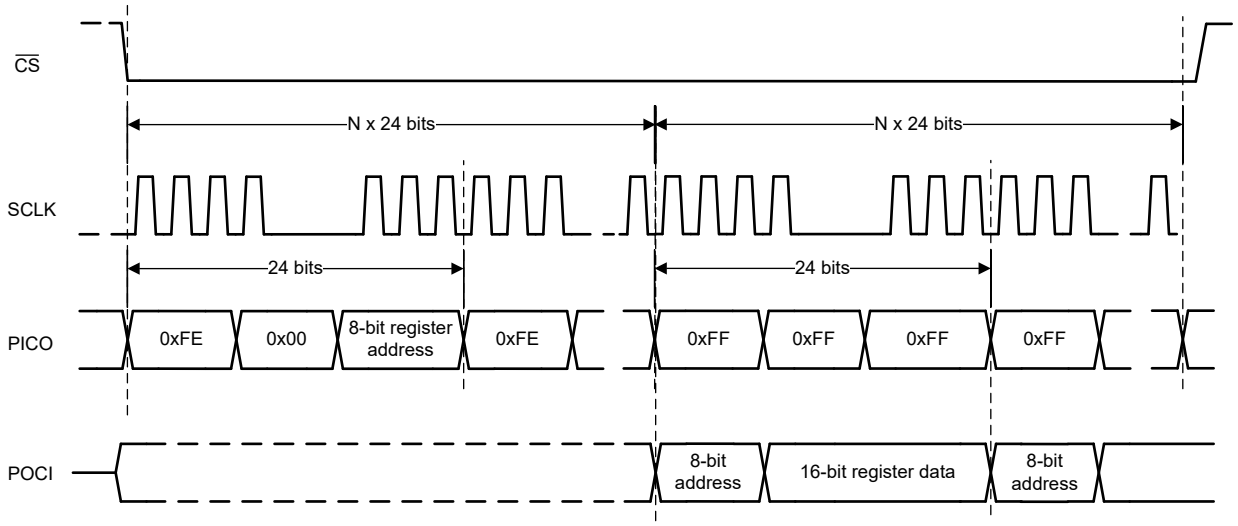

Figure 6-12. Register Read With Daisy-Chain

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7 Register Map

7.1 Register Bank 0

Figure 7-1. Register Bank 0 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	RESERVED													SPI_MODE	SPI_RD_EN	RESET
01h	RESERVED									DAISY_CHAIN_LEN					RESERVED	
03h	RESERVED									REG_BANK_SEL						
04h	RESERVED												INIT_1			
06h	REG_00H_READBACK															

Table 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.1.2 Register 00h (offset = 0h) [reset = 0h]

Figure 7-2. Register 00h

15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED					SPI_MODE	SPI_RD_EN	RESET
W-0h					W-0h	W-0h	W-0h

Figure 7-3. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	W	0h	Reserved. Do not change from the default reset value.
2	SPI_MODE	W	0h	Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface for register access. 0 : Daisy-chain SPI mode 1 : Legacy SPI mode
1	SPI_RD_EN	W	0h	Enable register read access in legacy SPI mode. This bit has no effect in daisy-chain SPI mode. 0 : Register read disabled 1 : Register read enabled
0	RESET	W	0h	ADC reset control. 0 : Normal device operation 1 : Reset ADC and all registers

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7.1.3 Register 01h (offset = 1h) [reset = 0h]

Figure 7-4. Register 01h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	DAISY_CHAIN_LEN					RESERVED	
R/W-0h	R/W-0h					R/W-0h	

Figure 7-5. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-2	DAISY_CHAIN_LEN	R/W	0h	Configure the number of ADCs connected in daisy-chain for the SPI configuration. 0 : 1 ADC 1 : 2 ADCs 31 : 32 ADCs
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.1.4 Register 03h (offset = 3h) [reset = 2h]

Figure 7-6. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
REG_BANK_SEL							
R/W-2h							

Figure 7-7. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-0	REG_BANK_SEL	R/W	2h	Register bank selection for read and write operations. 0 : Select register bank 0 2 : Select register bank 1 16 : Select register bank 2

ADVANCE INFORMATION

7.1.5 Register 04h (offset = 4h) [reset = 0h]

Figure 7-8. Register 04h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				INIT_1			
R/W-0h							

Figure 7-9. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
3-0	INIT_1	R/W	0h	INIT_1 field for device initialization. Write 1011b during the initialization sequence. Write 0000b for normal operation.

7.1.6 Register 06h (offset = 6h) [reset = 2h]

Figure 7-10. Register 06h

15	14	13	12	11	10	9	8
REG_00H_READBACK							
R-0h							
7	6	5	4	3	2	1	0
REG_00H_READBACK							
R-5h							

Figure 7-11. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	REG_00H_READBACK	R	2h	This register is a copy of the register address 0x00 for readback. The register address 0x00 is write-only. The default readback value is 2h because SPI_RD_EN in address 0x00 must be set to 1 for register reads.

ADVANCE INFORMATION

7.2 Register Bank 1

Figure 7-12. Register Bank 1 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	RESERVED		DATA_FORMAT	RESERVED					GE_CAL_EN1	OSR_EN	OSR				RESERVED	
12h	RESERVED												XOR_EN	DATA_LANES		
13h	RESERVED								RAMP_INC_ADC_A				TEST_PAT_MODE_ADC_A		TEST_PAT_EN_ADC_A	RESERVED
14h	TEST_PAT0_ADC_A															
15h	TEST_PAT1_ADC_A								TEST_PAT0_ADC_A							
16h	TEST_PAT1_ADC_A															
18h	RESERVED								RAMP_INC_ADC_B				TEST_PAT_MODE_ADC_B		TEST_PAT_EN_ADC_B	RESERVED
19h	TEST_PAT0_ADC_B															
1Ah	TEST_PAT1_ADC_B								TEST_PAT0_ADC_B							
1Bh	TEST_PAT1_ADC_B															
1Ch	RESERVED		USER_BITS_ADC_B						RESERVED		USER_BITS_ADC_A					
33h	RESERVED		GE_CAL_EN3	RESERVED						GE_CAL_EN2	INIT_KEY		RESERVED			
C0h	RESERVED			CLK1	OSR_INIT1				RESERVED						PD_CH	
C1h	RESERVED				PD_REF	RESERVED		DATA_RATE	RESERVED							CLK2
C4h	RESERVED											OSR_INIT2		RESERVED	OSR_INIT3	PD_CHIP
C5h	RESERVED						CLK3	RESERVED								
F4h	RESERVED														INIT	RESERVED
F6h	RESERVED														INIT_2	RESERVED
FBh	RESERVED													XOR_MODE	RESERVED	

Table 7-2. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

ADVANCE INFORMATION

7.2.1 Register 0Dh (offset = Dh) [reset = 2002h]

Figure 7-13. Register 0Dh

15	14	13	12	11	10	9	8
RESERVED		DATA_FORMAT	RESERVED				
R/W-0h		R/W-1h	R/W-0h				
7	6	5	4	3	2	1	0
GE_CAL_EN1	OSR_EN	OSR				RESERVED	
R/W-0h	R/W-2h						

Figure 7-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	DATA_FORMAT	R/W	1h	Select data format for the ADC conversion result. 0 : Straight binary format 1 : Two's-complement format
12-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-7	GE_CAL_EN1	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
6-6	OSR_EN	R/W	0h	Control for data averaging depth. 0 : Data averaging disabled 1 : Data averaging enabled
5-2	OSR	R/W	0h	Control for enabling data averaging. 0 : 2 samples averaged 1 : 4 samples averaged 2 : 8 samples averaged 3 : 16 samples averaged
1-0	RESERVED	R/W	2h	Reserved. Do not change from the default reset value.

7.2.2 Register 12h (offset = 12h) [reset = 2h]

Figure 7-15. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				XOR_EN	DATA_LANES		
R/W-0h				R/W-0h	R/W-2h		

Figure 7-16. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	XOR_EN	R/W	0h	Enables XOR operation on ADC conversion result. 0 : XOR operation is disabled 1 : ADC conversion result is bit-wise XOR with the LSB of the ADC conversion result
2-0	DATA_LANES	R/W	2h	Selects the number of output data-lanes and number of data bits per output lane.Enables XOR operation on ADC conversion result. 0 : ADC A and B data output on DOUTA and DOUTB respectively; 20bits per ADC. 2 : ADC A and B data output on DOUTA and DOUTB respectively; 24bits per ADC. 5 : ADC A and B data output on DOUTA; 20bits per ADC. 7 : ADC A and B data output on DOUTA; 24bits per ADC.

7.2.3 Register 13h (offset = 13h) [reset = 0h]

Figure 7-17. Register 13h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RAMP_INC_ADC_A				TEST_PAT_MODE_ADC_A		TEST_PAT_EN_ADC_A	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Figure 7-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_ADC_A	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TEST_PAT_MODE_ADC_A	R/W	0h	Select digital test pattern for ADC A. 0 : Fixed pattern as configured in the TEST_PAT0_ADC_A register 1 : Fixed pattern as configured in the TEST_PAT0_ADC_A register 2 : Digital ramp output 3 : Alternate fixed pattern output as configured in the TEST_PAT0_ADC_A and TEST_PAT1_ADC_A registers
1	TEST_PAT_EN_ADC_A	R/W	0h	Enable digital test pattern for data corresponding to ADC A. 0 : ADC conversion result is launched on the data interface 1 : Digital test pattern is launched corresponding to ADC A on the data interface
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.4 Register 14h (offset = 14h) [reset = 0h]

Figure 7-19. Register 14h

15	14	13	12	11	10	9	8
TEST_PAT0_ADC_A[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_ADC_A[15:0]							
R/W-0h							

Figure 7-20. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT0_ADC_A[15:0]	R/W	0h	Lower 16 bits of test pattern 0 for ADC A corresponding to ADC A.

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7.2.5 Register 15h (offset = 15h) [reset = 0h]

Figure 7-21. Register 15h

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_A[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_ADC_A[23:16]							
R/W-0h							

Figure 7-22. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TEST_PAT1_ADC_A[7:0]	R/W	0h	Lower eight bits of test pattern 1 for ADC A corresponding to ADC A.
7-0	TEST_PAT0_ADC_A[23:16]	R/W	0h	Upper eight bits of test pattern 0 for ADC A corresponding to ADC A.

7.2.6 Register 16h (offset = 16h) [reset = 0h]

Figure 7-23. Register 16h

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_A[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT1_ADC_A[23:8]							
R/W-0h							

Figure 7-24. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT1_ADC_A[23:8]	R/W	0h	Upper 16 bits of test pattern 1 for ADC A corresponding to ADC A.

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7.2.7 Register 18h (offset = 18h) [reset = 0h]

Figure 7-25. Register 18h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RAMP_INC_ADC_B				TEST_PAT_MODE_ADC_B		TEST_PAT_EN_ADC_B	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Figure 7-26. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_ADC_B	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TEST_PAT_MODE_ADC_B	R/W	0h	Select digital test pattern for ADC B. 0 : Fixed pattern as configured in the TEST_PAT0_ADC_B register 1 : Fixed pattern as configured in the TEST_PAT0_ADC_B register 2 : Digital ramp output 3 : Alternate fixed pattern output as configured in the TEST_PAT0_ADC_B and TEST_PAT1_ADC_B registers
1	TEST_PAT_EN_ADC_B	R/W	0h	Enable digital test pattern for data corresponding to channel 5, 6, 7, and 8. 0 : ADC conversion result is launched on the data interface 1 : Digital test pattern is launched corresponding to ADC B on the data interface
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.8 Register 19h (offset = 19h) [reset = 0h]

Figure 7-27. Register 19h

15	14	13	12	11	10	9	8
TEST_PAT0_ADC_B[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_ADC_B[15:0]							
R/W-0h							

Figure 7-28. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT0_ADC_B[15:0]	R/W	0h	Lower 16 bits of test pattern 0 for ADC B corresponding to ADC B.

ADVANCE INFORMATION

7.2.9 Register 1Ah (offset = 1Ah) [reset = 0h]

Figure 7-29. Register 1Ah

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_B[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_ADC_B[23:16]							
R/W-0h							

Figure 7-30. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TEST_PAT1_ADC_B[7:0]	R/W	0h	Lower eight bits of test pattern 1 for ADC B corresponding to ADC B.
7-0	TEST_PAT0_ADC_B[23:16]	R/W	0h	Upper eight bits of test pattern 0 for ADC B corresponding to ADC B.

7.2.10 Register 1Bh (offset = 1Bh) [reset = 0h]

Figure 7-31. Register 1Bh

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_B[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT1_ADC_B[23:8]							
R/W-0h							

Figure 7-32. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT1_ADC_B[23:8]	R/W	0h	Upper 16 bits of test pattern 1 for ADC B corresponding to ADC B.

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7.2.11 Register 1Ch (offset = 1Ch) [reset = 0h]

Figure 7-33. Register 1Ch

15	14	13	12	11	10	9	8
RESERVED		USER_BITS_ADC_B					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		USER_BITS_ADC_A					
R/W-0h		R/W-0h					

Figure 7-34. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-8	USER_BITS_ADC_B	R/W	0h	User-defined bits appended to the ADC conversion result from ADC B.
7-0	USER_BITS_ADC_A	R/W	0h	User-defined bits appended to the ADC conversion result from ADC A.

7.2.12 Register 33h (offset = 33h) [reset = 0h]

Figure 7-35. Register 33h

15	14	13	12	11	10	9	8
RESERVED		GE_CAL_EN3	RESERVED				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	GE_CAL_EN2	INIT_KEY		RESERVED			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

Figure 7-36. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	GE_CAL_EN3	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
12-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6	GE_CAL_EN2	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
5-4	INIT_KEY	R/W	0h	Device initialization sequence access key. Write 11b to access the device initialization sequence. Write 00b for normal operation.
3-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.13 Register C0h (offset = C0h) [reset = 0h]

Figure 7-37. Register C0h

15	14	13	12	11	10	9	8
RESERVED			CLK1	OSR_INIT1		RESERVED	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0

Figure 7-37. Register C0h (continued)

RESERVED	PD_CH
R/W-0h	R/W-0h

Figure 7-38. Register C0h Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
12-12	CLK1	R/W	0h	Selects the clock configuration based on output data-lanes. 0 : Configuration for DATA_LANES = 0 or 2 1 : Configuration for DATA_LANES = 5 or 7
11-10	OSR_INIT1	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 1 : Configuration for enabling data averaging
9-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1-0	PD_CH	R/W	0h	Power-down control for the analog input channels. 0 : Normal operation 1 : ADC A powered down 2 : ADC B powered down 3 : ADC A and B powered down

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7.2.14 Register C1h (offset = C1h) [reset = 0h]

Figure 7-39. Register C1h

15	14	13	12	11	10	9	8
RESERVED				PD_REF	RESERVED		DATA_RATE
R/W-0h				R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CLK2
R/W-0h							R/W-0h

Figure 7-40. Register C1h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
11	PD_REF	R/W	0h	ADC reference voltage source selection. 0 : Internal reference enabled. 1 : Internal reference disabled. Connect the external reference voltage to the REFIO pin.
10-9	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
8	DATA_RATE	R/W	0h	Select data rate for the data interface. 0 : Double data rate (DDR) 1 : Single data rate (SDR)
7-1	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
0	CLK2	R/W	0h	Select data rate for the data interface. 0 : Configuration for DATA_LANES = 2 or 7 1 : Configuration for DATA_LANES = 0 or 5

7.2.15 Register C4h (offset = C4h) [reset = 0h]

Figure 7-41. Register C4h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		OSR_INIT2		RESERVED		OSR_INIT3	PD_CHIP
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h

Figure 7-42. Register C4h Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
5-4	OSR_INIT2	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 2 : Configuration for enabling data averaging
3-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1-1	OSR_INIT3	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 1 : Configuration for enabling data averaging
0-0	PD_CHIP	R/W	0h	Full chip power-down control. 0 : Normal device operation 1 : Full device powered-down

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7.2.16 Register C5h (offset = C5h) [reset = 0h]

Figure 7-43. Register C5h

15	14	13	12	11	10	9	8
RESERVED						CLK3	RESERVED
R/W-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Figure 7-44. Register C5h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9	CLK3	R/W	0h	Select data rate for the data interface. 0 : Configuration for DATA_LANES = 0 or 2 1 : Configuration for DATA_LANES = 5 or 7

7.2.17 Register F4h (offset = F4h) [reset = 0h]

Figure 7-45. Register F4h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						CM_CTRL_EN	RESERVED
R/W-0h						R/W-0h	R/W-0h

Figure 7-46. Register F4h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT	R/W	0h	INIT field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

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7.2.18 Register F6h (offset = F6h) [reset = 0h]

Figure 7-47. Register F6h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						INIT_2	RESERVED
R/W-0h						R/W-0h	R/W-0h

Figure 7-48. Register F6h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT_2	R/W	0h	INIT_2 field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

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7.2.19 Register FBh (offset = FBh) [reset = 0h]

Figure 7-49. Register FBh

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					XOR_MODE	RESERVED	
R/W-0h					R/W-0h	R/W-0h	

Figure 7-50. Register FBh Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
2	XOR_MODE	R/W	0h	Selects the bit with which the ADC output data is XOR'ed when XOR output mode is enabled. 0 : PRBS bit is output after the ADC LSB. ADC output data is XOR with the PRBS bit. 1 : ADC output data is XOR with the LSB of the conversion result.
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

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7.3 Register Bank 2

Figure 7-51. Register Bank 2 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12h	RESERVED									INIT_3	RESERVED					
13h	INIT_4	RESERVED														
0Ah	RESERVED	INIT_2	RESERVED													

Table 7-3. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1 Register 12h (offset = 12h) [reset = 0h]

Figure 7-52. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	INIT_3	RESERVED					
R/W-0h	R/W-0h	R/W-0h					

Figure 7-53. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-6	INIT_3	R/W	0h	INIT_3 field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
5-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3.2 Register 13h (offset = 13h) [reset = 0h]

Figure 7-54. Register 13h

15	14	13	12	11	10	9	8
INIT_4	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Figure 7-55. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	INIT_4	R/W	0h	INIT_4 field for device initialization. Write 1b during initialization sequence. Write 0b for normal operation.
14-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

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7.3.3 Register 0Ah (offset = 0Ah) [reset = 0h]

Figure 7-56. Register 0Ah

15	14	13	12	11	10	9	8
RESERVED	INIT_5	RESERVED					
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Figure 7-57. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
14	INIT_5	R/W	0h	INIT_5 field for device initialization. Write 1b during initialization sequence. Write 0b for normal operation.
13-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The integrated ADC driver, low-latency, high-speed, low AC and DC errors, and low temperature drift make the ADS922x a high-performance signal-chain for applications where precision measurements with low-latency are required. The following section gives an example circuit and recommendations for using the ADS922x device family in a data acquisition (DAQ) system.

8.2 Typical Applications

8.2.1 Data Acquisition (DAQ) Circuit for ≤20-kHz Input Signal Bandwidth

Figure 8-1 shows a 2-channel signal-chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS922x with the 2-channel, fully differential amplifier (FDA) THS4552.

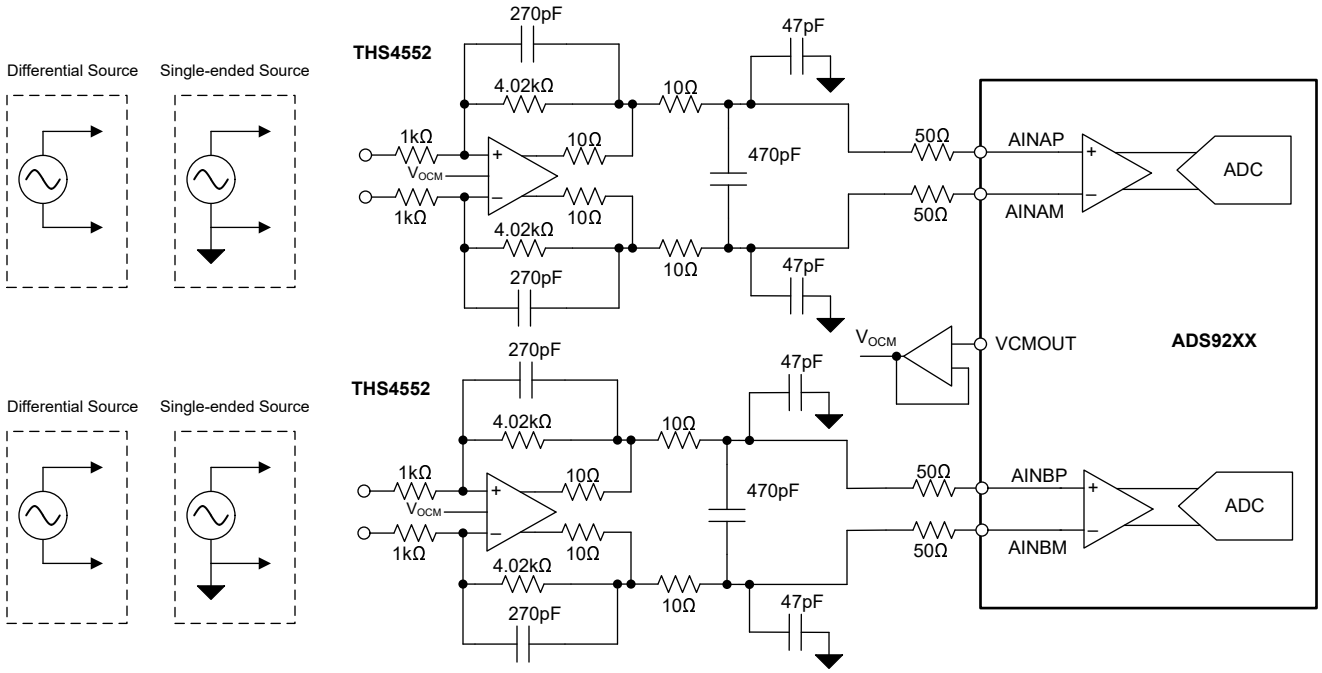


Figure 8-1. Data Acquisition (DAQ) Circuit for ≤20-kHz Input Signal Bandwidth

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Parameters

PARAMETER	VALUE
SNR	≥ 92 dB
THD	≤ –110 dB
Input signal frequency	≤ 20 kHz

ADVANCE INFORMATION

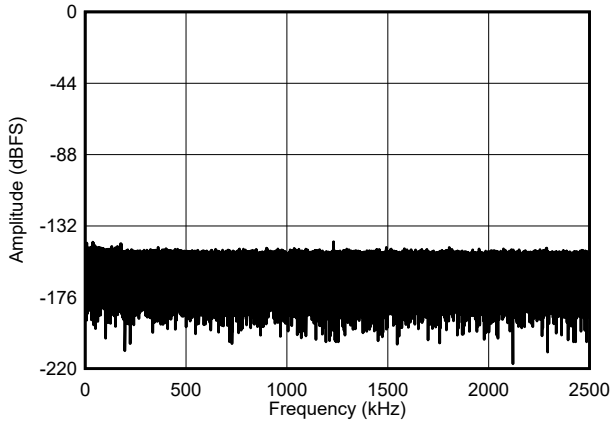
8.2.1.2 Detailed Design Procedure

The procedure discussed in this section can be used for any ADS922x application circuit.

- All ADS922x applications require the supply decoupling as provided in the *Power Supply Recommendations* section.
- The values provided in this section must meet the maximum throughput and input signal frequency design requirements given. A lower bandwidth signal-chain can be used in cases where lower noise performance is required.

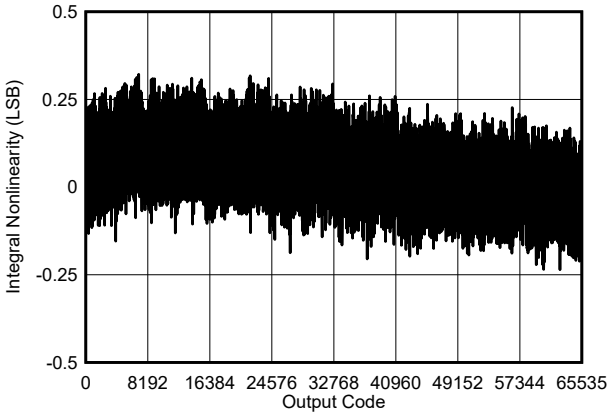
8.2.1.3 Application Curves

Figure 8-2 and Figure 8-3 show the SNR and INL performance for the circuit in Figure 8-1, respectively.



f_{IN} = 2 kHz, SNR = 93.4 dBFS, THD = –120 dB

Figure 8-2. Typical FFT at 5 MSPS/Channel: ADS9227



f_{IN} = 2 kHz, INL = ±0.3 LSB

Figure 8-3. Typical INL at 5 MSPS/Channel: ADS9227

ADVANCE INFORMATION

8.2.2 Data Acquisition (DAQ) Circuit for ≤100-kHz Input Signal Bandwidth

Figure 8-4 shows a 2-channel signal-chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS922x with the 2-channel, fully differential amplifier (FDA) THS4552.

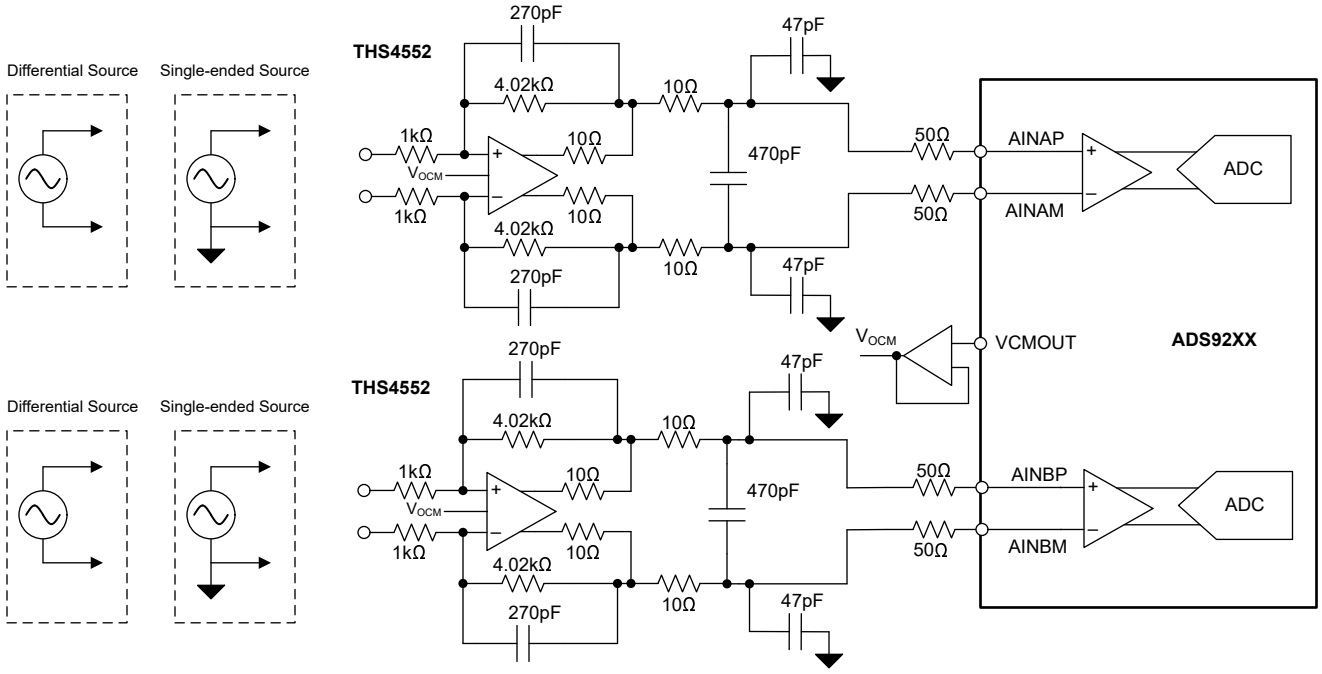


Figure 8-4. Data Acquisition (DAQ) Circuit for ≤100-kHz Input Signal Bandwidth

8.2.2.1 Design Requirements

Table 8-2 lists the parameters for this typical application.

Table 8-2. Design Parameters

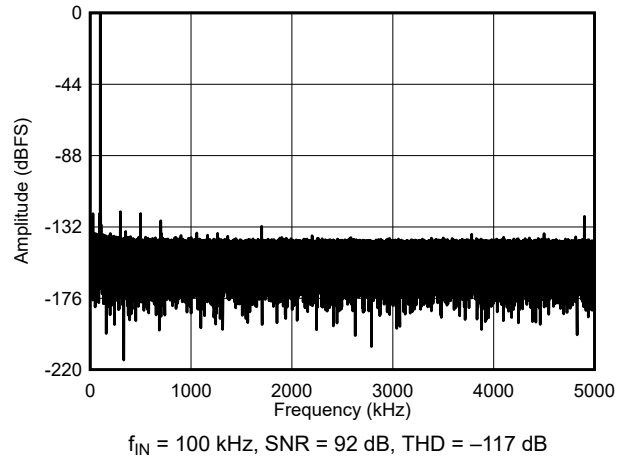
PARAMETER	VALUE
SNR	≥ 91 dB
THD	≤ –110 dB
Input signal frequency	≤ 100 kHz

ADVANCE INFORMATION

ADVANCE INFORMATION

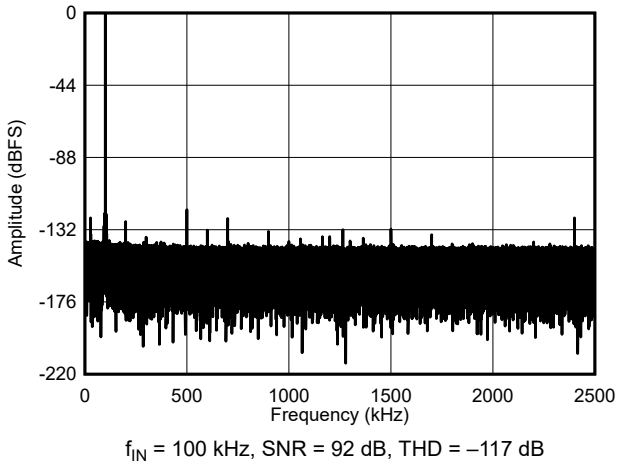
8.2.2.2 Application Curves

Figure 8-5 and Figure 8-6 show the FFT plots for the circuit in Figure 8-4.



f_{IN} = 100 kHz, SNR = 92 dB, THD = –117 dB

Figure 8-5. Typical FFT at 10 MSPS/Channel: ADS9228



f_{IN} = 100 kHz, SNR = 92 dB, THD = –117 dB

Figure 8-6. Typical FFT at 5 MSPS/Channel: ADS9227

8.2.3 Data Acquisition (DAQ) Circuit for ≤1-MHz Input Signal Bandwidth

Figure 8-7 shows a 2-channel solution with minimum external components. This signal-chain significantly reduces signal-chain size by driving the ADS9228 with the THS4541, which enables low-distortion performance with low power over wide signal bandwidth.

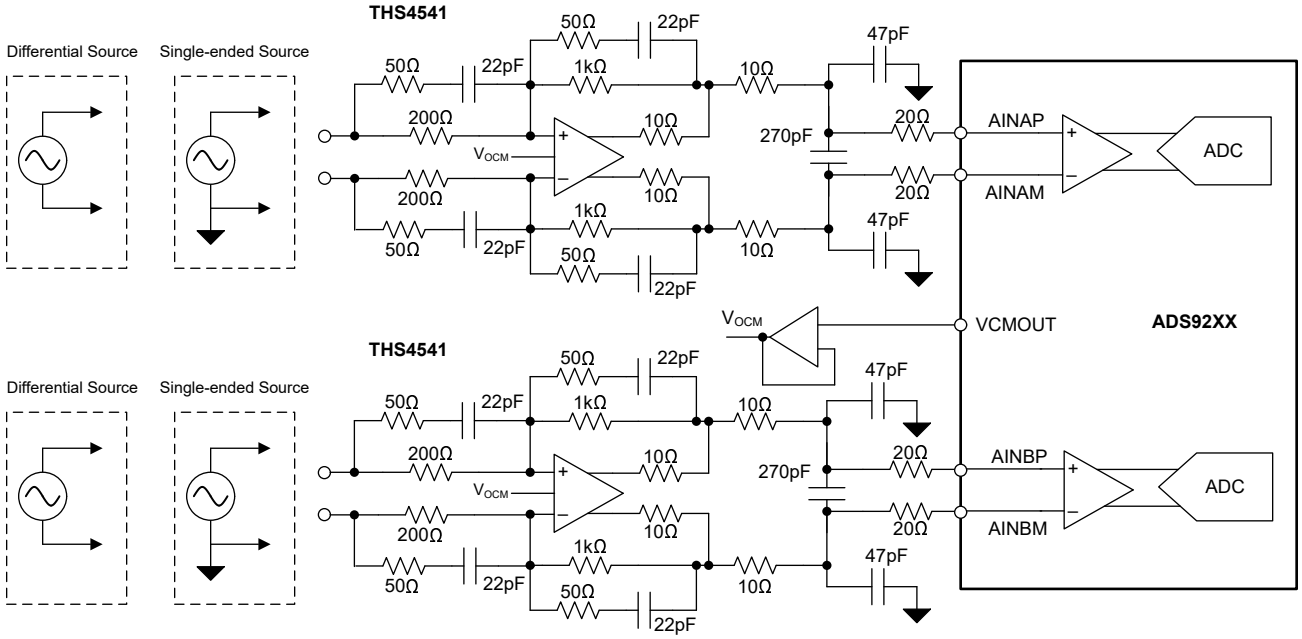


Figure 8-7. Data Acquisition (DAQ) Circuit for ≤1-MHz Input Signal Bandwidth

8.2.3.1 Design Requirements

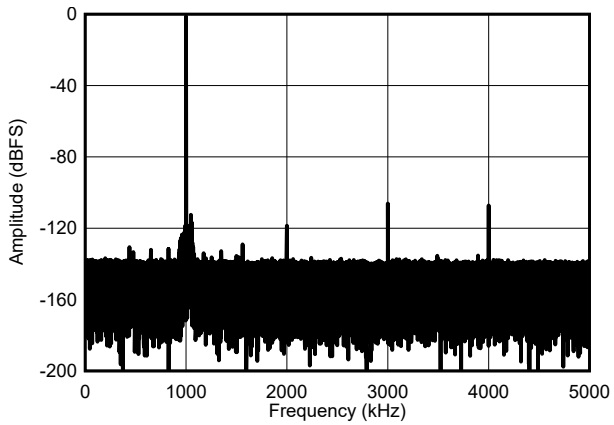
Table 8-3 lists the parameters for this typical application.

Table 8-3. Design Parameters

PARAMETER	VALUE
SNR	≥ 80 dB
THD	≤ –100 dB
Input signal frequency	≤ 1 MHz

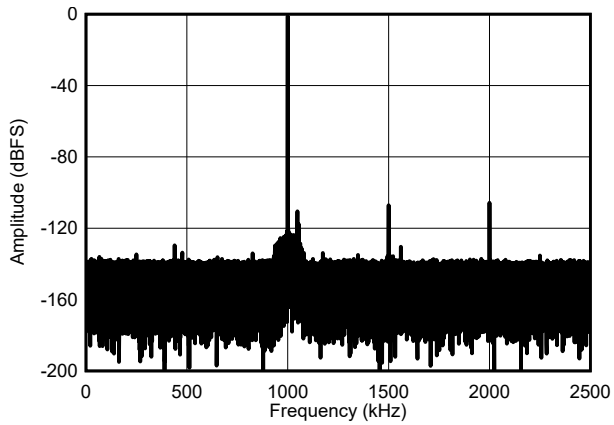
8.2.3.2 Application Curves

Figure 8-8 and Figure 8-9 show the FFT plots for the circuit in Figure 8-7.



f_{IN} = 1 MHz, SNR = 90.6 dB, THD = –104 dB

Figure 8-8. Typical FFT at 10 MSPS/Channel: ADS9228



f_{IN} = 1 MHz, SNR = 90.5 dB, THD = –104.2 dB

Figure 8-9. Typical FFT at 5 MSPS/Channel: ADS9227

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The ADS922x has three independent power supplies, AVDD_5V, AVDD_1V8, and DVDD_1V8. The AVDD_5V supply provides power to the ADC driver. The AVDD_1V8 provides power to the analog circuits. The DVDD_1V8 supply provides power to the digital interface. The AVDD_5, AVDD_1V8, and DVDD_1V8 supplies can be set independently to voltages within the permissible range. Figure 8-10 shows how to decouple the power supplies.

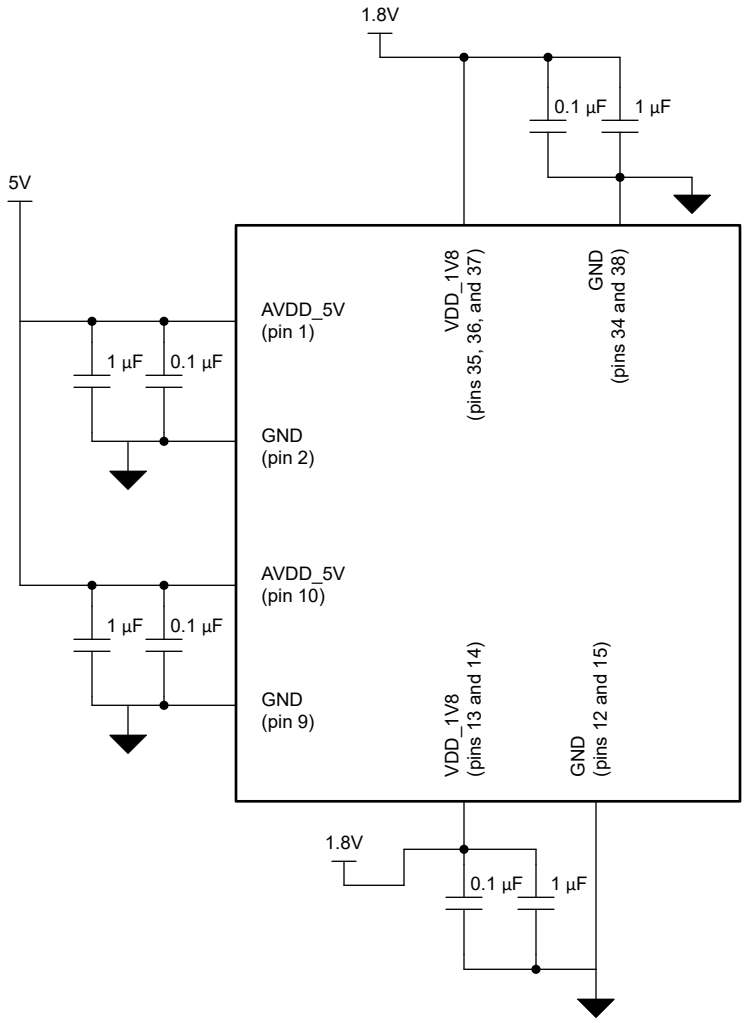


Figure 8-10. Power-supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

Figure 8-11 shows a board layout example for the ADS922x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 0.1-µF ceramic bypass capacitors in close proximity to the analog (AVDD_5V and AVDD_1V8), and digital (DVDD_1V8) power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors. Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

8.4.2 Layout Example

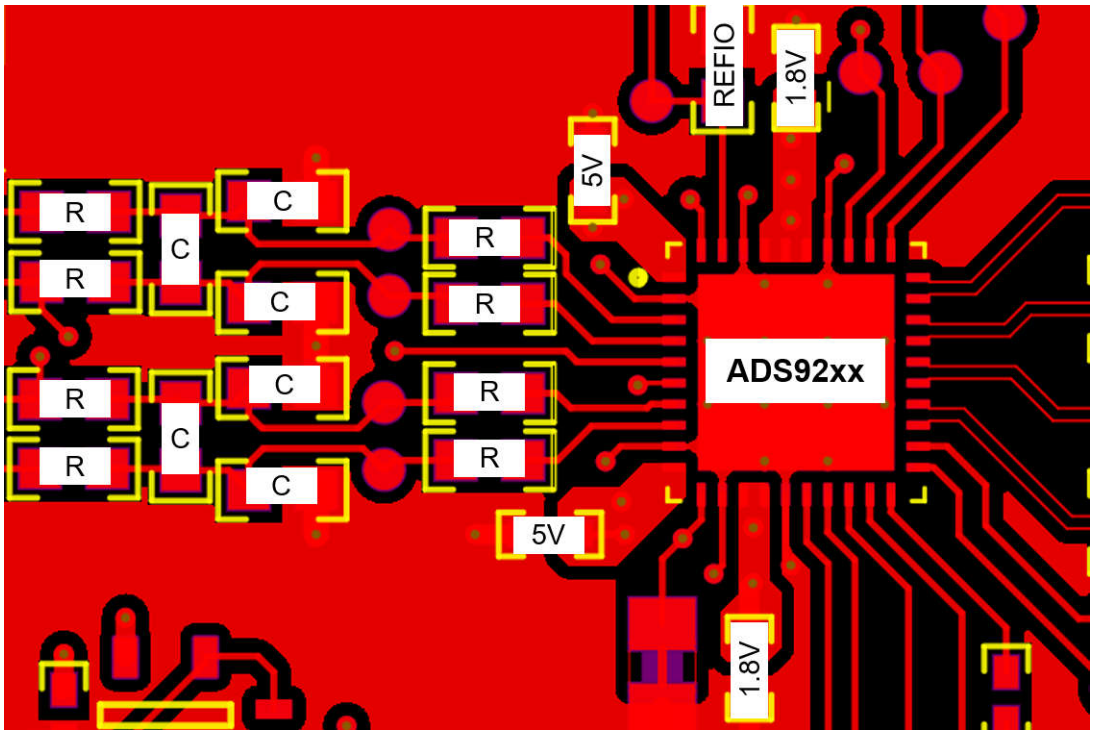


Figure 8-11. Example Layout

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *REF70 2 ppm/°C Maximum Drift, 0.23 ppm$_{p-p}$ 1/f Noise, Precision Voltage Reference*, data sheet
- Texas Instruments, *THS4552 Dual-Channel, Low-Noise, Precision, 150-MHz, Fully Differential Amplifier*, data sheet
- Texas Instruments, *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier*, data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PADS9227RHAT	ACTIVE	VQFN	RHA	40	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

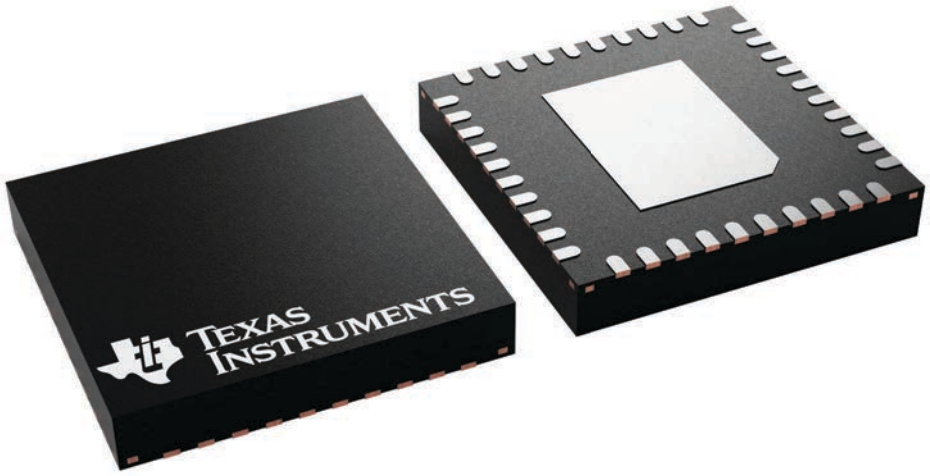
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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