DS90UH929-Q1 720p HDMI to FPD-Link III Bridge Serializer With HDCP

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 2: –40°C to +105°C, T_A
- Supports TMDS clock up to 96 MHz for WXGA and 720p60 or 1080i60 resolutions with 24-bit color depth
- FPD-Link III outputs
- High-definition multimedia (HDMI) v1.4b inputs
- HDMI-mode DisplayPort (DP++) inputs
- Integrated HDCP v1.4 cipher engine with storage for on-chip key
- HDMI audio extraction for up to 8 channels
- Supports up to 15 meters of cable with automatic temperature and aging compensation
- Monitors spread-spectrum input clock to reduce EMI
- I2C (master/slave) with 1-Mbps fast-mode plus
- Compatible with DS90UH926Q-Q1 and DS90UH928Q-Q1 FPD-Link III deserializers

2 Applications

- Automotive infotainment:
  - IVI head units and HMI modules
  - Rear seat entertainment systems
  - Digital instrument clusters
- Surveillance cameras
- Consumer input HDMI port

3 Description

The DS90UH929-Q1 is an HDMI to FPD-Link III bridge device which, in conjunction with the FPD-Link III DS90UH926Q-Q1/DS90UH928Q-Q1 deserializers, supplies 1-lane high-speed serial stream over cost-effective 50-Ω single-ended coaxial or 100-Ω differential shielded twisted-pair (STP) cable. It serializes an HDMI v1.4b input supporting video resolutions up to WXGA and 720p with 24-bit color depth. The DS90UH929-Q1 is also compatible with the DS90UH940-Q1/DS90UH948-Q1 deserializers.

The FPD-Link III interface supports video and audio data transmission and full duplex control, including I2C communication, over the same differential link. The consolidation of video data and control over one differential pair can reduce the interconnect size and weight and can simplify system design. EMI is minimized by the use of low-voltage differential signaling, data scrambling, and randomization.

The DS90UH929-Q1 supports HDCP Repeater applications where all authentication and encryption functions are handled without the need for an external controller. HDMI audio and video data are decrypted at the input and re-encrypted before the data is sent to the FPD-Link III interface.

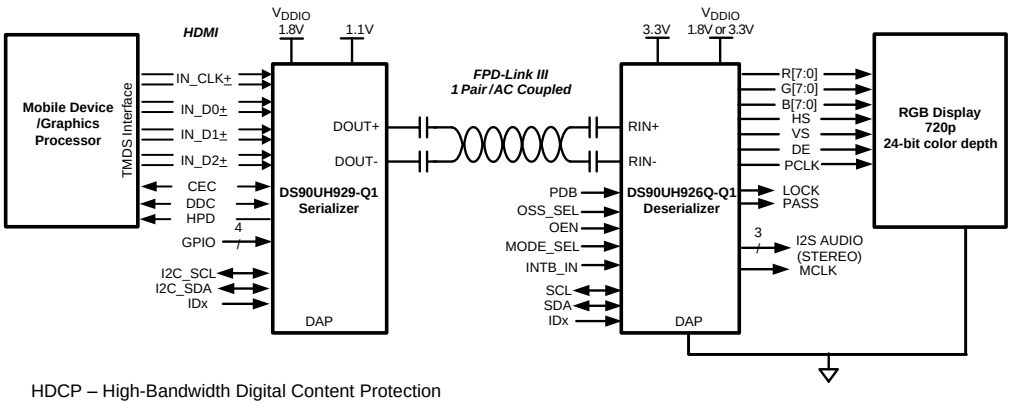
The DS90UH929-Q1 supports multi-channel audio received through HDMI or an external I2S interface. The device also supplies an optional auxiliary audio interface.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UH929-Q1	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



HDCP – High-Bandwidth Digital Content Protection
TMDS – Transition-Minimized Differential Signaling
HDMI – High Definition Multimedia Interface

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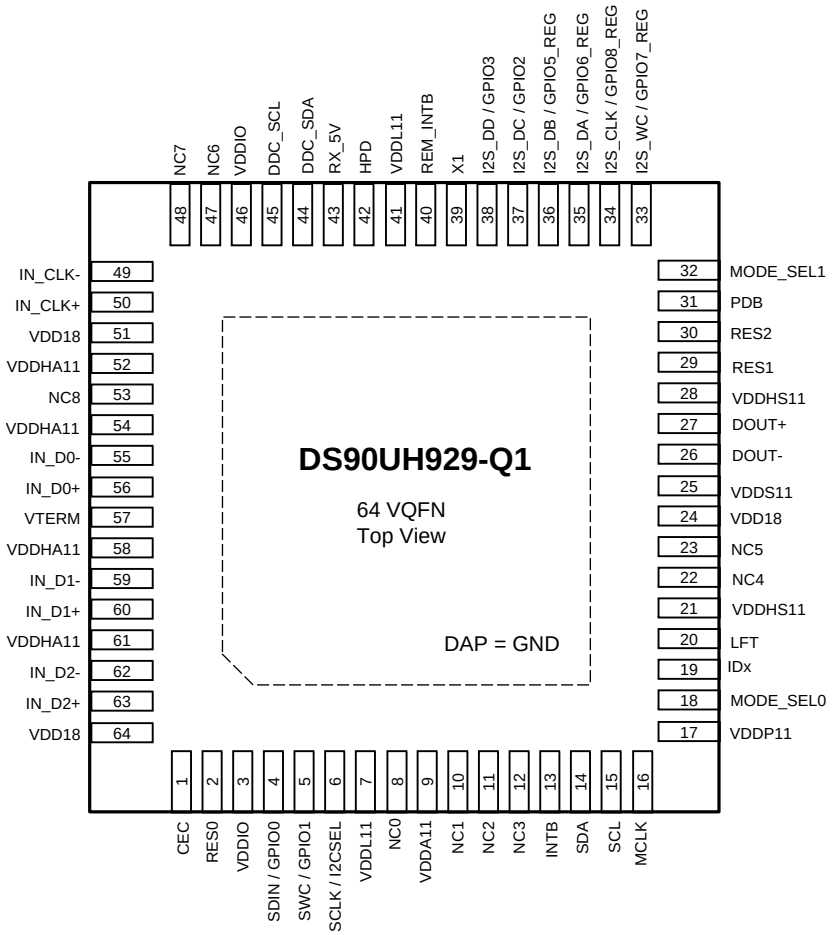
- Added Page 0x14 Register..... 62
- Changed graph caption from: *1080p60 Video at 2.6 Gbps Serial Line Rate (One of Two Lanes)* to: *720p60 Video at 2.6-Gbps Serial Line Rate, Single Lane FPD-Link III Output* 67
- Changed *Power-Up Requirements* section 68

5 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
HDMI TMDS INPUT			
IN_CLK- IN_CLK+	49 50	I, TMDS	TMDS Clock Differential Input
IN_D0- IN_D0+	55 56	I, TMDS	TMDS Data Channel 0 Differential Input
IN_D1- IN_D1+	59 60	I, TMDS	TMDS Data Channel 1 Differential Input

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
IN_D2- IN_D2+	62 63	I, TMDS	TMDS Data Channel 2 Differential Input
OTHER HDMI			
HPD	42	O, Open-Drain	Hot Plug Detect Output. Pull up to RX_5V with a 1-kΩ resistor
RX_5V	43	I	HDMI 5-V Detect Input
DDC_SDA	44	IO, Open-Drain	DDC Slave Serial Data Pullup to RX_5V with a 47-kΩ resistor
DDC_SCL	45	I, Open-Drain	DDC Slave Serial Clock Pullup to RX_5V with a 47-kΩ resistor
CEC	1	IO, Open-Drain	Consumer Electronic Control Channel Input/Output Interface. Pullup with a 27-kΩ resistor to 3.3 V
X1	39	I, LVCMOS	Optional Oscillator Input: This pin is the optional reference clock for CEC. It must be connected to a 25 MHz 0.1% (1000ppm), 45-55% duty cycle clock source at CMOS-level 1.8 V. Leave it open if unused.
FPD-LINK III SERIAL			
DOUT-	26	O	FPD-Link III Inverting Output The output must be AC-coupled with a 0.1-µF capacitor for interfacing with 92x deserializers and 33-nF capacitor for 94x deserializers
DOUT+	27	O	FPD-Link III True Output The output must be AC-coupled with a 0.1-µF capacitor for interfacing with 92x deserializers and 33-nF capacitor for 94x deserializers
LFT	20	Analog	FPD-Link III Loop Filter Connect to a 10-nF capacitor to GND
CONTROL			
SDA	14	IO, Open-Drain	I2C Data Input / Output Interface Open-drain. Must have an external pullup to resistor to 1.8 V or 3.3 V. See I2CSEL pin. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
SCL	15	IO, Open-Drain	I2C Clock Input / Output Interface Open-drain. Must have an external pullup resistor to 1.8 V or 3.3 V. See I2CSEL pin. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
I2CSEL	6	I, LVCMOS	I2C Voltage Level Strap Option Tie to V_{DDIO} with a 10-kΩ resistor for 1.8-V I2C operation. Leave floating for 3.3-V I2C operation. This pin is read as an input at power up.
IDx	19	Analog	I2C Serial Control Bus Device ID Address Select
MODE_SEL0	18	Analog	Mode Select 0. See Table 4.
MODE_SEL1	32	Analog	Mode Select 1. See Table 4.
PDB	31	I, LVCMOS	Power-Down Mode Input Pin
INTB	13	O, Open-Drain	Open Drain. Remote interrupt. Active LOW. Pullup to VDDIO with a 4.7-kΩ resistor.
REM_INTB	40	O, Open-Drain	Remote interrupt. Mirrors status of INTB_IN from the deserializer. Note: External pullup to 1.8 V required. Recommended pullup: 4.7 kΩ. INTB = H, Normal Operation INTB = L, Interrupt Request
BIDIRECTIONAL CONTROL CHANNEL (BCC) GPIO PINS			
GPIO0	4	IO, LVCMOS	BCC GPIO0. Shared with SDIN
GPIO1	5	IO, LVCMOS	BCC GPIO1. Shared with SWC
GPIO2	37	IO, LVCMOS	BCC GPIO2. Shared with I2S_DC
GPIO3	38	IO, LVCMOS	BCC GPIO3. Shared with I2S_DD
REGISTER-ONLY GPIO			

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
GPIO5_REG	36	IO, LVCMOS	General-Purpose Input/Output 5 Local register control only. Shared with I2S_DB
GPIO6_REG	35	IO, LVCMOS	General-Purpose Input/Output 6 Local register control only. Shared with I2S_DA
GPIO7_REG	33	IO, LVCMOS	General-Purpose Input/Output 7 Local register control only. Shared with I2S_WC
GPIO8_REG	34	IO, LVCMOS	General-Purpose Input/Output 8 Local register control only. Shared with I2S_CLK
SLAVE MODE LOCAL I2S CHANNEL PINS			
I2S_WC	33	I, LVCMOS	Slave Mode I2S Word Clock Input. Shared with GPIO7_REG
I2S_CLK	34	I, LVCMOS	Slave Mode I2S Clock Input. Shared with GPIO8_REG
I2S_DA	35	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO6_REG
I2S_DB	36	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO5_REG
I2S_DC	37	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO2
I2S_DD	38	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO3
AUXILIARY I2S CHANNEL PINS			
SWC	5	O, LVCMOS	Master Mode I2S Word Clock Output. Shared with GPIO1
SCLK	6	O, LVCMOS	Master Mode I2S Clock Output. Shared with I2CSEL. This pin is sampled following power-up as I2CSEL, then it will switch to SCLK operation as an output.
SDIN	4	I, LVCMOS	Master Mode I2S Data Input. Shared with GPIO0
MCLK	16	IO, LVCMOS	Master Mode I2S System Clock Input/Output
POWER AND GROUND			
VTERM	57	Power	Must be connected to 3.3-V or 1.8-V supply. Connect to 3.3-V (±5%) Supply if incoming video is DC coupled OR Connect to 1.8-V (±5%) Supply if incoming video is AC coupled Refer to Figure 22 or Figure 21.
VDD18	24 51 64	Power	1.8-V (±5%) Analog supply. Refer to Figure 22 or Figure 21.
VDDA11	9	Power	1.1-V (±5%) Analog supply. Refer to Figure 22 or Figure 21.
VDDHA11	52 54 58 61	Power	1.1-V (±5%) TMDS supply. Refer to Figure 22 or Figure 21.
VDDHS11	21 28	Power	1.1-V (±5%) supply. Refer to Figure 22 or Figure 21.
VDDL11	7 41	Power	1.1-V (±5%) Digital supply. Refer to Figure 22 or Figure 21.
VDDP11	17	Power	1.1-V (±5%) PLL supply. Refer to Figure 22 or Figure 21.
VDDS11	25	Power	1.1-V (±5%) Serializer supply. Refer to Figure 22 or Figure 21.
VDDIO	3 46	Power	1.8-V (±5%) IO supply. Refer to Figure 22 or Figure 21.
GND	Thermal Pad	GND	Ground. Connect to Ground plane with at least 9 vias.
OTHER			
RES0 RES1	2 29		Reserved. Tie to GND.
RES2	30		Reserved. Connect with 50Ω to GND.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8	8 10 11 12 22 23 47 48 53		No connect. Leave floating. Do not connect to VDD or GND.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
V_{DD11}	Supply Voltage	–0.3	1.7	V
V_{DD18}	Supply Voltage	–0.3	2.5	V
V_{DDIO}	Supply Voltage	–0.3	2.5	V
	OpenLDI Inputs	–0.3	2.75	V
	LVCMOS I/O Voltage	–0.3	V_{DDIO} + 0.3	V
	1.8-V Tolerant I/O	–0.3	2.5	V
	3.3-V Tolerant I/O	–0.3	4.0	V
	5-V Tolerant I/O	–0.3	5.3	V
	FPD-Link III Output Voltage	−0.3	1.7	V
	Junction Temperature		150	°C
T_{stg}	Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5		±750	
		ESD Rating (IEC 61000-4-2) R_D = 330 Ω, C_S = 150 pF	Air Discharge (D_{OUT+}, D_{OUT-})	±15000	
			Contact Discharge (D_{OUT+}, D_{OUT-})	±8000	
		ESD Rating (ISO10605) R_D = 330 Ω, C_S = 150 pF R_D = 2 kΩ, C_S = 150 pF or 330 pF	Air Discharge (D_{OUT+}, D_{OUT-})	±15000	
			Contact Discharge (D_{OUT+}, D_{OUT-})	±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD11}	Supply Voltage	1.045	1.1	1.155	V
V_{DD18}	Supply Voltage	1.71	1.8	1.89	V
V_{DDIO}	LVCMOS Supply Voltage	1.71	1.8	1.89	V

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
	V_{DDI2C}, 1.8-V Operation	1.71	1.8	1.89	V
	V_{DDI2C}, 3.3-V Operation	3.135	3.3	3.465	V
	HDMI Termination (V_{TERM}), DC-coupled	3.135	3.3	3.465	V
	HDMI Termination (V_{TERM}), AC-coupled	1.71	1.8	1.89	V
V_{RX_5V}	HDMI Detect Voltage	4.25	5	5.25	V
T_A	Operating Free Air Temperature	−40	25	105	°C
T_{CLH1}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under the following condition: –40°C ≤ starting ambient temperature (T_S) < 0°C.(1)	T_S		80	°C
T_{CLH2}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under the following condition: 0°C ≤ starting ambient temperature (T_S) ≤ 105°C.(1)	T_S		105	°C
T_{CHL1}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is falling under the following condition: 45°C < starting ambient temperature (T_S) ≤ 105°C.(1)	25		T_S	°C
T_{CHL2}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is falling under the following condition: –20°C ≤ starting ambient temperature (T_S) ≤ 45°C. (1)	T_S − 20		T_S	°C
	TMDS Frequency	25		96	MHz

(1) The input and output PLLs are calibrated at the ambient start up temperature (T_S) when the device is powered on or when reset using the PDB pin. The PLLs will stay locked up to the specified ending temperature. A more detailed description can be found in “Handling System Temperature Ramps on the DS90Ux949, DS90Ux929 and DS90Ux947”.

6.4 Thermal Information

THERMAL METRIC(1)		DS90UH929-Q1 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 DC Electrical Characteristics

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
1.8-V LVCMOS I/O							
V_{IH}	High Level Input Voltage		SCLK/I2CSEL, PDB, SDIN/GPIO0, SWC/GPIO1, MCLK I2S_DC/GPIO2, I2S_DD/GPIO3, I2S_DB/GPIO5_REG, I2S_DA/GPIO6_REG, I2S_CLK/GPIO8_REG, I2S_WC/GPIO7_REG	0.65 × V_{DDIO}			V
V_{IL}	Low Level Input Voltage			0		0.35 × V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0 V or 1.89 V		−10		10	µA

DC Electrical Characteristics (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	Same as above	0.7 × V_{DDIO}		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA		GND		0.26 × V_{DDIO}	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V			-50		mA
I_{OZ}	TRI-STATE™ Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L		−10		10	µA
TMDS INPUTS -- FROM HDMI v1.4b SECTION 4.2.5							
V_{ICM1}	Input Common-Mode Voltage	IN_CLK ≤ 96MHz	IN_D[2:0]+, IN_D[2:0]- IN_CLK+, IN_CLK- V_{TERM} = 1.8V (±5%) or VTERM = 3.3 V (±5%)	V_{TERM} - 300		V_{TERM} - 37.5	mV
V_{ICM2}	Input Common-Mode Voltage			V_{TERM} - 10		V_{TERM} + 10	mV
V_{IDIFF}	Input Differential Voltage Level			150		1200	mV_{P-P}
R_{TMDS}	Termination Resistance	Differential	IN_D[2:0]+, IN_D[2:0]- IN_CLK+, IN_CLK-	90	100	110	Ω
HDMI IO -- FROM HDMI v1.4b SECTION 4.2.7 to 4.2.9							
V_{RX_5V}	5-V Power Signal		RX_5V	4.8		5.3	V
I_{5V_Sink}	5-V Input Current					50	mA
$V_{OH,HPD}$	High Level Output Voltage, HPD	I_{OH} = –4 mA	HPD, R_{PU} = 1 kΩ	2.4		5.3	V
$V_{OL,HPD}$	Low Level Output Voltage, HPD	I_{OL} = 4 mA		GND		0.4	V
$I_{IZ,HPD}$	Power-Down Input Current, HPD	PDB = L		–10		10	uA
$V_{IL,DDC}$	Low Level Input Voltage, DDC		DDC_SCL, DDC_SDA			0.3 × $V_{DD,DDC}$	V
$V_{IH,DDC}$	High Level Input Voltage, DDC			2.7			V
$I_{IZ,DDC}$	Power-Down Input Current, DDC	PDB = L		–10		10	µA
$V_{IH,CEC}$	High Level Input Voltage, CEC		CEC	2			V
$V_{IL,CEC}$	Low Level Input Voltage, CEC					0.8	V
$V_{HY,CEC}$	Input Hysteresis, CEC				0.4		V
$V_{OL,CEC}$	Low Level Output Voltage, CEC			GND		0.6	V
$V_{OH,CEC}$	High Level Output Voltage, CEC			2.5		3.63	V
I_{OFF_CEC}	Power-Down Input Current, CEC	PDB = L		–1.8		1.8	µA

DC Electrical Characteristics (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III DIFFERENTIAL DRIVER							
V_{ODp-p}	Output Differential Voltage		DOUT+, DOUT-	900		1200	mV_{p-p}
ΔV_{OD}	Output Voltage Unbalance				1	50	mV
V_{OS}	Output Differential Offset Voltage				550		mV
ΔV_{OS}	Offset Voltage Unbalance				1	50	mV
I_{OS}	Output Short Circuit Current	FPD-Link III Outputs = 0 V			-50		mA
R_T	Termination Resistance	Single-ended		40	50	60	Ω
SUPPLY CURRENT (1)							
I_{DD11}	Supply Current, Normal Operation	Colorbar Pattern				330	mA
I_{DD18}						50	mA
$I_{DD,VTERM}$	V_{TERM} Current, Normal Operation	Colorbar Pattern			60		mA
I_{DDZ11}	Supply Current, Power Down Mode	PDB = L			15		mA
I_{DDZ18}					5		mA
$I_{DDZ,VTERM}$	V_{TERM} Current, Power Down Mode	Colorbar Pattern			5		mA

(1) Specification is tested by bench characterization.

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO FREQUENCY (1)							
$R_{b,FC}$	Forward Channel GPIO Frequency	IN_CLK = 25 MHz - 96 MHz	GPIO[3:0]			0.25 × IN_CLK	MHz
$t_{GPIO,FC}$	GPIO Pulse Width, Forward Channel	IN_CLK = 25 MHz - 96 MHz	GPIO[3:0]	>2 / IN_CLK			s
TMDS INPUT							
Skew-Intra	Maximum Intra-Pair Skew		IN_CLK±, IN_D[2:0]±			0.4	UI_{TMDS} (2)
Skew-Inter	Maximum Inter-Pair Skew					0.2 × T_{char} (3) + 1.78	ns
t_{IJIT}	TMDS Clock Input Jitter	Bit Error Rate ≤1E-10	IN_CLK±			0.3	UI_{TMDS} (2)
FPD-LINK III OUTPUT							
t_{LHT}	Low Voltage Differential Low-to-High Transition Time				80		ps
t_{HLT}	Low Voltage Differential High-to-Low Transition Time				80		ps
t_{XZD}	Output Active to OFF Delay	PDB = L			100		ns
t_{PLD}	Lock Time (HDMI Rx)				5		ms
t_{SD}	Delay — Latency		IN_CLK±		145*T (2)		s
t_{DJIT}	Output Total Jitter (Figure 5)	Random Pattern	Low pass filter IN_CLK/20		0.3		UI_{FPD3} (4)
λ_{STXBW}	Jitter Transfer Function (-3-dB Bandwidth)				960		kHz
δ_{STX}	Jitter Transfer Function Peaking				0.1		dB

(1) Back channel rates are available on the companion deserializer datasheet.
(2) One bit period of the TMDS input.
(3) Ten bit periods of the TMDS input.
(4) One bit period of the serializer output.

6.7 DC And AC Serial Control Bus Characteristics

over V_{DDI2C} supply and temperature ranges unless otherwise specified. V_{DDI2C} can be 1.8V (±5%) or 3.3V (±5%) (refer to I2CSEL pin description for 1.8-V or 3.3-V operation).

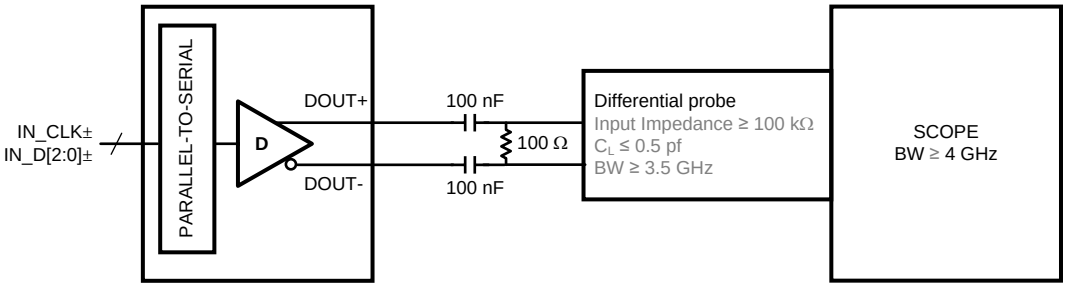
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH,I2C}$	Input High Level, I2C	SDA and SCL, V_{DDI2C} = 1.8 V	0.7 × V_{DDI2C}			V
		SDA and SCL, V_{DDI2C} = 3.3 V	0.7 × V_{DDI2C}			V
$V_{IL,I2C}$	Input Low Level Voltage, I2C	SDA and SCL, V_{DDI2C} = 1.8 V			0.3 × V_{DDI2C}	V
		SDA and SCL, V_{DDI2C} = 3.3 V			0.3 × V_{DDI2C}	V
V_{HY}	Input Hysteresis, I2C	SDA and SCL, V_{DDI2C} = 1.8 V or 3.3 V		>50		mV
$V_{OL,I2C}$	Output Low Level, I2C	SDA and SCL, V_{DDI2C} = 1.8-V, Fast-Mode, 3-mA Sink Current	GND		0.2 × V_{DDI2C}	V
		SDA and SCL, V_{DDI2C} = 3.3-V, 3-mA Sink Current	GND		0.4	V
$I_{IN,I2C}$	Input Current, I2C	SDA and SCL, V_{DDI2C} = 0 V	-800		-600	µA
		SDA and SCL, V_{DDI2C} = V_{DD18} or V_{DD33}	-10		10	µA
$C_{IN,I2C}$	Input Capacitance, I2C	SDA and SCL		5		pF

6.8 Recommended Timing for the Serial Control Bus

over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-Mode	>0		100	kHz
		Fast-Mode	>0		400	kHz
		Fast-Mode Plus	>0		1	MHz
t_{LOW}	SCL Low Period	Standard-Mode	4.7			µs
		Fast-Mode	1.3			µs
		Fast-Mode Plus	0.5			µs
t_{HIGH}	SCL High Period	Standard-Mode	4.0			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-Mode	4.0			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
$t_{SU;STA}$	Set Up time for a start or a repeated start condition	Standard-Mode	4.7			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
$t_{HD;DAT}$	Data Hold Time	Standard-Mode	0			µs
		Fast-Mode	0			µs
		Fast-Mode Plus	0			µs
$t_{SU;DAT}$	Data Set-Up Time	Standard-Mode	250			ns
		Fast-Mode	100			ns
		Fast-Mode Plus	50			ns
$t_{SU;STO}$	Set Up Time for STOP Condition	Standard-Mode	4.0			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
t_{BUF}	Bus Free Time Between STOP and START	Standard-Mode	4.7			µs
		Fast-Mode	1.3			µs
		Fast-Mode Plus	0.5			µs
t_r	SCL and SDA Rise Time,	Standard-Mode			1000	ns
		Fast-Mode			300	ns
		Fast-Mode Plus			120	ns
t_f	SCL and SDA Fall Time,	Standard-Mode			300	ns
		Fast-Mode			300	ns
		Fast-Mode Plus			120	ns
t_{SP}	Input Filter	Fast-Mode			50	ns
		Fast-Mode Plus			50	ns

6.9 Timing Diagrams



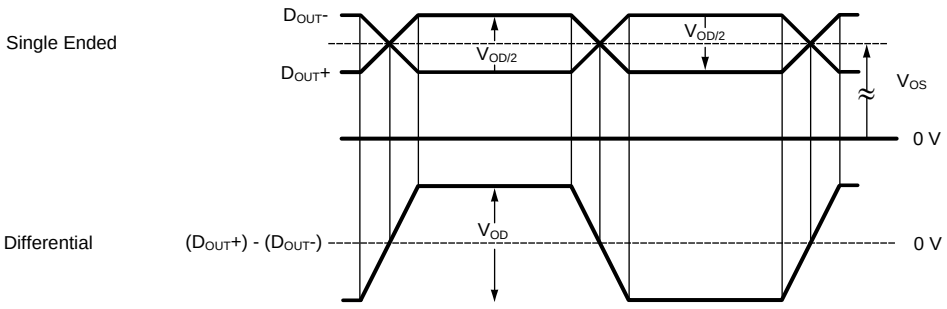


Figure 1. Serializer V_{OD} Output

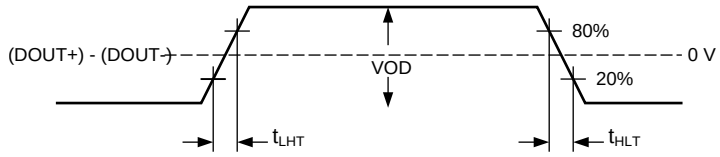


Figure 2. Output Transition Times

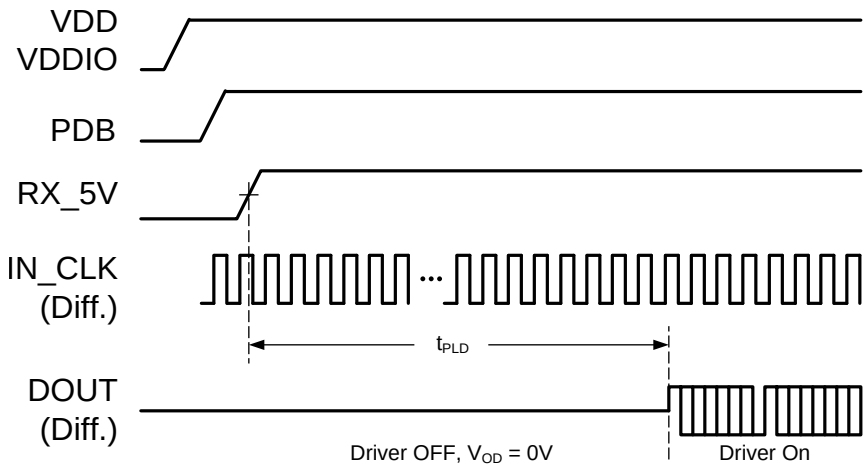


Figure 3. Serializer Lock Time

Timing Diagrams (continued)

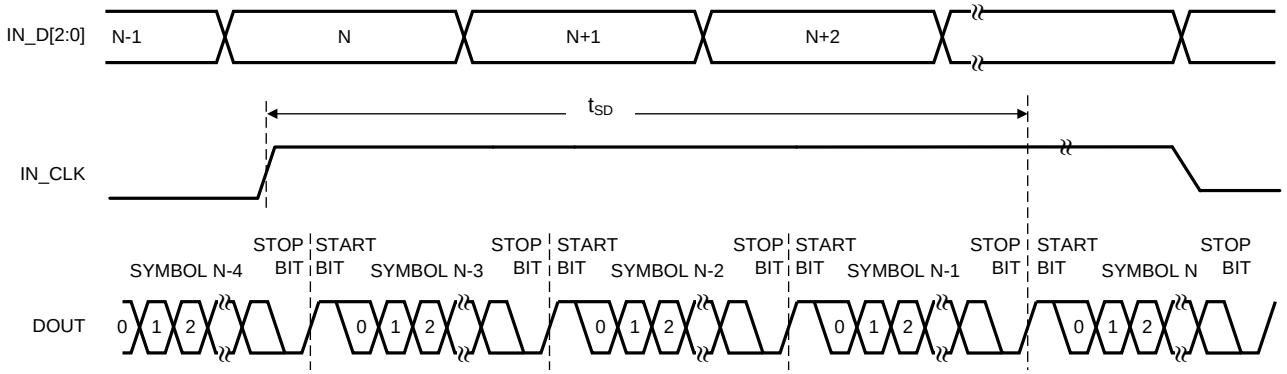


Figure 4. Latency Delay

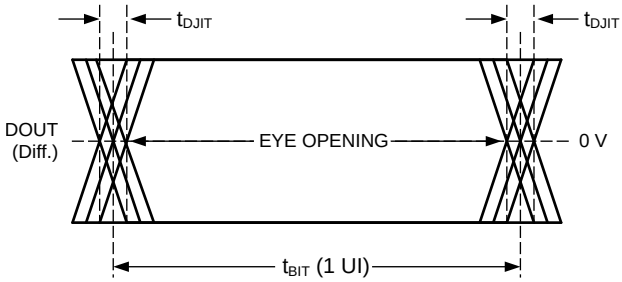


Figure 5. Serializer Output Jitter

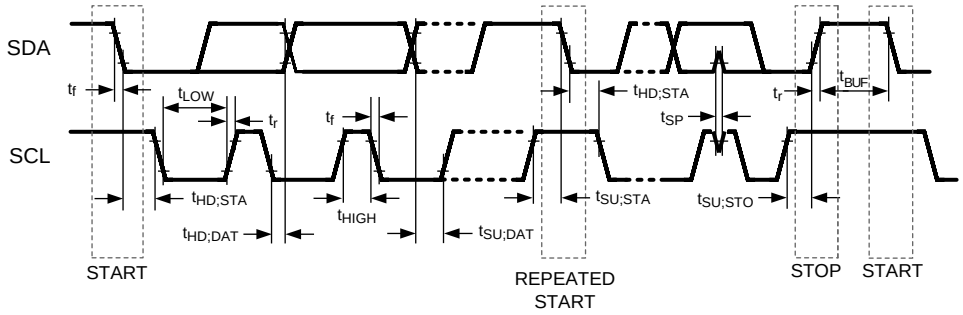


Figure 6. Serial Control Bus Timing Diagram

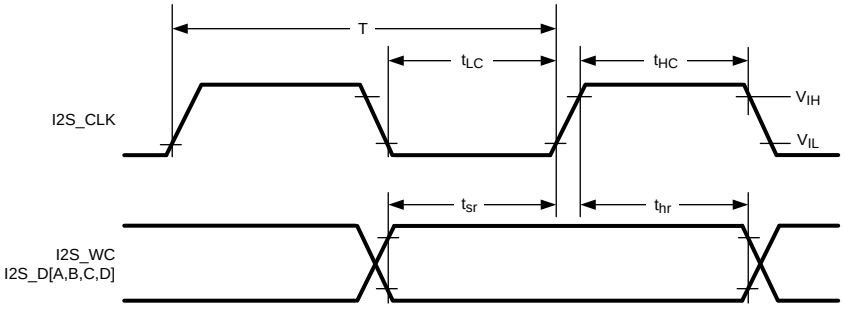


Figure 7. I2S Timing Diagram

6.10 Typical Characteristics

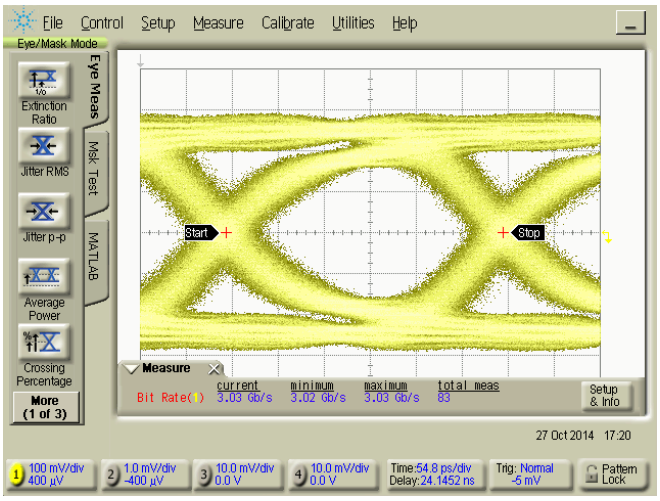


Figure 8. Serializer Output at 2.975 Gbps (85-MHz TMDS Clock)

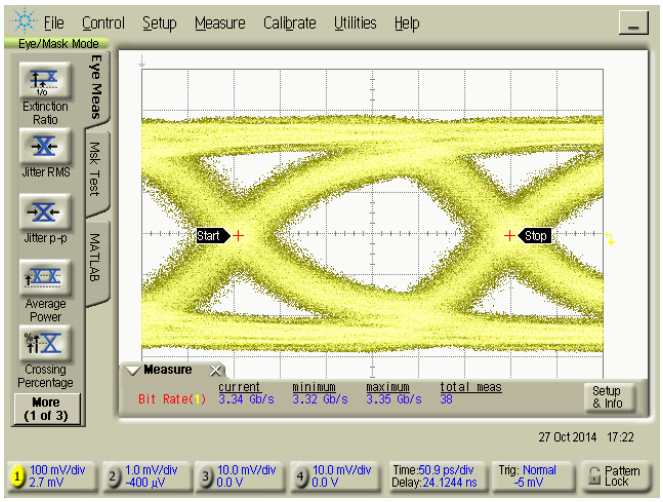


Figure 9. Serializer Output at 3.36 Gbps (96-MHz TMDS Clock)

7 Detailed Description

7.1 Overview

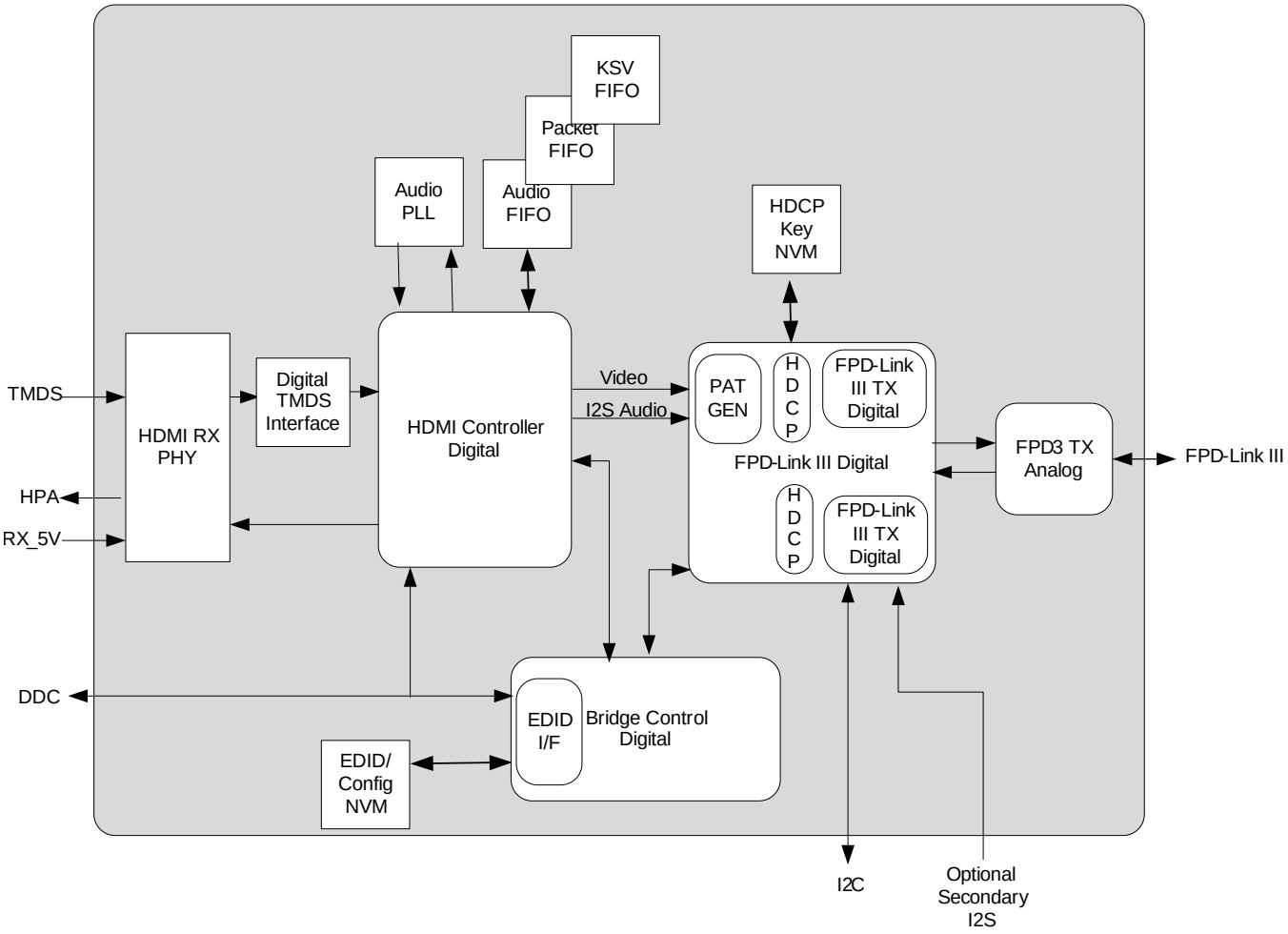
The DS90UH929-Q1 converts an HDMI interface (3 TMDS data channels + 1 TMDS Clock) to an FPD-Link III interface. This device transmits a 35-bit symbol over a single serial pair operating up to 3.36-Gbps line rate. The serial stream contains an embedded clock, video control signals, RGB video data, and audio data. The payload is DC-balanced to enhance signal quality and support AC coupling.

The DS90UH929-Q1 serializer is intended for use with a DS90UH926Q-Q1, DS90UH928Q-Q1, DS90UH940-Q1, DS90UH948-Q1 deserializer.

The DS90UH929-Q1 serializer and companion deserializer incorporate an I2C-compatible interface. The I2C-compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the device incorporates a bidirectional control channel (BCC) that allows communication between serializer and deserializer, as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C-compatible masters at either side of the serial link.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Definition Multimedia Interface (HDMI)

HDMI is a leading interface standard used to transmit digital video and audio from sources (such as a DVD player) to sinks (such as an LCD display). The interface is capable of transmitting high-definition video, audio, and also supports HDCP. Other HDMI signals consist of various control and status data that travel bidirectionally.

7.3.1.1 HDMI Receive Controller

The HDMI Receiver is an HDMI version 1.4b compliant receiver. The HDMI receiver is capable of operation at greater than 1080p resolutions. The DS90UH929-Q1 implementation is restricted to 720p operation (or 1080i or 1080p/30). The configuration used in the DS90UH929-Q1does not include version 1.4b features such as the ethernet channel (HEC) or Audio Return Channel (ARC).

7.3.2 Transition Minimized Differential Signaling

HDMI uses Transition Minimized Differential Signaling (TMDS) over four differential pairs (3 TMDS channels and 1 TMDS clock) to transmit video and audio data. TMDS is widely used to transmit high-speed serial data. The technology incorporates a form of 8b/10b encoding and the differential signaling allows the device to reduce electromagnetic interference (EMI) and achieve high skew tolerance.

7.3.3 Enhanced Display Data Channel

The Display Data Channel or DDC is a collection of digital communication protocols between a computer display and a graphics adapter that enables the display to list and send all the supported display modes to the adapter and allow the computer host to adjust monitor parameters, such as brightness and contrast.

7.3.4 Extended Display Identification Data (EDID)

EDID is a data structure provided by a digital display to list all the capabilities of the display to a video source. After receiving this information, the video source can send back video data with proper timing and resolution the display can support. The DS90UH929-Q1 supports several options for delivering display identification (EDID) information to the HDMI graphics source. The EDID information is accessible through the DDC interface and comply with the DDC and EDID requirements given in the HDMI v1.4b specification.

The EDID configurations supported are as follows:

- External local EDID (EEPROM)
- Internal EDID loaded into device memory
- Remote EDID connected to I2C bus at deserializer side
- Internal pre-programmed EDID

The selected EDID mode should be configurable from either the MODE_SEL pins or from internal control registers. For all modes, the EDID information should be accessible at the default address of 0xA0.

7.3.4.1 External Local EDID (EEPROM)

The DS90UH929-Q1 can be configured to allow a local EEPROM EDID device. The local EDID device may implement any EDID configuration allowable by the HDMI v1.4b and DVI 1.0 standards, including multiple extension blocks up to 32KB.

7.3.4.2 Internal EDID (SRAM)

The DS90UH929-Q1 also allows internal loading of an EDID profile up to 256 bytes. This SRAM storage is volatile and requires loading from an external I2C master (local or remote). The internal EDID is reloadable and readable (local/remote) from control registers during normal operation.

7.3.4.3 External Remote EDID

The serializer copies the remote EDID connected to the I2C bus of the remote deserializer into its internal SRAM. The remote EDID device can be a standalone I2C EEPROM, or integrated into the digital display panel. In this mode, the serializer automatically accesses the Bidirectional Control Channel to search for the EDID information at the default address 0xA0. Once found, the serializer copies the remote EDID into local SRAM.

Feature Description (continued)

7.3.4.4 Internal Pre-Programmed EDID

The serializer also has an internal eFuse that is loaded into the internal SRAM with pre-programmed 256-byte EDID data at start-up. This EDID profile supports several generic video (480p, 720p) and audio (2-channel audio) timing profiles within the single-link operating range of the device (25-MHz to 96-MHz pixel clock). In this mode, the internal EDID SRAM data is readable from the DDC interface. The EDID contents are below:

0x00	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x53	0x0E	0x49	0x09	0x01	0x00	0x00	0x00
0x1C	0x18	0x01	0x03	0x80	0x34	0x20	0x78	0x0A	0xEC	0x18	0xA3	0x54	0x46	0x98	0x25
0x0F	0x48	0x4C	0x00	0x00	0x00	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01
0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x1D	0x00	0x72	0x51	0xD0	0x1E	0x20	0x6E	0x50
0x55	0x00	0x00	0x20	0x21	0x00	0x00	0x18	0x00	0x00	0x00	0xFD	0x00	0x3B	0x3D	0x62
0x64	0x08	0x00	0x0A	0x20	0x20	0x20	0x20	0x20	0x20	0x00	0x00	0x00	0xFC	0x00	0x54
0x49	0x2D	0x44	0x53	0x39	0x30	0x55	0x78	0x39	0x34	0x39	0x0A	0x00	0x00	0x00	0x10
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x01	0x57
0x02	0x03	0x15	0x40	0x41	0x84	0x23	0x09	0x7F	0x05	0x83	0x01	0x00	0x00	0x66	0x03
0x0C	0x00	0x10	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x28

7.3.5 Consumer Electronics Control (CEC)

Consumer Electronics Control (CEC) is designed to allow the system user to command and control up-to ten CEC-enabled devices connected through HDMI, using only one of their remote controls (for example by controlling a television set, set-top box, and DVD player using only the remote control of the TV). CEC also allows for individual CEC-enabled devices to command and control each other without user intervention. CEC is a one-wire open drain bus with an external 27-kΩ (±10%) resistor pullup to 3.3 V.

CEC protocol can be implemented using an external clock reference or the 25-MHz internal oscillator inside the DS90UH929-Q1.

7.3.6 +5-V Power Signal

5 V is asserted by the HDMI source through the HDMI interface. The 5-V signal propagates through the connector and cable until it reaches the sink. The 5-V supply is used for various HDMI functions, such as HPD and DDC signals.

7.3.7 Hot Plug Detect (HPD)

The HPD pin is asserted by the sink to let the source know that it is ready to receive the HDMI signal. The source initiates the connection by first providing the 5-V power signal through the HDMI interface. The sink holds HPD low until it is ready to receive signals from the source, at which point it will release HPD to be pulled up to 5 V.

7.3.8 High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel is composed of 35 bits of data containing RGB data, sync signals, HDCP, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. Figure 10 shows the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced, and scrambled.

Figure 10. FPD-Link III Serial Stream

Feature Description (continued)

The device supports TMDS clocks in the range of 25 MHz to 96 MHz over one lane. The FPD-Link III serial stream rate is 3.36 Gbps maximum (875 Mbps minimum).

7.3.9 Back Channel Data Transfer

The Back Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, HDCP, CRC and 4 bits of standard GPIO information with 5-Mbps, 10-Mbps, or 20-Mbps line rate (configured by the compatible deserializer).

7.3.10 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}, where V_{DDIO} = 1.71 V to 1.89 V. To save power, disable the link when the display is not necessary (PDB = LOW). Ensure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, ensure that the pin is driven to 0 V for at least 3 ms before releasing or driving high. In the case where PDB is pulled up to V_{DDIO} directly, a 10-kΩ pullup resistor and a >10-µF capacitor to ground are required (*See Power-Up Requirements and PDB Pin*).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held low for a minimum of 3 ms before going high again.

7.3.11 Serial Link Fault Detect

The DS90UH929-Q1 can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Table 8). The DS90UH929-Q1 will detect any of the following conditions:

1. Cable open
2. “+” to “-” short
3. ”+” to GND short
4. ”-” to GND short
5. ”+” to battery short
6. ”-” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

The device will detect any of the above conditions, but does not report specifically which one has occurred.

7.3.12 Interrupt Pin (INTB)

The INTB pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions (see registers 0xC6 and 0xC7 of *Register Maps*). For the remote interrupt condition, the INTB pin works in conjunction with the INTB_IN pin on the deserializer. This interrupt signal, when configured, will propagate from the deserializer to the serializer.

1. On the Serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN pin is set *LOW* by some downstream device.
3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read ISR register.
5. A read to ISR will clear the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTB_IN. This would be when the downstream device releases the INTB_IN pin on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

Feature Description (continued)

7.3.13 Remote Interrupt Pin (REM_INTB)

REM_INTB will mirror the status of INTB_IN pin on the deserializer and does not need to be cleared. If the serializer is not linked to the deserializer, REM_INTB will be high.

7.3.14 General-Purpose I/O

7.3.14.1 GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers. See Table 1 for GPIO enable and configuration.

Table 1. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

7.3.14.2 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I^2S input if enabled into GPIO_REG mode. See Table 2 for GPIO enable and configuration.

A local GPIO value may be configured and read either through local register access, or remote register access through the Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 2. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG8	0x11[7:4] = 0x01	Output, L
	0x11[7:4] = 0x09	Output, H
	0x11[7:4] = 0x03	Input, Read: 0x1D[0]
GPIO_REG7	0x11[3:0] = 0x1	Output, L
	0x11[3:0] = 0x9	Output, H
	0x11[3:0] = 0x3	Input, Read: 0x1C[7]
GPIO_REG6	0x10[7:4] = 0x1	Output, L
	0x10[7:4] = 0x9	Output, H
	0x10[7:4] = 0x3	Input, Read: 0x1C[6]
GPIO_REG5	0x10[3:0] = 0x1	Output, L
	0x10[3:0] = 0x9	Output, H
	0x10[3:0] = 0x3	Input, Read: 0x1C[5]
GPIO3	0x0F[3:0] = 0x1	Output, L
	0x0F[3:0] = 0x9	Output, H
	0x0F[3:0] = 0x3	Input, Read: 0x1C[3]

Table 2. GPIO_REG and GPIO Local Enable and Configuration (continued)

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO2	0x0E[7:4] = 0x1	Output, L
	0x0E[7:4] = 0x9	Output, H
	0x0E[7:4] = 0x3	Input, Read: 0x1C[2]
GPIO1	0x0E[3:0] = 0x1	Output, L
	0x0E[3:0] = 0x9	Output, H
	0x0E[3:0] = 0x3	Input, Read: 0x1C[1]
GPIO0	0x0D[3:0] = 0x1	Output, L
	0x0D[3:0] = 0x9	Output, H
	0x0D[3:0] = 0x3	Input, Read: 0x1C[0]

7.3.15 Backward Compatibility

This FPD-Link III serializer is backward-compatible to the DS90UH926Q-Q1 and DS90UH928Q-Q1 for TMDS clock frequencies ranging from 25 MHz to 85 MHz. Backward compatibility does not need to be enabled.

7.3.16 Audio Modes

The DS90UH929-Q1 supports several audio modes and functions:

- HDMI Mode
- DVI Mode
- AUX Audio Channel

When using with the DS90UH926-Q1 because the default audio mode is I2S Surround Sound and DS90UH926-Q1 can not receive more than 2 channels of audio while in 24-bit mode, the DS90UH929-Q1 will automatically transmit 18-bit video to a DS90UH926-Q1. To transmit 24-bit video to a DS90UH926-Q1, I2S Surround must be disabled by writing to register 0x1A[0]=0.

7.3.16.1 HDMI Audio

The DS90UH929-Q1 allows embedded audio in the HDMI interface to be transported over the FPD-Link III serial link and output on the compatible deserializer. Depending on the number of channels, HDMI audio can be output on several I^2S pins on the deserializer, or it can be converted to TDM to output on one audio output pin on the deserializer.

7.3.16.2 DVI I2S Audio Interface

The DS90UH929-Q1 serializer features six I^2S input pins that, when paired with a compatible deserializer, supports 7.1 High-Definition (HD) Surround Sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the lesser of IN_CLK/2 or 13 MHz. Four I^2S data inputs transport two channels of I^2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input. Refer to Figure 11 and Figure 12 for I2S connection diagram and timing information.

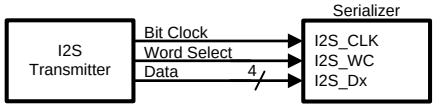


Figure 11. I^2S Connection Diagram

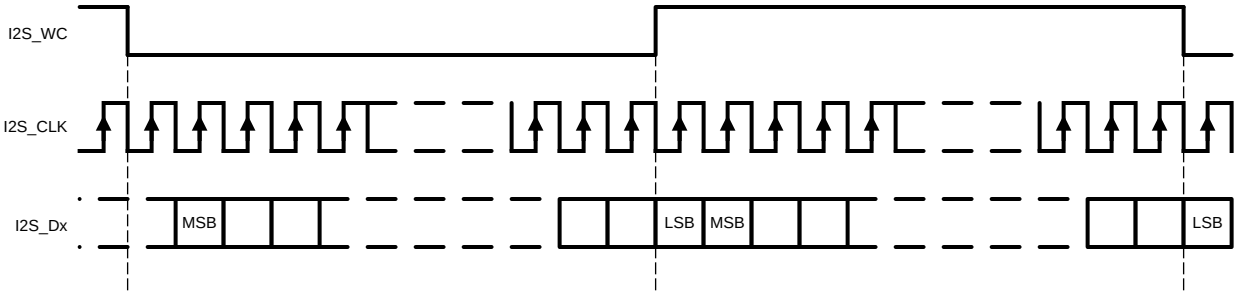


Figure 12. I2S Frame Timing Diagram

Table 3 covers several common I^2S sample rates:

Table 3. Audio Interface Frequencies

SAMPLE RATE (kHz)	I^2S DATA WORD SIZE (BITS)	I^2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

7.3.16.2.1 I2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames may be disabled from control registers if Forward Channel Frame Transport of I^2S data is desired. In this mode, only I2S_DA is transmitted to a DS90UH928Q-Q1, DS90UH940-Q1, or a DS90UH948-Q1 deserializer. If connected to a DS90UH926Q-Q1 deserializer, I2S_DA and I2S_DB are transmitted. Surround Sound Mode, which transmits all four I^2S data inputs (I2S_D[A..D]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UH928Q-Q1, DS90UH940-Q1, or a DS90UH948-Q1 deserializer.

7.3.16.2.2 I2S Repeater

I^2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated through Data Island Transport during the video blanking periods. If frame transport is desired, then the I^2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level deserializer automatically configures downstream serializers and deserializers for surround sound transport using Data Island Transport. If 4-channel operation using I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (Table 8).

7.3.16.3 AUX Audio Channel

The AUX Audio Channel is a single separate I^2S audio data channel that may be transported independently of the main audio stream received in either HDMI Mode or DVI Mode. This channel is shared with the GPIO[1:0] interface and is supported by DS90UH940-Q1 and DS90UH948-Q1 deserializers.

7.3.16.4 TDM Audio Interface

In addition to the I²S audio interface, the DS90UH929-Q1 serializer also supports TDM format. Since a number of specifications for TDM format are in common use, the DS90UH929-Q1 offers flexible support for word length, bit clock, number of channels to be multiplexed, and so forth. For example, assume that the word clock signal (I2S_WC) period = 256 × bit clock (I2S_CLK) time period. In this case, the DS90UH929-Q1 can multiplex 4 channels with maximum word length of 64 bits each, or 8 channels with maximum word length of 32 bits each. Figure 13 shows the multiplexing of 8 channels with 24-bit word length, in a format similar to I2S.

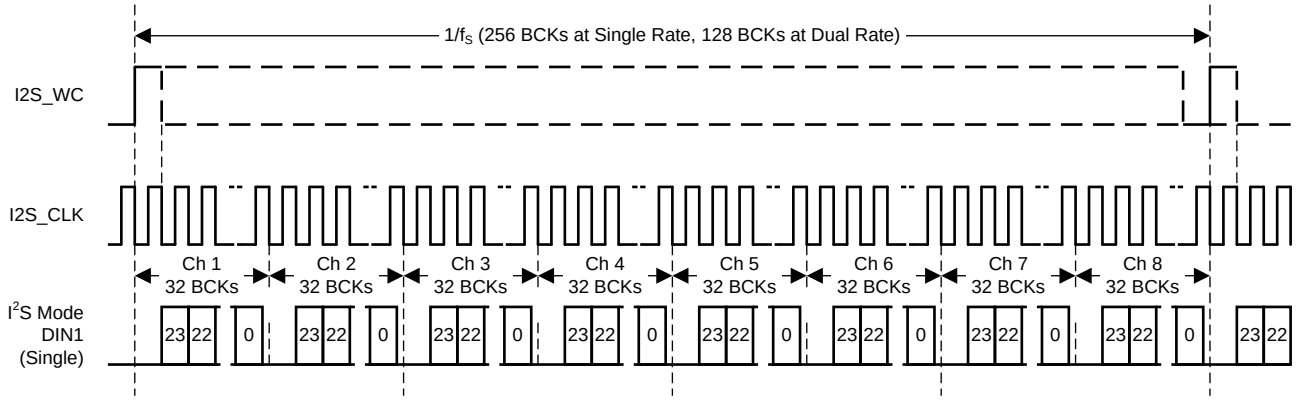


Figure 13. TDM Format

7.3.17 HDCP

The HDCP Cipher function is implemented in the serializer per HDCP v1.4 specification. The serializer provides HDCP encryption of audiovisual content when connected to an HDCP capable source. HDCP authentication and shared key generation is performed using the HDCP Control Channel, which is embedded in the forward and backward channels of the serial link. On-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

7.3.17.1 HDCP I2S Audio Encryption

Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. When HDCP is active, packetized Data Island Transport audio is also encrypted along with the video data per HDCP v.1.4. I2S audio transmitted in Forward Channel Frame Transport mode is not encrypted. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

7.3.18 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.18.1 BIST Configuration And Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external TMDS clock or the internal Oscillator clock (OSC) frequency. In the absence of the TMDS clock, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored in real time on the deserializer PASS pin with each detected error resulting in a half-pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A High on PASS indicates no errors were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See Figure 14 for the BIST mode flow diagram.

Step 1: The Serializer is paired with another FPD-Link III Deserializer, then BIST Mode is enabled through the BISTEN pin or through register on the Deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x04[5] be toggled locally on the Serializer (set 0x04[5]=1, then set 0x04[5]=0). The desired clock source is selected through the deserializer BISTC pin or through register on the Deserializer.

Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. When the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one-half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To stop the BIST mode, the deserializer BISTEN pin is set low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error-free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is reset, or the device is powered down. The BIST duration is user-controlled by the duration of the BISTEN signal.

Step 4: The link returns to normal operation after the deserializer BISTEN pin is low. Figure 15 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

For more information on using BIST, refer to the white paper: Using BIST on 94x.

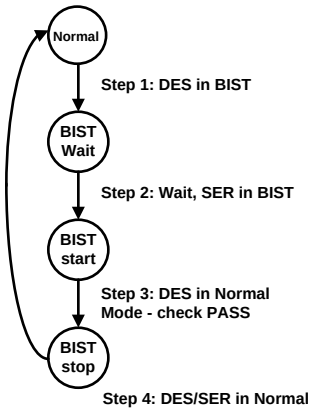


Figure 14. BIST Mode Flow Diagram

7.3.18.2 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal all-zeroes pattern. The internal all-zeroes pattern goes through the scrambler, DC-balancing, and so forth and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 8). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only, and the register keeps a record of the last BIST run until the register is cleared or the serializer enters BIST mode again.

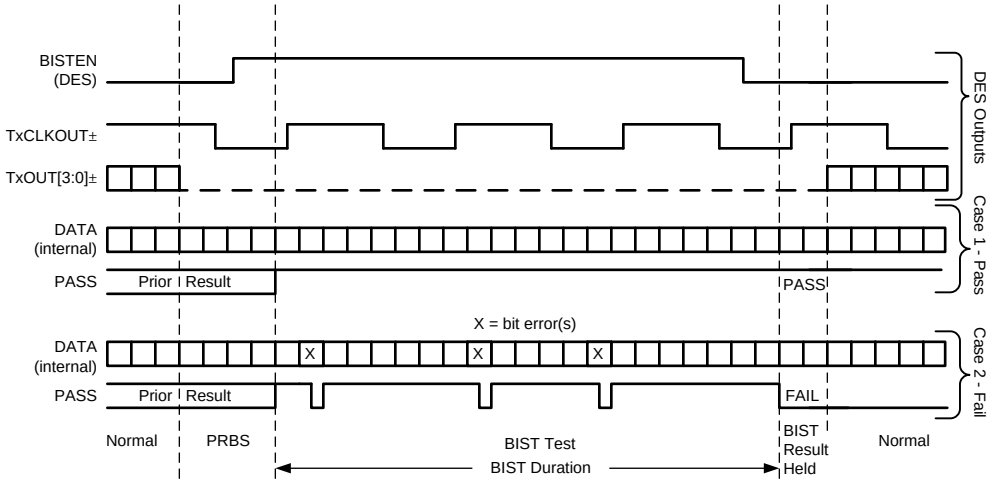


Figure 15. BIST Waveforms, in Conjunction With Deserializer Signals

7.3.19 Internal Pattern Generation

The DS90UH929-Q1 serializer provides an internal pattern generation feature that allows for basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and provide quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For more information, refer to *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).

7.3.19.1 Pattern Options

The DS90UH929-Q1 serializer pattern generator is capable of generating 17 default patterns designers can use for basic testing and debugging of panels. Each can be inverted using register bits (Table 8), shown below:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White
8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color (or its inversion) configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

Additionally, the Pattern Generator incorporates one configurable full-screen, 24-bit color pattern, which is controlled by the PGRS, PGGS, and PGBS registers. This is pattern #14. One of the pattern options is statically selected in the PGCTL register when Auto-Scrolling is disabled. The PGTSC and PGTSO1-8 registers control the pattern selection and order when Auto-Scrolling is enabled.

7.3.19.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (Table 8). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0.

7.3.19.3 Video Timing Modes

The Pattern Generator has two video timing modes—external and internal. In external timing mode, the Pattern Generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the Pattern Generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the Pattern Generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or internal timing with external clock are enabled by the control registers (Table 8).

7.3.19.4 External Timing

In external timing mode, the Pattern Generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two-pixel clock delay. It extracts the active frame dimensions from the incoming signals to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the Pattern Generator determines the Vertical Blank time by detecting a long period of pixel clocks without DE asserted.

7.3.19.5 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen Cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

7.3.19.6 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

7.3.19.7 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. It consists of the Pattern Generator Indirect Address (PGIA reg_0x66 — Table 8) and the Pattern Generator Indirect Data (PGID reg_0x67 — Table 8). See *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).

7.3.20 Spread Spectrum Clock Tolerance

The DS90UH929-Q1 (for DVI mode) tolerates a spread spectrum input clock to help reduce EMI. The following triangular SSC profile is supported:

- Frequency deviation ≤ 2.5%
- Modulation rate ≤ 100 kHz

Maximum frequency deviation and maximum modulation rate are not supported simultaneously. Some typical examples:

- Frequency deviation: 2.5%, modulation rate: 50 kHz
- Frequency deviation: 1.25%, modulation rate: 100 kHz

7.4 Device Functional Modes

7.4.1 Mode Select Configuration Settings (MODE_SEL[1:0])

Configuration of the device may be done through the MODE_SEL[1:0] input pins, or through the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs. See Table 5 and Table 6. These values will be latched into the register location during power-up:

Table 4. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
EDID_SEL: Display ID Select	0	Look for remote EDID. If none found, use internal SRAM EDID. Can be overridden from register. Remote EDID address may be overridden from default 0xA0.
	1	Use external local EDID.
AUX_I2S: AUX Audio Channel	0	HDMI audio.
	1	HDMI + AUX audio channel.
EXT_CTL: External Controller Override	0	Internal HDCP/HDMI control.
	1	External HDCP/HDMI control from I2C interface pins.
COAX: Cable Type	0	Enable FPD-Link III for twisted-pair cabling.
	1	Enable FPD-Link III for coaxial cabling.
REM_EDID_LOAD: Remote EDID Load	0	Use internal SRAM EDID.
	1	If available, remote EDID is copied into internal SRAM EDID.

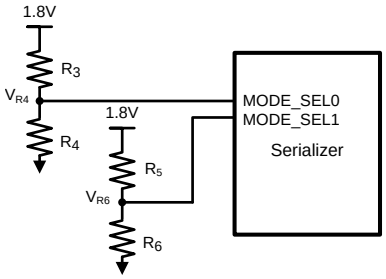


Figure 16. MODE_SEL[1:0] Connection Diagram

Table 5. Configuration Select (MODE_SEL0)

#	RATIO V_{R4}/V_{DD18}	TARGET V_{R4} (V)	SUGGESTED RESISTOR PULLUP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULLDOWN R4 kΩ (1% tol)	EDID_SEL	AUX_I2S
1	0	0	OPEN	Any value less than 100 (1)	0	0
2	0.208	0.374	118	30.9	0	1
3	0.553	0.995	82.5	102	1	0
4	0.668	1.202	68.1	137	1	1

(1) This resistor does not need to be 1% tolerance. 5% is acceptable.

Table 6. Configuration Select (MODE_SEL1)

#	RATIO V_{R6}/V_{DD18}	TARGET V_{R6} (V)	SUGGESTED RESISTOR PULLUP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULLDOWN R6 kΩ (1% tol)	EXT_CTL	COAX	REM_EDID_LOAD
1	0	0	OPEN	Any value less than 100 (1)	0	0	0

(1) This resistor does not need to be 1% tolerance. 5% is acceptable.

Table 6. Configuration Select (MODE_SEL1) (continued)

#	RATIO V_{R6}/V_{DD18}	TARGET V_{R6} (V)	SUGGESTED RESISTOR PULLUP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULLDOWN R6 kΩ (1% tol)	EXT_CTL	COAX	REM_EDID_LOAD
2	0.208	0.374	118	30.9	0	0	1
3	0.323	0.582	107	51.1	0	1	0
4	0.440	0.792	113	88.7	0	1	1
5	0.553	0.995	82.5	102	1	0	0
6	0.668	1.202	68.1	137	1	0	1
7	0.789	1.420	56.2	210	1	1	0
8	1	1.8	Any value less than 100 (1)	OPEN	1	1	1

The strapped values can be viewed and/or modified in the following locations:

- EDID_SEL : Latched into BRIDGE_CTL[0], EDID_DISABLE (0x4F[0]).
- AUX_I2S : Latched into BRIDGE_CFG[1], AUDIO_MODE[1] (0x54[1]).
- EXT_CTL: Latched into BRIDGE_CFG[7], EXT_CONTROL (0x54[7]).
- COAX : Latched into DUAL_CTL1[7], COAX_MODE (0x5B[7]).
- REM_EDID_LOAD : Latched into BRIDGE_CFG[5] (0x54[5]).

7.4.2 FPD-Link III Single Link Operation

The single link mode of the device transmits the video over a single FPD-Link III to a single receiver. Single link mode supports frequencies up to 96 MHz for 24-bit video when paired with the DS90UH940-Q1/DS90UH948-Q1. This mode is compatible with the DS90UH926Q-Q1/DS90UH928Q-Q1 when operating below 85 MHz.

7.4.3 Frequency Detection Circuit May Reset the FPD-Link III PLL During a Temperature Ramp

When ambient temperature around the DS90UH929-Q1 changes by more than 40°C, the frequency detection logic in the device can RESET the FPD-Link III PLL even though the input PCLK has not changed. This behavior may result in a loss of lock in the Deserializer and flicker on the system display.

The following programming sequence is required for all systems. This should be written after the user register configuration of the DS90UH929-Q1 and downstream deserializer configuration.

- Disable the “Reset FPD-Link III PLL on Frequency Change” feature after the DS90UX9X9-Q1 power-up.
  - Set Reg0x5B[5]=0b (Disable PLL reset feature via RST_PLL_FREQ field in DUAL_CTL1 register)

Any device configuration including this one should be written as a part of the Init A sequence as shown in Figure 29.

7.5 Programming

7.5.1 Serial Control Bus

This serializer may also be configured by the use of a I2C-compatible serial control bus. Multiple devices may share the serial control bus (up to 8 device addresses supported). The device address is set through a resistor divider (R1 and R2 — see Figure 17 below) connected to the IDx pin.

Programming (continued)

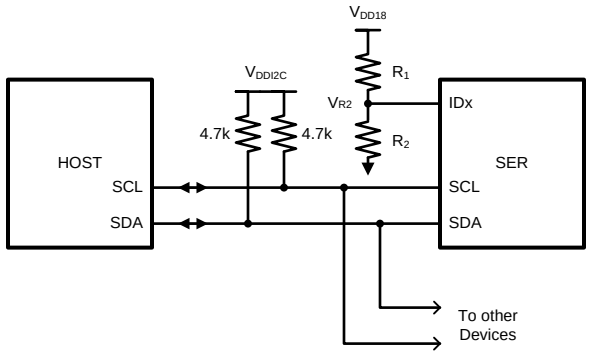


Figure 17. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{DD18} or V_{DD33}. For most applications, a 4.7-kΩ pullup resistor is recommended. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 8 possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage on the IDx input pin See Table 8. 1% or 5% resistors can be used.

Table 7. Serial Control Bus Addresses for IDx

#	RATIO V_{R2} / V_{DD18}	IDEAL V_{R2} (V)	SUGGESTED RESISTOR R1 kΩ (1% tol)	SUGGESTED RESISTOR R2 kΩ (1% tol)	7-BIT ADDRESS	8-BIT ADDRESS
1	0	0	OPEN	Any value less than 100 (1)	0x0C	0x18
2	0.208	0.374	118	30.9	0x0E	0x1C
3	0.323	0.582	107	51.1	0x10	0x20
4	0.440	0.792	113	88.7	0x12	0x24
5	0.553	0.995	82.5	102	0x14	0x28
6	0.668	1.202	68.1	137	0x16	0x2C
7	0.789	1.420	56.2	210	0x18	0x30
8	1	1.8	Any value less than 100 (1)	OPEN	0x1A	0x34

(1) This resistor does not need to be 1% tolerance. 5% is acceptable.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 18.

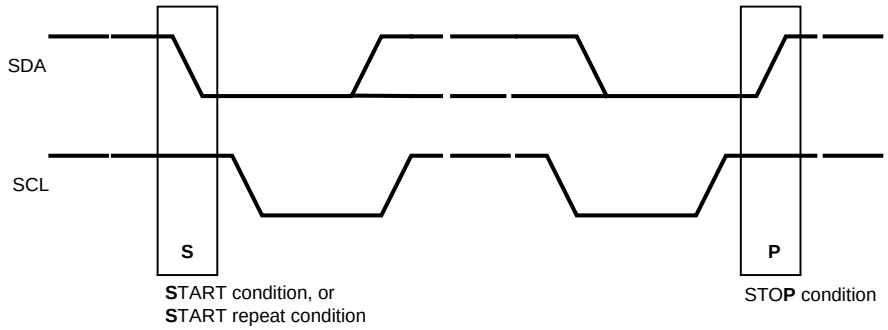


Figure 18. Start and Stop Conditions

To communicate with an I2C slave, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus Low. If the address does not match a slave address of the device, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know that the host is ready to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 19 and a WRITE is shown in Figure 20.

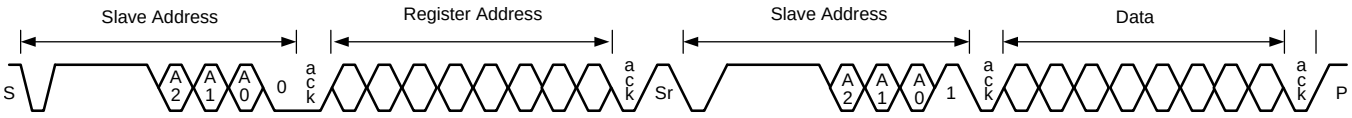


Figure 19. Serial Control Bus — Read

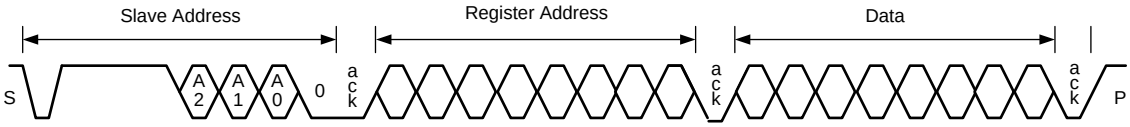


Figure 20. Serial Control Bus — Write

The I2C Master located at the serializer must support I2C clock stretching. For more information on I^2C interface requirements and throughput considerations, refer to the TI Application Note *AN-2173 I2C Communication Over FPD-Link III with Bidirectional Control Channel* (SNLA131).

7.5.2 Multi-Master Arbitration Support

The Bidirectional Control Channel in the FPD-Link III devices implements I^2C-compatible bus arbitration in the proxy I2C master implementation. When sending a data bit, each I2C master senses the value on the SDA line. If the master is sending a logic 1 but senses a logic 0, the master has lost arbitration. It will stop driving SDA, retrying the transaction when the bus becomes idle. Thus, multiple I2C masters may be implemented in the system.

Ensure that all I2C masters on the bus support multi-master arbitration.

Assign I2C addresses with more than a single bit set to 1 for all devices on the I^2C bus. 0x6A, 0x7B, and 0x37 are examples of good choices for an I2C address. 0x40 and 0x20 are examples of bad choices for an I2C address.

If the system does require master-slave operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available read/write registers in the deserializer to allow masters to communicate with each other to pass control between the two masters. An example would be to use register 0x18 or 0x19 in the deserializer as a mailbox register to pass control of the channel from one master to another.

7.5.3 I2C Restrictions on Multi-Master Operation

The I2C specification does not provide for arbitration between masters under certain conditions. The system should make sure the following conditions cannot occur to prevent undefined conditions on the I^2C bus:

- One master generates a repeated Start while another master is sending a data bit.
- One master generates a Stop while another master is sending a data bit.
- One master generates a repeated Start while another master sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I2C slave.

7.5.4 Multi-Master Access to Device Registers for Newer FPD-Link III Devices

When using the latest generation of FPD-Link III devices, DS90UH929-Q1 or DS90UH940-Q1/DS90UH948-Q1 registers may be accessed simultaneously from both local and remote I2C masters. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I2C slaves would still be allowed in only one direction at a time.

7.5.5 Multi-Master Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices, simultaneous access to serializer or deserializer registers from both local and remote I2C masters may cause incorrect operation, thus restrictions should be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in an errored read or write.

Two basic options are recommended. The first is to allow device register access only from one controller. This would allow only the Host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer would not be allowed to access the deserializer or serializer registers.

The second basic option is to allow local register access only with no access to remote serializer or deserializer registers. The Host controller would be allowed to access the serializer registers while a controller at the deserializer could access those register only. Access to remote I2C slaves would still be allowed in one direction.

In a very limited case, remote and local access could be allowed to the deserializer registers at the same time. Register access can work as intended if both local and remote masters are accessing the same deserializer register. This allows a simple method of passing control of the Bidirectional Control Channel from one master to another.

7.5.6 Restrictions on Control Channel Direction for Multi-Master Operation

Only one direction should be active at any time across the Bidirectional Control Channel. If both directions are required, some method of transferring control between I2C masters should be implemented.

7.6 Register Maps

Table 8. Serial Control Bus Registers

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
0	0x00	I2C Device ID	7:1	RW	Strap	DEVICE_ID	7-bit address of Serializer. Defaults to address configured by the IDx strap pin.
			0	RW	0x00	ID Setting	I2C ID setting. 0: Device I2C address is from IDx strap pin (default). 1: Device I2C address is from 0x00[7:1].
1	0x01	Reset A software I2C reset command issued by writing to register 0x01 is supported only when operating I2C in the 3.3V mode.	7:5		0x00		Reserved.
			4	RW		HDMI Reset	HDMI Digital Reset. Resets the HDMI digital block. This bit is self-clearing. 0: Normal operation. 1: Reset.
			3:2				Reserved.
			1	RW		Digital RESET1	Reset the entire digital block including registers. This bit is self-clearing. 0: Normal operation (default). 1: Reset. Following the setting of this bit, the software should also set bit 0x4F[1] (BRIDGE_CTL register). This will restore register values that are initially loaded from Non-Volatile Memory to their default state.
			0	RW		Digital RESET0	Reset the entire digital block except registers. This bit is self-clearing. 0: Normal operation (default). 1: Reset. Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table. Registers 0x00, 0x13, 0x15, 0x18, 0x19, 0x1A, 0x48-0x55, 0x58, 0x5B, 0xC0, 0xC2, 0xC3, 0xC6, 0xC8, 0xCE and 0xD0 are also restored to their default value when this bit is set.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
3	0x03	General Configuration	7	RW	0xD2	Back channel CRC Checker Enable	Enable/disable back channel CRC Checker. 0: Disable. 1: Enable (default).
			6				***Reserved***.
			5	RW		I2C Remote Write Auto Acknowledge	Automatically acknowledge I2C remote writes. When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. Note: this mode will prevent any NACK from a remote device from reaching the I2C master. 0: Disable (default). 1: Enable.
			4	RW		Filter Enable	HS, VS, DE two-clock filter. When enabled, pulses less than two full TMDS clock cycles on the DE, HS, and VS inputs will be rejected. 0: Filtering disable. 1: Filtering enable (default).
			3	RW		I2C Pass-through	I2C pass-through mode. Read/Write transactions matching any entry in the Slave Alias registers will be passed through to the remote Deserializer. 0: Pass-through disabled (default). 1: Pass-through enabled.
			2				***Reserved.***
			1	RW		TMDS Clock Auto	Switch over to internal oscillator in the absence of TMDS Clock. 0: Disable auto-switch. 1: Enable auto-switch (default).
			0				***Reserved.***
4	0x04	Mode Select	7	RW	0x80	Failsafe State	Input failsafe state. 0: Failsafe to High. 1: Failsafe to Low (default).
			6				***Reserved.***
			5	RW		CRC Error Reset	Clear back channel CRC Error counters. This bit is NOT self-clearing. 0: Normal operation (default). 1: Clear counters.
			4	RW		Video gate	Set to 1. This prevents video from being sent during the blanking interval.
			3:0				Reserved.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
5	0x05	I2C Control	7:5		0x00		***Reserved.***
			4:3	RW		SDA Output Delay	Configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns (default). 01: 280ns. 10: 320ns. 11: 360ns.
			2	RW		Local Write Disable	Disable remote writes to local registers. Setting this bit to 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer. 0: Enable (default). 1: Disable.
			1	RW		I2C Bus Timer Speedup	Speed up I2C bus Watchdog Timer. 0: Watchdog Timer expires after approximately 1s (default). 1: Watchdog Timer expires after approximately 50µs.
			0	RW		I2C Bus Timer Disable	Disable I2C bus Watchdog Timer. The I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1s, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 0: Enable (default). 1: Disable.
6	0x06	DES ID	7:1	RW	0x00	DES Device ID	7-bit I2C address of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
			0	RW		Freeze Device ID	Freeze Deserializer Device ID. 1: Prevents auto-loading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. 0: Allows auto-loading of the Deserializer Device ID from the Bidirectional Control Channel.
7	0x07	Slave ID[0]	7:1	RW	0x00	Slave ID 0	7-bit I2C address of the remote Slave 0 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 0.
			0				***Reserved.***

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
8	0x08	Slave Alias[0]	7:1	RW	0x00	Slave Alias ID 0	7-bit Slave Alias ID of the remote Slave 0 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 0 register. A value of 0 in this field disables access to the remote Slave 0.
			0				***Reserved.***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB	Number of back channel CRC errors – 8 least significant bits. Cleared by 0x04[5].
11	0x0B		7:0	R	0x00	CRC Error MSB	Number of back channel CRC errors – 8 most significant bits. Cleared by 0x04[5].
12	0x0C	General Status	7:5				***Reserved.***
			4		0x00	Link Lost	Link lost flag for selected port: This bit indicates that loss of link has been detected. This register bit will stay high until cleared using the CRC Error Reset in register 0x04.
			3	R		BIST CRC Error	Back channel CRC error(s) during BIST communication with Deserializer. This bit is cleared upon loss of link, restart of BIST, or assertion of CRC Error Reset bit in 0x04[5]. 0: No CRC errors detected during BIST. 1: CRC error(s) detected during BIST.
			2	R		TMDS Clock Detect	Pixel clock status: 0: Valid clock not detected at HDMI input. 1: Valid clock detected at HDMI input.
			1	R		DES Error	CRC error(s) during normal communication with Deserializer. This bit is cleared upon loss of link or assertion of 0x04[5]. 0: No CRC errors detected. 1: CRC error(s) detected.
			0	R		Link Detect	Link detect status: 0: Cable link not detected. 1: Cable link detected.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
13	0x0D	GPIO0 Configuration	7:4	R		Revision ID	Revision ID.
			3	RW	0x00	GPIO0 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			2:0	RW		GPIO0 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™ 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.
14	0x0E	GPIO1 and GPIO2 Configuration	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			6:4	RW		GPIO2 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.
			3	RW		GPIO1 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			2:0	RW		GPIO1 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
15	0x0F	GPIO3 Configuration	7:4		0x00		***Reserved.***
			3	RW		GPIO3 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			2:0	RW		GPIO3 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.
16	0x10	GPIO5_REG and GPIO6_REG Configuration	7	RW	0x00	GPIO6_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			6				***Reserved.***
			5:4	RW		GPIO6_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE™. 01: GPIO mode, output. 11: GPIO mode; input.
			3	RW		GPIO5_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			2				***Reserved.***
			1:0	RW		GPIO5_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE™. 01: GPIO mode, output. 11: GPIO mode; input.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
17	0x11	GPIO7_REG and GPIO8_REG Configuration	7	RW	0x00	GPIO8_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			6				***Reserved.***
			5:4	RW		GPIO8_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.
			3	RW		GPIO7_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			2				***Reserved.***
			1:0	RW		GPIO7_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
18	0x12	Data Path Control	7		0x00		***Reserved.***
			6	RW		Pass RGB	Setting this bit causes RGB data to be sent independent of DE. However, setting this bit prevents HDCP operation and blocks packetized audio. 0: Normal operation. 1: Pass RGB independent of DE.
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low). 1: DE is inverted (active low, idle high).
			4	RW		I2S Repeater Regen	Regenerate I2S data from Repeater I2S pins. 0: Repeater pass through I2S from video pins (default). 1: Repeater regenerate I2S from I2S pins.
			3	RW		I2S Channel B Enable Override	I2S Channel B Enable Override. 0: Disable I2S Channel B override. 1: Set I2S Channel B Enable from 0x12[0].
			2	RW		18-Bit Video Select	0: Select 24-bit video mode. 1: Select 18-bit video mode.
			1	RW		I2S Transport Select	Select I2S transport mode: 0: Enable I2S Data Island transport (default). 1: Enable I2S Data Forward Channel Frame transport.
			0	RW		I2S Channel B Enable	I2S Channel B Enable. 0: I2S Channel B disabled. 1: Enable I2S Channel B on B1 input. Note that in a repeater, this bit may be overridden by the in-band I2S mode detection.
19	0x13	General Purpose Control	7	R	0x88	MODE_SEL1 Done	Indicates MODE_SEL1 value has stabilized and has been latched.
			6:4	R		MODE_SEL1 Decode	Returns the 3-bit decode of the MODE_SEL1 pin.
			3	R		MODE_SEL0 Done	Indicates MODE_SEL0 value has stabilized and has been latched.
			2:0	R		MODE_SEL0 Decode	Returns the 3-bit decode of the MODE_SEL0 pin.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
20	0x14	BIST Control	7:3		0x00		***Reserved.***
			2:1	RW		OSC Clock Source	Allows choosing different OSC clock frequencies for forward channel frame. OSC clock frequency in functional mode when TMDS clock is not present and 0x03[2]=1: 00: 50 MHz oscillator. 01: 50 MHz oscillator. 10: 100 MHz oscillator. 11: 25 MHz oscillator. Clock source in BIST mode i.e. when 0x14[0]=1: 00: External pixel clock. 01: 33 MHz oscillator. 1x: 100 MHz oscillator.
			0	RW		BIST Enable	BIST control: 0: Disabled (default). 1: Enabled.
21	0x15	I2C Voltage Select	7:0	RW	0x01	I2C Voltage Select	Selects 1.8 or 3.3V for the I2C_SDA and I2C_SCL pins. This register is loaded from the I2C_VSEL strap option from the SCLK pin at power-up. At power-up, a logic LOW will select 3.3V operation, while a logic HIGH (pull-up resistor attached) will select 1.8V signaling. Issuing either of the digital resets via register 0x01 will cause the I2C_VSEL value to be reset to 3.3V operation. Reads of this register return the status of the I2C_VSEL control: 0: Select 1.8V signaling. 1: Select 3.3V signaling. This bit may be overwritten via register access or via eFuse program by writing an 8-bit value to this register: Write 0xb5 to set I2C_VSEL. Write 0xb6 to clear I2C_VSEL.
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0. Set to 0x01.
			0	RW		Timer Control	Disable Bidirectional Control Channel (BCC) Watchdog Timer: 0: Enable BCC Watchdog Timer operation (default). 1: Disable BCC Watchdog Timer operation.
23	0x17	I2C Control	7	RW	0x1E	I2C Pass All	0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID (default). 1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID.
			6:4	RW		SDA Hold Time	Internal SDA hold time: Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
			3:0	RW		I2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
24	0x18	SCL High Time	7:0	RW	0x7F	TX_SCL_HIGH	I2C Master SCL high time: This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional oscillator clock periods. Min_delay = 38.0952ns * (TX_SCL_HIGH + 5).
25	0x19	SCL Low Time	7:0	RW	0x7F	TX_SCL_LOW	I2C Master SCL low time: This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay = 38.0952ns * (TX_SCL_LOW + 5).
26	0x1A	Data Path Control 2	7:4				***Reserved.***
			3	R	Strap	SECONDARY_AUDIO	Enable Secondary Audio. This register indicates that the AUX audio channel is enabled. The control for this function is via the AUX_AUDIO bit in the BRIDGE_CFG register register offset 0x54). The AUX_AUDIO control is strapped from the MODE_SEL0 pin at power-up.
			2		0x01		Reserved.
			1	RW		MODE_28B	Enable 28-bit Serializer Mode. 0: 24-bit high-speed data + 3 low-speed control (DE, HS, VS). 1: 28-bit high-speed data mode.
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport: 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0. 1: 5.1- or 7.1-channel audio is enabled. Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection (default).
27	0x1B	BIST BC Error Count	7:0	R	0x00	BIST BC Error	BIST back channel CRC error counter. This register stores the back channel CRC error count during BIST Mode (saturates at 255 errors). Clears when a new BIST is initiated or by 0x04[5].

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
28	0x1C	GPIO Pin Status 1	7	R	0x00	GPIO7_REG Pin Status	GPIO7_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			6	R		GPIO6_REG Pin Status	GPIO6_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			5	R		GPIO5_REG Pin Status	GPIO5_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			4				***Reserved.***
			3	R		GPIO3 Pin Status	GPIO3 input pin status. Note: status valid only if pin is set to GPI (input) mode.
			2	R		GPIO2 Pin Status	GPIO2 input pin status. Note: status valid only if pin is set to GPI (input) mode.
			1	R		GPIO1 Pin Status	GPIO1 input pin status. Note: status valid only if pin is set to GPI (input) mode.
			0	R		GPIO0 Pin Status	GPIO0 input pin status. Note: status valid only if pin is set to GPI (input) mode.
29	0x1D	GPIO Pin Status 2	7:1		0x00		***Reserved***
			0	R		GPIO8_REG Pin Status	GPIO8_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
30	0x1E	Transmitter Port Select	7:3				Reserved.
			2	RW	0x01	PORT1_I2C_EN	Port1 I2C Enable. Enables secondary I2C address. The second I2C address provides access to Port1 registers as well as registers that are shared between Port0 and Port1. The second I2C address value will be set to DeviceID + 1 (7-bit format). The PORT1_I2C_EN bit must also be set to allow accessing remote devices over the second link when the device is in Replicate mode.
			1	RW		PORT1_SEL	Selects Port1 for register access from primary I2C address. For writes, Port1 registers and shared registers will both be written. For reads, Port1 registers and shared registers will be read. This bit must be cleared to read Port0 registers. This bit is ignored if PORT1_I2C_EN is set.
			0	RW		PORT0_SEL	Selects Port0 for register access from primary I2C address. For writes, Port0 registers and shared registers will both be written. For reads, Port0 registers and shared registers will be read. Note that if PORT1_SEL is also set, then Port1 registers will be read. This bit is ignored if PORT1_I2C_EN is set.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
31	0x1F	Frequency Counter	7:0	RW	0x00	Frequency Count	Frequency counter control. A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 40ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.
32	0x20	Deserializer Capabilities 1	7	RW	0x00	FREEZE_DES_CAP	Freeze Deserializer Capabilities. Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x20 and 0x21.
			6				Reserved.
			5			SEND_FREQ	Send Frequency Training Pattern. Indicates the DS90UH929-Q1 should send the Frequency Training Pattern. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
			4	RW	0x00	SEND_EQ	Send Equalization Training Pattern. Indicates the DS90UH929-Q1 should send the Equalization Training Pattern. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
			3	RW		DUAL_LINK_CAP	Dual link Capabilities. Indicates if the Deserializer is capable of dual link operation. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
			2	RW		DUAL_CHANNEL	Dual Channel 0/1 Indication. In a dual-link capable device, indicates if this is the primary or secondary channel. 0: Primary channel (channel 0). 1: Secondary channel (channel 1). This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
32	0x20	Deserializer Capabilities 1	1	RW	0x00	VID_24B_HD_AUD	Deserializer supports 24-bit video concurrently with HD audio. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
			0	RW		DES_CAP_FC_GPIO	Deserializer supports GPIO in the Forward Channel Frame. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
33	0x21	Deserializer Capabilities 2	7:2				Reserved.
			1:0				Reserved.
38	0x26	Link Detect Control	7:3				Reserved.
			2:0	RW	0x00	LINK DETECT TIMER	Bidirectional Control Channel Link Detect Timer. This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 000: 162 microseconds. 001: 325 microseconds. 010: 650 microseconds. 011: 1.3 milliseconds. 100: 10.25 microseconds. 101: 20.5 microseconds. 110: 41 microseconds. 111: 82 microseconds.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
48	0x30	SCLK_CTRL	7	RW	0x00	SCLK/WS	SCLK to Word Select Ratio. 0 : 64. 1 : 32.
			6:5	RW		MCLK/SCLK	MCLK to SCLK Select Ratio. 00 : 4. 01 : 2. 10 : 1. 11 : 8.
			4:3	RW		CLEAN CLOCK_DIV	Clock Cleaner divider. 00 : FPD_VCO_CLOCK/8. 01 : FPD_VCO_CLOCK/4. 10 : FPD_VCO_CLOCK/2. 11 : AON_OSC.
			2:1	RW		CLEAN Mode	If non-zero, the SCLK Input or HDMI N/CTS generated Audio Clock is cleaned digitally before being used. 00 : Off. 01 : ratio of 1. 10 : ratio of 2. 11 : ratio of 4.
			0	RW		MASTER	If set, the SCLK I/O and the WS_IO are used as an output and the Clock Generation Circuits are enabled, otherwise they are inputs.
49	0x31	AUDIO_CTS0	7:0	RW	0x00	CTS[7:0]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
50	0x32	AUDIO_CTS1	7:0	RW	0x00	CTS[15:8]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
51	0x33	AUDIO_CTS2	7:0	RW	0x00	CTS[23:16]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
52	0x34	AUDIO_N0	7:0	RW	0x00	N[7:0]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
53	0x35	AUDIO_N1	7:0	RW	0x00	N[15:8]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
54	0x36	AUDIO_N2_COEFF	7:4	RW	0x00	COEFF[3:0]	Selects the LPF_COEFF in the Clock Cleaner (Feedback is divided by 2^COEFF).
			3:0	RW	0x00	N[19:16]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
55	0x37	CLK_CLEAN_STS	7:6				Reserved.
			5:3	R	0x00	IN_FIFO_LVL	Clock Cleaner Input FIFO Level.
			2:0	R	0x00	OUT_FIFO_LVL	Clock Cleaner Output FIFO Level.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
64	0x40	ANA_IA_CNTL	7:5		0x00		Reserved.
			4:2	RW		ANA_IA_SEL	Analog register select Selects target for register access 000b: Disabled 001b - 011b: Reserved 100b: HDMI Registers 101b: FPD3 TX Registers 11xb: Reserved
			1	RW		ANA_AUTO_INC	Analog Register Auto Increment 0: Disable auto-increment mode 1: Enable auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1.
			0	RW		ANA_IA_READ	Start Analog Register Read 0: Write analog register 1: Read analog register
65	0x41	ANA_IA_ADDR	7:0	RW	0x00	ANA_IA_ADDR	Analog register offset This register contains the 8-bit register offset for the indirect access.
66	0x42	ANA_IA_DATA	7:0	RW	0x00	ANA_IA_DATA	Analog register data Writing this register will cause an indirect write of the ANA_IA_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register.
72	0x48	APB_CTL	7:5				Reserved.
			4:3	RW	0x00	APB_SELECT	APB Select: Selects target for register access. 00 : HDMI APB interface. 01 : EDID SRAM. 10 : Configuration Data (read only). 11 : Die ID (read only).
			2	RW		APB_AUTO_INC	APB Auto Increment: Enables auto-increment mode. Upon completion of an APB read or write, the APB address will automatically be incremented by 0x4 for HDMI registers or by 0x1 for others.
			1	RW		APB_READ	Start APB Read: Setting this bit to a 1 will begin an APB read. Read data will be available in the APB_DATAx registers. The APB_ADRx registers should be programmed prior to setting this bit. This bit will be cleared when the read is complete.
			0	RW		APB_ENABLE	APB Interface Enable: Set to a 1 to enable the APB interface. The APB_SELECT bits indicate what device is selected.
73	0x49	APB_ADR0	7:0	RW	0x00	APB_ADR0	APB Address byte 0 (LSB).
74	0x4A	APB_ADR1	7:0	RW	0x00	APB_ADR1	APB Address byte 1 (MSB).
75	0x4B	APB_DATA0	7:0	RW	0x00	APB_DATA0	Byte 0 (LSB) of the APB Interface Data.
76	0x4C	APB_DATA1	7:0	RW	0x00	APB_DATA1	Byte 1 of the APB Interface Data.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
77	0x4D	APB_DATA2	7:0	RW	0x00	APB_DATA2	Byte 2 of the APB Interface Data.
78	0x4E	APB_DATA3	7:0	RW	0x00	APB_DATA3	Byte 3 (MSB) of the APB Interface Data.
79	0x4F	BRIDGE_CTL	7:5				Reserved.
			4	RW	0x00	CEC_CLK_SRC	CEC Clock Source Select: Selects clock source for generating the 32.768kHz clock for CEC operations in the HDMI Receive Controller. 0 : Selects internal generated clock. 1 : Selects external 25MHz oscillator clock.
			3	RW		CEC_CLK_EN	CEC Clock Enable: Enable CEC clock generation. Enables generation of the 32.768kHz clock for the HDMI Receive controller. This bit should be set prior to enabling CEC operation via the HDMI controller registers.
			2	RW		EDID_CLEAR	Clear EDID SRAM: Set to 1 to enable clearing the EDID SRAM. The EDID_INIT bit must be set at the same time for the clear to occur. This bit will be cleared when the initialization is complete.
			1	RW		EDID_INIT	Initialize EDID SRAM from EEPROM: Causes a reload of the EDID SRAM from the non-volatile EDID EEPROM. This bit will be cleared when the initialization is complete.
			0	R	Strap	EDID_DISABLE	Disable EDID access via DDC/I2C: Disables access to the EDID SRAM via the HDMI DDC interface. This value is loaded from the MODE_SEL0 pin at power-up.
80	0x50	BRIDGE_STS	7	R	0x03	RX5V_DETECT	RX +5V detect: Indicates status of the RX_5V pin. When asserted, indicates the HDMI interface has detected valid voltage on the RX_5V input.
			6	R		HDMI_INT	HDMI Interrupt Status: Indicates an HDMI Interrupt is pending. HDMI interrupts are serviced through the HDMI Registers via the APB Interface.
			5	R		HDCP_INT	HDCP Interrupt Status: Indicates an HDCP Transmitter Interrupt is pending. HDCP Transmit interrupts are serviced through the HDCP Interrupt Control and Status registers.
			4	R		INIT_DONE	Initialization Done: Initialization sequence has completed. This step will complete after configuration complete (CFG_DONE).
			3	R		REM_EDID_LOAD	Remote EDID Loaded: Indicates EDID SRAM has been loaded from a remote EDID EEPROM device over the Bidirectional Control Channel. The EDID_CKSUM value indicates if the EDID load was successful.
			2	R		CFG_DONE	Configuration Complete: Indicates automatic configuration has completed. This step will complete prior to initialization complete (INIT_DONE).
			1	R		CFG_CKSUM	Configuration checksum status: Indicates result of Configuration checksum during initialization. The device verifies the 2's complement checksum in the last 128 bytes of the EEPROM. A value of 1 indicates the checksum passed.
			0	R		EDID_CKSUM	EDID checksum Status: Indicates result of EDID checksum during EDID initialization. The device verifies the 2's complement checksum in the first 256 bytes of the EEPROM. A value of 1 indicates the checksum passed.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
81	0x51	EDID_ID	7:1	RW	0x50	EDID_ID	EDID I2C Slave Address: I2C address used for accessing the EDID information. These are the upper 7 bits in 8-bit format addressing, where the lowest bit is the Read/Write control.
			0	RW	0	EDID_RDONLY	EDID Read Only: Set to a 1 puts the EDID SRAM memory in read-only mode for access via the HDMI DDC interface. Setting to a 0 allows writes to the EDID SRAM memory.
82	0x52	EDID_CFG0	7				Reserved.
			6:4	RW	0x01	EDID_SDA_HOLD	Internal SDA Hold Time: This field configures the amount of internal hold time provided for the DDC_SDA input relative to the DDC_SCL input. Units are 40 nanoseconds. The hold time is used to qualify the start detection to avoid false detection of Start or Stop conditions.
			3:0	RW	0x0E	EDID_FLTR_DPTH	I2C Glitch Filter Depth: This field configures the maximum width of glitch pulses on the DDC_SCL and DDC_SDA inputs that will be rejected. Units are 5 nanoseconds.
83	0x53	EDID_CFG1	7:2				Reserved.
			1:0	RW	0x00	EDID_SDA_DLY	SDA Output Delay: This field configures output delay on the DDC_SDA output when the EDID memory is accessed. Setting this value will increase output delay in units of 40ns. Nominal output delay values for DDC_SCL to DDC_SDA are: 00 : 240ns. 01 : 280ns. 10 : 320ns. 11 : 360ns.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
84	0x54	BRIDGE_CFG	7	RW	Strap	EXT_CTL	External Control: When this bit Is set, the internal bridge control function is disabled. This disables initialization of the HDMI Receiver as well as initiation of HDCP functions. These operations must be controlled by an external controller attached to the I2C interface. This value is loaded from the MODE_SEL1 pin at power-up.
			6	RW	0x00	HDMI_INT_EN	HDMI Interrupt Enable: When this bit is set, Interrupts from the HDMI Receive controller will be reported on the INTB pin. Software may check the BRIDGE_STS register to determine if the interrupt is from the HDMI Receiver or the HDCP Transmitter.
			5	RW	Strap	DIS_REM_EDID	Disable Remote EDID load: Disables automatic load of EDID SRAM from a remote EDID EEPROM. By default, the device will check the remote I2C bus for an EEPROM with a valid EDID, and load the EDID data to local EDID SRAM. If this bit is set to a 1, the remote EDID load will be bypassed. This value is loaded from the MODE_SEL1 pin at power-up.
			4	RW	0x00	AUTO_INIT_DIS	Disable Automatic initialization: The Bridge control will automatically initialize the HDMI Receiver for operation. Setting this bit to a 1 will disable automatic initialization of the HDMI Receiver. In this mode, initialization of the HDMI Receiver must be done through EEPROM configuration or via external control.
			3	RW	0x00	AUTO_HDCP_DIS	Disable Automatic HDCP_CTRL setting: By default the internal bridge control function will configure the HDMI Receiver for HDCP operation using default settings for bits in the HDCP_CTRL register. Setting this bit to a 1 will disable automatic control of the HDCP_CTRL register in the HDMI Receiver.
			2	RW	0x00	AUDIO_TDM	Enable TDM Audio: Setting this bit to a 1 will enable TDM audio for the HDMI audio.
			1	RW		AUDIO_MODE	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0 : HDMI audio. 1 : Local/DVI audio. Local audio is sourced from the device I2S pins rather than from HDMI, and is useful in modes such as DVI that do not include audio.
			0	RW	Strap	AUX_AUDIO_EN	AUX Audio Channel Enable: Setting this bit to a 1 will enable the AUX audio channel. This allows sending additional 2-channel audio in addition to the HDMI or DVI audio. This bit is loaded from the MODE_SEL0 pin at power-up.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
85	0x55	AUDIO_CFG	7	RW	0x00	TDM_2_PARALLEL	Enable I2S TDM to parallel audio conversion: When this bit is set, the i2s tdm to parallel conversion module is enabled. The clock output from the i2s tdm to parallel conversion module is them used to send data to the deserializer.
			6	RW		HDMI_I2S_OUT	HDMI Audio Output Enable: When this bit is set, the HDMI I2S audio data will be output on the I2S audio interface pins. This control is ignored if the BRIDGE_CFG:AUDIO_MODE is not set to 00 (HDMI audio only).
			5:4				Reserved.
			3	RW	0x0C	RST_ON_TYPE	Reset Audio FIFO on Type Change: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio type.
			2	RW		RST_ON_AIF	Reset Audio FIFO on Audio Infoframe: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio Infoframe checksum.
			1	RW		RST_ON_AVI	Reset Audio FIFO on Audio Video Information Infoframe: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio Video Information Infoframe checksum.
			0	RW		RST_ON_ACR	Reset Audio FIFO on Audio Control Frame: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio Control Frame N or CTS fields.
90	0x5A	FPD3_STS	7	R	0x00	FPD3_LINK_RDY	This bit indicates that the FPD-Link III has detected a valid downstream connection and determined capabilities for the downstream link.
			6	R		FPD3_TX_STS	FPD-Link III transmit status: This bit indicates that the FPD-Link III transmitter is active and the receiver is LOCKED to the transmit clock. It is only asserted once a valid input has been detected, and the FPD-Link III transmit connection has entered the correct mode (Single vs. Dual mode).
			5:4	R		FPD3_PORT_STS	FPD3 Port Status: If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 01: Single FPD-Link III Transmit on port 0.
			3	R		TMDS_VALID	HDMI TMDS Valid: This bit indicates the TMDS interface is recovering valid TMDS data from HDMI.
			2	R		HDMI_PLL_LOCK	HDMI PLL lock status: Indicates the HDMI PLL has locked to the incoming TMDS clock.
			1	R		NO_HDMI_CLK	No TMDS Clock Detected: This bit indicates the Frequency Detect circuit did not detect an TMDS clock greater than the value specified in the FREQ_LOW register.
			0	R		FREQ_STABLE	HDMI Frequency is Stable: Indicates the Frequency Detection circuit has detected a stable TMDS clock frequency.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
91	0x5B	FPD3_CTL1	7	RW	Strap	FPD3_COAX_MODE	FPD3 Coax Mode: Enables configuration for the FPD3 Interface cabling type. 0 : Twisted Pair. 1 : Coax This bit is loaded from the MODE_SEL1 pin at power-up.
			6				Reserved.
			5	RW	1	RST_PLL_FREQ	Reset FPD3 PLL on Frequency Change: When set to a 1, frequency changes detected by the Frequency Detect circuit will result in a reset of the FPD3 PLL. Set to 0.
			4	RW	0	FREQ_DET_PLL	Frequency Detect Select PLL Clock: Determines the clock source for the Frequency detection circuit: 0 : TMDS clock (prior to PLL). 1: HDMI PLL clock.
			3				Reserved.
			2				Reserved.
			1				Reserved.
			0				Reserved.
92	0x5C	FPD3_CTL2	7				Reserved.
			6	RW	0x00	FORCE_LINK_RDY	Force Link Ready: Forces link ready indication, bypassing back channel link detection.
			5	RW		FORCE_CLK_DET	Force Clock Detect: Forces the HDMI/OpenLDI clock detect circuit to indicate presence of a valid input clock. This bypasses the clock detect circuit, allowing operation with an input clock that does not meet frequency or stability requirements.
			4:3	RW		FREQ_STBL_THR	Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40us. 01 : 80us. 10 : 320us. 11 : 1.28ms.
			2:0	RW	0x02	FREQ_HYST	Frequency Detect Hysteresis: The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz.
93	0x5D	FREQ_LOW	7				Reserved.
			6	RW	0	HDMI_RST_MODE	HDMI Phy Reset Mode: 0 : Reset HDMI Phy on change in mode or frequency. 1 : Don't reset HDMI Phy on change in mode or frequency if +5 V is asserted.
			5:0	RW	6	FREQ_LO_THR	Frequency Low Threshold: Sets the low threshold for the TMDS Clock frequency detect circuit in MHz. This value is used to determine if the TMDS clock frequency is too low for proper operation.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
95	0x5F	HDMI Frequency	7:0	R	0x00	HDMI_FREQ	HDMI frequency: Returns the value of the HDMI frequency in MHz. A value of 0 indicates the HDMI receiver is not detecting a valid signal.
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted. 0000: Checkerboard. 0001: White/Black (default). 0010: Black/White. 0011: Red/Cyan. 0100: Green/Magenta. 0101: Blue/Yellow. 0110: Horizontal Black-White/White-Black. 0111: Horizontal Black-Red/White-Cyan. 1000: Horizontal Black-Green/White-Magenta. 1001: Horizontal Black-Blue/White-Yellow. 1010: Vertical Black-White/White-Black. 1011: Vertical Black-Red/White-Cyan. 1100: Vertical Black-Green/White-Magenta. 1101: Vertical Black-Blue/White-Yellow. 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers. 1111: VCOM. See TI App Note AN-2198.
			3				***Reserved.***
			2	RW		Color Bars Pattern	Enable color bars: 0: Color Bars disabled (default). 1: Color Bars enabled. Overrides the selection from reg_0x64[7:4].
			1	RW		VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern: 0: Color sequence from top left is (YCBR) (default). 1: Color sequence from top left is (RBCY).
			0	RW		Pattern Generator Enable	Pattern Generator enable: 0: Disable Pattern Generator (default). 1: Enable Pattern Generator.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
101	0x65	Pattern Generator Configuration	7		0x00		***Reserved.***
			6	RW		Checkerboard Scale	Scale Checkered Patterns: 0: Normal operation (each square is 1x1 pixel) (default). 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels). Setting this bit gives better visibility of the checkered patterns.
			5	RW		Custom Checkerboard	Use Custom Checkerboard Color: 0: Use white and black in the Checkerboard pattern (default). 1: Use the Custom Color and black in the Checkerboard pattern.
			4	RW		PG 18–bit Mode	18-bit Mode Select: 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness (default). 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.
			3	RW		External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default). 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Timing Select	Timing Select Control: 0: The Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals (default). 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. See *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).
			1	RW		Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output (default). 1: Invert the color output. See *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).
			0	RW		Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern (default). 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).
102	0x66	PGIA	7:0	RW	0x00	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
103	0x67	PGID	7:0	RW	0x00	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).
112	0x70	Slave ID[1]	7:1	RW	0x00	Slave ID 1	7-bit I2C address of the remote Slave 1 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 1.
			0				***Reserved.***
113	0x71	Slave ID[2]	7:1	RW	0x00	Slave ID 2	7-bit I2C address of the remote Slave 2 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 2.
			0				***Reserved.***
114	0x72	Slave ID[3]	7:1	RW	0x00	Slave ID 3	7-bit I2C address of the remote Slave 3 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 3.
			0				***Reserved.***
115	0x73	Slave ID[4]	7:1	RW	0x00	Slave ID 4	7-bit I2C address of the remote Slave 4 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 4.
			0				***Reserved.***
116	0x74	Slave ID[5]	7:1	RW	0x00	Slave ID 5	7-bit I2C address of the remote Slave 5 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 5.
			0				***Reserved.***
117	0x75	Slave ID[6]	7:1	RW	0x00	Slave ID 6	7-bit I2C address of the remote Slave 6 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 6.
			0				***Reserved.***
118	0x76	Slave ID[7]	7:1	RW	0x00	Slave ID 7	7-bit I2C address of the remote Slave 7 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 7.
			0				***Reserved.***

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
119	0x77	Slave Alias[1]	7:1	RW	0x00	Slave Alias ID 1	7-bit Slave Alias ID of the remote Slave 1 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 1 register. A value of 0 in this field disables access to the remote Slave 1.
			0				***Reserved.***
120	0x78	Slave Alias[2]	7:1	RW	0x00	Slave Alias ID 2	7-bit Slave Alias ID of the remote Slave 2 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 2 register. A value of 0 in this field disables access to the remote Slave 2.
			0				***Reserved.***
121	0x79	Slave Alias[3]	7:1	RW	0x00	Slave Alias ID 3	7-bit Slave Alias ID of the remote Slave 3 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 3 register. A value of 0 in this field disables access to the remote Slave 3.
			0				***Reserved.***
122	0x7A	Slave Alias[4]	7:1	RW	0x00	Slave Alias ID 4	7-bit Slave Alias ID of the remote Slave 4 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 4 register. A value of 0 in this field disables access to the remote Slave 4.
			0				***Reserved.***
123	0x7B	Slave Alias[5]	7:1	RW	0x00	Slave Alias ID 5	7-bit Slave Alias ID of the remote Slave 5 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 5 register. A value of 0 in this field disables access to the remote Slave 5.
			0				***Reserved.***
124	0x7C	Slave Alias[6]	7:1	RW	0x00	Slave Alias ID 6	7-bit Slave Alias ID of the remote Slave 6 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 6 register. A value of 0 in this field disables access to the remote Slave 6.
			0				***Reserved.***
125	0x7D	Slave Alias[7]	7:1	RW	0x00	Slave Alias ID 7	7-bit Slave Alias ID of the remote Slave 7 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 7 register. A value of 0 in this field disables access to the remote Slave 7.
			0				***Reserved.***
128	0x80	RX_BKSV0	7:0	R	0x00	RX_BKSV0	BKSV0: Value of byte0 of the Receiver KSV.
129	0x81	RX_BKSV1	7:0	R	0x00	RX_BKSV1	BKSV1: Value of byte1 of the Receiver KSV.
130	0x82	RX_BKSV2	7:0	R	0x00	RX_BKSV2	BKSV2: Value of byte2 of the Receiver KSV.
131	0x83	RX_BKSV3	7:0	R	0x00	RX_BKSV3	BKSV3: Value of byte3 of the Receiver KSV.
132	0x84	RX_BKSV4	7:0	R	0x00	RX_BKSV4	BKSV4: Value of byte4 of the Receiver KSV.
144	0x90	TX_KSV0	7:0	R	0x00	TX_KSV0	TX_KSV0: Value of byte0 of the Transmitter KSV.
145	0x91	TX_KSV1	7:0	R	0x00	TX_KSV1	TX_KSV1: Value of byte1 of the Transmitter KSV.
146	0x92	TX_KSV2	7:0	R	0x00	TX_KSV2	TX_KSV2: Value of byte2 of the Transmitter KSV.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
147	0x93	TX_KSV3	7:0	R	0x00	TX_KSV3	TX_KSV3: Value of byte3 of the Transmitter KSV.
148	0x94	TX_KSV4	7:0	R	0x00	TX_KSV4	TX_KSV4: Value of byte4 of the Transmitter KSV.
160	0xA0	RX_BCAPS	7				Reserved.
			6	R	0x01	Repeater	Repeater: Indicates if the attached Receiver supports downstream connections. This bit is valid once the Bksv is ready as indicated by the BKSV_RDY bit in the HDCP.
			5	R		KSV_FIFO_RDY	KSV FIFO Ready: Indicates the receiver has built the list of attached KSVs and computed the verification value V'.
			4	R		FAST_I2C	Fast I2C: The HDCP Receiver supports fast I2C. Since the I2C is embedded in the serial data, this bit is not relevant.
			3:2				Reserved.
			1	R	0x03	FEATURES_1_1	1.1_Features: The HDCP Receiver supports the Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options.
			0	R		FAST_REAUTH	Fast Reauthentication: The HDCP Receiver is capable of receiving (unencrypted) video signal during the session re-authentication.
161	0xA1	RX_BSTATUS0	7	R	0x00	MAX_DEVS_EXCEEDED	Maximum Devices Exceeded: Indicates a topology error was detected. Indicates the number of downstream devices has exceeded the depth of the Repeater's KSV FIFO.
			6:0	R		DEVICE_COUNT	Device Count: Total number of attached downstream device. For a Repeater, this will indicate the number of downstream devices, not including the Repeater. For an HDCP Receiver that is not also a Repeater, this field will be 0.
162	0xA2	RX_BSTATUS1	7:4				Reserved.
			3	R	0x00	MAX_CASC_EXCEEDED	Maximum Cascade Exceeded: Indicates a topology error was detected. Indicates that more than seven levels of repeaters have been cascaded together.
			2:0	R		Cascade Depth	Cascade Depth: Indicates the number of attached levels of devices for the Repeater.
163	0xA3	KSV_FIFO	7:0	R	0x00	KSV_FIFO	KSV FIFO: Each read of the KSV FIFO returns one byte of the KSV FIFO list composed by the downstream Receiver.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
192	0xC0	HDCP_DBG	7				Reserved.
			6	RW	0x00	HDCP_I2C_TO_DIS	HDCP I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the HDCP I2C master. When enabled, the bus timeout function allows the I2C master to assume the bus is free if no signaling occurs for more than 1 second.
			5				Reserved.
			4	RW	0x00	DIS_RI_SYNC	Disable Ri Synchronization check: Ri is normally checked both before and after the start of frame 128. The check at frame 127 ensures synchronization between the two. Setting this bit to a 1 will disable the check at frame 127.
			3	RW		RGB_CHKSUM_EN	Enable RBG video line checksum: Enables sending of ones-complement checksum for each 8-bit RBG data channel following end of each video data line.
			2	RW		FC_TESTMODE	Frame Counter Test mode: Speeds up frame counter used for Pj and Ri verification. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames.
			1	RW		TMR_SPEEDUP	Timer Speedup: Speed up HDCP authentication timers.
			0	RW		HDCP_I2C_FAST	HDCP I2C Fast Mode Enable Setting this bit to a 1 will enable the HDCP I2C Master in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Master will operation with Standard mode timing. This bit is mirrored in the IND_STS register.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
194	0xC2	HDCP_CFG	7	RW	0xA8	ENH_LV	Enable Enhanced Link Verification: Enables enhanced link verification. Allows checking of the encryption Pj value on every 16th frame. 0 = Enhanced Link Verification disabled. 1 = Enhanced Link Verification enabled.
			6	RW		HDCP_EESS	Enable Enhanced Encryption Status Signaling: Enables Enhanced Encryption Status Signaling (EESS) instead of the Original Encryption Status Signaling (OESS). 0 = OESS mode enabled. 1 = EESS mode enabled.
			5	RW		TX_RPTR	Transmit Repeater Enable: Enables the transmitter to act as a repeater. In this mode, the HDCP Transmitter incorporates the additional authentication steps required of an HDCP Repeater. 0 = Transmit Repeater mode disabled. 1 = Transmit Repeater mode enabled.
			4:3	RW		ENC_MODE	Encryption Control Mode: Determines mode for controlling whether encryption is required for video frames. 00 = Enc_Authenticated. 01 = Enc_Reg_Control. 10 = Enc_Always. 11 = Enc_InBand_Control (per frame).
			2	RW		WAIT_100MS	Enable 100MS Wait: The HDCP 1.3 specification allows for a 100Ms wait to allow the HDCP Receiver to compute the initial encryption values. The FPD-Link III implementation guarantees that the Receiver will complete the computations before the HDCP Transmitter. Thus the timer is unnecessary. To enable the 100ms timer, set this bit to a 1.
			1	RW		RX_DET_SEL	RX Detect Select: Controls assertion of the Receiver Detect Interrupt. If set to 0, the Receiver Detect Interrupt will be asserted on detection of an FPD-Link III Receiver. If set to 1, the Receiver Detect Interrupt will also require a receive lock indication from the receiver.
			0	RW		HDCP_AVMUTE	Enable AVMUTE: Setting this bit to a 1 will initiate AVMUTE operation. The transmitter will ignore encryption status controls while in this state. If this bit is set to a 0, normal operation will resume. This bit may only be set if the HDCP_EESS bit is also set.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
195	0xC3	HDCP_CTL	7	RW	0x00	HDCP_RST	HDCP Reset : Setting this bit will reset the HDCP transmitter and dis-able HDCP authentication. This bit is self-clearing.
			6				Reserved.
			5	RW	0x00	KSV_LIST_VALID	KSV List Valid : The controller sets this bit after validating the Repeater's KSV List against the Key revocation list. This allows completion of the Authentication process. This bit is self-clearing.
			4	RW		KSV_VALID	KSV Valid : The controller sets this bit after validating the Receiver's KSV against the Key revocation list. This allows continuation of the Authentication process. This bit will be cleared upon assertion of the KSV_RDY flag in the HDCP_STS register. Setting this bit to a 0 will have no effect.
			3	RW		HDCP_ENC_DIS	HDCP Encrypt Disable : Disables HDCP encryption. Setting this bit to a 1 will cause video data to be sent without encryption. Authentication status will be maintained. This bit is self-clearing.
			2	RW		HDCP_ENC_EN	HDCP Encrypt Enable : Enables HDCP encryption. When set, if the device is authenticated, encrypted data will be sent. If device is not authenticated, a blue screen will be sent. Encryption should always be enabled when video data requiring content protection is being supplied to the transmitter. When this bit is not set, video data will be sent without encryption. Note that when CFG_ENC_MODE is set to Enc_Always, this bit will be read only with a value of 1.
			1	RW		HDCP_DIS	HDCP Disable: Disables HDCP authentication. Setting this bit to a 1 will disable the HDCP authentication. This bit is self-clearing.
			0	RW		HDCP_EN	HDCP Enable/Restart: Enables HDCP authentication. If HDCP is already enabled, setting this bit to a 1 will restart authentication. Setting this bit to a 0 will have no effect. A register read will return the current HDCP enabled status.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
196	0xC4	HDCP_STS	7	R	0x00	I2C_ERR_DET	HDCP I2C Error Detected: This bit indicates an error was detected on the embedded communications channel with the HDCP Receiver. Setting of this bit might indicate that a problem exists on the link between the HDCP Transmitter and HDCP Receiver. This bit will be cleared on read.
			6	R		RX_INT	RX Interrupt : Status of the RX Interrupt signal. The signal is received from the attached HDCP Receiver and is the status on the INTB_IN pin of the HDCP Receiver. The signal is active low, so a 0 indicates an interrupt condition.
			5	R		RX_LOCK_DET	Receiver Lock Detect : This bit indicates that the downstream Receiver has indicated Receive Lock to incoming serial data.
			4	R		DOWN_HPD	Downstream Hot Plug Detect: This bit indicates a downstream repeater has reported a Hot Plug event, indicating addition of a new receiver. This bit will be cleared on read.
			3	R		RX_DETECT	Receiver Detect : This bit indicates that a downstream Receiver has been detected.
			2	R		KSV_LIST_RDY	HDCP Repeater KSV List Ready : This bit indicates that the Receiver KSV list has been read and is available in the KSV_FIFO registers. The device will wait for the controller to set the KSV_LIST_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_LIST_VALID bit.
			1	R		KSV_RDY	HDCP Receiver KSV Ready : This bit indicates that the Receiver KSV has been read and is available in the HDCP_BKSV registers. If the de-vice is not a Repeater, it will wait for the controller to set the KSV_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_VALID bit.
			0	R		AUTHED	HDCP Authenticated: Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication.
198	0xC6	ICR	7	RW	0x00	IE_IND_ACC	Interrupt on Indirect Access Complete: Enables interrupt on completion of Indirect Register Access.
			6	RW		IE_RXDET_INT	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If HDCP_CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	RW		IE_RX_INT	Interrupt on Receiver interrupt: Enables interrupt on indication from the HDCP Receiver. Allows propagation of interrupts from downstream devices.
			4	RW		IE_LIST_RDY	Interrupt on KSV List Ready: Enables interrupt on KSV List Ready.
			3	RW		IE_KSV_RDY	Interrupt on KSV Ready: Enables interrupt on KSV Ready.
			2	RW		IE_AUTH_FAIL	Interrupt on Authentication Failure: Enables interrupt on authentication failure or loss of authentication.
			1	RW		IE_AUTH_PASS	Interrupt on Authentication Pass: Enables interrupt on successful completion of authentication.
			0	RW		INT_EN	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
199	0xC7	ISR	7	R	0x00	IS_IND_ACC	Interrupt on Indirect Access Complete: Indirect Register Access has completed.
			6	R		IS_RXDET_INT	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If HDCP_CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	R		IS_RX_INT	Interrupt on Receiver interrupt: Receiver has indicated an interrupt request from down-stream device.
			4	R		IS_LIST_RDY	Interrupt on KSV List Ready: The KSV list is ready for reading by the controller.
			3	R		IS_KSV_RDY	Interrupt on KSV Ready: The Receiver KSV is ready for reading by the controller.
			2	R		IS_AUTH_FAIL	Interrupt on Authentication Failure: Authentication failure or loss of authentication has occurred.
			1	R		IS_AUTH_PASS	Interrupt on Authentication Pass: Authentication has completed successfully.
			0	R		INT	Global Interrupt: Set if any enabled interrupt is indicated.
200	0xC8	NVM_CTL	7	R	0x00	NVM_PASS	NVM Verify pass: This bit indicates the completion status of the NVM verification process. This bit is valid only when NVM_DONE is asserted. 0: NVM Verify failed. 1: NVM Verify passed.
			6	R		NVM_DONE	NVM Verify done: This bit indicates that the NVM Verification has completed.
			5	RW		NVM_PARALLEL	NVM Parallel Load Enable: Setting this bit enables external parallel data to be written to NVM SRAM. Byte data and a memory clock are brought in on the R[7:0] and G[0] pins respectively. In this mode of operation NVM_DATA[0] acts as a memory enable to enable writes to the NVM SRAM.
			4:3				Reserved.
			2	RW	0x00	NVM_VFY	NVM Verify: Setting this bit will enable a verification of the NVM contents. This is done by reading all NVM keys, computing a SHA-1 hash value, and verifying against the SHA-1 hash stored in NVM. This bit will be cleared upon completion of the NVM Verification.
			1	RW		NVM_PROG	NVM Program: Setting this bit to a 1 allows programming of the NVM memory from the NVM SRAM.
			0	RW		NVM_PROG_EN	NVM Program Enable: Set to a 1 to allow erase or programming of NVM.
206	0xCE	BLUE_SCREEN	7:0	RW	0xFF	BLUE_SCREEN_VAL	Blue Screen Data Value: Provides the 8-bit data value sent on the Blue channel when the HDCP Transmitter is sending a blue screen.
224	0xE0	HDCP_DBG_ALIAS	7:0	R		HDCP_DBG	Read-only alias of HDCP_DBG register.
226	0xE2	HDCP_CFG_ALIAS	7:0	R		HDCP_CFG	Read-only alias of HDCP_CFG register.
227	0xE3	HDCP_CTL_ALIAS	7:0	R		HDCP_CTL	Read-only alias of HDCP_CTL register.

Register Maps (continued)

Table 8. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
228	0xE4	HDCP_STS_ALIAS	7:0	R		HDCP_STS	Read-only alias of HDCP_STS register.
230	0xE6	HDCP_ICR_ALIAS	7:0	R		HDCP_ICR	Read-only alias of HDCP_ICR register.
231	0xE7	HDCP_ISR_ALIAS	7:0	R		HDCP_ISR	Read-only alias of HDCP_ISR register.
240	0xF0	TX ID	7:0	R	0x5F	ID0	First byte ID code: "_".
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code: "U".
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code: "H".
243	0xF3		7:0	R	0x39	ID3	Fourth byte of ID code: "9".
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: "2".
245	0xF5		7:0	R	0x39	ID5	Sixth byte of ID code: “9”.

NOTE

Registers 0x40, 0x41, and 0x42 of the Serial Control Bus Registers are used to access the Page 0x10 and 0x14 registers.

Table 9. Page 0x10 Register

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
73	0x49	OLDI_PLL_STATE_MC_CNTL	7:5		0x00		Reserved
			4	RW		OLDI_STATE_MC_RESET	Enable HDMI PLL reset state 0: Disable state machine reset (normal operation). 1: Enable state machine reset.
			3:0				Reserved, when writing to this register always write '0000b to these bits.

Table 10. Page 0x14 Register

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
73	0x49	FPD_PLL_STATE_MC_CNTL	7:5		0x00		Reserved
			4	RW		FPD_STATE_MC_RESET	Enable FPD PLL reset state 0: Disable state machine reset (normal operation). 1: Enable state machine reset.
			3:0				Reserved, when writing to this register always write '0000b to these bits.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Applications Information

The DS90UH929-Q1, in conjunction with the DS90UH926Q-Q1/DS90UH928Q-Q1deserializer, is intended to interface between a host (graphics processor) and a display, supporting 24-bit color depth (RGB888) and high definition (720p) digital video format. It can receive an 8-bit RGB stream with a pixel clock rate up to 96 MHz together with four I2S audio streams when paired with the DS90UH940-Q1/DS90UH948-Q1 deserializer.

8.2 Typical Applications

Bypass capacitors should be placed near the power supply pins. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable. See and for typical STP and coax connection diagrams.

Typical Applications (continued)

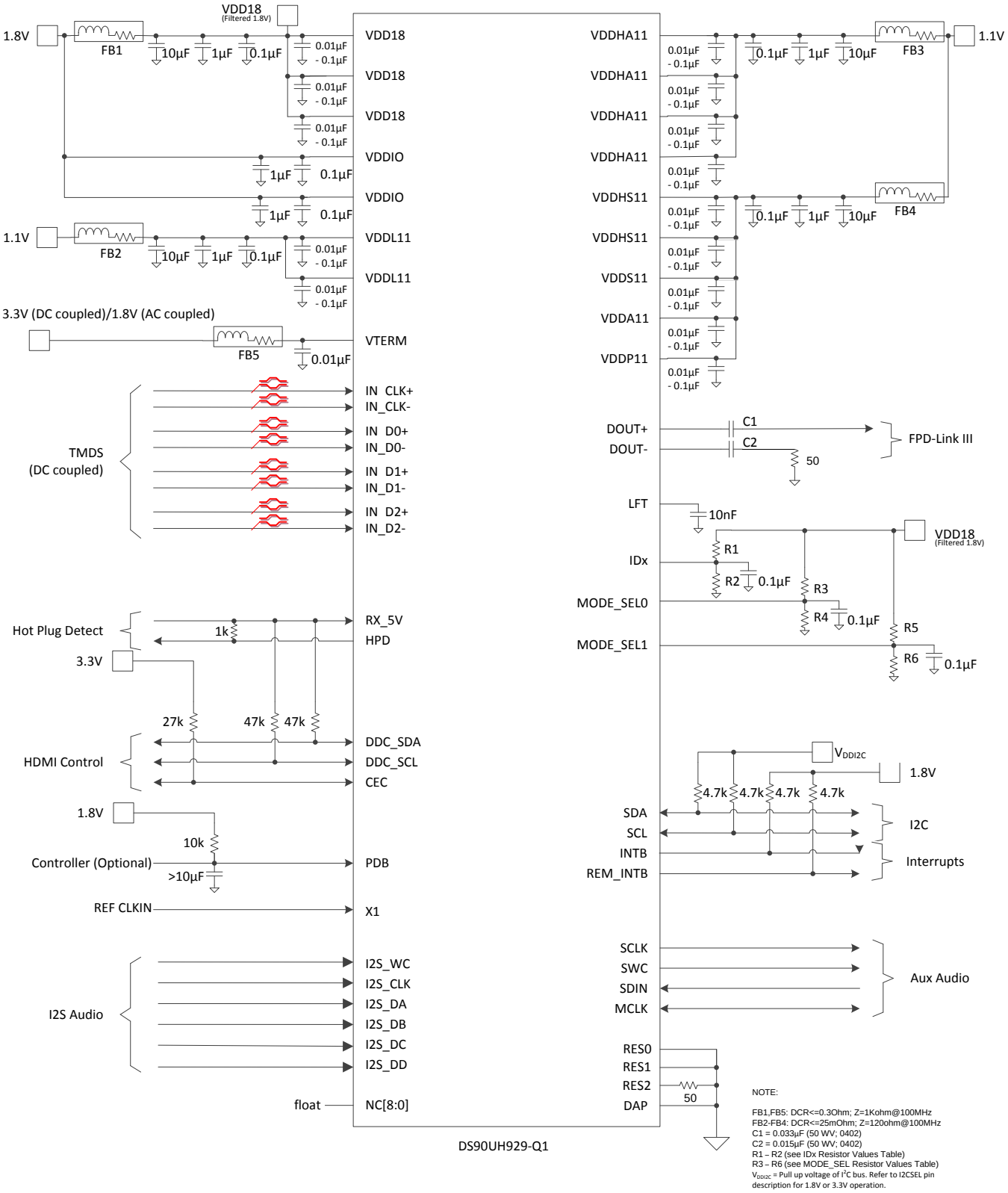


Figure 21. Typical Application Connection -- Coax

Typical Applications (continued)

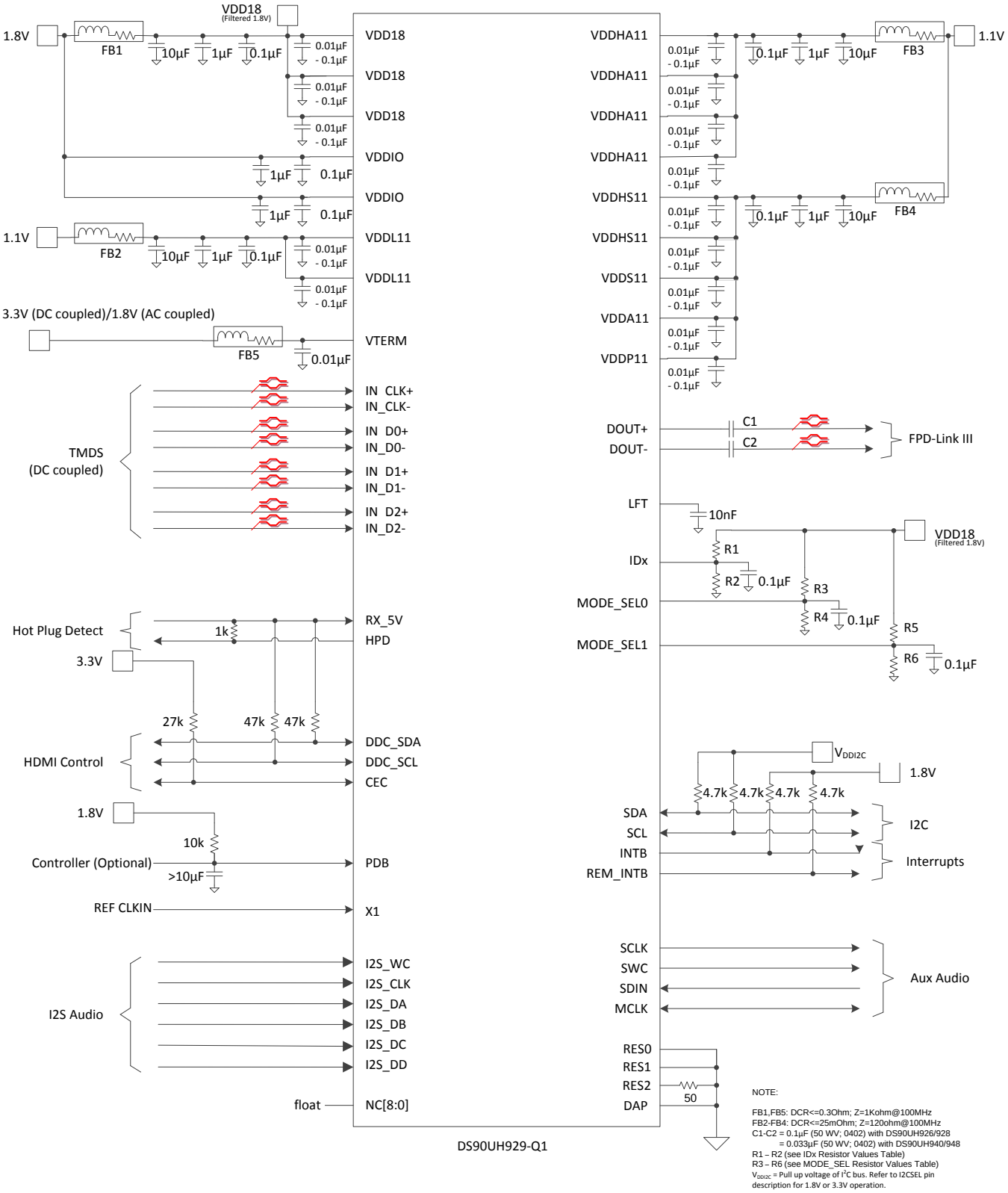
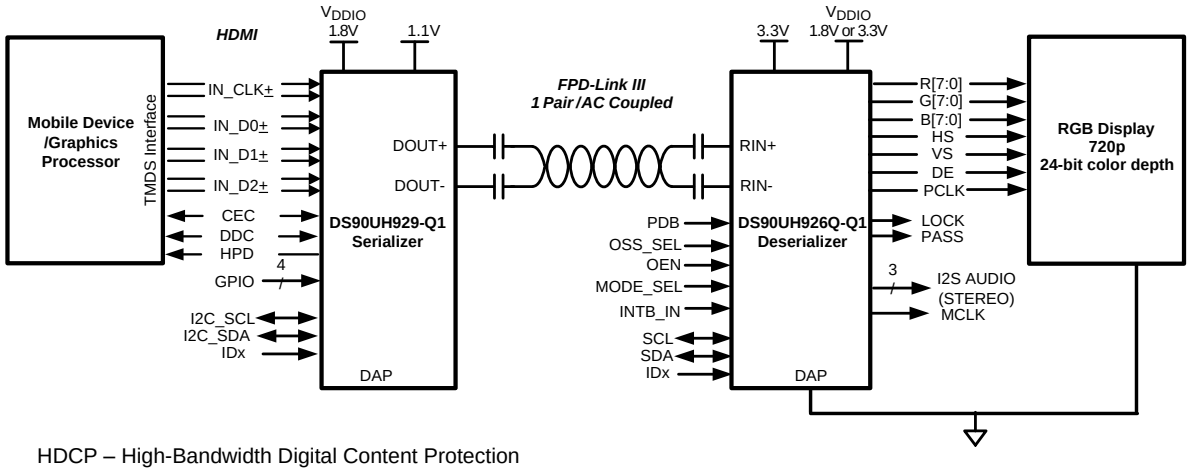


Figure 22. Typical Application Connection -- STP

Typical Applications (continued)



HDCP – High-Bandwidth Digital Content Protection
TMDS – Transition-Minimized Differential Signaling
HDMI – High Definition Multimedia Interface

Figure 23. Typical System Diagram

8.2.1 Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 24.

Table 11. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V
AC-Coupling Capacitor for DOUT0± and DOUT1± with 92x deserializers	100 nF
AC-Coupling Capacitor for DOUT0± and DOUT1± with 94x deserializers	33 nF

For applications using single-ended 50-Ω coaxial cable, the unused data pins (DOUT-) should use a 15-nF capacitor and should be terminated with a 50-Ω resistor.

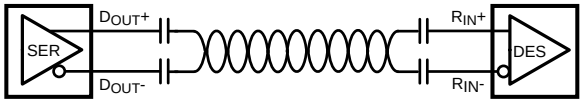


Figure 24. AC-Coupled Connection (STP)

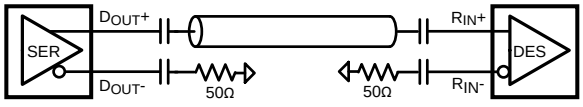


Figure 25. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC-coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

8.2.2 Detailed Design Procedure

8.2.2.1 High-Speed Interconnect Guidelines

See *LVDS SerDes Gen I PCB and Interconnect Design-In Guidelines* (SNLA008) and *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: *LVDS Owner's Manual* (SNLA187).

8.2.3 Application Curves

8.2.3.1 Application Performance Plots

Figure 26 corresponds to 720p60 video application with single lane FPD-Link III output. Figure 27 corresponds to 3.36-Gbps single-lane output from 96-MHz input TMDS clock.

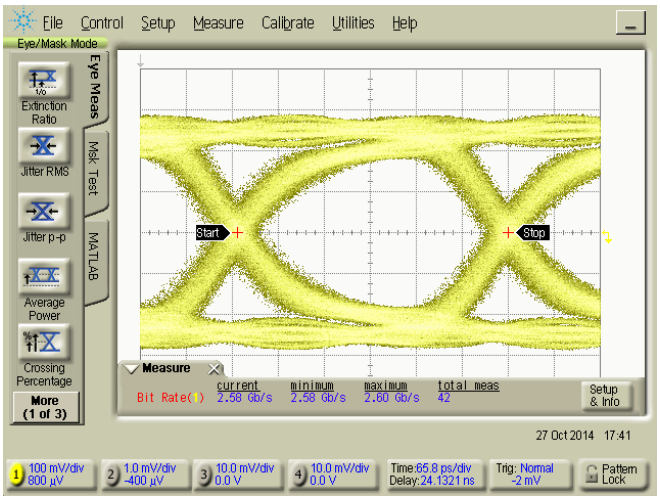


Figure 26. 720p60 Video at 2.6-Gbps Serial Line Rate, Single Lane FPD-Link III output

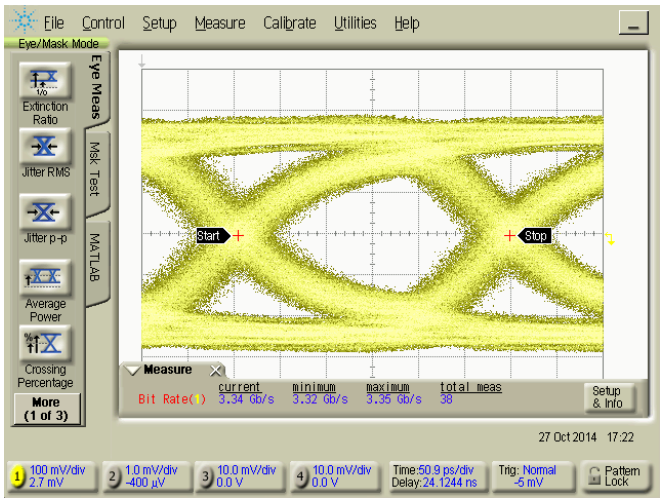


Figure 27. Serializer Output at 3.36-Gbps (96-MHz TMDS Clock)

9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The Pin Functions table in the *Pin Configuration and Functions* section provides guidance on which circuit blocks are connected to which power pins. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 Power-Up Requirements and PDB Pin

The power supply ramp should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin may be used to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V_{DDIO}, a 10-kΩ pullup and a >10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until all power supplies have reached steady state.

The recommended power up sequence is as follows:

- V_{DD18}
- V_{TERM}
- V_{DD11}
- Wait until all supplies have settled
- Activate PDB
- Apply HDMI input

There will be no functional impact to using a different sequence than shown below, but the current draw on V_{TERM} during power up may be higher in other cases.

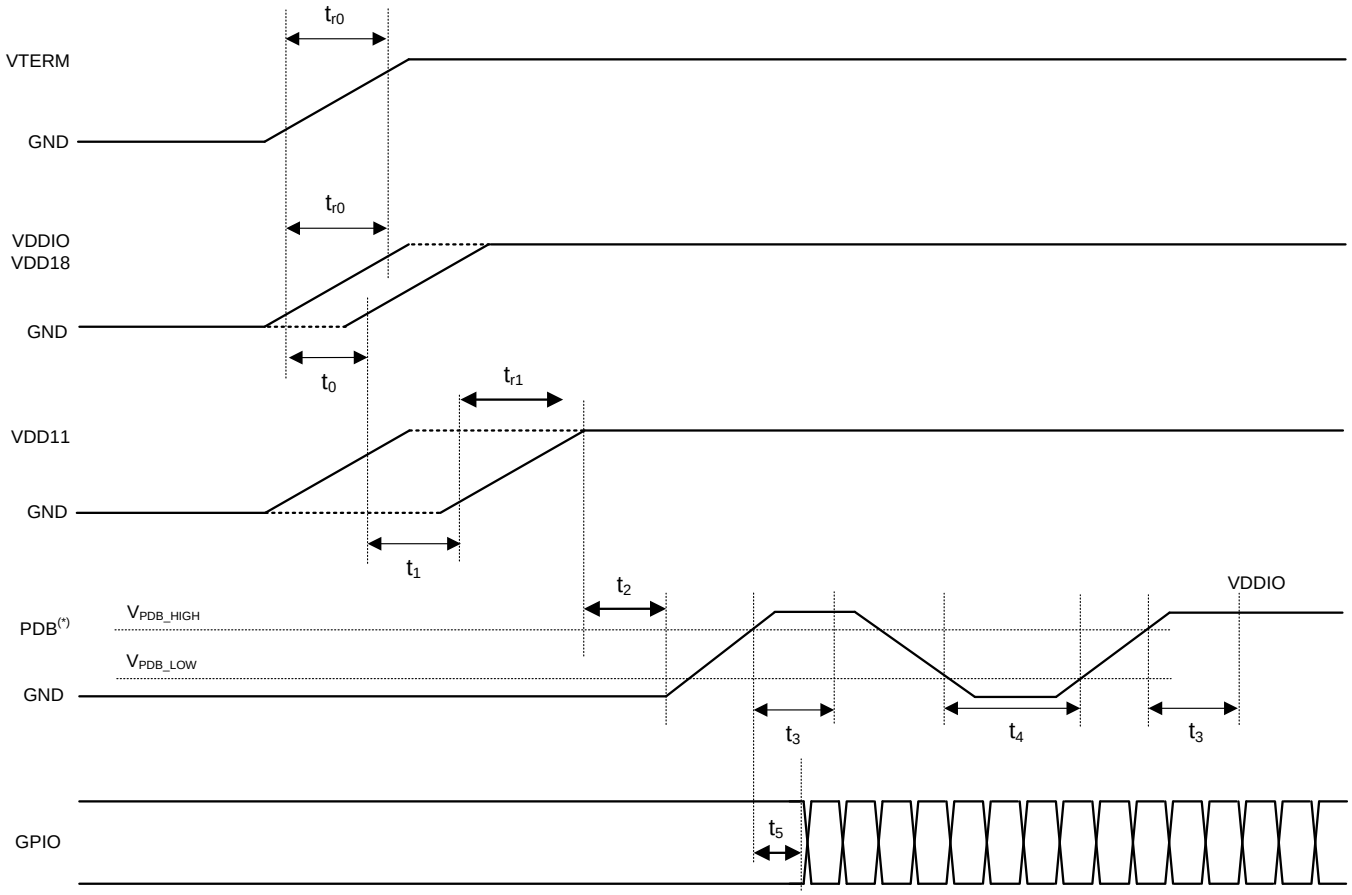
The initialization sequence A shown in Figure 29 consists of any user-defined device configurations and the following:

1. Set Register 0x5B bit 5 to 0. This disables the FPD3 PLL from resetting when a frequency change is detected.
2. Set Register 0x16 to 0x02. This minimizes the duration of inadvertent I2C events.
3. Set Register 0x04 bit 4 to 1. This prevents video from being sent during the blanking interval.

The initialization sequence B shown in Figure 29 should be performed after the TMDS clock has stabilized. Sequence B consists of the following:

1. Reset the HDMI PLL by writing the following registers:
   - Register 0x40 = 0x10
   - Register 0x41 = 0x49
   - Register 0x42 = 0x10
   - Register 0x42 = 0x00
2. Reset the FPD PLL by writing the following registers:
   - Register 0x40 = 0x14
   - Register 0x41 = 0x49
   - Register 0x42 = 0x10
   - Register 0x42 = 0x00

Power-Up Requirements and PDB Pin (continued)



(*) TI recommends that the designer assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

Figure 28. Recommended Power Sequencing

Power-Up Requirements and PDB Pin (continued)

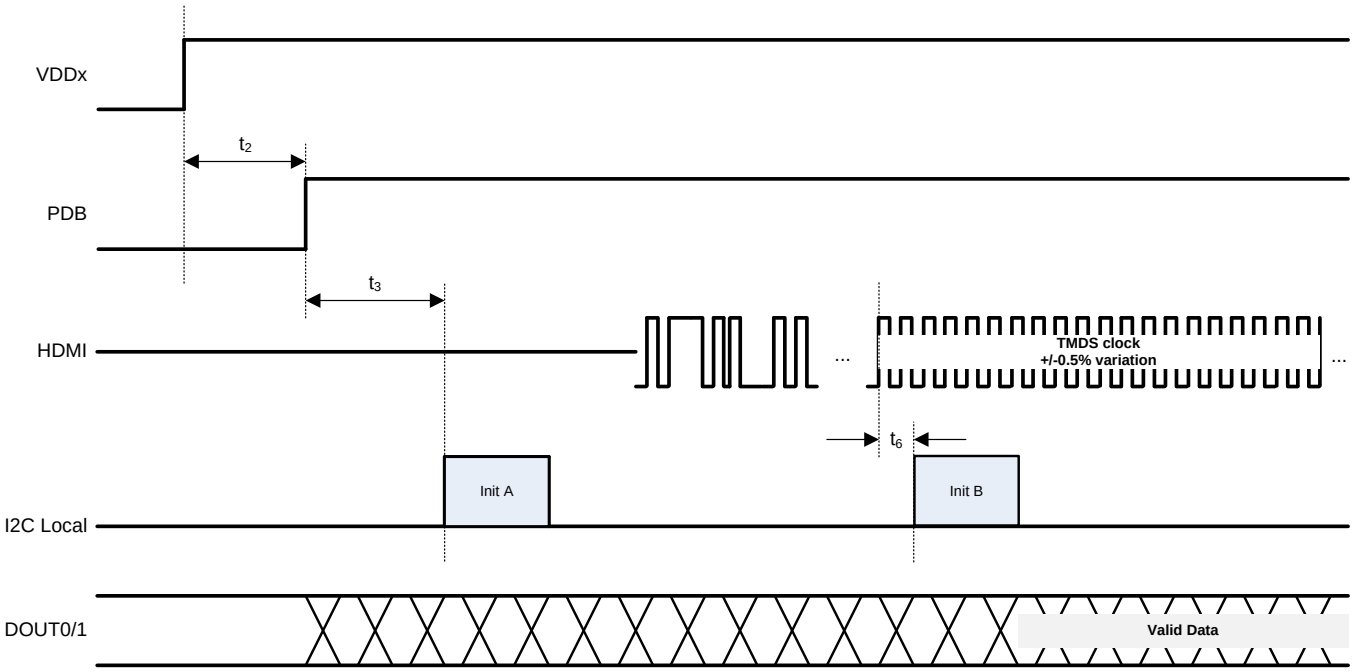


Figure 29. Initialization Sequencing

Table 12. Power-Up Sequencing Constraints

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD18, VDDIO	VDD18 / VDDIO voltage range		1.71		1.89	V
VTERM	VTERM voltage range	DC-coupled HDMI termination	3.135		3.465	V
		AC-coupled HDMI termination	1.71		1.89	V
VDD11	VDD11 voltage range		1.045		1.155	V
V_{PDB_LOW}	PDB LOW threshold Note: V_{PDB} should not exceed limit for respective I/O voltage before 90% voltage of VDD12	VDDIO = 1.8V ± 5%	0.35 * VDDIO			V
V_{PDB_HIGH}	PDB HIGH threshold	VDDIO = 1.8V ± 5%			0.65 * VDDIO	V
t_{r0}	VTERM / VDDIO / VDD18 rise time	These time constants are specified for rise time of power supply voltage ramp (10% -90%).			1.5	ms
t_{r1}	VDD11 rise time	These time constants are specified for rise time of power supply voltage ramp (10% -90%).			1.5	ms
t_0	VDDIO / VDD18 delay time	VTERM needs to ramp-up before VDD18 and VDDIO.	0			ms
t_1	VDD11 delay time	VDDIO and VDD18 need to ramp-up before VDD11.	0			ms
t_2	PDB delay time	PDB should be released after all supplies are stable.	0			ms
t_3	I2C ready time	Starting from PDB high, the local I2C access is available after this time.	2			ms
t_4	Hard reset time	PDB negative pulse width required for the device reset.	2			ms

Power-Up Requirements and PDB Pin (continued)

Table 12. Power-Up Sequencing Constraints (continued)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_5	PDB to HDMI delay time	Keep GPIOs low or high until after PDB release.	0			ms
t_6	TMDS Clock Stable to PLL Reset (Init B)	TMDS Clock must be within 0.5% of the target frequency and stable.	1			µs

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement uses the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01-µF to 10-µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50-µF to 100-µF range and will smooth low frequency switching noise. TI recommends to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. For DS90UH929-Q1, only one common ground plane is required to connect all device related ground pins.

Use at least a four-layer board with a power and ground plane. Place LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the LLP style package, including PCB design and manufacturing requirements, is provided in TI Application Note: AN-1187 (SNOA401).

10.2 Layout Example

Figure 30 is derived from a layout design of the DS90UH929-Q1. This graphic is used to demonstrate proper high-speed routing when designing in the Serializer.

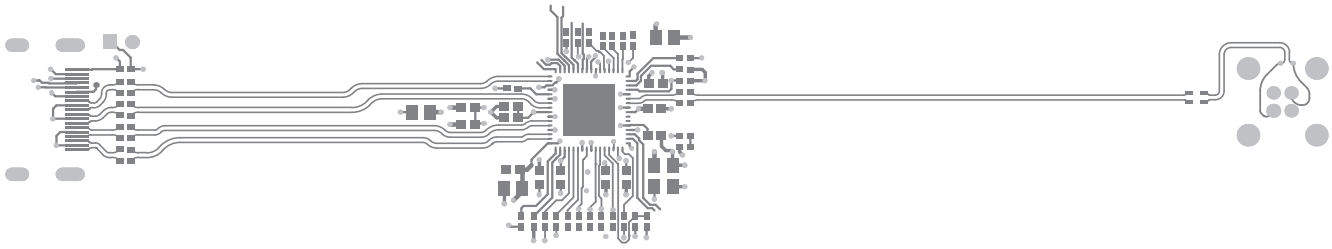


Figure 30. DS90UH929-Q1 Serializer Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Absolute Maximum Ratings For Soldering* (SNOA549)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008)
- *Transmission Line RAPIDESIGNER Operation and Application Guide* (SNLA035)
- *Leadless Leadframe Package (LLP) Application Report* (SNOA401)
- *LVDS Owner's Manual* (SNLA187)
- *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131)
- *Using The I2s Audio Interface of DS90Ux92x FPD-Link III Devices* (SNLA221)
- *Exploring The Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Trademarks

TRI-STATE is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UH929TRGCRQ1	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	(UH929EQ, UH929Q)	Samples
DS90UH929TRGCTQ1	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	(UH929EQ, UH929Q)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

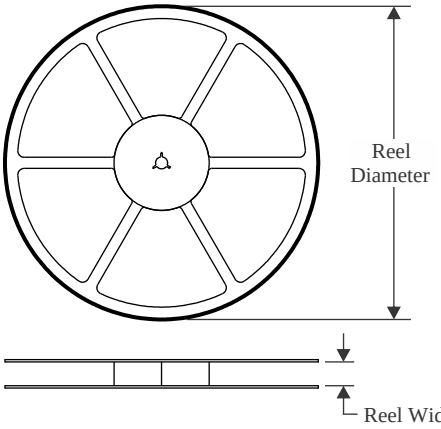
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

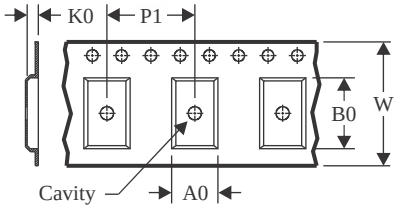
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

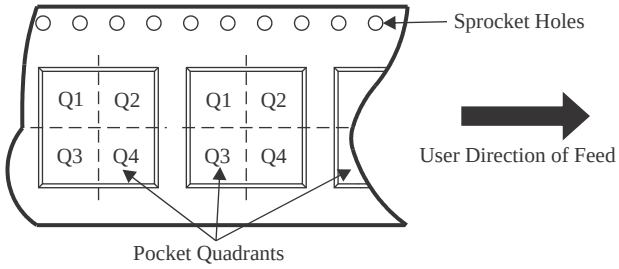


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

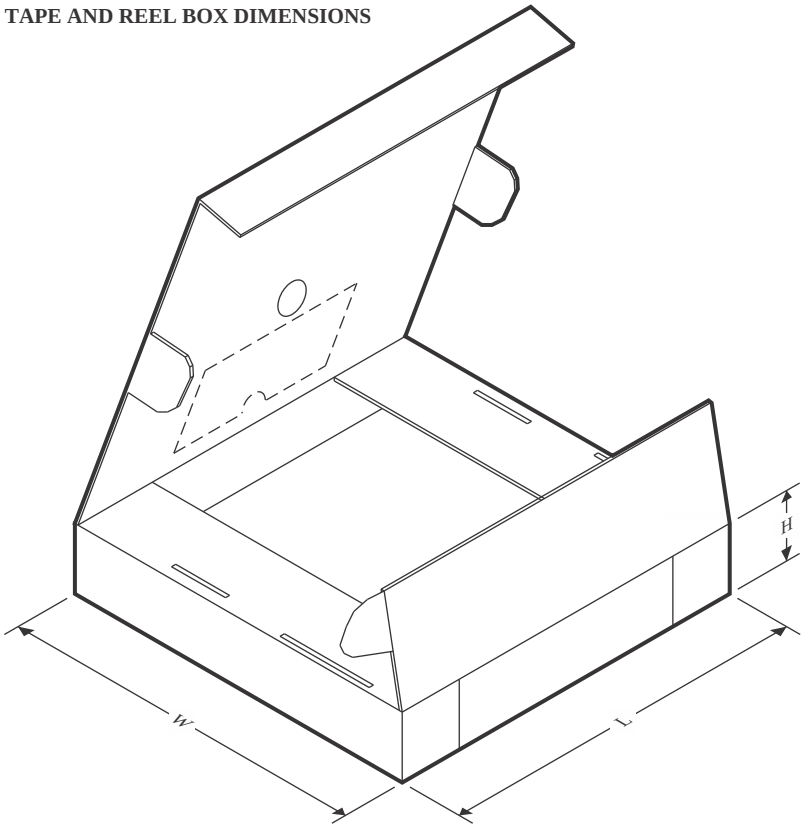
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH929TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90UH929TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90UH929TRGCTQ1	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90UH929TRGCTQ1	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH929TRGCRQ1	VQFN	RGC	64	2000	367.0	367.0	38.0
DS90UH929TRGCRQ1	VQFN	RGC	64	2000	367.0	367.0	35.0
DS90UH929TRGCTQ1	VQFN	RGC	64	250	210.0	185.0	35.0
DS90UH929TRGCTQ1	VQFN	RGC	64	250	210.0	185.0	35.0

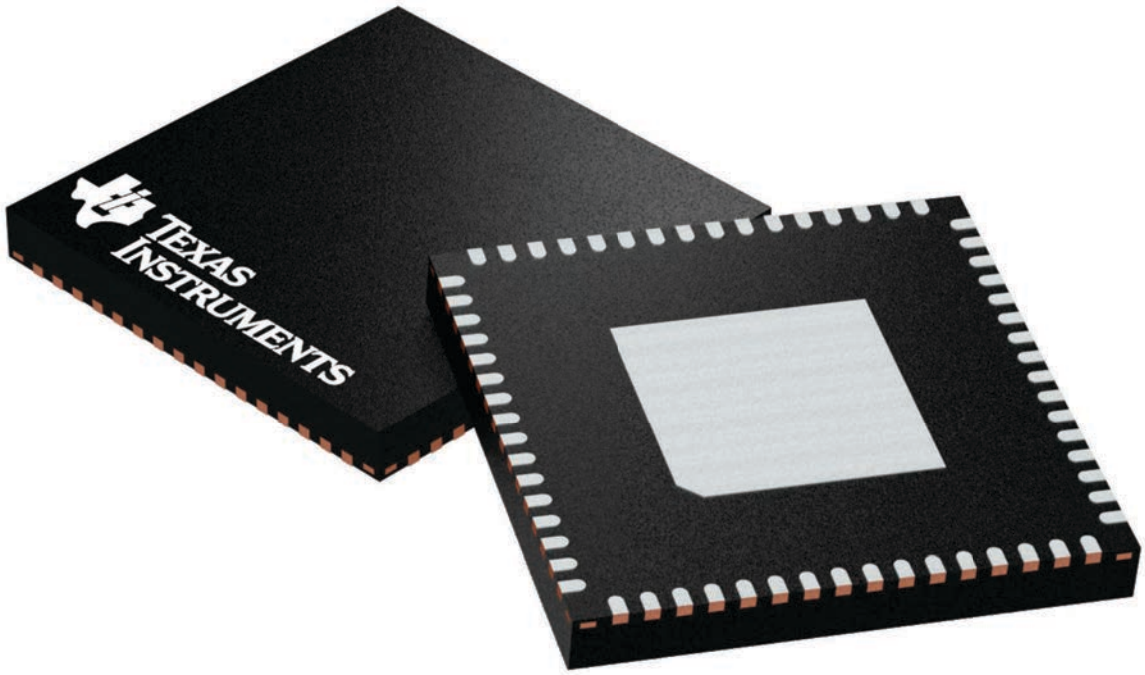
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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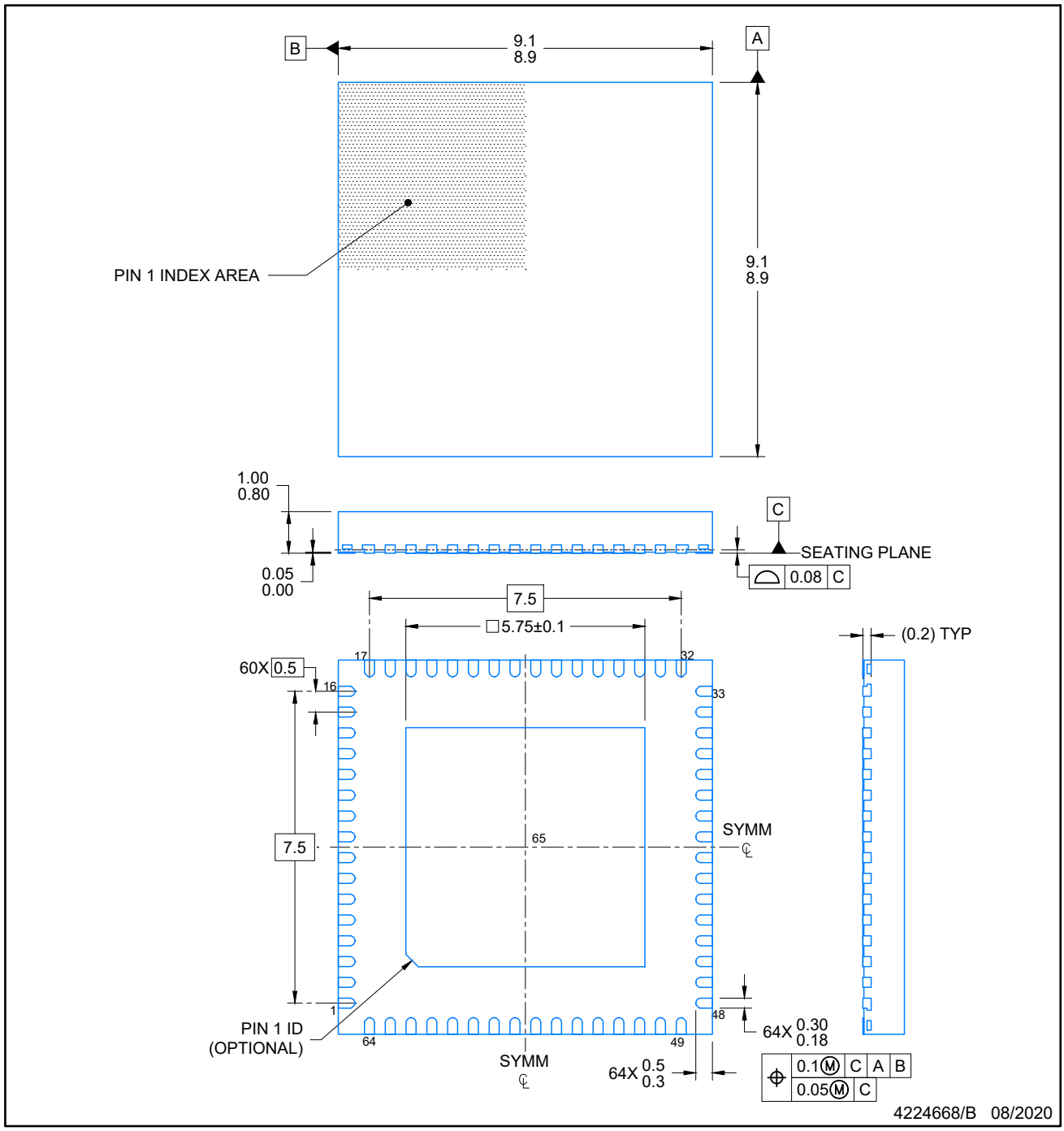
PACKAGE OUTLINE

RGC0064K

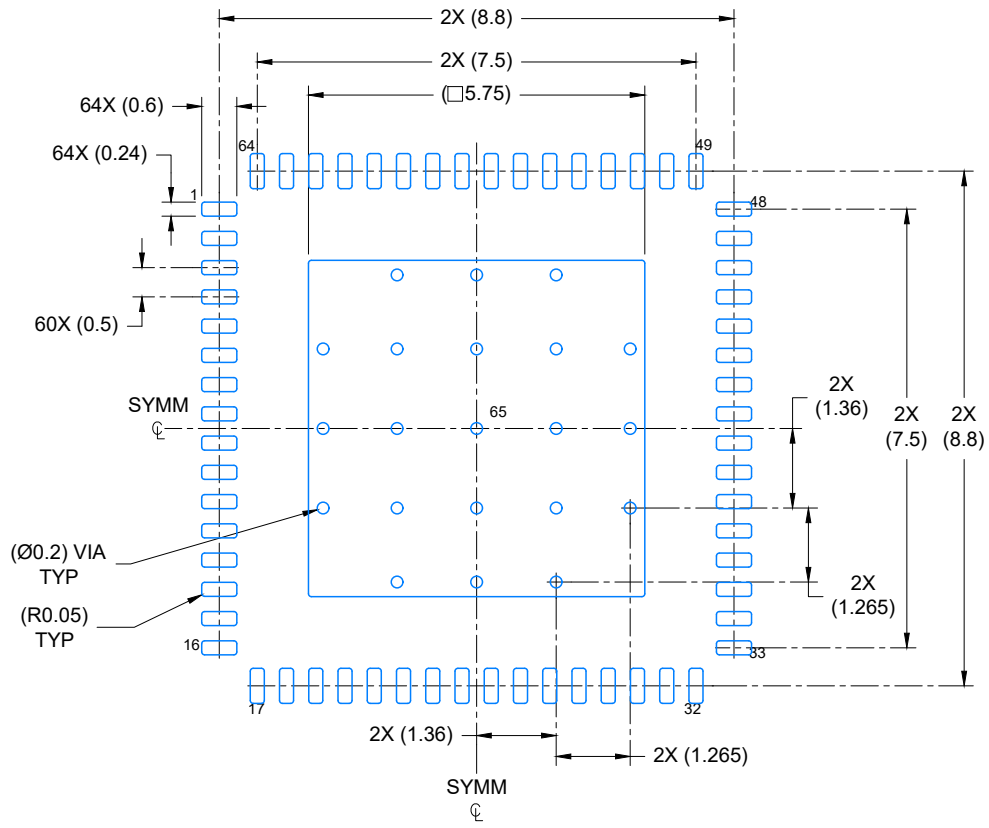
VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

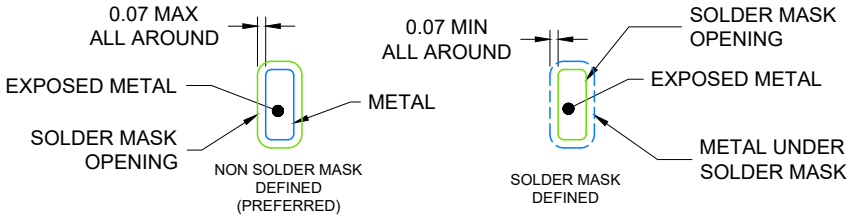


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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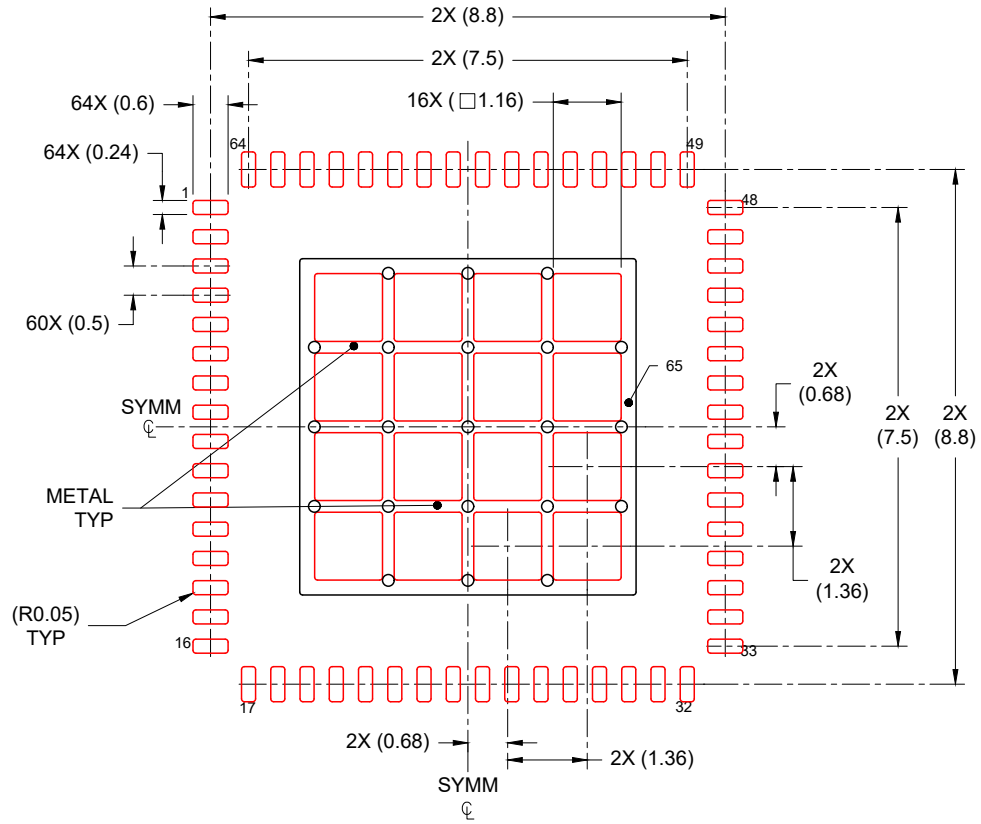
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED COVERAGE BY AREA
SCALE: 8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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