UCC5871-Q1 30-A Isolated IGBT/SiC MOSFET Gate Driver with Advanced Protection Features for Automotive Applications

1 Features

- Split output driver provides 30-A peak source and 30-A peak sink currents
- Interlock and shoot-through protection with 150-ns(max) propagation delay and programmable minimum pulse rejection
- Primary and secondary side active short circuit (ASC) support
- Configurable power transistor protections
  - DESAT based short circuit protection
  - Shunt resistor based overcurrent and short circuit protection
  - NTC based overtemperature protection
  - Programmable soft turnoff (STO) and two-level turnoff (2LTOFF) during power transistor faults
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL D
- Integrated diagnostics:
  - Built-in self test (BIST) for protection comparators
  - IN+ to transistor gate path integrity
  - Power transistor threshold monitoring
  - Internal clock monitoring
  - Fault alarm (nFLT1) and warning (nFLT2) outputs
- Integrated 4-A active Miller clamp or optional external drive for Miller clamp transistor
- Advanced high voltage clamping control
- Internal and external supply undervoltage and overvoltage protection
- Active output pulldown and default low outputs with low supply or floating inputs
- Driver die temperature sensing and overtemperature protection
- 100-kV/µs minimum common mode transient immunity (CMTI) at V_{CM} = 1000 V
- SPI based device reconfiguration, verification, supervision, and diagnosis
- Integrated 10-bit ADC for power transistor temperature, voltage, and current monitoring

2 Applications

- HEV and EV traction inverter
- HEV and EV power modules

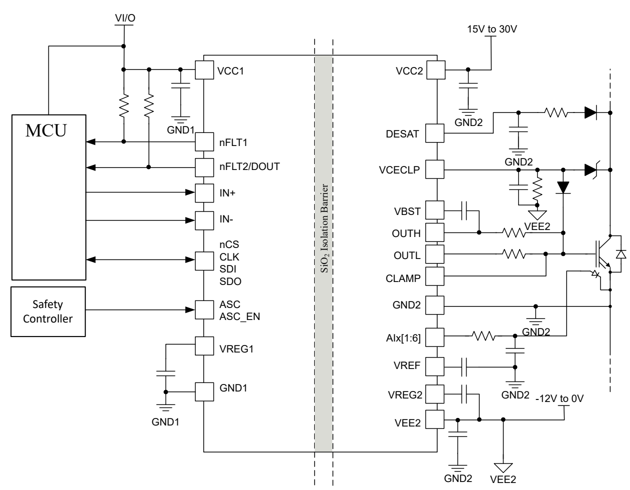
3 Description

The UCC5871-Q1 device is an isolated, highly configurable single-channel gate driver targeted to drive high power SiC MOSFETs and IGBTs in EV/HEV applications. Power transistor protections, such as shunt-resistor–based overcurrent, NTC-based overtemperature, and DESAT detection, include selectable soft turn-off or two-level turn-off during these faults. To further reduce the application size, the UCC5871-Q1 integrates a 4-A active Miller clamp during switching, and an active gate pulldown while the driver is unpowered. An integrated 10-bit ADC enables monitoring of up to six analog inputs and the gate driver temperature for enhanced system management. Diagnostics and detection functions are integrated to simplify the system design. The parameters and thresholds for these features are configurable using the SPI interface, which allows the device to be used with nearly any SiC MOSFET or IGBT.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
UCC5871-Q1	SSOP (36)	12.8 mm × 7.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

1 Features.......1
2 Applications.......1
3 Description.......1
4 Revision History.......2
5 Pin Configuration and Functions.......3
6 Specifications.......6
6.1 Absolute Maximum Ratings.......6
6.2 ESD Ratings.......6
6.3 Recommended Operating Conditions.......6
6.4 Thermal Information.......7
6.5 Power Ratings.......7
6.6 Insulation Specifications.......7
6.7 Safety Limiting Values.......8
6.8 Electrical Characteristics.......9
6.9 SPI Timing Requirements.......16
6.10 Switching Characteristics.......16
6.11 Typical Characteristics.......18
7 Layout.......22
7.1 Layout Guidelines.......22
7.2 Layout Example.......23
8 Device and Documentation Support.......24
8.1 Device Support.......24
8.2 Documentation Support.......24
8.3 Receiving Notification of Documentation Updates.......24
8.4 Support Resources.......24
8.5 Trademarks.......24
8.6 Electrostatic Discharge Caution.......24
8.7 Glossary.......24
9 Mechanical, Packaging, and Orderable Information.......24

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

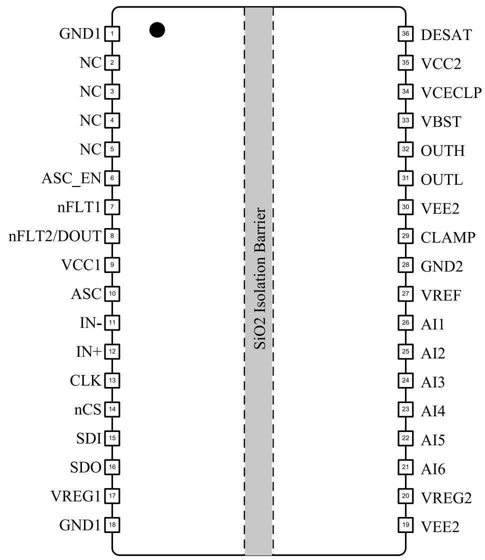


Figure 5-1. DWJ 36-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
1	GND1	G	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side.
2	NC	—	No internal connection. Connect to GND1.
3	NC	—	No internal connection. Connect to GND1.
4	NC	—	No internal connection. Connect to GND1.
5	NC	—	No internal connection. Connect to GND1.
6	ASC_EN	I	Active Short Circuit Enable Input. ASC_EN enables the ASC function and forces the output of the driver to the state defined by the ASC input. If ASC is high, OUTH is pulled high. If ASC is low, OUTL is pulled low.
7	nFLT1	O	Fault Indicator Output 1. nFLT1 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT1 low when the fault occurs. nFLT1 is high when all faults are either non-existent or masked.
8	nFLT2/DOUT	O	Fault Indicator Output 2. nFLT2 is used to interrupt the host when a fault occurs. Additionally, nFLT2 may be configured as DOUT to provide the host controller a PWM signal with a duty cycle relative to the ADC input of interest. Faults that are unmasked pull nFLT2 low when the fault occurs. nFLT2 is high when all faults are either non-existent or masked.
9	V_{CC1}	P	Primary Side Power Supply. Connect a 3V to 5.5V power supply to VCC1. Bypass VCC1 to GND1 with ceramic bulk capacitance as close to the VCC1 pin as possible.
10	ASC	I	Active Short Circuit Control Input. ASC sets the drive state when ASC_EN is high. If ASC is high, OUTH is pulled high. If ASC is low, OUTL is pulled low.
11	IN–	I	Negative PWM Input. IN- is connected to the IN+ from the opposite arm of the half-bridge. If IN+ and IN- overlap, the Shoot Through Protection (STP) fault is asserted.
12	IN+	I	Positive PWM Input. IN+ drives the state of the driver output. With the driver enabled, when IN+ is high, OUTH is pulled high. When IN+ is low, OUTL is pulled low. Drive IN+ with a 1kHz to 50kHz PWM signal, with a logic level determined by the VCC1 voltage. IN+ is connected to the IN- of the opposite arm of the half-bridge. If IN+ and IN- overlap, the Shoot Through Protection (STP) fault is asserted.
13	CLK	I	SPI Clock. CLK is the clock signal for the main SPI interface. The SPI interface operates with clock rates up to 4MHz.
14	nCS	I	SPI Chip Selection Input. nCS is an active low input used to activate the SPI peripheral device. Drive nCS low during SPI communication. When nCS is high, the CLK and SDI inputs are ignored.
15	SDI	I	SPI Data Input. SDI is the data input for the main SPI interface. Data is sampled on the falling edge of CLK, SDI must be in a stable condition to ensure proper communication.

Table 5-1. Pin Functions (continued)

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
16	SDO	O	SPI Data Output. SDO is the data output for the main SPI interface. Data is clocked out on the falling edge of CLK, SDO is changed with a rising edge of CLK.
17	V_{REG1}	P	Internal Voltage Regulator Output. VREG1 provides a 1.8V rail for internal primary-side circuits. Bypass VREG1 to GND1 with at least 4.7µF of ceramic capacitance. Do not put any additional load on VREG1.
18	GND1	G	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side.
19	V_{EE2}	P	Secondary Negative Power Supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of ceramic capacitance as close to the VEE1 pin as possible.
20	V_{REG2}	P	Internal voltage regulator output. VREG2 provides a 1.8V rail for internal secondary-side circuits. Bypass VREG2 to VEE2 with at least 4.7µF of ceramic capacitance. Do not put any additional load on VREG2.
21	AI6	I	Analog Input 6. AI6 is a multi-function input. It is configurable as an input to the internal ADC, a power FET current sense protection comparator input, and an ASC input for the secondary side.
22	AI5	I	Analog Input 5. AI5 is a multi-function input. It is configurable as an input to the internal ADC, a power FET over temperature protection comparator input, and an ASC_EN input for the secondary side.
23	AI4	I	Analog Input 4. AI4 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input.
24	AI3	I	Analog Input 3. AI3 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input.
25	AI2	I	Analog Input 2. AI2 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input.
26	AI1	I	Analog Input 1. AI1 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input.
27	V_{REF}	P	Internal ADC Voltage Regulator Output. VREF provides an internal 4V, reference for the ADC. Bypass VREF to GND2 with at least 1uF of ceramic capacitance. If an external reference is desired, disable the internal VREF using the SPI register, and connect a 4V reference supply to VREF. Loads up to 5mA on VREF are allowed.
28	GND2	G	Gate Drive Common Input. Connect GND2 to the power FET source/ IGBT emitter. All AIx inputs, VREF, and DESAT are referenced to GND2.
29	CLAMP	IO	Miller Clamp Input. The CLAMP input is used to hold the gate of the power FET strongly to VEE2 while the power FET is "off". CLAMP is configurable as an internal Miller clamp, or to drive an external clamping circuit. When using the internal clamping function, connect CLAMP directly the power FET gate. When configured as an external clamp, connect CLAMP to the gate of an external pulldown MOSFET.
30	V_{EE2}	P	Secondary negative power supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of ceramic capacitance as close to the VEE2 pin as possible. Additional capacitance may be needed depending on the required drive current.
31	OUTL	O	Negative Gate Drive Voltage Output. When the driver is active, OUTL drives the gate of the power FET low when INP is low. Connect OUTL to the gate of the power FET through a gate resistor. The value of the gate resistor is chosen based on the slew rate required for the application.
32	OUTH	O	Positive Gate Drive Voltage Output. When the driver is active, OUTH drives the gate of the power FET high when INP is high. Connect OUTH to the gate of the power FET through a gate resistor. The value of the gate resistor is chosen based on the slew rate required for the application.
33	V_{BST}	P	Bootstrap Supply. VBST supplies power for the OUTH drive. Connect a 0.1µF ceramic capacitor between VBST and OUTH.
34	V_{CECLP}	I	VCE Clamp Input. VCECLP clamps to a diode above the VCC2 rail and indicates a fault when the voltage at VCECLP is above the VCECLPth threshold. Bypass VCECLP to VEE2 with ceramic capacitor and, in parallel, connect a resistor. Additionally, connect VCECLP to the anode of a zener diode to the collector of the power FET.
35	V_{CC2}	P	Secondary Positive Power Supply. Connect a 15V to 30V power supply to VCC2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VCC2 to GND2 and VCC2 to VEE2 with bulk ceramic capacitance as close to the VCC2 pin as possible. Additional capacitance may be needed depending on the required drive current.

Table 5-1. Pin Functions (continued)

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
36	DESAT	I	Desaturation based Short Circuit Detection Input. DESAT is used to detect a short circuit in the power FET. Bypass DESAT to GND2 with a ceramic capacitor to program the DESAT blanking time. In parallel, connect a schottky diode with the cathode connected to the DESAT. Additionally, connect DESAT to a resistor to the anode of a diode to the collector of the power FET to adjust the DESAT protection threshold. DESAT detects a fault when the VCE voltage of the power FET exceeds the defined threshold while the power FET is on.

(1) P = Power, G = Ground, I = Input, O = Output, - = NA

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC1}	Supply voltage primary side referenced to GND1	–0.3	6	V
V_{CC2}	Positive supply voltage secondary side referenced to GND2	–0.3	33	V
V_{EE2}	Negative supply voltage output side referenced to GND2	–15	0.3	V
V_{SUP2}	Total supply voltage output side (V_{CC2} - V_{EE2})	–0.3	33	V
V_{OUTH}, V_{OUTL}	Voltage on the driver output pins referenced to GND2	V_{EE2}–0.3	V_{CC2}+0.3	V
V_{IOP}	Voltage on IO pins (ASC, ASC_EN, CLK, IN+, IN-, nCS, nFLTx, SDI, SDO) on primary side referenced to GND1	–0.3	V_{CC1}+0.3	V
V_{CLAMP}	Voltage on the Miller clamp pin referenced to GND2	V_{EE2}–0.3	V_{CC2} +0.3	V
V_{DESAT}	Voltage on DESAT referenced to GND2	–0.3	V_{CC2} +0.3	V
V_{CECLP}	Voltage on VCECLP referenced to GND2	V_{EE2}–0.3	V_{CC2} +0.3	V
V_{REG1}	Voltage on VREG1 referenced to GND1	–0.3	2	V
V_{REG2}	Voltage on VREG2 referenced to VEE2	–0.3	2	V
V_{REF}	Voltage on VREF referenced to GND2	–0.3	5.5	V
V_{BST}	Voltage on VBST referenced to OUTH	-0.3	5.3	V
V_{AI}	Voltage on the analog inputs referenced to GND2	–0.3	5.5	V
T_J	Junction temperature	–40	150	ºC
T_{stg}	Storage temperature	–65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (GND1 and VEE2)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage input side	3		5.5	V
V_{CC2}	Positive supply voltage secondary side (V_{CC2} - GND2)	15		30	V
V_{EE2}	Negative supply voltage output side (V_{EE2} - GND2)	–12		0	V
V_{SUP2}	Total supply voltage output side (V_{CC2} - V_{EE2})	15		30	V
V_{IH}	High-level IO voltage (ASC, ASC_EN, IN+, IN-, nCS, SCLK, SDI)	0.7*V_{CC1}		V_{CC1}	V
V_{IL}	Low-level IO voltage (ASC, ASC_EN, IN+, IN-, nCS, SCLK, SDI)	0		0.3*V_{CC1}	V
I_{OHP}	Source current for primary side outputs (nFLT2, SDO)			5	mA
I_{OLP}	Sink current for primary side outputs (nFLTx, SDO)			5	mA
I_{OH}	Driver output source current from OUTH [1]			15	A
I_{OL}	Driver output sink current into OUTL [1]			15	A
V_{AI*}	Voltage on analog input (AI) pins referenced to GND2	0		V_{REF}+0.1	V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VREG1}	Output voltage at VREG1 referenced to GND1 [(2)]		1.8		V
V_{VREG2}	Output voltage at VREG2 referenced to VEE2[(3)]		1.8		V
V_{VBST}	Output voltage at VBST referenced to OUTH[(4)]		V_{cc2} + 4.5		V
V_{VREF}	Voltage on the VREF pin vs GND2[(5)]	0	4	4.1	V
CMTI	Common mode transient immunity rating (dV/dt rate across the isolation barrier)			100	kV/us
f_{PWM}	PWM input frequency (IN+ and IN- pins)			50	kHz
f_{SPI}	SPI clock frequency			4	MHz
T_J	Maximum junction temperature	– 40		150	℃
t_{PWM}	PWM input pulse width (IN+ and IN- pins)	250			ns

(1) External gate resistor needs to be used to limit the max drive current to be not more than 15A.
(2) Connect a decoupling capacitor of 0.1uF+4.7uF between VREG1 and GND1. Do not connect external supply.
(3) Connect a decoupling capacitor of 0.1uF+4.7uF between VREG2 and VEE2. Do not connect external supply.
(4) Connect a decoupling capacitor of 100nF between VBST and OUTH. Do not connect external supply.
(5) Connect a decoupling capacitor of 1.0uF on the VREF pin.

6.4 Thermal Information

THERMAL METRIC[(1)]		UCC5870/UCC5871	UNIT
		DWJ	
		36 SOIC	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	T_A = 125C			500	mW
P_{D1}	Maximum power dissipation (side-1)	T_A = 125C			50	mW
P_{D2}	Maximum power dissipation (side-2)	T_A = 125C			450	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
PACKAGE SPECIFICATIONS				
CLR	External clearance[(1)]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[(1)]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	600	V
	Material group	According to IEC60664-1	I	

6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
Test 1				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	8000	V_{PK}
q_{pd}	Apparent charge	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
Test 2				
C_{IO}	Barrier capacitance, input to output(2)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	2	pF
R_{IO}	Insulation resistance, input to output(2)	V_{IO} = 500 V, T_A = 25°C	10^12	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	10^11	
		V_{IO} = 500 V at T_S = 150°C	10^9	
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = V_{RMS}$, t = 1 s (100% production)		V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator onthe printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases.Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
36-DWJ PACKAGE						
I_S	Safety output supply current	$R_{\theta JA}$ = 50.6°C/W, V_{VCC2} = 15V, T_J = 150°C, T_A = 25°C			164	mA
		$R_{\theta JA}$ = 50.6°C/W, V_{VCC2} = 30V, T_J = 150°C, T_A = 25°C			82	
P_S	Safety input power	$R_{\theta JA}$ = 50.6°C/W, T_J = 150°C, T_A = 25°C			83	mW
P_S	Safety output power	$R_{\theta JA}$ = 50.6°C/W, T_J = 150°C, T_A = 25°C			2460	mW
P_S	Safety total power	$R_{\theta JA}$ = 50.6°C/W, T_J = 150°C, T_A = 25°C			2543	mW

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, TS, has the same value as the maximum junction temperature, TJ, specified for the device. The IS and PS parameters represent the safety current and safety power respectively. The maximum limits of IS and PS should not be exceeded. These limits vary with the ambient temperature, TA. The junction-to-air thermal resistance, RθJA, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:TJ = TA + RθJA × P, where P is the power dissipated in the device.TJ(max) = TS = TA + RθJA × PS, where TJ(max) is the maximum allowed junction temperature.PS = IS × VI, where VI is the maximum input voltage.

6.8 Electrical Characteristics

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IT+} (UVLO1)	UVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 0	2.6	2.75	2.9	V
V_{IT+} (UVLO1)	UVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 1	4.5	4.65	4.8	V
V_{IT-} (UVLO1)	UVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 0	2.3	2.45	2.6	V
V_{IT-} (UVLO1)	UVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 1	4.2	4.35	4.5	V
V_{HYS} (UVLO1)	UVLO threshold hysteresis of V_{CC1}			0.30		V
t_{UVLO1}	VCC1 UVLO detection deglitch time			20		µs
V_{IT-} (OVLO1)	OVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 0	3.7	3.85	4.0	V
V_{IT-} (OVLO1)	OVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 1	5.2	5.35	5.5	V
V_{IT+} (OVLO1)	OVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 0	4.0	4.15	4.3	V
V_{IT+} (OVLO1)	OVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 1	5.5	5.65	5.8	V
V_{HYS} (OVLO1)	OVLO threshold hysteresis of V_{CC1}			0.30		V
t_{OVLO1}	VCC1 OVLO detection deglitch time			20		µs
V_{IT+} (UVLO2)	UVLO threshold voltage of V_{CC2} rising with reference to GND2	UVLO2TH = 00b	15.2	16	16.8	V
		UVLO2TH = 01b	13.3	14	14.7	V
		UVLO2TH = 10b	11.4	12	12.6	V
		UVLO2TH = 11b	9.5	10	10.5	V
V_{IT-} (UVLO2)	UVLO threshold voltage of V_{CC2} falling with reference to GND2	UVLO2TH = 00b	14.25	15	15.75	V
		UVLO2TH = 01b	12.35	13	13.65	V
		UVLO2TH = 10b	10.45	11	11.55	V
		UVLO2TH = 11b	8.55	9	9.45	V
V_{HYS} (UVLO2)	UVLO threshold voltage hysteresis of V_{CC2}			1		V
t_{UVLO2}	VCC2 UVLO detection deglitch time			20		µs
V_{IT-} (OVLO2)	OVLO threshold voltage of $V_{CC2\ falling}$ with reference to GND2	OVLO2TH = 00b	21.85	23	24.15	V
		OVLO2TH = 01b	19.95	21	22.05	V
		OVLO2TH = 10b	18.05	19	19.95	V
		OVLO2TH = 11b	16.15	17	17.85	V

6.8 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+} (OVLO2)	OVLO threshold voltage of $V_{CC2\ rising}$ with reference to GND2	OVLO2TH = 00b	22.8	24	25.2	V
		OVLO2TH = 01b	20.9	22	23.1	V
		OVLO2TH = 10b	19	20	21	V
		OVLO2TH = 11b	17.1	18	18.9	V
V_{HYS} (OVLO2)	OVLO threshold voltage hysteresis of V_{CC2}			1		V
t_{OVLO2}	VCC2 OVLO detection blanking time			20		µs
V_{IT-} (UVLO3)	UVLO threshold voltage of $V_{EE2\ falling}$ with reference to GND2	UVLO3TH = 00b	–3.15	–3	–2.85	V
		UVLO3TH = 01b	–5.25	–5	–4.75	V
		UVLO3TH = 10b	–8.4	–8	–7.6	V
		UVLO3TH = 11b	–10.5	–10	–9.5	V
V_{IT+} (UVLO3)	UVLO threshold voltage of $V_{EE2\ rising}$ with reference to GND2	UVLO3TH = 00b	–2.1	–2	–1.9	V
		UVLO3TH = 01b	–4.2	–4	–3.8	V
		UVLO3TH = 10b	–7.35	–7	–6.65	V
		UVLO3TH = 11b	–9.45	–9	–8.55	V
V_{HYS} (UVLO3)	UVLO threshold voltage hysteresis of V_{EE2}			1		V
t_{UVLO3}	VEE2 UVLO detection blanking time			20		µs
V_{IT+} (OVLO3)	OVLO threshold voltage of V_{EE2} rising with reference to GND2	OVLO3TH = 00b	–5.25	–5	–4.75	V
		OVLO3TH = 01b	–7.35	–7	–6.65	V
		OVLO3TH = 10b	–10.5	–10	–9.5	V
		OVLO3TH = 11b	–12.6	–12	–11.4	V
V_{IT-} (OVLO3)	OVLO threshold voltage of V_{EE2} falling with reference to GND2	OVLO3TH = 00b	–6.3	–6	–5.7	V
		OVLO3TH = 01b	–8.4	–8	–7.6	V
		OVLO3TH = 10b	–11.55	–11	–10.45	V
		OVLO3TH = 11b	–13.65	–13	–12.35	V
$V_{HYS(OVLO3)}$	OVLO threshold voltage hysteresis of V_{EE2}			1		V
t_{OVLO3}	VEE2 OVLO detection blanking time			20		µs
I_{QVCC1}	Quiescent Current of V_{CC1}	No switching, VCC1 = 5V			7.7	mA
I_{QVCC2}	Quiescent Current of V_{CC2}	No switching, VCC2 = 20V, VEE2 = -10V			15	mA
I_{QVEE2}	Quiescent Current of V_{EE2}	No switching, VCC2 = 20V, VEE2 = -10V			15	mA
$t_{RP(VCC1)}$	Slew rate of V_{CC1}				0.1	V/µs
$t_{RP(VCC2)}$	Slew rate of V_{CC2}				0.1	V/µs
$t_{RP(VEE2)}$	Slew rate of V_{EE2}				0.1	V/µs
LOGIC IO						
V_{IH}	Input-high threshold voltage of primary IO (IN+, IN-, ASC, and ASC_EN)	Input rising, VCC1 = 3.3V			0.7*V_{CC1}	V
	Input-high threshold voltage of secondary IO in ASC mode (AI5, and AI6)	Input rising, VREF=4V			3.0	V
V_{IL}	Input-low threshold voltage of primary IO (IN+, IN-, ASC, and ASC_EN)	VCC1 = 3.3V	0.3*V_{CC1}			V
	Input-low input-threshold voltage of secondary IO in ASC mode (AI5 and AI6)	Input falling	1.5			V

6.8 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS(IN)}$	Input hysteresis voltage of primary IO (IN+, IN-, ASC, and ASC_EN)	VCC1=3.3V		$0.1^{*}V_{CC1}$		V
	Input hysteresis voltage of secondary IO in ASC mode (AI5, and AI6)			0.5		V
I_{LI}	Leakage current on the input IO pins ASC, ASC_EN, IN+, IN-, CLK, and SDI	V_{IO} = GND1, V_{IO} is the voltage on IO pins			5	µA
	Leakage current on nCS	V_{IO} = VCC1, V_{IO} is the voltage on IO pins			5	µA
R_{PUI}	Pullup resistance for nCS		40		100	kΩ
R_{PDI}	Pulldown resistance for ASC, ASC_EN, IN+, IN-, CLK, and SDI		40		100	kΩ
	Pulldown resistance for AI5 and AI6 in ASC mode		800		1200	kΩ
V_{OH}	Output logic-high voltage (SDO)	4.5mA output current, VCC1 = 5V	$0.9^{*}V_{CC1}$			V
V_{OL}	Output logic-low voltage (nFLT1, nFLT2, and SDO)	4.5mA sink current, VCC1 = 5V			$0.1^{*}V_{CC1}$	V
f_{DOUT}	Output frequency of DOUT pin	FREQ_DOUT = 00b		13.9		kHz
		FREQ_DOUT = 01b		27.8		kHz
		FREQ_DOUT = 10b		55.7		kHz
		FREQ_DOUT = 11b		111.4		kHz
D_{DOUT}	Duty of DOUT	V_{AI^*} = 0.36 V		10		%
		V_{AI^*} = 1.8 V		50		%
		V_{AI^*} = 3.24 V		90		%
I_{LO}	Leakage current on pin nFLT*	nFLT* = HiZ, VCC1 on nFLT* pin	–5		5	µA
	Leakage current on pin SDO	nCS = 1	–5		5	µA
R_{PUO}	Pullup resistance for pin nFLT*		40		100	kΩ
DRIVER STAGE						
V_{OUTH}	High-level output voltage (OUT and OUTH)	I_{OUT} = -100 mA	VCC2 – 0.033			V
V_{OUTL}	Low-level output voltage (OUT and OUTL)	I_{OUT} = 100 mA			33	mV
I_{OUTH}	Gate driver high output current	IN+= high, IN- = low, VCC2 - VOUTH = 5 V	15			A
I_{OUTL}	Gate driver low output current	IN- = low, IN + = high, VOUTL - VEE2 = 5 V	15			A
I_{STO}	Driver low output current during SC and OC faults	VOUTL - VEE2 = 6 V and STO_CURR = 00b, 100℃ to 150℃	0.24	0.3	0.36	A
		VOUTL - VEE2 = 6 V and STO_CURR = 01b, 100℃ to 150℃	0.48	0.6	0.72	A
		VOUTL - VEE2 = 6 V and STO_CURR = 10b, 100℃ to 150℃	0.72	0.9	1.08	A
		VOUTL - VEE2 = 6 V and STO_CURR = 11b, 100℃ to 150℃	0.96	1.2	1.44	A
ACTIVE MILLER CLAMP						
V_{CLP}	Low-level clamp voltage (internal Miller clamp)	I_{CLP} = 100 mA			100	mV
	Miller clamp current	MCLPTH=11b, V_{CLAMP} = V_{EE2}+4 V	3.2			A

6.8 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CLPTH}	Clamp threshold voltage with reference to VEE2	MCLPTH = 00b	1.2	1.5	1.8	V
		MCLPTH = 01b	1.6	2	2.5	V
		MCLPTH = 10b	2.25	3	3.75	V
		MCLPTH = 11b	3	4	5	V
V_{ECLP}	CLAMP output voltage in external Miller clamp mode		4.5	5	5.5	V
R_{ECLP_PD}	CLAMP pull-down resistance in external Miller clamp mode			13		Ω
R_{ECLP_PU}	CLAMP pull-up resistance in external Miller clamp mode			13		Ω
SHORT CIRCUIT CLAMPING						
$V_{CLP\text{-}OUT}$	Clamping voltage (V_{OUTH} - $V_{CC2,}$ V_{CLAMP} - V_{CC2})	IN+= high, IN- = low, t_{CLP} = 10us, I_{OUTH} or I_{CLAMP} = 500 mA		0.8	1.6	V
ACTIVE PULLDOWN						
V_{OUTSD}	Active shut-down voltage on OUTL	I_{OUTL} = 30mA, VCC2 = open			1.55	V
V_{OUTSD}	Active shut-down voltage on OUTL	I_{OUTL} = 0.1xI_{OUTL}, V_{CC2} = open			2.5	V
DESAT SHORT-CIRCUIT PROTECTION						
$V_{DESATth}$	DESAT detection threshold voltage with respect to GND2	DESATTH = 0000b	2.25	2.5	2.75	V
		DESATTH = 0001b	2.7	3	3.3	V
		DESATTH = 0010b	3.15	3.5	3.85	V
		DESATTH = 0011b	3.6	4	4.4	V
		DESATTH = 0100b	4.05	4.5	4.95	V
		DESATTH = 0101b	4.5	5	5.5	V
		DESATTH = 0110b	4.95	5.5	6.05	V
		DESATTH = 0111b	5.4	6	6.6	V
		DESATTH = 1000b	5.85	6.5	7.15	V
		DESATTH = 1001b	6.3	7	7.7	V
		DESATTH = 1010b	6.75	7.5	8.25	V
		DESATTH = 1011b	7.2	8	8.8	V
		DESATTH = 1100b	7.65	8.5	9.35	V
		DESATTH = 1101b	8.1	9	9.9	V
		DESATTH = 1110b	8.55	9.5	10.45	V
		DESATTH = 1111b	9	10	11	V
V_{DESATL}	DESAT voltage with respect to GND2 when OUTL is driven low				1	V
I_{CHG}	Blanking capacitor charging current	V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 00b	0.555	0.6	0.645	mA
		V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 01b	0.6475	0.7	0.7525	mA
		V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 10b	0.74	0.8	0.86	mA
		V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 11b	0.925	1	1.075	mA
I_{DCHG}	Blanking capacitor discharging current	V(DESAT) - GND2 = 6 V	14			mA
t_{LEB}	DESAT leading edge blanking time		127	158	250	ns
t_{DESFLT}	DESAT pin glitch filter	DESAT_DEGLITCH=0	90	158	190	ns
t_{DESFLT}	DESAT pin glitch filter	DESAT_DEGLITCH=1	270	316	401	ns

6.8 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DESAT} (90%)	DESAT protection reaction time from event to action (includes deglitch time)	V_{DESAT}>$V_{DESATth}$ to VOUTL 90% of V_{CC2}, C_{LOAD} = 1 nF, DESAT_DEGLITCH=0			160 + t_{DESFLT}	ns
OVERCURRENT PROTECTION						
V_{OCth}	Over current detection threshold voltage	OCTH = 0000b	170	200	225	mV
		OCTH = 0001b	220	250	275	mV
		OCTH = 0010b	270	300	330	mV
		OCTH = 0011b	315	350	375	mV
		OCTH = 0100b	360	400	440	mV
		OCTH = 0101b	410	450	475	mV
		OCTH = 0110b	460	500	525	mV
		OCTH = 0111b	520	550	575	mV
		OCTH = 1000b	570	600	630	mV
		OCTH = 1001b	610	650	690	mV
		OCTH = 1010b	660	700	740	mV
		OCTH = 1011b	710	750	790	mV
		OCTH = 1100b	760	800	840	mV
		OCTH = 1101b	807	850	893	mV
		OCTH = 1110b	855	900	945	mV
		OCTH = 1111b	902	950	998	mV
V_{SCth}	Short circuit protection threshold	SCTH = 00b	460	500	530	mV
		SCTH = 01b	700	750	785	mV
		SCTH = 10b	945	1000	1050	mV
		SCTH = 11b	1185	1250	1312	mV
t_{SCBLK}	Short circuit protection blanking time with reference to system clock	SC_BLK = 00b		100		ns
		SC_BLK = 01b		200		ns
		SC_BLK = 10b		400		ns
		SC_BLK = 11b		800		ns
t_{OCBLK}	Over current protection blanking time with reference to system clock	OC_BLK = 000b		500		ns
		OC_BLK = 001b		1000		ns
		OC_BLK = 010b		1500		ns
		OC_BLK = 011b		2000		ns
		OC_BLK = 100b		2500		ns
		OC_BLK = 101b		3000		ns
		OC_BLK = 110b		5000		ns
		OC_BLK = 111b		10000		ns
t_{SCFLT}	Short circuit protection deglitch filter		50	150	200	ns
t_{OCFLT}	Over current protection deglitch filter		50	150	200	ns
$t_{SC(90\%)}$	Short circuit protection reaction time from event to action (includes deglitch time)	V_{AIx} > V_{SCth} to VOUTL at 90% of VCC2, C_{LOAD} = 1nF, t_{SCBLK} expired			175 + t_{SCFLT}	ns
$t_{OC(90\%)}$	Over current protection reaction time from event to action (includes deglitch time)	V_{AIx} > V_{OCth} to VOUTL at 90% of VCC2, C_{LOAD} = 1nF, t_{OCBLK} expired			175 + t_{OCFLT}	ns
TWO-LEVEL TURN-OFF PLATEAU VOLTAGE LEVEL						

6.8 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{2\ LOFF}$	Plateau voltage (with respect to GND2) during two-level turnoff	2LOFF_VOLT = 000b	5	6	7	V
		2LOFF_VOLT = 001b	6	7	8	V
		2LOFF_VOLT = 010b	7	8	9	V
		2LOFF_VOLT = 011b	8	9	10	V
		2LOFF_VOLT = 100b	9	10	11	V
		2LOFF_VOLT = 101b	10	11	12	V
		2LOFF_VOLT = 110b	11	12	13	V
		2LOFF_VOLT = 111b	12	13	14	V
$t_{2\ LOFF}$	Plateau voltage during two-level turnoff hold time	2LOFF_TIME = 000b		150		ns
		2LOFF_TIME = 001b		300		ns
		2LOFF_TIME = 010b		450		ns
		2LOFF_TIME = 011b		600		ns
		2LOFF_TIME = 100b		1000		ns
		2LOFF_TIME = 101b		1500		ns
		2LOFF_TIME = 110b		2000		ns
		2LOFF_TIME = 111b		2500		ns
$I_{2\ LOFF}$	Discharge current for transition to plateau voltage level	2LOFF_CURR = 00b, 100℃ to 150℃	0.24	0.3	0.36	A
		2LOFF_CURR = 01b, 100℃ to 150℃	0.48	0.6	0.72	A
		2LOFF_CURR = 10b, 100℃ to 150℃	0.72	0.9	1.08	A
		2LOFF_CURR = 11b, 100℃ to 150℃	0.96	1.2	1.44	A
HIGH VOLTAGE CLAMPING						
$V_{CECLPTH}$	VCE clamping threshold with respect to VEE2		1.5	2.2	2.9	V
$V_{CECLPHYS}$	VCE clamping threshold hysteresis			200		mV
t_{VCECLP}	VCE clamping intervention-time			30		ns
t_{VCECLP_HLD}	VCE clamping hold on time	VCE_CLMP_HLD_TIME = 00b		100		ns
		VCE_CLMP_HLD_TIME = 01b		200		ns
		VCE_CLMP_HLD_TIME = 10b		300		ns
		VCE_CLMP_HLD_TIME = 11b		400		ns
OVERTEMPERATURE PROTECTION						
T_{SD_SET}	Overtemperature protection set for driver		155			°C
T_{SD_CLR}	Overtemperature protection clear for driver		135			°C
T_{WN_SET}	Overtemperature warning set for driver		130			°C
T_{WN_CLR}	Overtemperature warning clear for driver		110			°C
T_{HYS}	Hysteresis for thermal comparators			20		°C
I_{TO}	Bias current for temp sensing diode for pins AI1, AI3, and AI5	TEMP_CURR = 00b, Tj = 100C to 150C	0.097	0.1	0.103	mA
		TEMP_CURR = 01b, Tj = 100C to 150C	0.291	0.3	0.309	mA
		TEMP_CURR = 10b, Tj = 100C to 150C	0.582	0.6	0.618	mA
		TEMP_CURR = 11b, Tj = 100C to 150C	0.97	1	1.03	mA

6.8 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PS_TSDth}	The threshold of power switch over temperature protection.	TSDTH_PS = 000b	0.95	1	1.05	V
		TSDTH_PS = 001b	1.1875	1.25	1.3125	V
		TSDTH_PS = 010b	1.425	1.5	1.575	V
		TSDTH_PS = 011b	1.6625	1.75	1.8375	V
		TSDTH_PS = 100b	1.9	2	2.1	V
		TSDTH_PS = 101b	2.1375	2.25	2.3625	V
		TSDTH_PS = 110b	2.375	2.5	2.625	V
		TSDTH_PS = 111b	2.6125	2.75	2.8875	V
t_{PS_TSDFLT}	Power switch thermal shutdown deglitch time	PS_TSD_DEGLITCH = 00b		250		ns
		PS_TSD_DEGLITCH = 01b		500		ns
		PS_TSD_DEGLITCH = 10b		750		ns
		PS_TSD_DEGLITCH = 11b		1000		ns
GATE VOLTAGE MONITOR						
V_{GMH}	Gate monitor threshold value with reference to VCC2	IN+= high and IN- = low	– 4	– 3	– 2	V
V_{GML}	Gate monitor threshold value with reference to VEE2	IN + = low and IN- = high	2	3	4	V
t_{GMBLK}	Gate voltage monitor blanking time after driver receives PWM transition	GM_BLK = 00b		500		ns
		GM_BLK = 01b		1000		ns
		GM_BLK = 10b		2500		ns
		GM_BLK = 11b		4000		ns
t_{GMFLT}	Gate voltage monitor deglitch time			250		ns
I_{VGTHM}	Charge current for VGTH measurement	VCC2 - VOUTH = 10V		2		mA
t_{dVGTHM}	Delay time between VGTH measurement control command to gate voltage sampling point.			2300		µs
ADC						
FSR	Full scale input voltage range for A1 to A6		0	3.6	3.636	V
V_{REF}	Required voltage for external VREF	Accuracy of external reference directly affects the accuracy of the ADC		4		V
	Internal VREF output voltage			4		V
INL	Integral non-linearity	External reference, VREF = 4V	-1.2		1.2	LSB
		Internal reference	-4		9	LSB
DNL	Differential non-linearity	External reference, VREF = 4V	-0.75		0.75	LSB
		Internal reference	-0.75		0.75	LSB
$t_{ADREFEXT}$	External ADC reference turn on delay time from VCC2 > $V_{IT-(UVLO2)}$	$V_{IT-(UVLO2)}$ to 10% of VREF	10			µs
I_{TO2}	Pull up current on AI2,4,6 pins	$V_{AI2,4,6}$= VREF/2, ITO2_EN=H		10	15	µA
t_{hybrid}	IN+ hold time to cause switchover between center mode and edge mode	ADC in hybrid mode configuration		0.4		ms
t_{CONV}	Time to complete ADC conversion			5.1		µs
t_{RR}	Time between ADC conversions in Edge mode	ADC in edge mode or hybrid mode (after t_{HYBRID}) configuration		7.5		µs

6.9 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock frequency(1)			4	MHz
t_{CLK}	SPI clock period(1)	250			ns
t_{CLKH}	CLK logic high duration(1)	90			ns
t_{CLKL}	CLK logic low duration(1)	90			ns
t_{SU_NCS}	time between falling edge of nCS and rising edge of CLK(1)	50			ns
t_{SU_SDI}	setup time of SDI before the falling edge of CLK(1)	30			ns
t_{HD_SDI}	SDI data hold time (1)	45			ns
t_{D_SDO}	time delay from rising edge of CLK to data valid at SDO(1)			60	ns
t_{HD_SDO}	SDO output hold time(1)	40			ns
t_{HD_NCS}	time between the falling edge of CLK and rising edge of nCS(1)	50			ns
t_{HI_NCS}	SPI transfer inactive time(1)	250			ns
t_{ACC}	nCS low to SDO out of high impedance(1)		60	80	ns
t_{DIS}	time between rising edge of nCS and SDO in tri-state(1)		30	50	ns

(1) Ensured by bench characterization.

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	OUTH rise time	C_{LOAD} = 10 nF			150	ns
t_f	OUTL fall time	C_{LOAD} = 10 nF			150	ns
t_{PLH}, t_{PHL}	Propagation delay from INP to OUTx	C_{LOAD} = 0.1 nF, t_{GLITCH_IO} = 00b			150	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	C_{LOAD} = 0.1 nF		20	50	ns
$t_{sk\text{-}pp}$	Part-to-part skew - same edge	C_{LOAD} = 0.1 nF		20	50	ns
f_{max}	Maximum switching frequency	C_{LOAD} = 0.1 nF, ADC disabled			50	kHz
t_{dFLT1}	Delay from fault detection to nFLT1 pin goes LOW.	C_{LOAD} = 100pF, R_{EPU} = 10kΩ			5	µs
t_{dFLT2}	Delay from fault detection to nFLT2 pin goes LOW.	C_{LOAD} = 100pF, R_{EPU} = 10kΩ			25	µs
t_{ASC_EN}	Required hold time for ASC after ASC_EN transition			1		µs
t_{ASC_DLY}	Delay from the ASC edge to OUTx transition (primary side)	ASC rising	2			µs
		ASC falling		0.1		µs
t_{ASC_DLY}	Delay from the AI6 (ASC) edge to OUTx transition (secondary side)	AI6 rising		1.8		µs
		AI6 falling		0.3		µs
t_{MUTE}	PWM input mute time in case of DESAT, SC, and PS_TSD fault	PWM_MUTE_EN = 1	10			ms
t_{GLITCH_IO}	Deglitch time for the primary side IO pins (exclude nCS, CLK, SDI, and SDO pins)	IO_DEGLITCH = 00b		0		ns
		IO_DEGLITCH = 01b		70		ns
		IO_DEGLITCH = 10b		140		ns
		IO_DEGLITCH = 11b		210		ns
t_{DEAD}	Dead time for shoot through protection	TDEAD = 000000b		0		ns
		TDEAD = 000001b	93	105	154	ns
		TDEAD = 000010b	159	175	228	ns
		TDEAD = 000011b	225	245	302	ns
		TDEAD = 000100b	291	315	376	ns
		TDEAD = 111111b	4178.3	4445	4748.8	ns

6.10 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{STARTUP}$	System start-up time (from power ready to nFLTx pins go high)				5	ms
$t_{VREGxOV}$	VREG1 and VREG2 overvoltage detection deglitch time			30		µs

6.11 Typical Characteristics

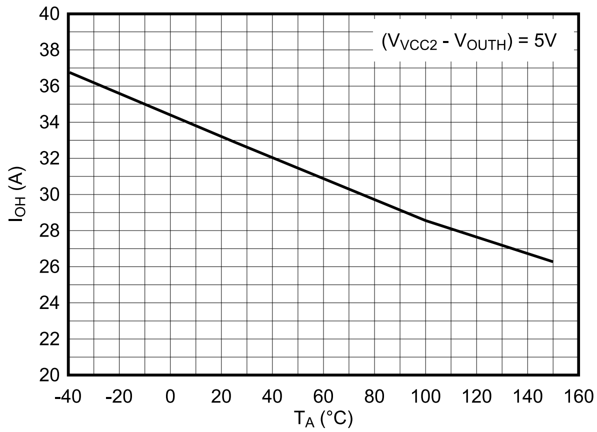


Figure 6-1. I_{OUTH} vs. Temperature

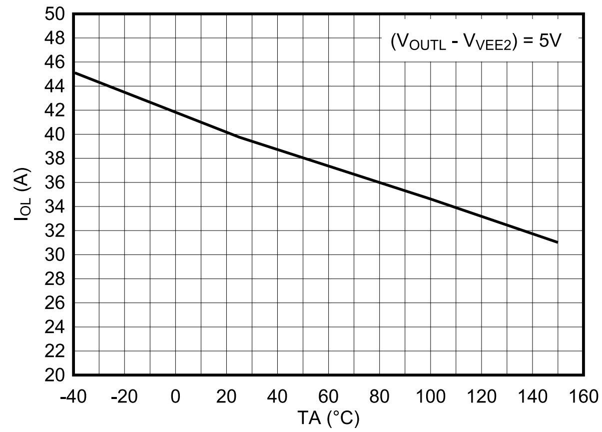


Figure 6-2. I_{OUTL} vs. Temperature

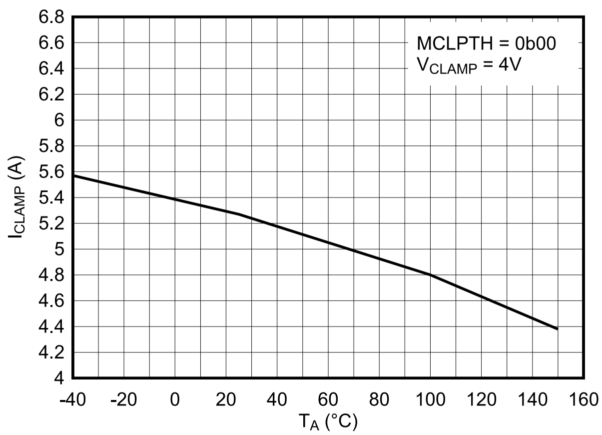


Figure 6-3. Internal Miller Clamp Current vs. Temperature

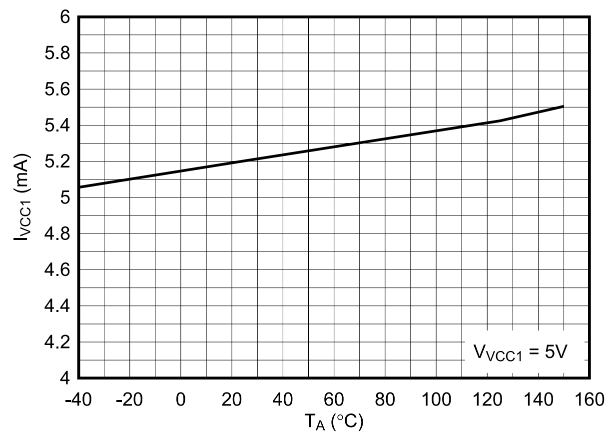


Figure 6-4. VCC1 Quiescent Current vs. Temperature

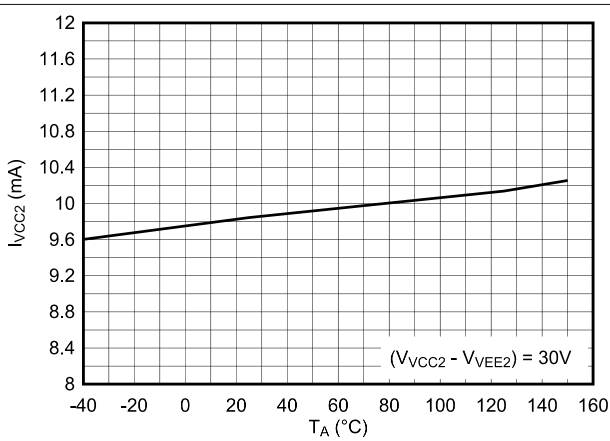


Figure 6-5. VCC2 Quiescent Current vs. Temperature

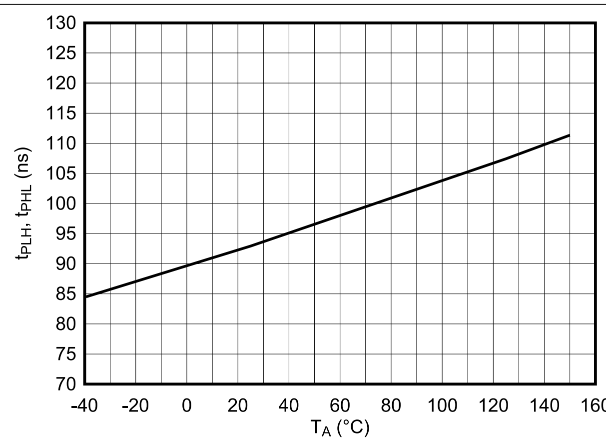


Figure 6-6. Propagation Delay vs. Temperature

6.11 Typical Characteristics (continued)

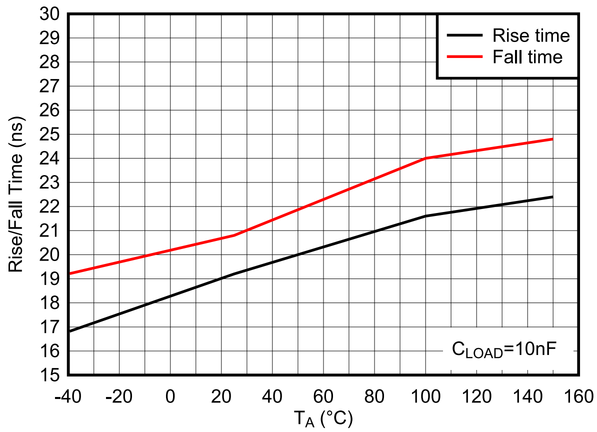


Figure 6-7. Rise/Fall Time vs. Temperature

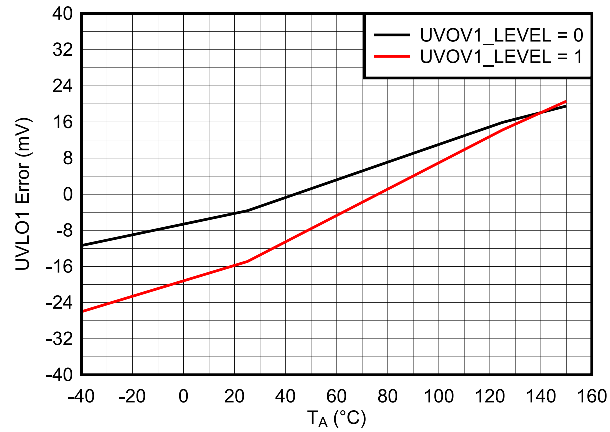


Figure 6-8. UVLO Threshold Error vs. Temperature

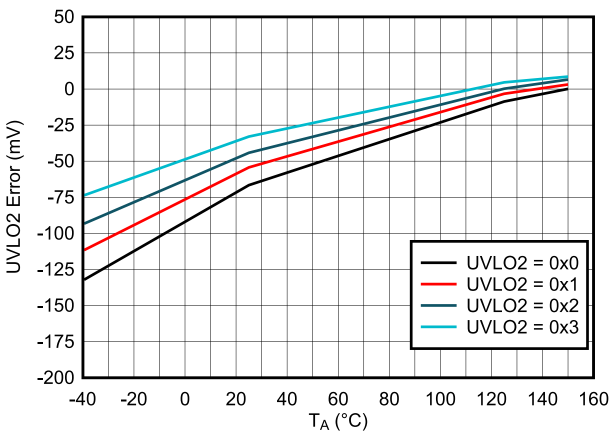


Figure 6-9. UVLO2 Error vs. Temperature

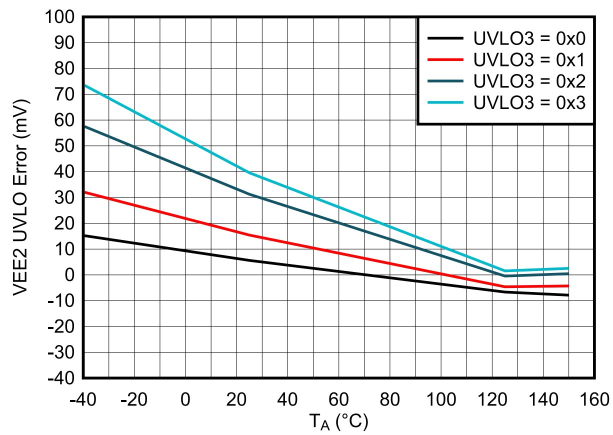


Figure 6-10. VEE2 UVLO Error vs. Temperature

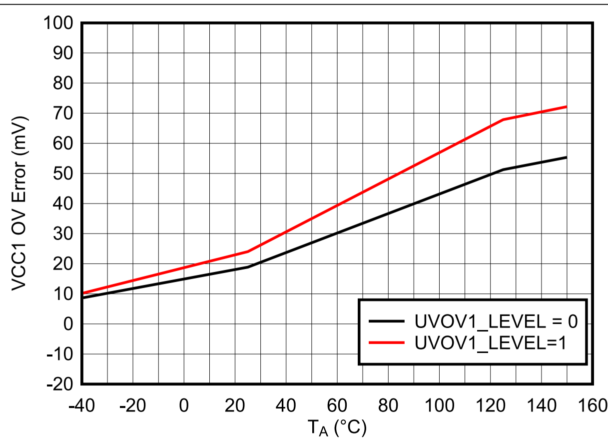


Figure 6-11. VCC1 OVLO Error vs. Temperature

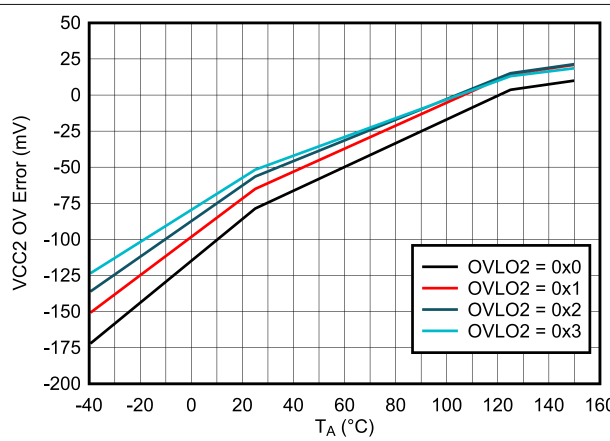


Figure 6-12. VCC2 OVLO Error vs. Temperature

6.11 Typical Characteristics (continued)

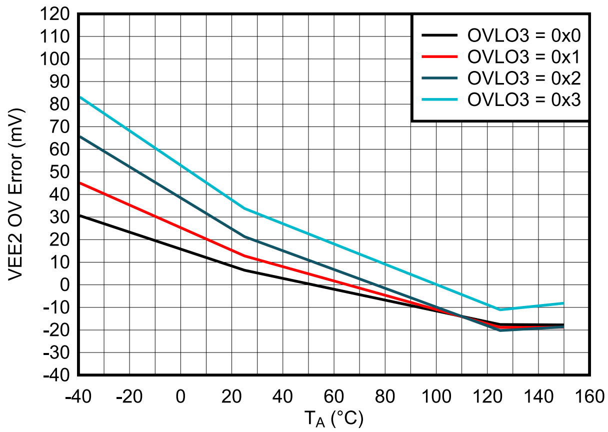


Figure 6-13. VEE2 OVLO Error vs. Temperature

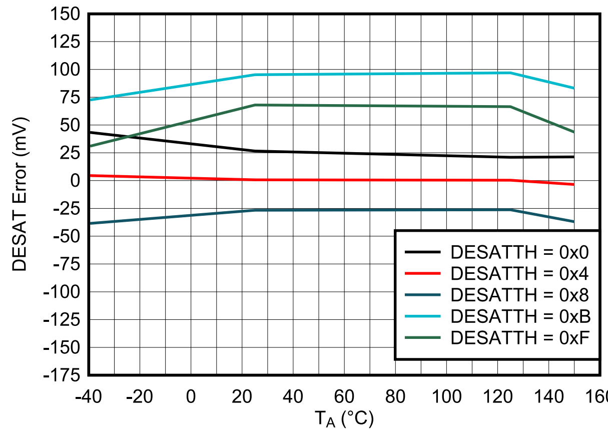


Figure 6-14. DESAT Threshold Error vs. Temperature

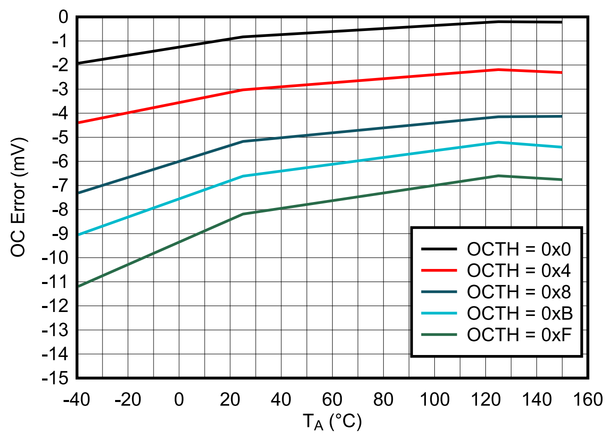


Figure 6-15. OC Threshold Error vs. Temperature

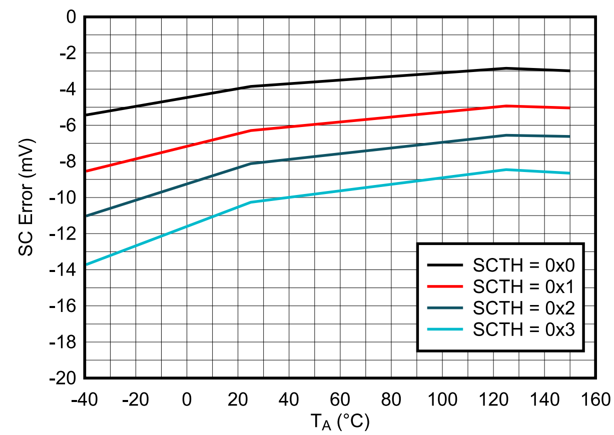


Figure 6-16. SC Threshold Error vs. Temperature

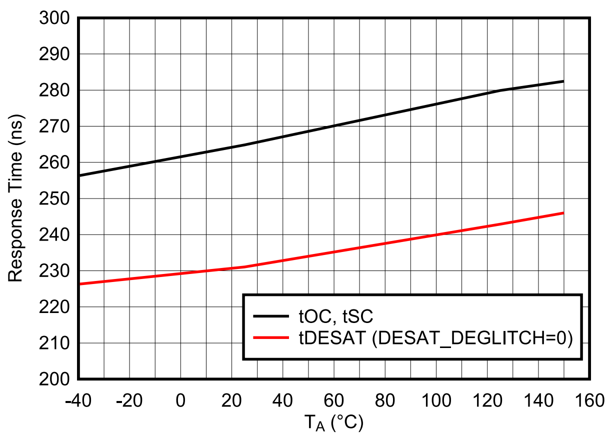


Figure 6-17. Overcurrent Protection Response Time vs. Temperature

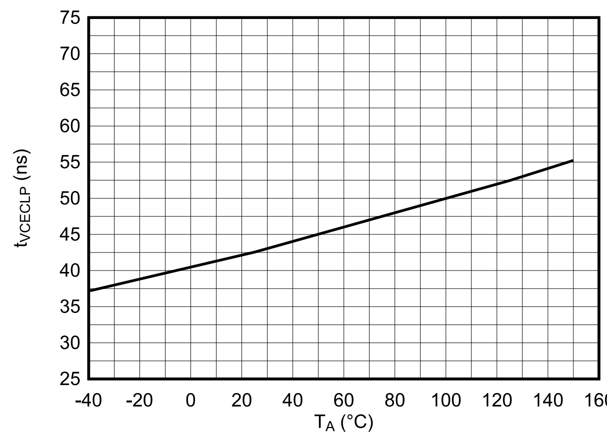


Figure 6-18. VCECLP Intervention Time vs. Temperature

6.11 Typical Characteristics (continued)

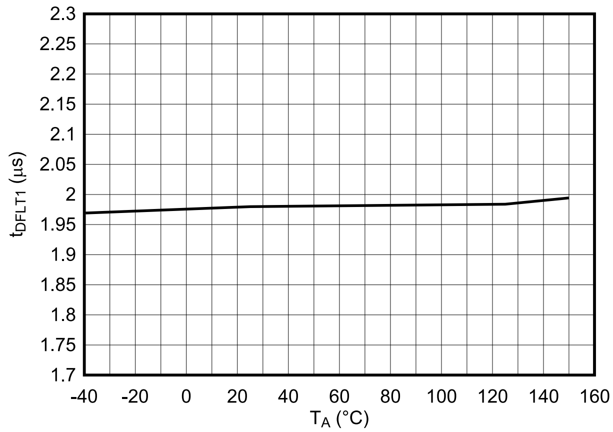


Figure 6-19. nFLT1 Response Time vs Temperature

7 Layout

7.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the device.

7.1.1 Component Placement

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCC1 and GND1 pins and between the VCC2, VEE2 and GND2 pins to support high peak currents when turning on the external power transistor.
- Place the VBST and VREF caps as close to the device as possible.

7.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This decreases the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the diode by the VCC2 bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

7.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC51870's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the high-side and low-side drivers could operate with a DC-link voltage up to 1000 VDC, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

7.1.4 Thermal Considerations

- The power dissipated by the device is directly proportional to the drive voltage, heavy capacitive loading, and/or high switching frequency. Proper PCB layout helps dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VCC2 and VEE2 is recommended, with priority on maximizing the connection to VEE2. However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VCC2 and VEE2 to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

7.2 Layout Example

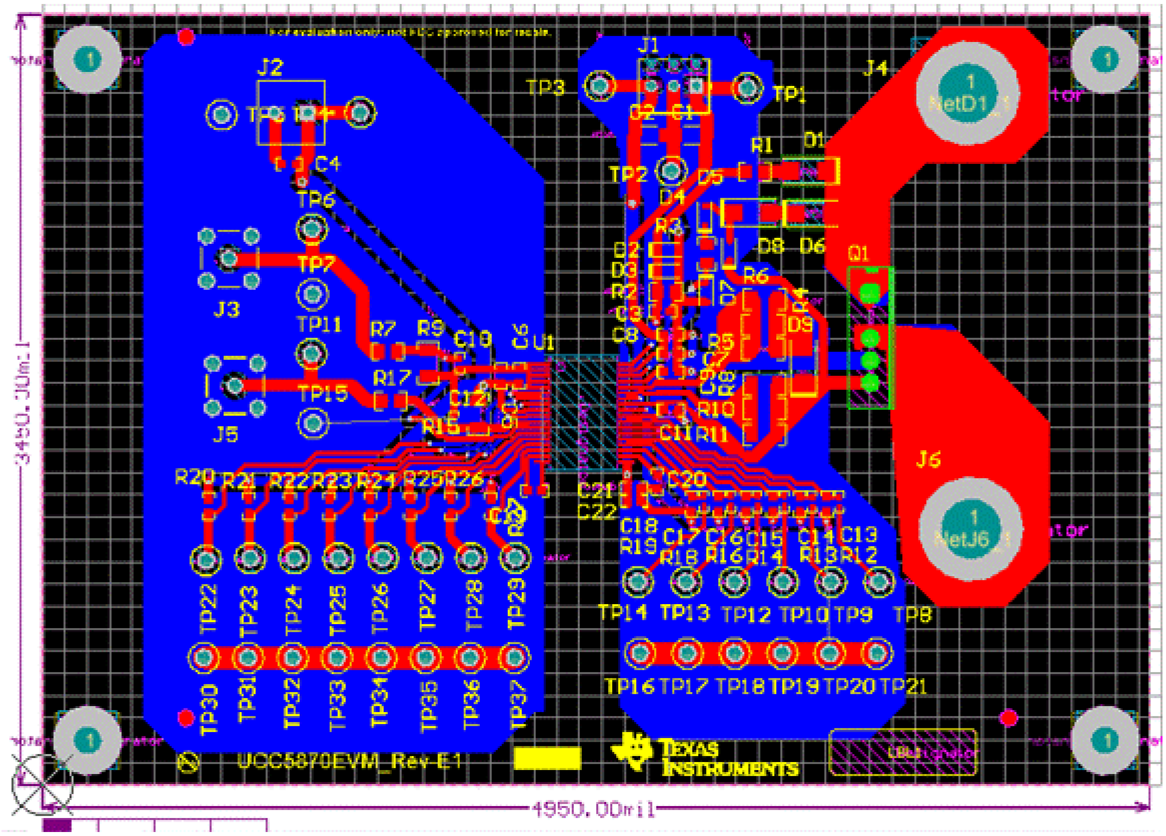


Figure 7-1. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*
- *Isolation Glossary*
- Documentation available to aid ISO 26262 system design up to ASIL D

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5871QDWJRQ1	ACTIVE	SSOP	DWJ	36	750	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5871Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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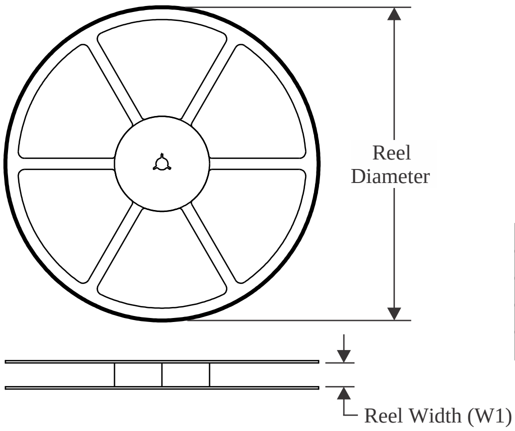
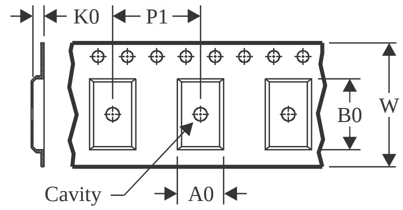
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

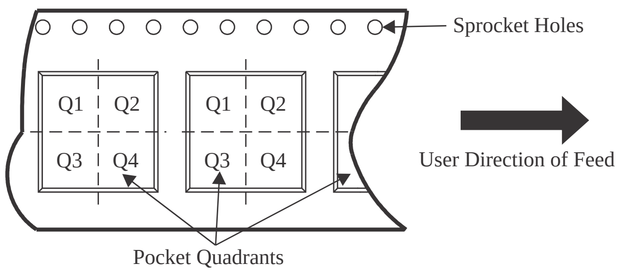


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

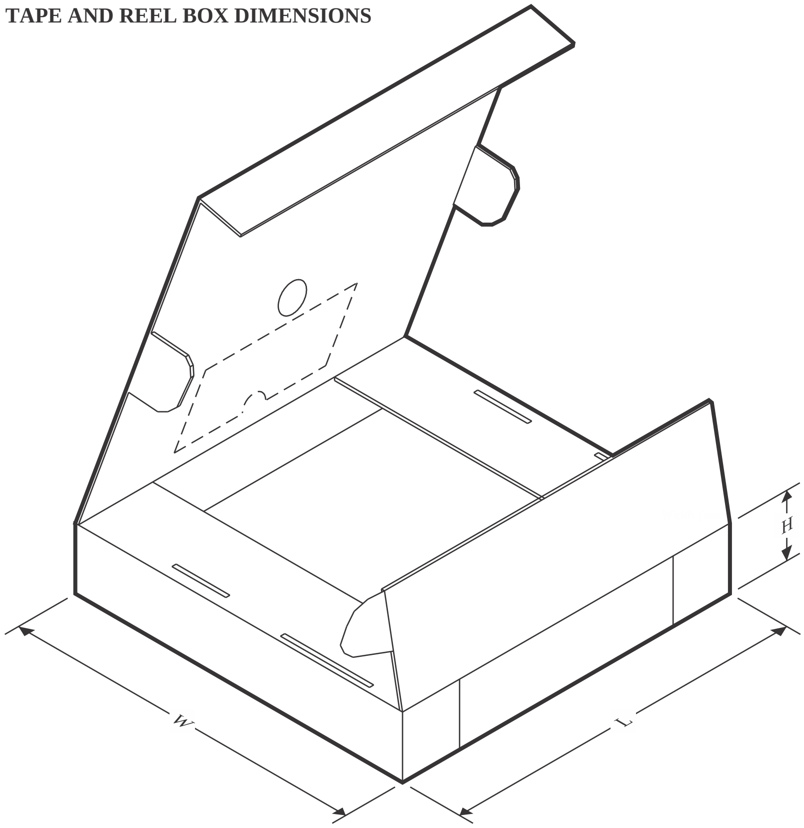
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

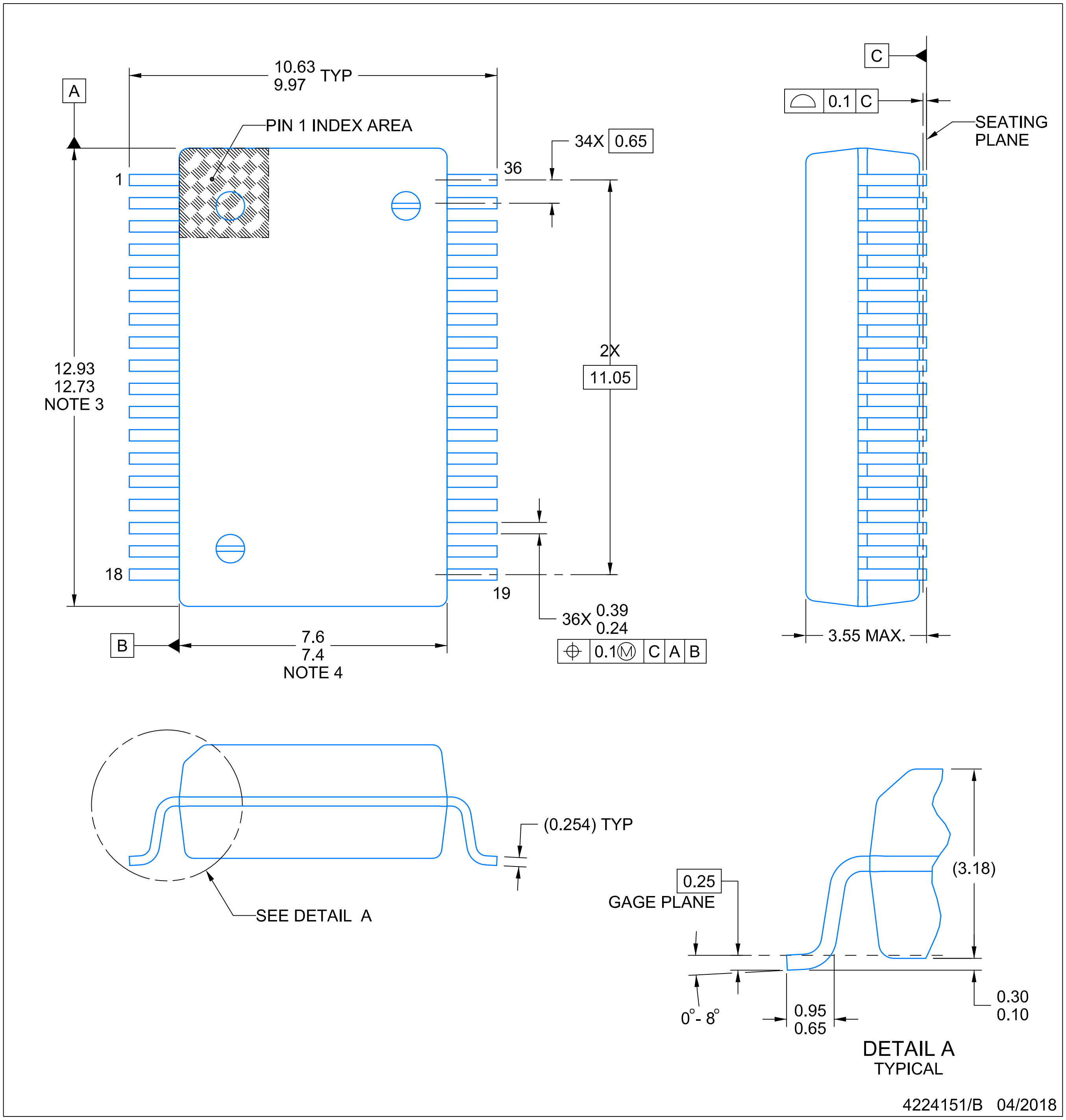
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5871QDWJRQ1	SSOP	DWJ	36	750	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



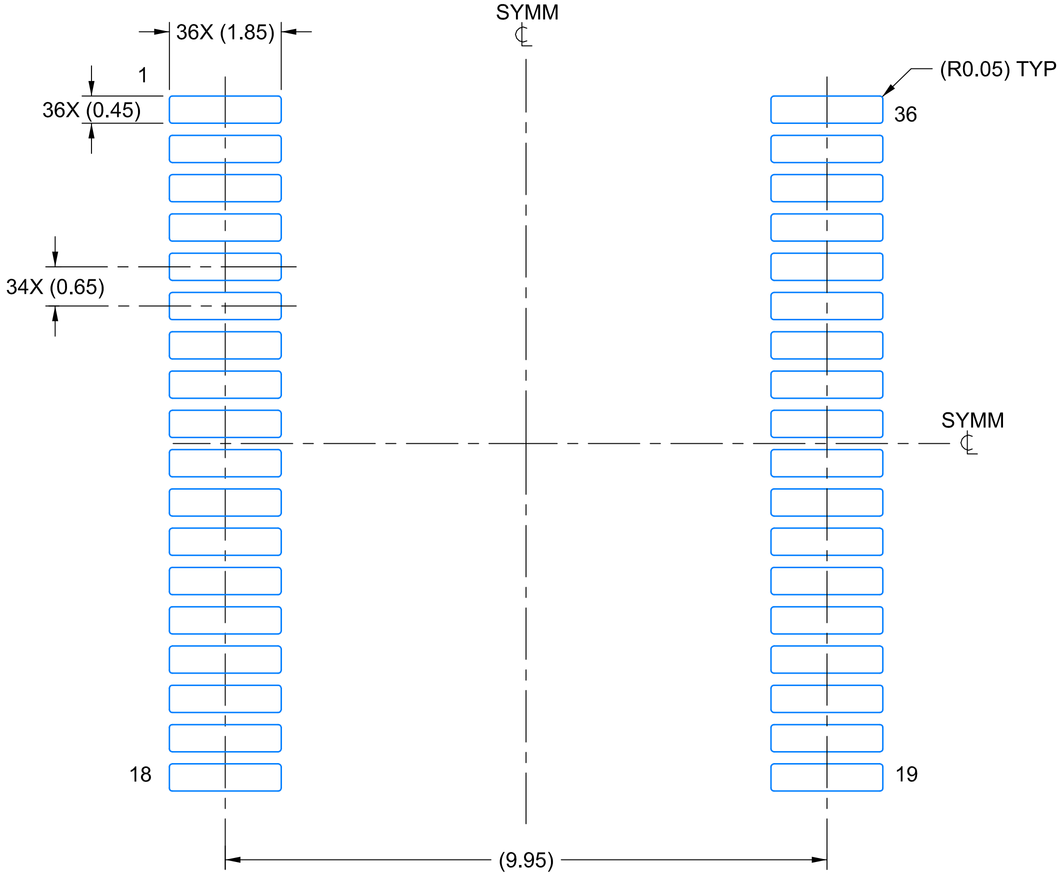
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5871QDWJRQ1	SSOP	DWJ	36	750	350.0	350.0	43.0

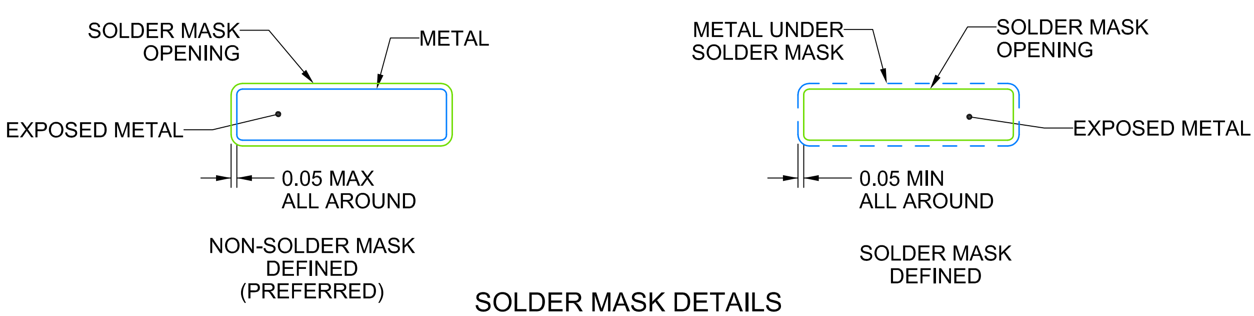


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

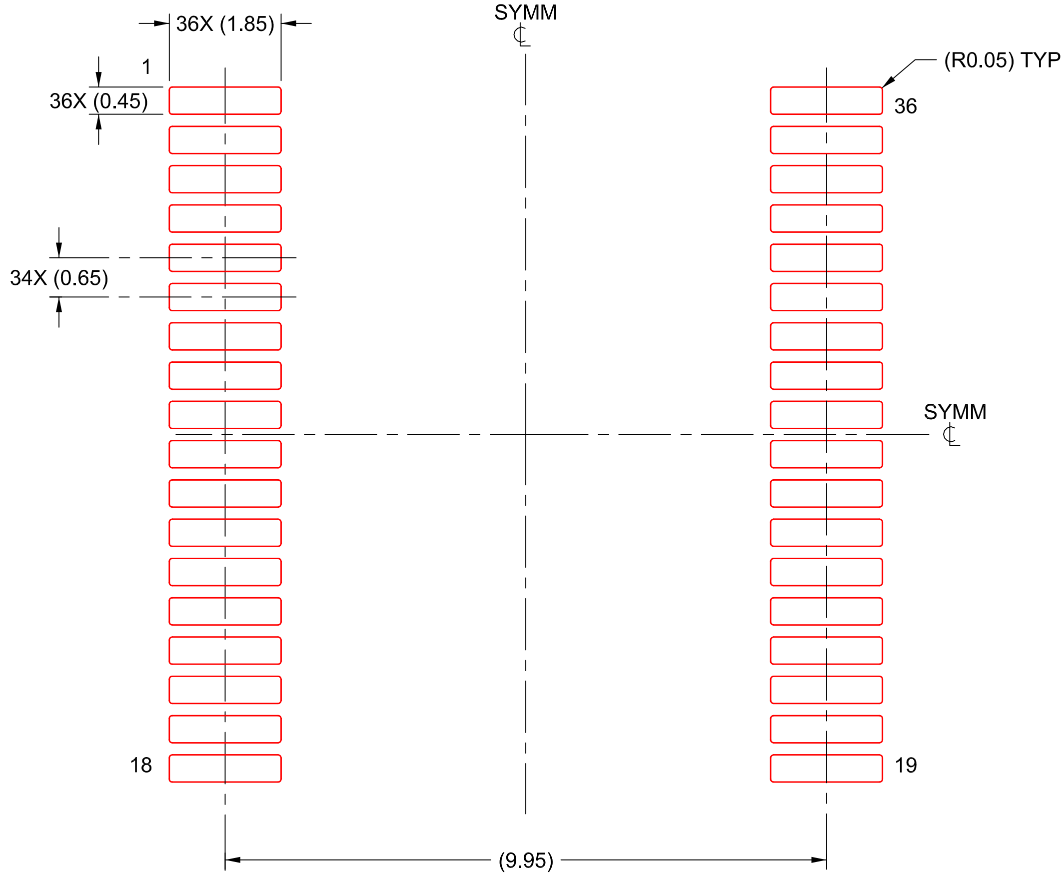


SOLDER MASK DETAILS

4224151/B 04/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4224151/B 04/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265