Application Brief **Optimizing Strain Gauge Accuracy With INA851 vs. Discrete Design**



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This application brief shares a compact integrated design analog front-end using the fully-differential output INA851, and share the benefits and tradeoffs compared to a discrete design consisting of a precision dual operation amplifier (op-amp), OPA2210, and a fully differential amplifier, THP210. The amplifier front-end intrinsic error analysis of each circuit is presented, by measuring an input signal source consisting of a Wheatstone bridge cell with a full scale of ±30mV while configuring the instrumentation amplifier on a gain of approximately 119.8 V/V.

The resistive strain gauge is one of the most popular sensors used to measure strain or force applied an object. The amount of force or stress in the object can be inferred from the change in the sensor resistance as the object is stretched or compressed. The gauge factor of a strain gauge is the ratio of relative change in electrical resistance to the mechanical strain. The gauge factor of these sensors can vary depending on the strain gauge material or the type of strain sensor used. Depending on the gauge sensitivity and excitation voltage, many of these bridge sensors provide small full-scale signals in the few tens of millivolt range and hence require to interface with high-resolution ADCs. A strain gauge measurement system often consists of a Wheatstone bridge, an instrumentation amplifier gain stage, and a buffer stage that drives an Analog to Digital Converter (ADC). Most high-resolution ADCs, 18-bit and above resolution, implement fully-differential inputs; fully differential systems provide advantages such as increased immunity to extrinsic noise and twice the dynamic range compared to single-ended designs.

TI's newest differential output instrumentation amplifier, the INA851, incorporates a high precision, low noise, differential input gain stage and a fully differential amplifier output stage into a single chip design. The current-feedback input stage front-end provides ultra-low noise [3.37 nV/ \sqrt{Hz} at a gain of 120 V/V], low offset voltage [10 μ V (typ)], and drift [0.1 μ V/°C (typ)]. The input stage offers overvoltage protection up to ±40 V beyond the supply rails. The INA851 requires only a single external precision resistor to set the gain. The integrated four-resistor fully differential output stage benefits from the internal ratiometric resistors, providing low gain error and gain error drift performance. The INA851 can shift the common-mode voltage to the level required by the subsequent ADC. The output stage is designed for driving directly high-resolution ADCs supporting sampling rates up to 1 MSPS without requiring an additional buffer amplifier stage or a single-ended to differential conversion circuit. Figure 1 shows the INA851 strain gauge measurement circuit.



Figure 1. INA851 Strain Gauge Measurement Circuit



In an equivalent discrete design, the Wheatstone bridge is connected to an OPA2210, dual super-beta op-amp connected in a differential input amplifier configuration, followed by a fully differential amplifier, the THP210, which drives the ADC. The complete circuit requires seven high-precision, low-drift resistors, R1-R7. Figure 2 shows the OPA2210-THP210 strain gauge measurement circuit.





Both circuits are designed for this sensor, each providing different tradeoffs. The integrated INA851 design simplifies the design process, decreasing the overall design size and cost while maintaining high-precision performance. In contrast, the discrete design can provide outstanding performance at a higher footprint and higher cost when selecting high-precision, low-drift or ratio metrically matched resistors.

Overall, the design process of the integrated INA851 design is much simpler, requiring only one external gain setting resistor, while the discrete design requires seven high-precision resistors.

The total system design size also benefits from the integrated INA851 design by resulting in an area of 137.16 mm² compared to the OPA2210-THP210 discrete design size of 255.6 mm², decreasing the total amount of space required on a board to implement the analog front end by 46%. The lower number of components needed for the integrated design also decreases the cost of the bill of materials. The integrated INA851 design can cost an average of 30% less than the OPA2210-THP210 discrete design, with prices varying based on the resistor tolerance used. Figure 3 and Table 1 show an area and cost comparison of the INA851 design vs the OPA2210-THP210 discrete circuit.



Figure 3. Estimated PCB area, INA851 vs OPA2210-THP210



	Input stage	Differential Stage	Precision Resistors	Total Estimated Cost	Precision Resistors	Total Estimated Cost
Integrated design	INA851		1 - 0.1%, 15 ppm/°C	\$4.12 ⁽¹⁾	1 - 0.01%, 5 ppm/°C	\$4.52 ⁽¹⁾
Discrete design	OPA2210	THP210	7 - 0.1%, 15 ppm/°C	\$5.75 ⁽¹⁾	7 - 0.01%, 5 ppm/°C	\$6.74 ⁽¹⁾

Table 1. Estimated Cost, INA851 vs OPA2210-THP210

(1) Based on 2023 cost estimates, 5-k volumes

When evaluating the performance of the two systems, it is essential to note that the noise and offset errors of the first input instrumentation amplifier gain stage will dominate; thus, the best practice is to place most of the gain in the first stage for best accuracy and noise performance. For this reason, it is critical to use a high-performing device for the first input stage. The OPA2210 in the discrete design is a low-offset, ultra-low offset drift device. The THP210 is a precision FDA offering ultra-low offset and low drift. Both devices are built on TI's precision, super-beta, complementary bipolar semiconductor process, which offers ultra-low flicker noise, providing a direct benefit to low-noise, low-drift measurements.

The gain error and gain drift performance of the discrete design is highly dependent on the accuracy and matching of the OPA2210 input stage gain resistors (R1-R3) and the second stage FDA gain resistors (R5-R7). The INA851 provides a clear benefit incorporating a ratio metrically matched gain resistor network, providing low gain error, gain error drift, and high CMRR performance requiring a single external precision resistor. When using 0.1% tolerance, 15 ppm/°C drift resistors, the INA851 provides better accuracy than the discrete design. Figure 4 shows a plot of the referred-to-input (RTI) error in microvolts of the estimated accuracy of each circuit when using 0.1% tolerance 15 ppm/°C drift resistors.





Gain = 119.8 V/V; Resistors: 0.1%, 15 ppm/°C. Temp Range: 25°C ±60°C



When choosing higher-performance resistors with 0.01% tolerance and a temperature coefficient of 5 ppm/°C, the OPA2210-THP210 discrete design can offer the most accurate design with a cost and area tradeoff. Figure 5 plots the estimated RTI error in microvolts for both circuits using 0.01% tolerance, 5 ppm/°C drift resistors.





Gain = 119.81 V/V; Resistors: 0.01%, 5ppm/°C. Temp Range: 25°C ±60°C

Table 2 shows the typical estimated errors of the INA851 versus the discrete THP210-OPA2210 design when using different tolerance resistors. The table shows the total error as a function of the root-sum-of -squares of the typical device specifications and the estimated worst-case error as a function of the maximum specifications. The detailed error analysis calculations for Table 2 are shown on the Estimated DC Accuracy Calculations section of this document.

Circuit	Resistor Specification	Tota Error RTI (μV, Typical)	Total Error RTI (µV, Maximum)	% Typical Error of 30 mV Full Scale	% Maximum Error of 30 mV Full Scale
INA851	0.10%, 15 ppm/°C	54.3	191.8	0.18	0.64
INA851	0.01%, 5 ppm/°C	48.6	177.6	0.16	0.59
OPA2210-THP210	0.10%, 15 ppm/°C	75.0	239.3	0.25	0.80
OPA2210-THP210	0.01%, 5 ppm/°C	24.2	110.4	0.08	0.37

Table 2. INA851 vs OPA2210-THP210 Calculated DC Accuracy



Estimated DC Accuracy Calculations

Table 3 shows an example of the INA851 estimated DC accuracy calculations. This calculation uses the maximum INA851 data sheet specifications and maximum resistor tolerances to yield an estimate of the worst case uncalibrated DC accuracy. The typical estimated accuracy is calculated using typical INA851 performance specifications. The typical error analysis assumes 1/3 of the resistor tolerance specification (R_{TOL}) on a Gaussian resistor distribution, with the center at the nominal value and the specified tolerance at ±3 standard deviations.

Error Source	Error Calculation	Spec (Max)	Error RΠ (μV)	mV FS
Absolute accuracy at 25 °	C			
Input stage offset voltage V _{OSI}	V _{OSI}	35 µV	35.0	0.12
FDA output stage offset voltage V _{OSO}	$\frac{V_{OSO}(GOUT = 1)}{G_{IN}}, G_{IN} = 119.8 V/V$	650 μV	5.4	0.02
Calculated total input referred offset V _{OS_TOTAL}	$\sqrt{V_{OSI}^2 + \left(\frac{V_{OSO}(GOUT = 1)}{G_{IN}}\right)^2}$, $G_{IN} = 119.8 \text{ V/V}$		35.4	0.12
Common-mode rejection ratio CMRR _{ERROR}	$10 \frac{V_{CM}}{\frac{CMRR}{20}}, V_{CM} = 2.048 V$	120 dB	2.05	0.01
Gain error from INA851 GE _{INA}	$GE_{INA} \% \times FullScale_{Sensor}$	0.20 %	60.0	0.20
Gain error from RG ext. resistor 0.1% GE _{Resistor}	$R_{TOL}\% \times FullScale_{Sensor}$	0.10 %	30.0	0.10
Calculated total gain error GE _{TOTAL}	$\sqrt{{\rm GE}_{\rm INA}^2 + {\rm GE}_{\rm Resistor}^2}^2$		67.1	0.22
Total error at 25°C (RSS)	$\sqrt{V_{OS}_{TOTAL}^2 + GE_{TOTAL}^2 + CMRR_{ERROR}^2}$		75.9	0.25
Calculated max drift error	with ± 60 °C temperature change			
Input stage offset voltage drift V _{OSI Drift}	V _{OSI_Drift} •∆T	0.3 µV/°C	18.0	0.06
FDA output stage offset voltage drift V _{OSO_Drift} (RTI)	$\frac{V_{OSO_Drift(GOUT = 1)}}{G_{IN}} \bullet \Delta T, G_{IN} = 119.8 \text{ V/V}$	15 µV/°C	7.5	0.03
Calculated total RTI offset drift V _{OS_Drift_TOTAL}	$\sqrt{V_{OSI_Drift}^2 + \left(\frac{V_{OSO_Drift}(GOUT = 1)}{G_{IN}}\right)^2}$, $G_{IN} = 119.8 \text{ V/V}$		19.5	
Gain error drift from INA851	$\frac{\text{GE}_{\text{INA}}\text{Drift}\text{PPM} \bullet \Delta T}{10^4} \% \text{*FullScale}_{\text{Sensor}}$	35 ppm/°C	105.0	0.21
Gain error Drift from RG ext. resistor	$\frac{\text{R}_{G_Drift_PPM} \bullet \Delta T}{10^4} \% \text{FullScale}_{\text{Sensor}}$	15 ppm/°C	45.0	0.09
Calculated total	$\sqrt{V_{OS}_{Drift}_{TOTAL}^2 + GE_{INA}_{Drift}^2 + RG_{Drift}^2}$		115.9	0.39

Table 3. INA851: Estimated DC Accuracy Calculations From Max Spec With 0.1%, 15 ppm/°C Resistors

temperature drift error Calculated total absolute

error

191.8

0.64

5

Total error at 25°C + Total temp drift error



Table 4 shows an example of the OPA2210-THP210 discrete design estimated DC error calculations. This calculation uses the maximum device specifications, and resistor tolerances (R_{TOL}) to yield an estimate of the worst case uncalibrated DC accuracy. The typical error is calculated using typical specifications and 1/3 of the resistor tolerance. The typical error analysis assumes a Gaussian resistor distribution, with the center at the nominal value, and the specified resistor tolerance at ±3 standard deviations. Alternatively, a PSPICE-FOR-TI Monte Carlo simulation using R_{TOL} provides an estimate of the circuit gain error.

Table 4. OPA2210-THP210: Estimated DC Accuracy Calculations From Max Spec with 0.1%,	15 pr	pm/°C
resistors		

Error Source	e Error Calculation		Error RTI (µV)	% Error of 30 mV Full-Scale		
Absolute accuracy at 25 °C						
Input stage offset voltage V _{OS_Input}	$\sqrt{V_{OS_OPA_A}^2 + V_{OS_OPA_B}^2}$	35 µV	49.5	0.16		
FDA output stage offset voltage V _{OS_FDA}	$\frac{V_{OS}FDA}{G_{IN}}, G_{IN} = 119.8V/V$	40 µV	0.3	0.001		
Calculated total input referred offset V _{OS_TOTAL}	$\sqrt{V_{OS_Input}^2 + \left(\frac{V_{OS_FDA}}{G_{IN}}\right)^2}$, $G_{IN} = 119.8V/V$		49.5	0.16		
Common-mode rejection ratio (dB) CMRR based on FDA resistor mismatch	$CMRR(dB) = 20 \times LOG\left(\frac{1 + R_F/R_G}{4 \times R_{TOL}\%/100}\right), R_F = R_G = 2k\Omega$	Calculated CMRR (dB) = 53.98dB) = 53.98dB		
Common Mode Rejection Ratio CMRR _{ERROR}	$\frac{\left(\frac{V_{CM}}{10^{CMRR(dB) / 20}}\right)}{G_{IN}}, G_{IN} = 119.8 \text{ V/V}, V_{CM} = 2.048 \text{ V}$		37.6	0.13		
Gain Error from Input Stage GE _{Input}	$2 \times R_{TOL}\% \times FullScale_{Sensor}$	0.10 %	60.0	0.20		
Gain Error from FDA Stage GE _{FDA}	$2 \times R_{TOL}\% \times FullScale_{Sensor}$	0.10 %	60.0	0.20		
Calculated total gain error GE _{Total}	$\sqrt{{\rm GE}_{\rm Input}^2 + {\rm GE}_{\rm FDA}^2}$		84.82	0.28		
Total error at 25°C (RSS)	$\sqrt{{V_{OS}}^2 + {GE_{TOTAL}}^2 + {CMRR_{ERROR}}^2}$		105.2	0.35		
Calculated max drift error	with ± 60 °C temperature change					
Input stage offset voltage drift Vos Input Drift	$\sqrt{\left(V_{OS_{OPA},A_{Drift} \times \Delta T\right)^{2} + \left(V_{OS_{OPA},B_{Drift} \times \Delta T\right)^{2}}$	0.5 µV/°C	42.4	0.14		
FDA output stage offset voltage drift V _{OS FDA Drift} (RTI)	$\frac{V_{OS_FDA_Drift}}{G_{IN}} \times \Delta T, \ G_{IN} = 119.8 \ V/V$	0.35 µV/°C	0.2	0.001		
Calculated total RTI offset drift V _{OS_Drift_TOTAL}	$\sqrt{2 \times \left(V_{OS_OPA_Drift} \times \Delta T\right)^2 + \left(\frac{V_{OS_FDA_Drift}}{G_{IN}} \times \Delta T\right)^2}$		42.4			
Gain error drift from input stage GE _{Input_Drift}	$\frac{2 \times R_{OPA_Drift_PPM} \times \Delta T}{10^4} \% \times FullScale_{Sensor}$	15 ppm/°C	90.0	0.36		
Gain error drift from input stage GE _{FDA_Drift}	$\frac{2 \times R_{FDA_Drift_PPM} \times \Delta T}{10^4} \% \times FullScale_{Sensor}$	15 ppm/°C	90.0	0.36		
Calculated total temperature drift error	$\sqrt{V_{OS_Drift_TOTAL}^2 + GE_{Input_Drift}^2 + GE_{FDA_Drift}^2}$		134.2	0.45		
Calculated total absolute error	Total error at 25°C + Total temp drift error		239.3	0.80		



Summary

The INA851 integrated design can provide a compact, low-cost, compelling design offering high-precision performance. Even higher performance can be achieved with the discrete OPA2210-THP210 design when using high-precision, low-drift, matched external resistors at a higher cost.

The preceding discussion presents the design tradeoffs and performance difference between an integrated fully-differential output instrumentation amplifier design using the INA851 versus a discrete design using the OPA2210 and THP210 with precision discrete resistors. This document provides the information to assist the design engineer in implementing a design per the cost and performance requirements.

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