TEXAS INSTRUMENTS

Designing with the TL1454 PWM Controller

User's Guide

1998

Mixed Signal Products

Texas Instruments

Printed in U.S.A.
11/98

SLVU012

Designing with the TL1454 PWM Controller User's Guide

Literature Number: SLVU012
November 1998

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Preface

Read This First

About This Manual

This user's guide reviews the design of two 500 kHz dc-to-dc converters. The first is a 3.3-V, 1.5-A buck converter, and the other is a 12-V, 0.2-A boost converter. Both converters operate from a 4.5-V to 7-V power source. The user's guide also provides a schematic, parts list, measured performance data, and typical waveforms.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 Designing with the TL1454 PWM Controller
- Chapter 2 3.3-V Step-Down Regulator
- Chapter 3 12-V Step-Up Regulator
- Chapter 4 Test Results
- Chapter 5 EVM Documentation

Related Documentation From Texas Instruments

- TL1454 Dual-Channel PWM controller data sheet (literature number SLVS086)
- TPS1110 Single P-Channel Logic Level MOSFETs data sheet (literature number SLVS100)
- Designing with the TL5001 (literature number SLVA034A)

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Chapter 1

Designing with the TL1454 PWM Controller

With the trend in electronics of downsizing, both in hardware and power, the pulse-width-modulation (PWM) method is frequently used in power supply circuits. High-frequency operation enables an increase in efficiency and a reduction in size and cost of switching power supplies.

The TL1454 is a dual-channel PWM control IC that incorporates all the functions required to control two high-frequency dc-to-dc converters. The TL1454 internally provides undervoltage lockout, short-circuit protection, independent dead time controls, adjustable oscillator, voltage reference, error amplifiers, and drivers for power MOSFET switches in a compact 16-pin package.

This user's guide reviews the design of two 500-kHz, dc-to-dc converters, both operating from a 4.5-V to 7-V power source. This user's guide provides a schematic diagram, a parts list, performance data, and typical waveforms. A detailed description of the TL1454 is found in the *Power Supply Circuits Data Book*, Texas Instruments Literature Number SLVD002. A more detailed explanation of step-down converter design and component selection is available in a related document, *Designing with the TL5001*, Texas Instruments Literature Number SLVA034A.

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1.1 Introduction

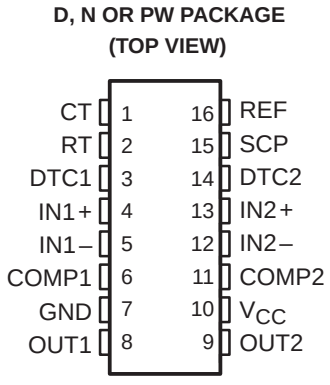
The dual dc-to-dc converter provides a simple power supply solution for applications requiring two independently regulated output voltages, where one of the required voltages is less than the input supply and the other output voltage is higher than the input. The user will save in cost and board space because the power supply and control functions are incorporated in a single IC.

Design simplicity and low component count make step-down (buck) converters popular solutions where the regulated output voltage is lower than the input and isolation is not a requirement. Similarly, step-up (boost) converters are popular solutions where the regulated output voltage is higher than the input and isolation is not a requirement. The TL1454 controller provides the following features:

- 3.6-V to 20-V operating input-voltage range
- 50-kHz to 2-MHz oscillator-frequency range
- 3.5-mA typical current consumption
- MOSFET drive outputs for each channel
- 1.25-V reference voltage
- Input undervoltage lock out protection
- Short circuit protection
- 0% to 100% dead time adjustment range

The TL1454 is available in the D, N, or PW package. The package layout is shown in Figure 1–1.

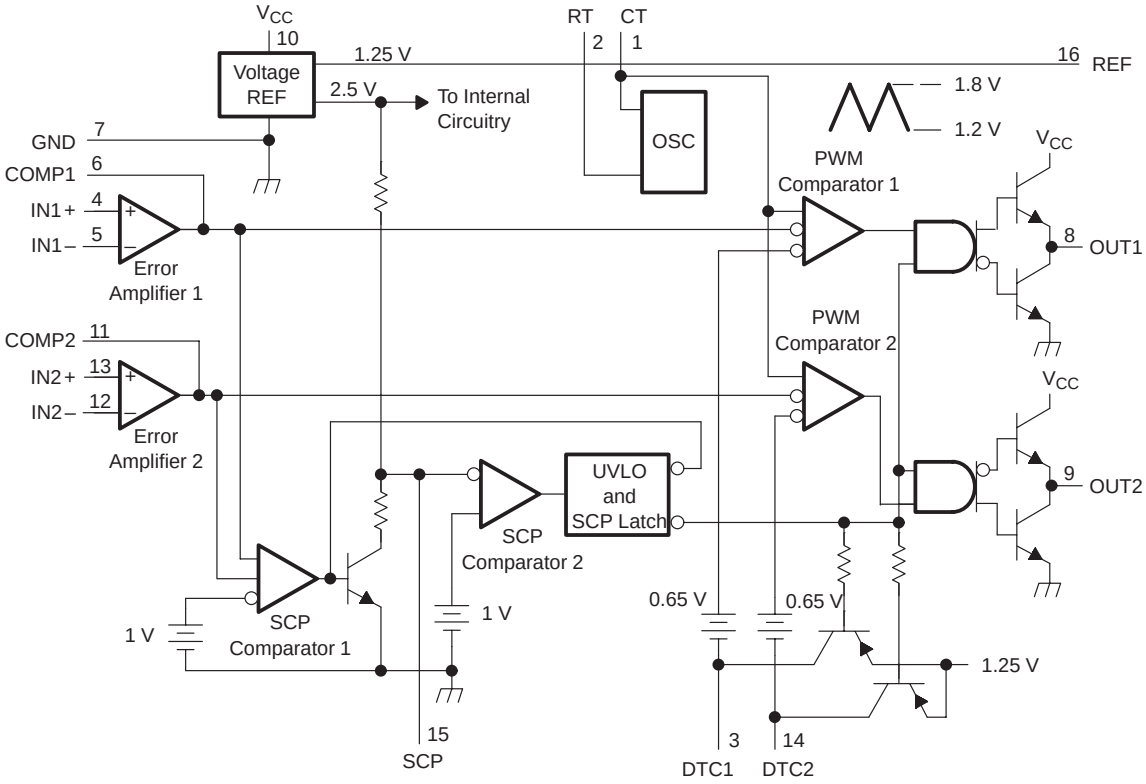
Figure 1–1. Package Layout



A functional block diagram of the TL1454 is shown in Figure 1–2. In the TL1454 controller, channel 1 is configured to drive n-channel MOSFETs in boost or flyback converters, and channel 2 is configured to drive p-channel MOSFETs in step-down or inverting converters. The operating frequency is set with an external resistor and an external capacitor, and dead time for each channel is

continuously adjustable from 0% to 100% duty cycle with a resistive divider network. Adding a capacitor to the dead-time control (DTC) network provides a soft start capability. The error-amplifier common-mode input range includes ground, which allows the TL1454 to function in ground-sensing battery chargers as well as voltage converters.

Figure 1–2. TL1454 Functional Block Diagram



1.2 Specification Summary

When used in the EVM board, the two converter designs in this user's guide meet the performance specifications summarized in Table 1–1. Since the design requires no input-to-output isolation, a discontinuous-mode, step-up (boost) converter is used for the 12-V output. A continuous mode, step-down (buck) converter is used for the 3.3-V output. Both converters operate at a frequency of 500 kHz. In Table 1–1, V_{O1} is the 12-V boost converter output and is controlled by channel 1 of the TL1454. V_{O2} is the 3.3-V buck converter output and is controlled by channel 2 of the TL1454.

Table 1–1. Specification Summary

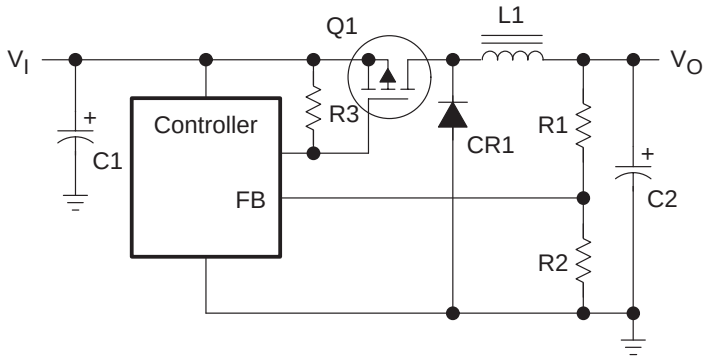
	MIN	TYP	MAX	UNITS
Input voltage range	4.5		7	V
Ambient temperature range, T_A	0		55	°C
Efficiency	80%			
Output voltage, V_{O1}		12		V
Output current, I_{O1}	0		200	mA
Output ripple voltage, $V_{O1(PP)}$		120		mV
Regulation (V_{O1})		±4%		
Output voltage, V_{O2}		3.3		V
Output current, I_{O2}	0		1.5	A
Output ripple voltage, $V_{O2(PP)}$		33		mV
Regulation (V_{O2})		±4%		

The design uses surface-mount packages wherever feasible to minimize size and simplify assembly.

1.3 Buck Regulator Circuit Operation

The basic circuit can be represented by an output filter, a controller, and a MOSFET switch and commutating diode providing the switching function. The schematic diagram in Figure 1–3 provides a simplified circuit representation of the buck converter.

Figure 1–3. Typical Buck Converter Schematic Diagram

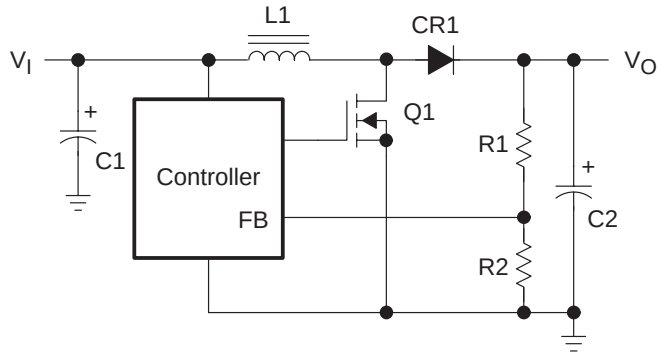


The buck converter passes a duty-cycle-modulated waveform through a low-pass output filter (L1, C2). A controller senses the output voltage, compares it to an internal reference voltage, and adjusts the duty cycle of the power switch (Q1) to maintain the desired output voltage. A commutating diode (CR1) maintains continuous current through the inductor when the power switch is turned off.

1.4 Boost Regulator Circuit Operation

The boost converter circuit can simply be represented by an output filter, a controller, and a MOSFET switch and diode providing the switching function. Figure 1–4 provides a simplified circuit representation of the boost converter.

Figure 1–4. Typical Boost Converter Schematic Diagram



The power switch (Q1) turns on to apply the input voltage across the inductor (L1) storing energy in the inductor. When Q1 turns off, the energy in L1 is delivered to the load and output capacitor through the output diode CR1. The controller senses the output voltage, compares it to an internal reference voltage, and adjusts the duty cycle of the power switch (Q1) to maintain the desired output voltage.

1.5 Controller Functions

The following functions set by the controller govern the operation of both converters. Reference designators refer to components on the Evaluation Module TL1454EVM-085 (EVM), and a schematic for the EVM is given in Figure 5–1.

1.5.1 Oscillator Frequency

Using Figure 6 in the TL1454 data sheet, choose R4 = 10 kΩ and C5 = 120 pF to set the oscillator frequency to f_S = 500 kHz (T_S = 2 μs). R4 is connected between the RT terminal and ground, and C5 is connected between the CT terminal and ground. Tight tolerance, temperature stable components are recommended for both R4 and C5 to minimize the oscillator frequency variation. R4 is a 1%, metal-film device and C5 is a 10%, or better, NPO ceramic.

1.5.2 Short Circuit Protection (SCP) Timing

In normal operation, the TL1454 SCP terminal (15) is held low at approximately 185 mV. If the switching power supply becomes short-circuited, the protection-enable capacitor (C7) connected externally from the SCP terminal to ground will begin charging. If the voltage across C7 reaches 1 V, the SCP latch is activated and the converter is shut down. The value of C7 is chosen to insure that SCP will not trip during start-up. Selecting a time constant 10 times the output start-up rise time will insure that the short-circuit protection circuit is disabled long enough for the output to come into regulation. The time constant is selected to be 120 ms. The expression to calculate C7 is:

$$C7 = \frac{t_{PE}}{80300} = \frac{0.120}{80300} = 1.49\ \mu F \rightarrow 1.5\ \mu F$$

Chapter 2

3.3-V Step-Down Regulator

The following sections describe the design procedures for this 3.3-V step-down (buck) regulator. Selection and/or design guidelines for the external power components are given. As stated in the TL1454 data sheet, channel 2 of the controller is configured to control and provide drive signals for a step-down regulator using a p-channel power MOSFET.

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2.1 Duty-Cycle Estimates

Before starting the detailed design, the designer should estimate the duty cycle (D) for various input voltages. Duty cycle is the ratio of the power-switch conduction time to the period of the operating frequency. The duty cycle for a step-down converter operating in continuous-mode is stated as:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where:

V_d = Catch rectifier conduction voltage (assume 0.6 V)
V_{sat} = Power switch conduction voltage (assume 0.1 V).

The duty cycles for V_I = 4.5 V, 5 V, and 7 V are 0.89, 0.80, and 0.57, respectively.

2.2 Output Inductor

Choose the inductance value to maintain continuous-mode operation down to approximately 10% to 15% of the rated output current. The average of the inductor current is equal to the output current. Since inductor current is triangular in shape, the peak-to-peak value of the current for a load of 10% of rated load will be:

$$\Delta I_{L2} = 2(0.1)\left(I_{O(Max)}\right) = 2(0.1)\ (1.5) = 0.3\ A_{(p\text{-}p)}$$

Worst case ripple current occurs at maximum input voltage. Calculate the inductor value using:

$$L2 = \frac{\left(V_I - V_{sat} - V_O\right)(D)(t_s)}{\Delta I_{L2}} = \frac{(7 - 0.1 - 3.3)(0.57)\left(2 \times 10^{-6}\right)}{0.3}$$
$$= 14\ \mu H \rightarrow 10\ \mu H$$

Use an inexpensive 10-µH, 0.052-Ω, 2.6-A surface-mount inductor from Sumida (or equivalent) for this design.

2.3 Output Capacitor

Select the output capacitor to limit the output ripple voltage to the level required by the specification (See Table 1–1). The three elements of a capacitor that contribute to ripple are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance. It is necessary to provide a great deal of capacitance to get ESR to acceptable levels. ESL can be a problem at high frequencies. Control ESL by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

Assuming that all the inductor ripple current flows through the filter capacitor and ESR is zero, the capacitance needed to limit the ripple voltage to 33 mV p-p is:

$$C = \frac{\Delta I_{L2}}{\left(8\ f_s \Delta V_O\right)} = \frac{0.3}{8\left(500 \times 10^3\right)\left(33 \times 10^{-3}\right)} = 2.3\ \mu F$$

Assuming that the capacitance is very large and does not contribute to ripple, the ESR needed to limit the ripple to 33 mV p–p is:

$$ESR_{(max)} = \frac{\Delta V_O}{\Delta I_{L2}} = \frac{\left(33 \times 10^{-3}\right)}{0.3} = 110\ m\Omega$$

Capacitor ripple current is seldom a problem in low-voltage converters. However, the following formula calculates the rms ripple current:

$$I_{C\ RMS} = \Delta I_{L2}\frac{\sqrt{3}}{6} = \Delta I_{L2}(0.289) = 0.3(0.289) = 86\ mA_{RMS}$$

The capacitance and ESR requirements are met with a single 10-µF multilayer ceramic capacitor with an ESR less than 10 mΩ.

The output inductor, L2, and the capacitor, C17, make up a very high-Q output filter. In order to reduce the Q of the filter, add a larger electrolytic capacitor, C13, and series resistance, R17, in parallel with C17. This reduces the resonant peaking and slows the phase transition of the output filter. C13 is a 100-µF, 100-mΩ tantalum capacitor from AVX. R17 is made up of four 1-Ω resistors in parallel. The resulting filter response, offset by the gain of the pulse-width modulator and the dc gain of the power stage, is shown as the buck uncompensated loop response in Figure 2–2.

2.4 Power-Stage Design

The power-stage design includes selecting the power switch, the catch rectifier, and the rectifier snubbing network (if needed). Also, the design includes calculating the power dissipations, calculating the junction temperatures, and ensuring that the semiconductors have adequate heatsinking.

2.4.1 Power Switch

The power switch uses a P-channel MOSFET that simplifies the drive circuit design and minimizes component count. To meet the preliminary duty cycle estimate, the MOSFET $r_{DS(on)}$ should be less than 0.1 V ÷ 1.5 A = 67 mΩ with a 5 V gate drive and a drain-to-source breakdown voltage rating appropriate for a 7-V supply. The TPS1110 meets these requirements. It is a –7 V P-channel power MOSFET in an SO-8 package with $r_{DS(on)}$ = 65 mΩ typical at V_{GS} = –4.5 V (The voltages are negative because this is a P-channel MOSFET).

Power dissipation, which includes both conduction and switching losses, is given by:

$$P_D = \left[\left(I_O^2\right)\left(r_{DS(on)}\right)(D)\right] + \left[0.5\left(V_I\right)\left(I_O\right)\left(t_{(r+f)}\right)\left(f_S\right)\right]$$

where $r_{DS(on)}$ is adjusted for junction temperature and $t_{(r+f)}$ = total MOSFET switching time (turn-on and turn-off)

Assuming that the drive circuit is adequate for $t_{(r+f)}$ = 100 ns, and the junction temperature is 100°C with a 55°C ambient, the $r_{DS(on)}$ of the TPS1110 increases approximately 35%.

At 4.5 V input:

$$P_D = \left[\left(1.5^2\right)(1.35 \times 0.065)(0.89)\right] + \left[0.5(4.5)(1.5)\left(0.1 \times 10^{-6}\right)\left(500 \times 10^3\right)\right] = 345\ mW$$

At 7 V input:

$$P_D = \left[\left(1.5^2\right)(1.35 \times 0.065)(0.57)\right] + \left[0.5(7)(1.5)\left(0.1 \times 10^{-6}\right)\left(500 \times 10^3\right)\right] = 375\ mW$$

The junction temperature can be estimated using a value of 100°C/W for the junction-to-ambient thermal impedance, Using the worst case power dissipation from above, the junction temperature is approximately:

$$T_J = T_A + R_{\theta JA} \times P_D = 55 + (100)(0.375) = 93°C$$

The original assumptions turned out to be conservative because the calculated junction temperature is 93°C instead of the assumed 100°C. Also, the worst case for power dissipation occurs at the maximum input voltage in this application but may not be in others. It is recommended to check dissipation at the extreme limits of input voltage to find the worst case.

2.4.2 Catch Rectifier

When the transistor turns off, the catch rectifier conducts and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current capability, low forward voltage drop, and appropriate packaging. Typically, derating a diode to 50% of its current rating will achieve the proper derating of the junction temperature. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low-voltage outputs is usually a Schottky rectifier. CR2 is an SS32 surface-mount Schottky rectifier with a 20-V breakdown voltage and 3-A current rating.

The maximum power dissipation occurs at minimum duty cycle (maximum rectifier conduction time).

$$P_D = \left(V_d\right)\left(I_O\right)(1–D) = (0.5)(1.5)(1–0.57) = 323\ mW$$

Junction temperature for this diode may be estimated using a thermal resistance of 55°C/W (printed circuit board mounted with 0.55″ × 0.55″ copper pad area):

$$T_J = T_A + R_{\theta JA} \times P_D = 55 + (55)(0.323) = 73°C$$

2.4.3 Catch-Rectifier Snubber Network

Step-down converters usually suffer from ringing on the voltage waveform at the node where the power switch, output inductor, and catch-rectifier cathode connect. The ringing, which results from driving parasitic inductances and capacitances with fast rise-time waveforms, ranges in severity from objectionable to unacceptable depending on component selection and printed circuit board layout. An RC snubber damping network in parallel with the catch rectifier is by far the simplest way to minimize or eliminate the problem. Since deleting components from a printed-circuit layout is usually easier than adding them, it is best to include the network in the initial design and delete the components if they prove unnecessary.

The initial design is straightforward, but the printed circuit board layout may require component-value adjustments during the prototype phase. The capacitor value chosen is 2 to 5 times the rectifier junction capacitance; higher values improve the snubbing but dissipate more power. The SS32 has a typical junction capacitance of approximately 500 pF, so a snubber capacitor value should be at least 1000 pF, and *C11* is 1500 pF. Rectifiers normally ring in the range from 1 to 50 MHz. Choose the snubber resistor, *R11*, so that the snubber-capacitor can fully charge during the ringing. So, for a 15-nS ringing time constant, choose *R11* as:

$$R11 = \frac{t_{Ringing}}{3 \times C11} = \frac{15 \times 10^{-9}}{3 \times 1500 \times 10^{-12}} = 3.3\ \Omega \rightarrow 2.7\ \Omega$$

Because the snubber is charged and discharged during each cycle, the power dissipation in *R11* is:

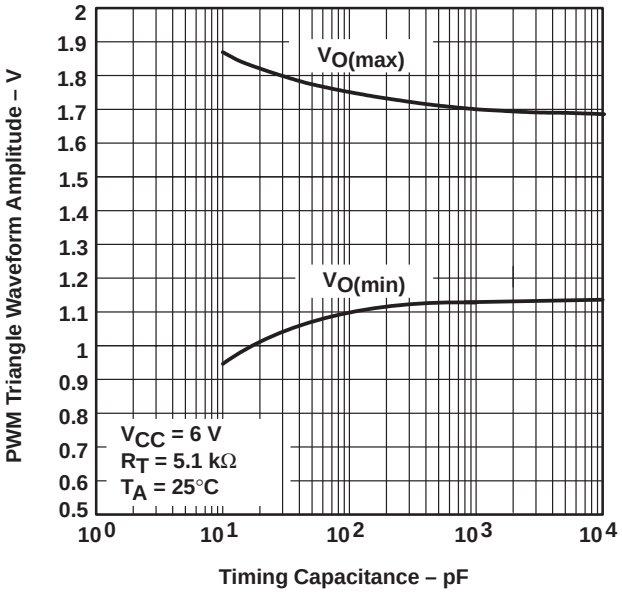
$$P_{R11} = 2(C11)\left(V_I^2\right)\left(\frac{f}{2}\right) = 2\left(1500 \times 10^{-12}\right)\left(7^2\right)\left(\frac{500 \times 10^3}{2}\right) = 37\ mW$$

2.5 Dead-Time Control

Dead-time control provides a minimum period of time during each cycle when the power switch cannot be on: that is, it limits the duty cycle to some value less than 100%. Even though dead-time is not necessary in this application, a small amount of dead time would minimize the surge current that would result from a short circuit while the protection circuit is timing out.

Referring to Figure 2–1 below (Figure 9 in the TL1454 data sheet), for a timing capacitor value of 120 pF, the duty cycle of the power switch is 100% when V_{DT}, the dead-time control voltage, is less than approximately 1.1 V ($V_{O(min)}$) and 0% when V_{DT} is greater than 1.75 V ($V_{O(max)}$).

Figure 2–1. PWM Triangle Wave Amplitude vs. Timing Capacitance



The following expression is used to set V_{DT}, where D = maximum allowed duty cycle:

$$V_{DT} = V_{O(max)} - D\left(V_{O(max)} - V_{O(min)}\right) - 0.65$$

$$V_{DT} = 1.75 - 1(1.75 - 1.1) - 0.65 = 0.45\ V$$

This is the maximum voltage allowed to guarantee 100% duty cycle; grounding DTC2 will suffice for this application.

2.6 Soft-Start Timing

Soft start can be accomplished by adding a capacitor in parallel with the upper dead-time divider resistor. This design has a dead time of 0% which requires no divider. A lower resistor must be added for soft-start timing purposes. This design uses an output rise time of 5 ms. Selecting the lower resistor to be 47 kΩ as recommended in the data sheet, capacitor *C13* can be calculated as:

$$C15 = \frac{t_{SS}}{R3} = \frac{5 \times 10^{-3}}{47 \times 10^{3}} = 0.11\ \mu F \rightarrow 0.1\ \mu F$$

2.7 Output Sense Network

The output sense network is a resistive divider connected between the converter output and ground with the output connected to the TL1454 IN2+ terminal (13) of channel 2 (see Figure 5–1). The divider ratio was chosen for a 1.25-V output (the TL1454 reference voltage) when the converter output is at the desired value.

Establishing the proper divider ratio is critical: selecting values for the sense network can affect operation. Choosing values that are too high can result in converter-output voltage-accuracy problems because the error-amplifier input-bias current loads the network. Values that are too low may dissipate too much power, drain too much power from limited power sources such as batteries, or result in loop-compensation capacitor values that are too high to be practical. The dc-source resistance of the error-amplifier inputs should be ≥10 kΩ and approximately matched to minimize output voltage errors caused by the input-bias current. A simple procedure for determining appropriate values for the resistors is to choose a convenient value for *R1* (10 kΩ in this case) and calculate *R6* and *R8* using:

$$R6 = \frac{R1 \times V_O}{V_O - V_{ref}} = \frac{10\ k\Omega \times 3.3\ V}{3.3\ V - 1.25\ V} = 16.1\ k\Omega \rightarrow 16.2\ k\Omega$$

$$R8 = \frac{R1 \times V_O}{V_{ref}} = \frac{10\ k\Omega \times 3.3\ V}{1.25\ V} = 26.4\ k\Omega \rightarrow 26.7\ k\Omega$$

Resistors with 1% tolerance with low and/or reasonably well matched temperature coefficients are recommended to minimize output voltage errors. A device with a ±5% tolerance is suitable for R1.

2.8 Loop Compensation

The loop compensation design consists of shaping the error amplifier frequency response with external components to stabilize the feedback of the dc-to-dc converter control loop without destroying the control loop's ability to respond to line and/or load transients.

The following is a network design approach to stabilize continuous-mode step-down converters. This approach works well as long as the open loop gain is below unity at a frequency much less than the power supply switching frequency. Notice that the equations given in this section are applicable to buck converters only. The procedure and applicable equations for loop compensation of discontinuous-mode step-up (boost) converters are given in another part of this user's guide.

2.8.1 Buck Power Stage and Pulse-Width Modulator

Disregarding the error-amplifier frequency response, the combined response of the pulse-width modulator and buck power stage operating in continuous mode can be modeled as a simple gain block followed by an LC-filter transfer function.

The magnitude of the gain is the change in output voltage for a change in the pulse-width-modulator input voltage (error-amplifier COMP2 terminal voltage). For this design, decreasing the COMP2 voltage from 1.75 V to 1.1 V increases the duty cycle from 0% to 100%, and the output voltage from 0 V to approximately 5 V (= V_I) at the nominal input voltage. The gain, $G_{C–VO}$, is:

$$G_{C–VO} = \frac{\Delta V_O}{\Delta V_{COMP}} = \frac{5–0}{1.75–1.1} = 7.69 \rightarrow 17.7 \ dB.$$

Similarly, the gain is 16.9 dB at low line (4.5-V input) and 20.6 dB at high line (7-V input). For converters with wider input ranges, 2:1 or more, the designer should check for stability at several line voltages to insure that gain variation does not cause a problem.

The phase shift associated with $G_{C–VO}$ is –180° because a decrease in COMP2 voltage causes an increase in output voltage. This is a function of the TL1454 controller.

The output filter response is a two-pole low-pass filter that includes an underdamped complex pole pair near the filter's resonant frequency, f_p, and the capacitor ESR which adds a zero, f_{z1}. The complex poles are located at:

$$f_p = \frac{1}{2 \times \pi \times \sqrt{L_2 \times C_{13} \times \left(1 + \frac{R_C}{R}\right)}}$$

$$= \frac{1}{2 \times \pi \times \sqrt{(10\ \mu H) \times (100\ \mu F) \times \left(1 + \frac{0.35}{2.2}\right)}} = 4.67\ kHz$$

The capacitor ESR zero is located at:

$$f_{z1} = \frac{1}{2 \times \pi \times R_C \times C_{13}} = \frac{1}{2 \times \pi \times 0.35\ \Omega \times 100\ \mu F} = 4.55\ kHz.$$

Combining the two equations above and including the effects of the damping due to ESR, provides an expression for the output filter response.

$$G_{FIL}(s) = V_i \times \frac{R}{R + R_L} \times \frac{1 + s \times R_C \times C_{13}}{1 + s \times \left(R_C \times C_{13} + \frac{L_2}{R}\right) + s^2 \times \left(L_2 \times C_{13} \times \left(1 + \frac{R_C}{R}\right)\right)} \times \frac{1}{1 + s \times C_{17} \times \frac{R \times R_C}{R + R_C}}$$

Where:

R = Load resistance = $\frac{3.3\ V}{1.5\ A} = 2.2\ \Omega$

C_{13} = Output capacitance = 100 µF

R_C = Capacitor ESR + R17 = 0.35 Ω

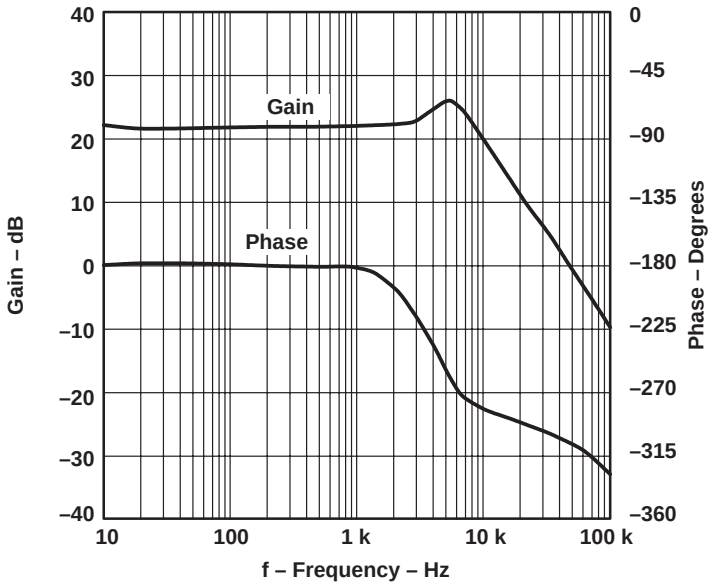
L_2 = Output inductance = 10 µH

R_L = Equivalent resistance of Inductor and FET $R_{DS(on)}$

C_{17} = Ceramic capacitance = 10 µF

The uncompensated loop response for this buck converter is the product of the gain, $G_{C\text{-}VO}$, and the output filter gain, G_{FIL}. Figure 2–2 includes the gain and phase plots of the open loop response (error amplifier not included) obtained from a simple Mathcad analysis. The graph is for the case where maximum gain occurs (at maximum input voltage of 7 V). The presence of the complex pole pair is evident from the resonant peaking in the gain at 5 kHz and the rapid phase transition in the vicinity of 5 kHz.

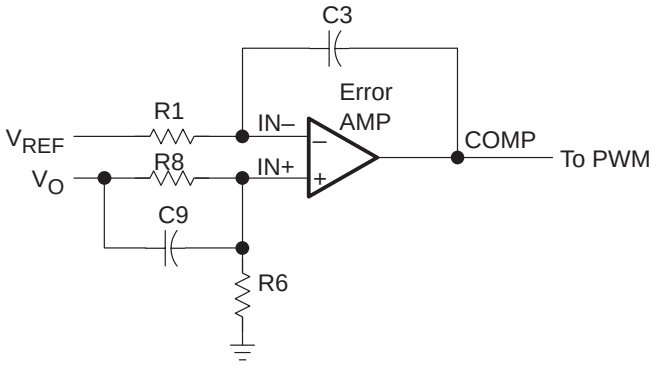
Figure 2–2. Buck Uncompensated Loop Response



2.8.2 Error Amplifier

Unless the designer is trying to meet an unusual requirement, such as very wide band response, many of the decisions regarding gains, compensation pole and zero locations, and loop unity-gain bandwidth are largely arbitrary. Generally, the loop gain at low frequencies is very high, to minimize any dc error in the output voltage. Compensation zeros are added to correct for the sharp change in phase encountered near the filter's resonant frequency. An open loop unity gain frequency is selected higher than the filter resonant frequency, but 10% or less than the converter operating frequency. In this instance, choose an open loop unity gain frequency of 40 kHz to provide good transient response. The compensation network shown in Figure 2–3 is picked for this design.

Figure 2–3. Buck Compensation Circuit



Assuming an ideal amplifier, the transfer function (from V_O to COMP) for this noninverting error-amplifier configuration is:

$$A_{ea}(s) = \left(\frac{R6}{R6 + R8} \times \frac{1 + s \times R8 \times C9}{1 + s \times \frac{R6 \times R8}{R6 + R8} \times C9} \right) \times \left(\frac{1 + s \times R1 \times C3}{s \times R1 \times C3} \right)$$

The transfer function is made up of two independent transfer functions. The first one is the voltage sense divider *(R6*, *R8,* and *C9)*. This represents the transfer function from the output voltage V_O to the noninverting amplifier input, IN+. The second transfer function, made up of *R1* and *C3,* provides high dc gain and can be referred to as the integrator gain.

The compensation component selection begins with the voltage sense divider. Other than sensing the output voltage, this network consisting of *R6*, *R8*, and *C9*, produces one zero and one pole. The zero is located at a frequency of:

$$f_z = \frac{1}{2 \times \pi \times C9 \times R8}$$

Similarly, the pole is located at a frequency of:

$$f_p = \frac{1}{2 \times \pi \times C9 \times \frac{R6 \times R8}{R6 + R8}}$$

Since *R6* and *R8* are already determined, it is necessary to choose capacitor *C9*. Choose C9 to provide a zero at approximately the same frequency as the filter resonance. Capacitor *C9* is calculated to be 1200 pF.

The zero associated with this network is positioned at approximately 5 kHz:

$$f_z = \frac{1}{2 \times \pi \times C9 \times R8} = \frac{1}{2 \times \pi \times \left(1200 \times 10^{-12}\right) \times \left(26.7 \times 10^{3}\right)} = 5 \ kHz$$

The pole associated with this network is positioned at approximately 13.3 kHz:

$$f_p = \frac{1}{2 \times \pi \times C9 \times \left(R8 \parallel R6\right)} = \frac{1}{2 \times \pi \times \left(1200 \times 10^{-12}\right) \times \left(10 \times 10^{3}\right)} = 13.3 \ kHz$$

For an open loop unity gain frequency of 40 kHz, the sum (in dB) of the gains of the modulator, LC filter, and error amplifier must be 0 dB at 40 kHz. The gain of the modulator/LC filter at 40 kHz may be obtained by any number of analysis methods, and for this design, the gain at 40 kHz is about 0 dB, as shown in Figure 2–2. The gain of the voltage sense network (*R6*, *R8,* and *C9*) is found to be approximately 0 dB at 40 kHz. Therefore, the integrator gain should be 0 dB at 40 kHz for an overall loop unity-gain frequency of 40 kHz.

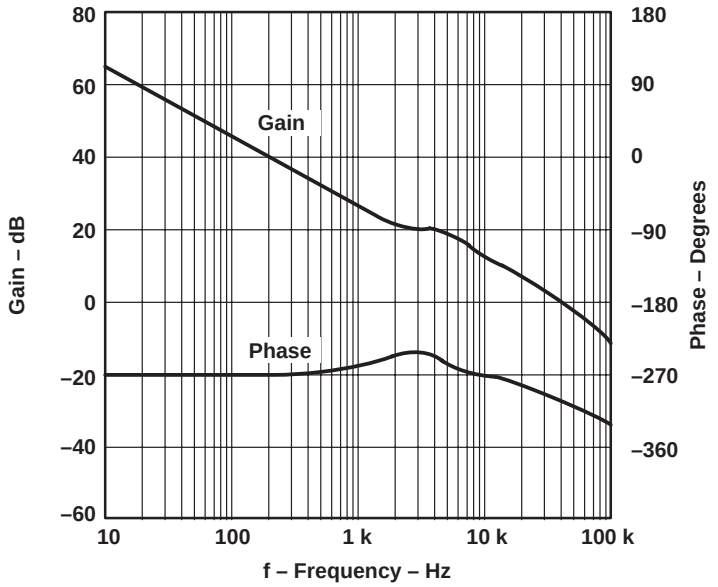
The next step is to calculate integrator components. *R1* was chosen to be 10 kΩ. *C3* is chosen to provide a zero at approximately 5 kHz giving unity gain (from the integrator portion of the error amplifier circuit) above 10 kHz.

C3 is calculated to produce a zero at 5 kHz:

$$C3 = \frac{1}{2 \times \pi \times f \times R1} = \frac{1}{2 \times \pi \times \left(5 \times 10^{3}\right) \times \left(10 \times 10^{3}\right)} = 3185 \ pF \rightarrow 3300 \ pF$$

Figure 2–4 shows the total open loop frequency response of the buck regulator (at maximum input voltage). The figure shows the results of adding the compensation network to the system response shown in Figure 2–2. The design goals are clearly met: high gain at low frequency, gradual phase shift around the filter resonant frequency, and unity gain frequency of 40 kHz (above filter resonance of 5 kHz and less than 10% of switching frequency of 500 kHz). In addition, the phase margin is about 50° indicating a stable system.

Figure 2–4. Buck Compensated Open Loop Response



Chapter 3

12-V Step-Up Regulator

The following sections describe the design procedure for this 12-V step-up (or boost) regulator. Selection and/or design guidelines are given for the external power components. As stated in the TL1454 data sheet, channel 1 of the controller is configured to control and provide drive signals for a step-up regulator using an n-channel power MOSFET.

Topic **Page**

3.1 Inductor Selection

The boost inductor, converter switching frequency, input and output voltages, and output power determine a boost converter's operating mode. This converter operates in the discontinuous-conduction mode (DCM). In discontinuous mode, the current in the inductor starts at zero and returns to zero in each switching cycle. To keep the converter in discontinuous mode, the inductor must be less than a computed maximum value. However, for a specified output power level, the smaller the inductance, the higher the peak and rms current in Q1 and CR1. Therefore, the value of inductance is not critical and can be left to the needs of the designer.

Discontinuous mode is desirable because the power-stage frequency response is stable and has a dc gain and a single pole. Continuous-mode boost converters have a dc gain, a complex pole pair, and a right-half-plane zero, making feedback loop stabilization difficult.

The maximum value of inductance L, can be calculated as a function of M, R, and T_S where M is defined as the converter voltage gain from input to output, R is the load resistance and T_S is the period of one switching cycle.

$$L \leq \frac{R \times T_S}{2} \times \frac{M - 1}{M^3}$$

M is defined as:

$$M = \frac{V_O}{V_I}$$

For this example, with M = 2.7, V_O = 12 V, V_I = 4.5 V, and R = 60 Ω the calculated value of L is:

$$L \leq \frac{60 \times 2 \times 10^{-6}}{2} \times \frac{2.7-1}{2.7^3} = 5.2\ \mu H \rightarrow 2.7\ \mu H$$

Allowing for startup transients and additional output current to charge the output filter capacitor, and since the exact value is not critical, a smaller standard-value inductor is chosen.

3.2 Duty Cycle Estimates

The duty cycle (D) is the ratio of the power switch conduction time to the period of one switching cycle. The duty cycle for a boost converter is calculated as:

$$D = \sqrt{K \times M \times (M–1)}$$

Where K is:

$$K = \frac{2 \times L}{R \times T_S}$$

For this example, assuming V_I = 5 V, V_O = 12 V, R = 60 Ω, corresponding to 200 mA output current, we get a duty cycle estimate of:

$$D = \sqrt{\frac{2 \times 2.7 \times 10^{–6}}{60 \times 2 \times 10^{–6}} \times \frac{12}{5} \times \left(\frac{12}{5} – 1\right)} = 0.39$$

For V_I = 5 V, V_O = 12 V, R = 600 Ω, corresponding to 20 mA output current, we get a duty cycle estimate of:

$$D = \sqrt{\frac{2 \times 2.7 \times 10^{–6}}{600 \times 2 \times 10^{–6}} \times \frac{12}{5} \times \left(\frac{12}{5} – 1\right)} = 0.12$$

3.3 Output Capacitor

The peak inductor current must be calculated to determine the amount of output capacitance needed. The expression for the peak inductor current, I_{PK}, is:

$$I_{PK} = \frac{V_I}{L} \times D \times T_S$$

The peak inductor current occurs when the converter is driving its maximum load of 200 mA and the input voltage is at the minimum of 4.5 V. Using the duty cycle calculated for V_I = 4.5 V and for a 200-mA load gives:

$$I_{PK} = \frac{4.5}{2.7 \times 10^{-6}} \times (0.45) \times \left(2 \times 10^{-6}\right) = 1.5\ A$$

The two criteria for selecting the output capacitor are the amount of capacitance needed and the capacitor's equivalent series resistance (ESR). After the capacitance and ESR requirements are determined, the capacitor can be selected.

The voltage variation due to the inductor current flow in the output capacitor is approximately:

$$\Delta V_O = \frac{I_{PK}^2 \times L}{2 \times C \times \left(V_O - V_I\right)}$$

The above equation is based on the assumption that all inductor ripple current flows through the capacitor and the ESR is zero. If the desired output ripple voltage is 120 mV, then the capacitance needed is:

$$C = \frac{(1.5)^2 \times \left(2.7 \times 10^{-6}\right)}{(2) \times (0.12) \times (12-5)} = 3.6\ \mu F$$

Now, given that the capacitance is very large, the ESR needed to limit the ripple to 120 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.12}{1.5} = 80\ m\Omega$$

The actual output filter capacitor should be rated at greater than the calculated capacitance and lower than the calculated ESR. This design used one 22-µF multilayer ceramic capacitor. With this ceramic capacitor, the ESR is significantly less than the calculated ESR requirement.

3.4 Power-Stage Design

The power-stage design includes selecting the power switch, the output rectifier, and the rectifier snubbing network (if needed), calculating the power dissipations and junction temperatures, and verifying that the semiconductors have adequate heatsinking.

3.4.1 Power Switch

The output drive of the TL1454 for this channel (OUT1) is set up to drive an N-channel MOSFET that is ideal for boost converters. In choosing the proper power switch, important criteria include: maximum switch current, peak switch voltage, $r_{DS(on)}$, power dissipation, and gate-drive voltage.

The peak drain current is the inductor current during the on time. This current was calculated previously as 1.5 A. The peak drain voltage is calculated as follows:

$$V_{PK} = V_O + V_d = 12 + 0.5 = 12.5\ V$$

The maximum allowable $r_{DS(on)}$ is calculated from an assumed $V_{Sat–pk}$ of 0.5 V and adjusted for temperature. Assume a temperature adjustment (K) of 1.4:

$$r_{DS(on)} \leq \frac{V_{Sat–pk}}{I_{PK} \times K} = \frac{0.5}{(1.5)\ (1.4)} = 0.24\ \Omega$$

The gate-drive voltage will range from approximately 4.5 V to 7.0 V, thus a MOSFET with low-level drive capability is required.

The transistor chosen is the IRLL014. This device is a 60-V, 2.7-A MOSFET with a maximum $r_{DS(on)}$ of 0.20 Ω at a 5-V gate drive. The transistor's turn-off time (t_{fall}) is 26 ns. The surface-mount SOT-223 package has a thermal resistance of 60°C/W when mounted on a 1″ square pcb. The conduction and switching losses for this device are calculated as follows (where D = duty cycle = $t_{on} \times f$ and K = 1.4):

$$P_D = \left[\left(r_{DS(on)} \times K\right)\left(I^2_{L(rms)}\right)\right] + \left[\left(\frac{1}{2}\right)\left(V_{PK}\right)\left(I_{L(PK)}\right)\left(t_{fall}\right)(f)\right]$$

and $I_{L(rms)}$ is:

$$I_{L(rms)} = I_{PK} \times \sqrt{\frac{D}{3}}$$

At 4.5 Vin, the power dissipation is:

$$P_D = \left[(0.2) \times (1.4) \times \left((1.5) \times \sqrt{\frac{0.45}{3}}\right)^2\right] + \left[\left(\frac{1}{2}\right)(12.5)\ (1.5)\ \left(26 \times 10^{-9}\right)\left(500 \times 10^3\right)\right] = 217\ mW$$

Worst-case junction temperature is calculated as:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (60 \times 0.217) = 68^{\circ}C$$

3.4.2 Output Rectifier

For low-voltage applications, a Schottky diode is recommended. This design uses an SS12 Schottky rectifier with a 1-A current rating, a 20-V reverse voltage rating, and a maximum forward drop of 0.5 V. Power dissipation for CR1 is:

$$P_{CR1} = \left(V_D\right)\left(I_O\right) = (0.5)\ (0.2) = 100\ mW$$

Junction temperature for this diode may be estimated using a thermal resistance of 88°C/W:

$$T_J = T_A + \left(R_{\Theta JA} \times P_{CR1}\right) = 55 + (88 \times 0.1) = 64^{\circ}C$$

3.4.3 Output-Rectifier Snubber Network

An RC snubber is placed across the diode to prevent ringing of the output diode due to parasitic inductances. Select a capacitor value that is 2 to 5 times the diode junction capacitance. With a diode junction capacitance of 200 pF, a reasonable capacitor value to use is 1000 pF. Assuming a ringing period of 30 ns, then choose the snubber resistor, *R10*, so that the snubber capacitor can fully charge during the ringing period. So, for a 30-ns ringing time constant, choose *R10* as

$$R10 = \frac{t_{Ringing}}{3 \times C10} = \frac{30 \times 10^{-9}}{3 \times 1000 \times 10^{-12}} = 10\ \Omega$$

The power dissipation for the resistor is:

$$P_{R10} = 2(C10)\ \left(V_{PK}^2\right)\left(\frac{f}{2}\right) = 2\left(1000 \times 10^{-12}\right)\left(12.5^2\right)\left(\frac{500 \times 10^3}{2}\right) = 78\ mW$$

3.5 Dead Time Control

Unlike step-down converters where 100% duty-cycle operation is acceptable, the duty cycle of step-up converters must be limited below 100%.

The maximum duty cycle for this design was calculated at approximately 0.5. Allowing for tolerances, the actual limit value should be somewhat higher. We chose a maximum duty cycle of 0.70. Using Figure 2-1 and the equation below, to determine the DTC input voltage required:

$$V_{DT} = 1.75–0.7(1.75–1.1)–0.65 = 0.65\ V$$

A voltage divider, R12/R13, connected from the reference voltage to ground, sets the dead time control voltage. The input bias current of the DTC1 pin is 10 μA maximum. Although a divider current of 1000 times the input current is preferred, this would excessively load the reference supply. The divider current will be set at 200 μA. The bottom divider resistor is calculated:

$$R13 = \frac{V_{DT}}{I_+} = \frac{0.65}{200 \times 10^{-6}} = 3250\ \Omega \rightarrow 3.32\ k\Omega$$

Using 3320 Ω, the divider current is 196 μA. *R12* is now calculated as:

$$R12 = \frac{V_{REF} - V_{DT}}{I_+} = \frac{1.25–0.65}{196 \times 10^{-6}} = 3261\ \Omega \rightarrow 3.01\ k\Omega$$

With the new calculated values, the actual dead-time voltage and duty cycle are:

$$V_{DT} = V_{REF}\left(\frac{R13}{R12 + R13}\right) = 1.25\left(\frac{3320}{3010 + 3320}\right) = 0.65\ V$$

$$D_{max} = \frac{V_{O(max)} - 0.65 - V_{DT}}{V_{O(max)} - V_{O(min)}} = \frac{1.75 - 0.65 - 0.65}{1.75 - 1.1} = 0.69$$

3.6 Soft-Start Timing

Soft start is achieved by adding a capacitor in parallel with the upper resistor of the dead-time control circuit. If dead-time control is not being used, soft start can still be implemented by using a capacitor in series with a resistor connected to DTC. The SCP time period of 120 ms was set in section 1.4.2. A good standard for the soft-start timing is no more than 1/10 of the SCP time period. Using 5 ms, the soft-start capacitor is calculated as:

$$C14 = \frac{t}{R12 \parallel R13} = \frac{5 \times 10^{-3}}{3010 \parallel 3320} = 3.2\ \mu F \rightarrow 3.3\ \mu F$$

3.7 Output Sense Network

Using the same approach as in the 3.3-V design:

$$R5 = \frac{R2 \times V_O}{V_O - V_{ref}} = \frac{10\ k\Omega \times 12\ V}{12\ V - 1.25\ V} = 11.2\ k\Omega \rightarrow 11\ k\Omega$$

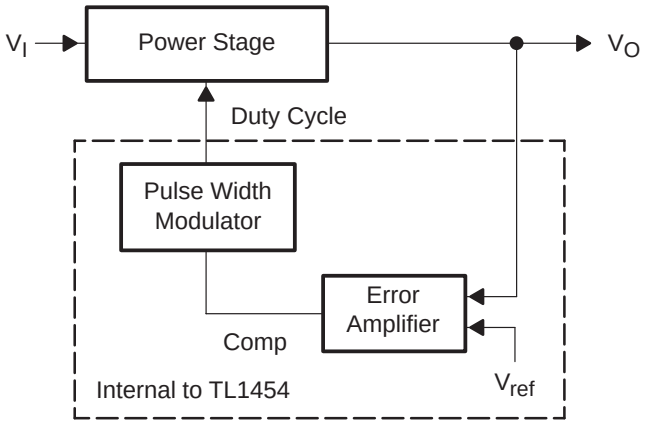
$$R7 = \frac{R2 \times V_O}{V_{ref}} = \frac{10\ k\Omega \times 12\ V}{1.25\ V} = 96\ k\Omega \rightarrow 95.3\ k\Omega$$

Precision resistors are used in this divider, not so much for the actual resistance value, but for the drift characteristics of the values.

3.8 Loop Compensation

The control loop for this converter consists of three gains: the power stage gain (G_{PS}), the error amplifier gain ($G_{E/A}$), and the internal TL1454 PWM modulator gain (G_{PWM}). For this converter, the pulse-width modulator and power stage frequency responses are computed separately as opposed to calculating the pulse-width modulator and power stage frequency response together as it was previously done with the buck converter above. Figure 3–1 shows a simplified block diagram of the control loop.

Figure 3–1. Control Loop Simplified Block Diagram



The loop-compensation design procedure consists of shaping the error-amplifier frequency response with external components to stabilize the dc-to-dc converter. The following is a simplified approach to designing networks to stabilize discontinuous mode boost converters that works well when the open-loop gain is below unity at a frequency much lower than the frequency of operation.

Before the error-amplifier frequency response can be designed, the frequency response of the rest of the loop must be determined. This consists of determining the power stage gain and phase, and the pulse width modulator gain and phase.

3.8.1 Boost Power Stage

The response of the boost power stage operating in discontinuous mode can be modeled as a simple gain block with a single real pole. The magnitude of the gain is the change in the output voltage divided by the change in the duty cycle.

The gain of the discontinuous boost power stage is:

$$G_{PS}(s) = \frac{\Delta V_O}{\Delta D} = G_{OD} \times \frac{1}{1 + \frac{s}{\omega_P}}$$

where,

$$G_{OD} = \frac{2 \times V_O}{(2 \times M)-1} \times \sqrt{\frac{M-1}{K \times M}}$$

$$\omega_P = \frac{(2 \times M)-1}{M-1} \times \frac{1}{R \times C}$$

and K and M are the same as previously defined. For this example, with V_I = 5 V and I_O = 200 mA, the dc gain, G_{OD} , is given by:

$$G_{OD} = \frac{2 \times 12}{\left(2 \times \frac{12}{5}\right)-1} \times \sqrt{\frac{\frac{12}{5}-1}{\frac{2 \times 2.7 \times 10^{-6}}{60 \times 2 \times 10^{-6}} \times \frac{12}{5}}} = 22.7 \rightarrow 27.1 \ dB$$

and, the single real pole is given by:

$$\omega_P = \frac{\left(2 \times \frac{12}{5}\right)-1}{\frac{12}{5}-1} \times \frac{1}{60 \times 22 \times 10^{-6}} = 2056 \ Rad/sec \rightarrow 327 \ Hz$$

This power stage gain is dependent on input voltage and output load resistance. For this circuit, the lowest gain occurs when the input voltage is at its maximum of 7 V and the output load resistance is at its minimum of 60 Ω (corresponding to 200 mA load current). This condition gives a minimum phase margin. It is good design practice to check for stability at the line voltage extremes, and at the limits of output loads to ensure that the gain and phase variations do not cause problems.

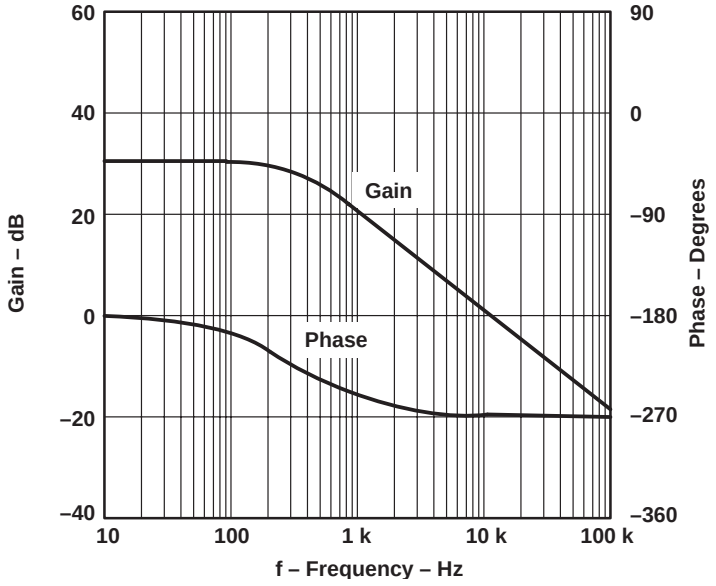
3.8.2 Pulse-Width Modulator

The response of the pulse-width modulator can be modeled as a simple gain block. The magnitude of the gain is the change in PWM output duty cycle for a change in the pulse-width-modulator input voltage (error-amplifier COMP voltage). Looking in Figure 2–1, the maximum PWM triangle wave amplitude is 1.75 V and its minimum is 1.1 V for this application. Even though the maximum duty cycle is limited to 0.69, if the duty cycle were allowed to attain 100%, the duty cycle output would change from 100% to 0% for COMP voltage changes from 1.1 to 1.75. Therefore, the gain, G_{PWM}, is:

$$G_{PWM} = \frac{\Delta D}{\Delta V_{O(COMP)}} = \frac{1-0}{1.75-1.1} = 1.54 \rightarrow 3.7 \ dB$$

The product (sum in dB) of the gains of the power stage, G_{PS}, and the pulse-width-modulator, G_{PWM} makes up the uncompensated open loop response. Figure 3–2 is a gain and phase plot of the uncompensated open loop response of this converter obtained from a Mathcad analysis. The presence of the single real pole is evident from the phase in the region of 327 Hz and the total phase shift is only 90 degrees.

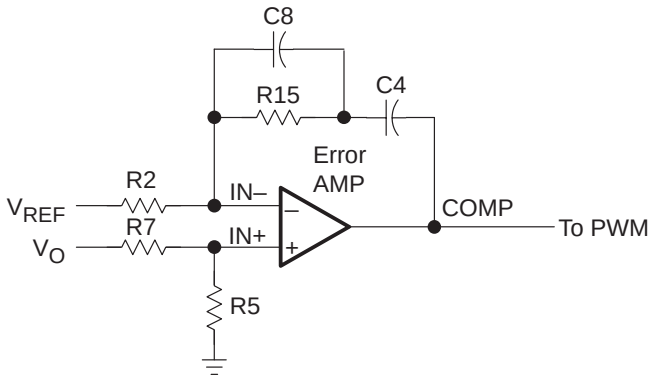
Figure 3–2. Boost Uncompensated Loop Response



3.8.3 Error Amplifier

Unless the design needs to meet an unusual requirement, (i.e., very wideband response) many of the decisions regarding gains, compensation pole and zero locations, and unity gain bandwidth are largely arbitrary. Generally, the gain at low frequencies is very high to minimize error in the output voltage. Compensation zero(s) are added near the filter pole(s) to correct for the change in phase encountered near the filter's pole frequency. An open loop unity gain frequency is selected beyond the filter's pole frequency, but 10% or less than the converter operating frequency. In this instance, choose a unity gain frequency of approximately 10 kHz to provide good transient response. The compensation network is shown in Figure 3–3.

Figure 3–3. Boost Compensation Circuit



For an ideal amplifier, the error amplifier transfer function is:

$$A_{ea}(s) = \frac{R5}{R5 + R7} \times \frac{1 + s \times C4 \times (R2 + R15)}{s \times C4 \times R2} \times \frac{1 + s \times C8 \times \frac{R2 \times R15}{R2 + R15}}{1 + s \times C8 \times R15}$$

This amplifier has a pole at dc, a zero positioned to approximately cancel the pole from the power stage, and a high frequency pole to prevent noise from upsetting the control loop.

The unity gain frequency is selected to be approximately 10 kHz. From the gain-phase plot of the uncompensated open loop response of the converter (Figure 3–2), the gain is approximately 0 dB, and the phase is –90 degrees at 10 kHz. Therefore, the amplifier needs to provide a gain of 0 dB at 10 kHz.

The gain is approximated by the ratio of *R15* to *R2* and the *R5 – R7* voltage divider because the zero provided by *C4* and *R2 + R15* is located much lower in frequency than the desired crossover frequency.

The gain at 10 kHz can be approximated by the following:

$$G_{ea(10\ kHz)} = \frac{R5}{R5 + R7} \times \frac{R2 + R15}{R2} = \frac{11\ k\Omega}{11\ k\Omega + 95.3\ k\Omega} \times \frac{10\ k\Omega + 91\ k\Omega}{10\ k\Omega} = 1.04$$

Expressed in dB, the gain is:

$$G_{ea(10\ kHz)} = 0.34\ dB$$

The zero provided by *C4* and *R2+ R15* is given by:

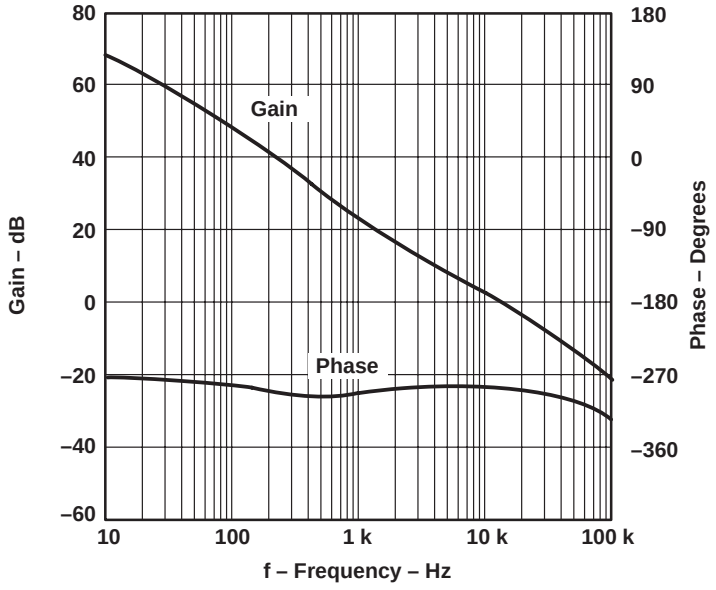
$$f_Z = \frac{1}{2 \times \pi \times C4 \times (R2 + R15)} = \frac{1}{2 \times \pi \times (2200\ pF) \times (10\ k\Omega + 91\ k\Omega)} = 717\ Hz$$

And finally, the high frequency pole is calculated as:

$$f_{P–HF} = \frac{1}{2 \times \pi \times C8 \times R15} = \frac{1}{2 \times \pi \times (22\ pF) \times (91\ k\Omega)} = 80\ kHz$$

The overall open loop frequency response of the converter is the product of the uncompensated open loop response and the error amplifier response. A Bode plot of the overall open loop frequency response of the converter is shown in Figure 3–4. The gain crosses 0 dB in the vicinity of 10 kHz and the phase margin is near 80 degrees.

Figure 3–4. Boost Compensated Open Loop Response



Chapter 4

Test Results

The following sections describe the procedure for test setup of the TL1454-EVM-085 Evaluation Module (EVM), and the test results. These results represent the typical performance of the EVM.

Topic **Page**

4.1 Test Setup

For initial powerup of the TL1454EVM-085 (SLVP085) evaluation board, perform the following steps:

1) Connect an electronic load from the 3.3-V output to GND (P2-1 and 2 to P2-3 and 4) adjusted to draw approximately 0.5 A at 3.3 V. Connect an electronic load from the 12-V output to GND (P2-5 to P2-3 and 4) adjusted to draw approximately 100 mA at 12 V. The exact current levels are not critical; any nominal current is sufficient. A fixed resistor may be used in place of the electronic load. The output current drawn by the resistor is $I_O = \frac{V_O}{R}$ Amps where R is the value of the load resistor and V_O is the output voltage. The power rating of the resistor, P_R should be at least:

$$P_R \geq \frac{V_O 2}{R} \times 2 \ \textit{Watts}$$

2) Connect a 5-V lab power supply from the V_I input to RTN (P1-1 and 2 to P1-3 and 4) of the SLVP085. A set current limit of 1.5 A should be adequate for the input power requirements.

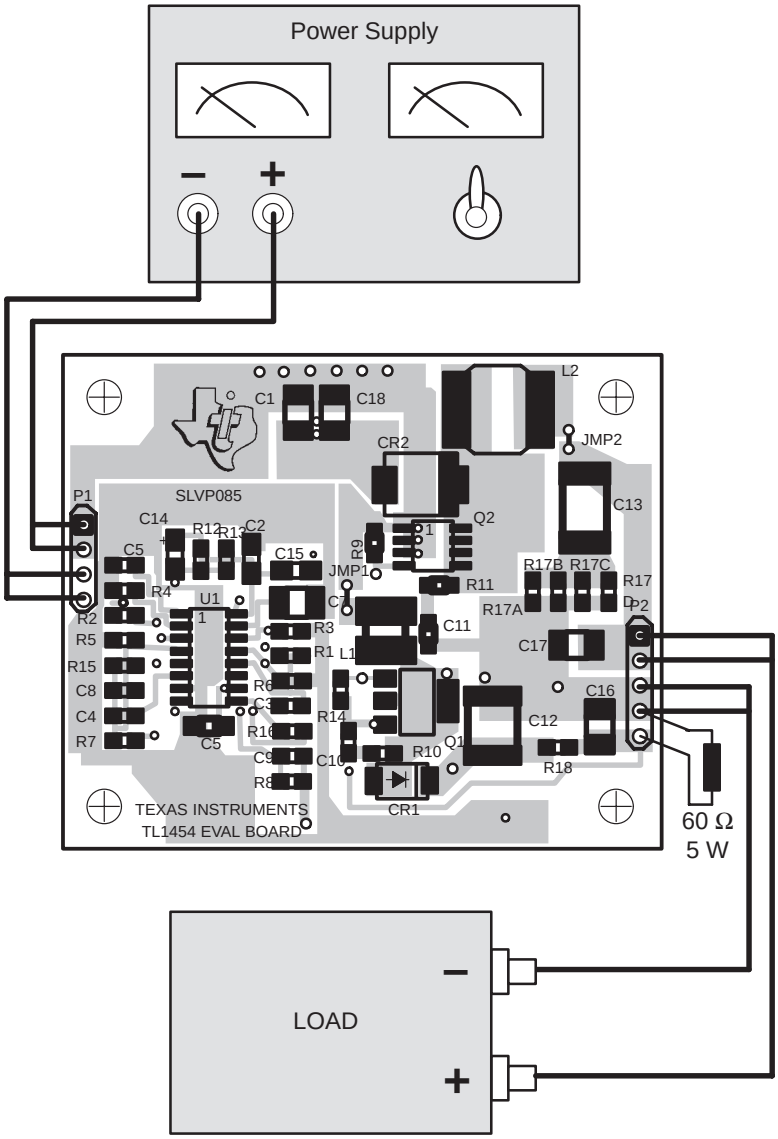
3) Turn on the 5-V supply and ramp the input voltage up to 5 V.

4) Verify that the EVM output voltages (measured at the module output pins) are 3.3 V ± 0.17 V, and 12 V ± 0.6 V.

5) For subsequent testing, ensure the lab supply output current capacity and current limit are at least 3 A so that the SLVP085 can be operated at maximum loads on both outputs.

6) See Section 4.2 for selected typical waveforms and operating conditions for verification of proper module operation.

Figure 4–1. Test Setup



4.2 Test Results

Figures 4–2 to 4–12 and Tables 4–1 and 4–2 show test results for the SLVP085 evaluation board.

Table 4–1. 3.3 V Measured Test Results

Parameter	Test Conditions	Measurement	Unit
Load regulation	V_I = 5 V, I_O(12 V) = 200 mA	± 0.1 Max	%
Line regulation	I_O(3.3 V) = 1.5 A, I_O(12 V) = 200 mA	± 0.1 Max	%
Output ripple	V_I = 5 V, I_O(12 V) = 200 mA	25	mV
Transient response	V_I = 5 V, I_O(12 V) = 200 mA, I_O(3.3 V) pulsed from 1.5 A to 3 A	50	mV pk
Efficiency	V_I = 5 V, I_O(3.3 V) = 1.5 A, I_O(12 V) = 0 mA	90	%

Table 4–2. 12 V Measured Test Results

Parameter	Test Conditions	Measurement	Unit
Load regulation	V_I = 5 V, I_O(3.3 V) = 1.5 mA	0	%
Line regulation	I_O(3.3 V) = 1.5 A, I_O(12 V) = 200 mA	0	%
Output ripple	V_I = 5 V, I_O(3.3 V) = 1.5 mA	35	mV
Transient response	V_I = 5 V, I_O(3.3 V) = 3 A, I_O(12 V) pulsed from 100 mA to 200 mA	20	mV pk
Efficiency	V_I = 5 V, I_O(3.3 V) = 0 A, I_O(12 V) = 200 mA	83	%

Figure 4–2. SLVP085 Measured Efficiency

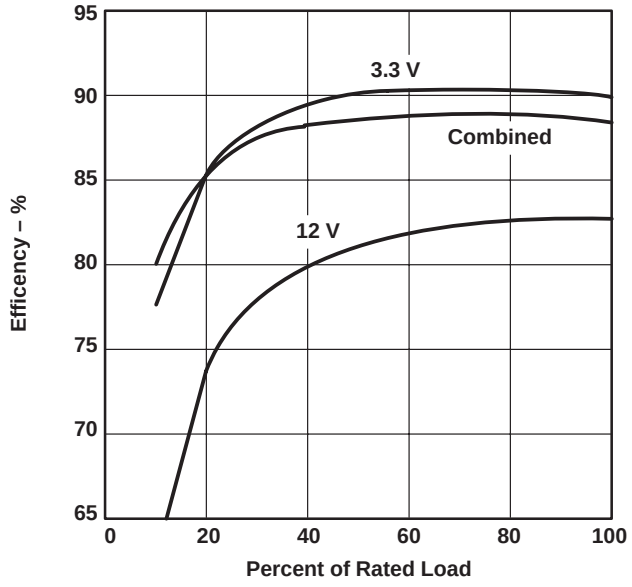


Figure 4–3. SLVP085 Measured Line Regulation

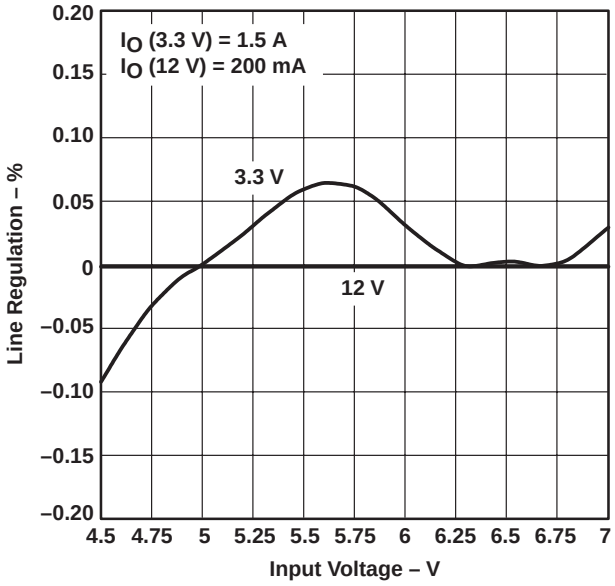


Figure 4–4. SLVP085 Measured Load Regulation

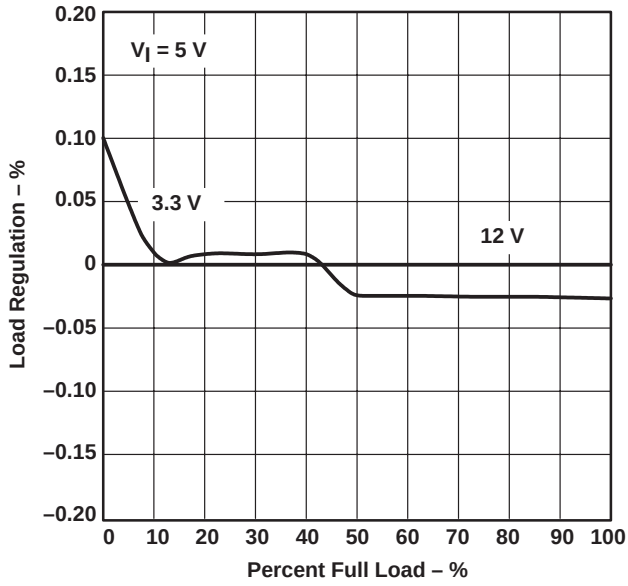


Figure 4–5. SLVP085 CR2-Cathode Switching Waveform

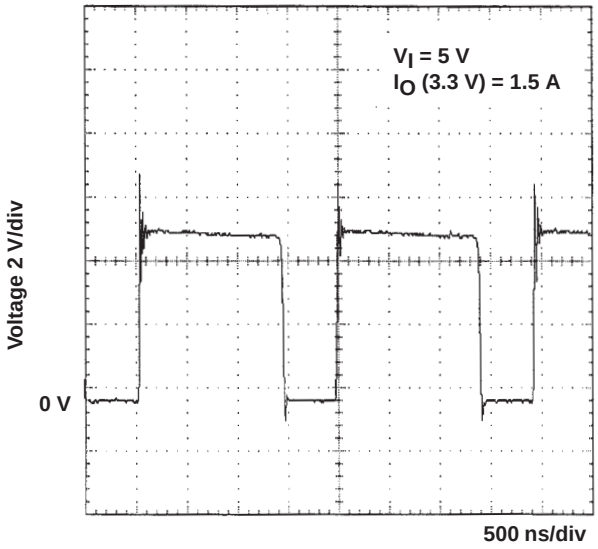


Figure 4–6. SLVP085 3.3-V Output Start-Up

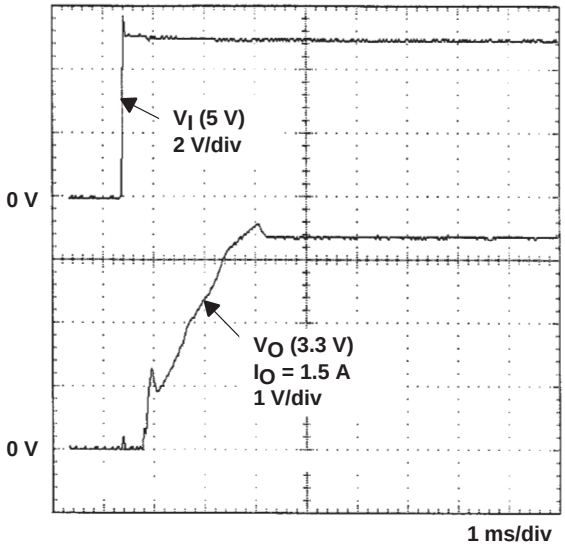


Figure 4–7. SLVP085 3.3-V Output Voltage Ripple

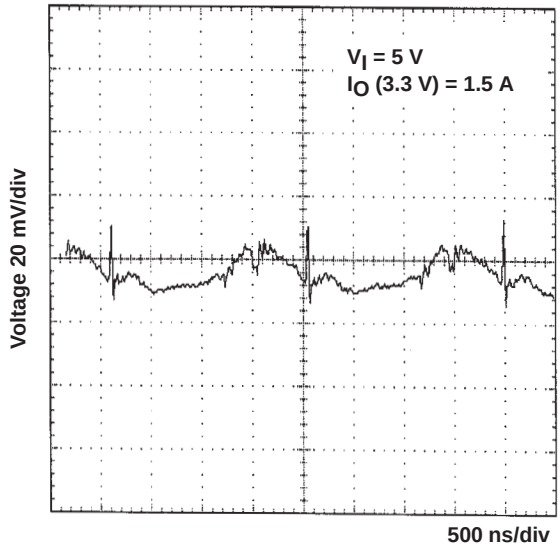


Figure 4–8. SLVP085 3.3-V Load Transient Response

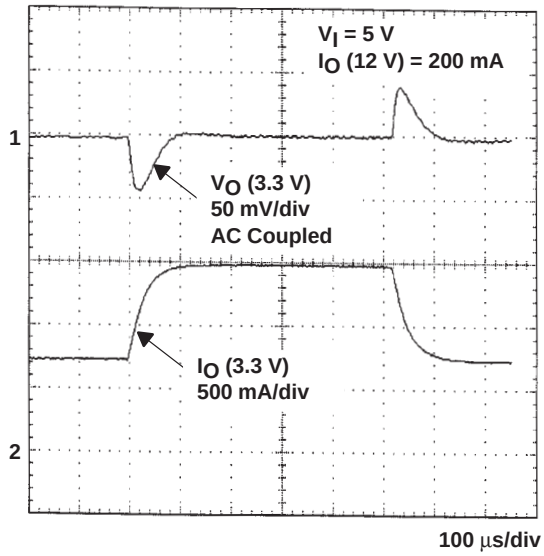


Figure 4–9. SLVP085 Q1 V_{DS} Switching Waveform

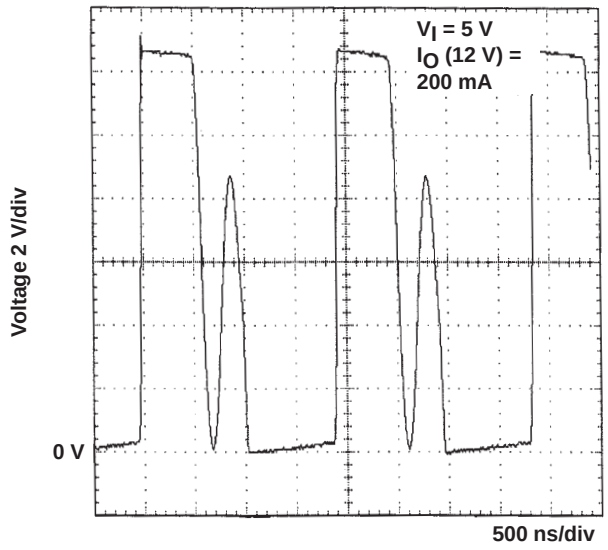


Figure 4–10. SLVP085 12-V Output Start-Up

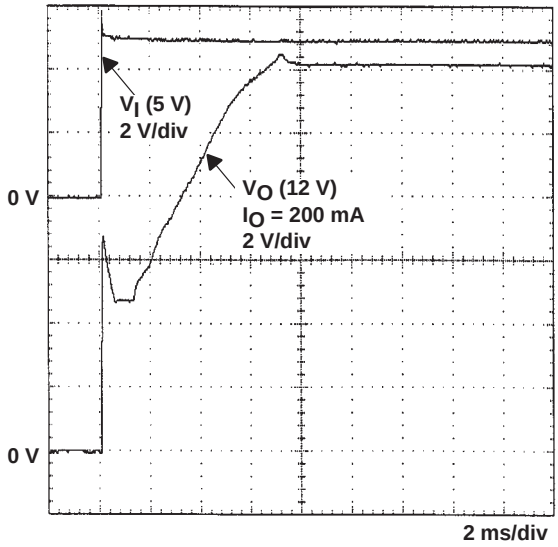


Figure 4–11. SLVP085 12-V Output Voltage Ripple

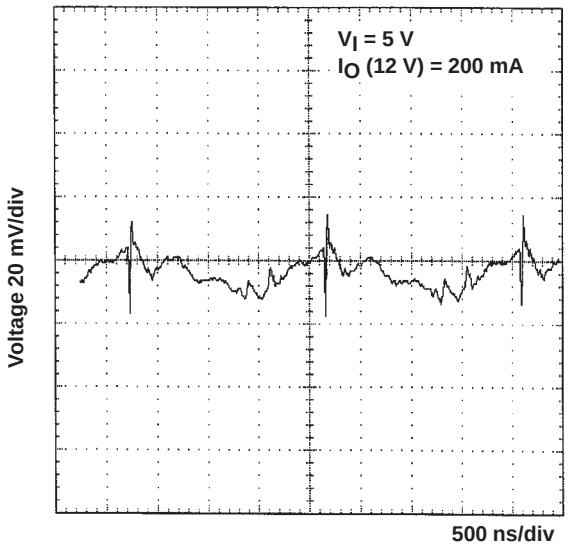
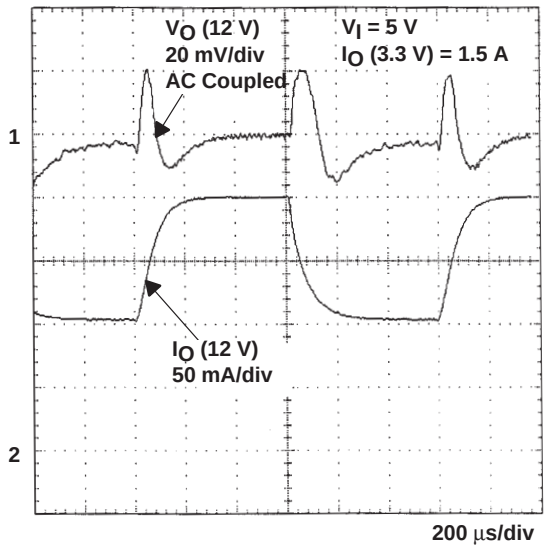


Figure 4–12. SLVP085 12-V Load Transient Response



Chapter 5

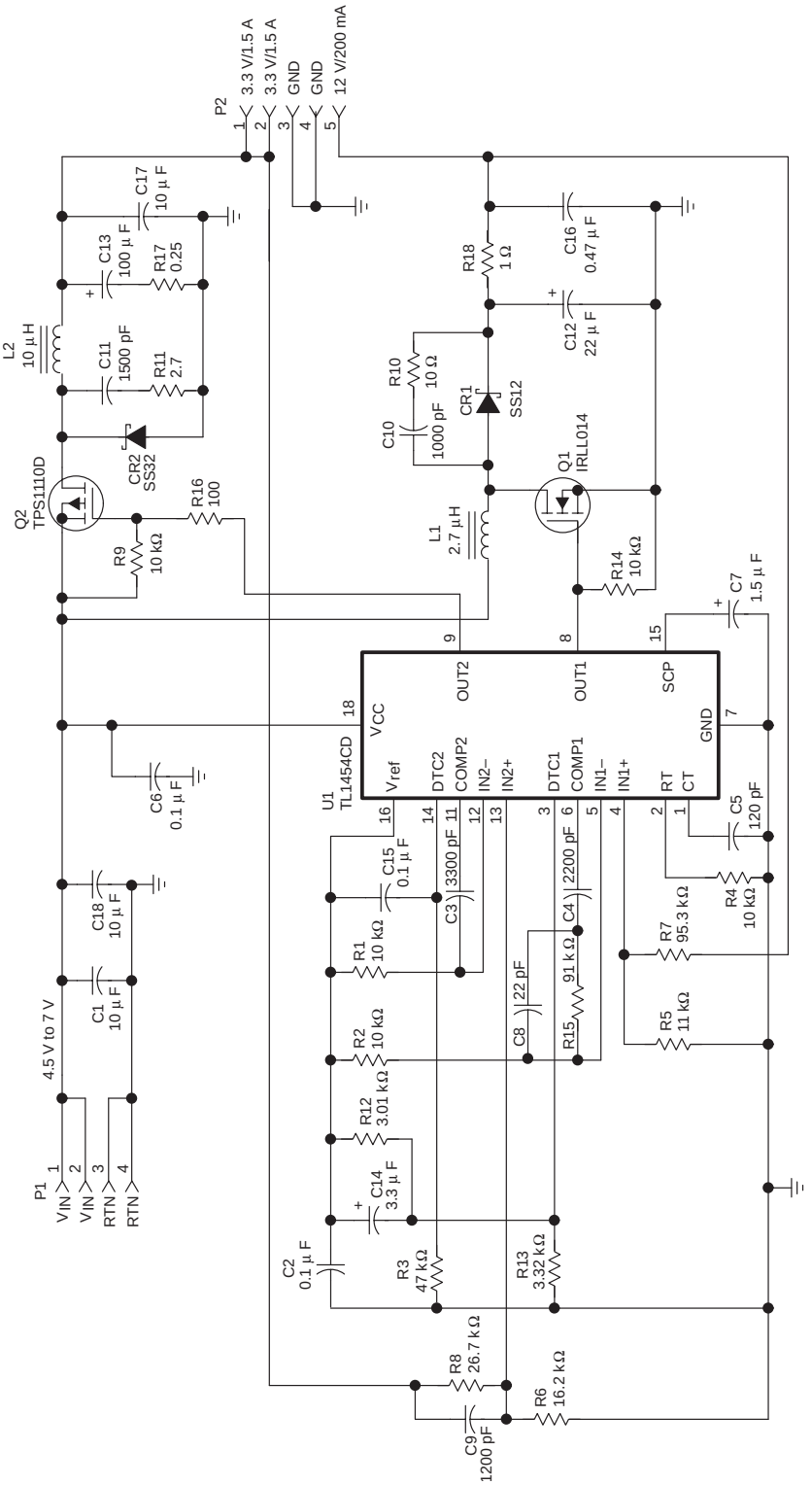
EVM Documentation

The schematic, board layout, and bill of materials are provided to document the SLVP085 EVM dual regulator assembly.

Topic **Page**

5.1 EVM Schematic

Figure 5–1. Dual Regulator EVM Schematic



5.2 EVM Bill of Materials

Table 5–1. EVM Bill of Materials

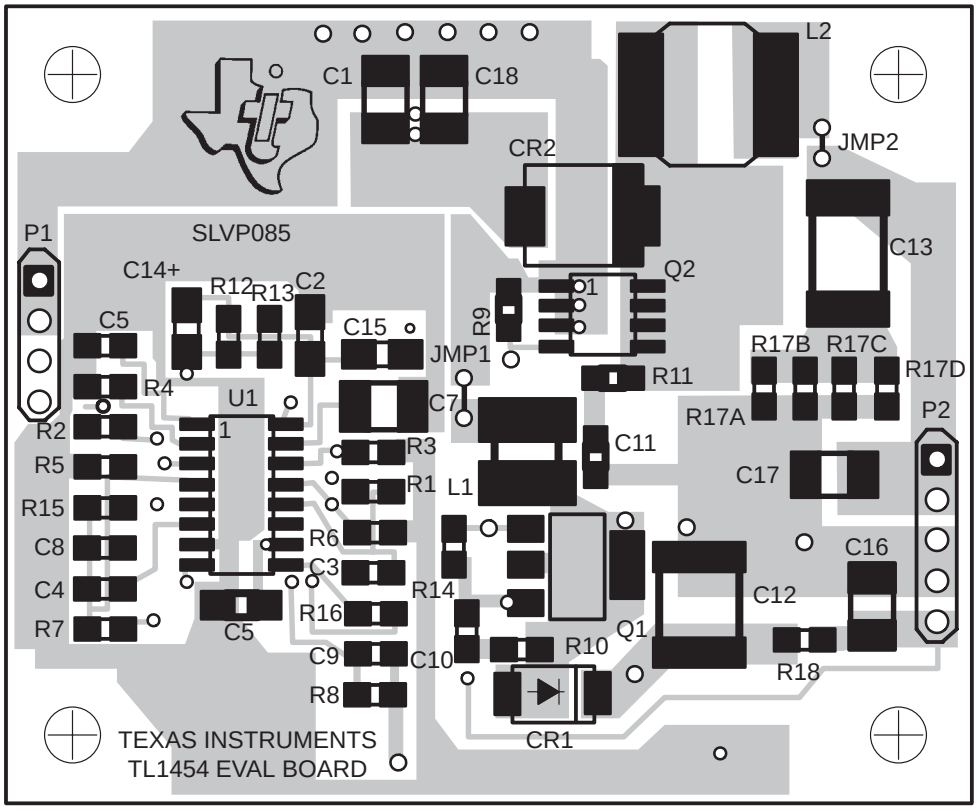
ITEM	QTY	REF. DES./COMM	PART NO.	PART DESCRIPTION	APPROVED VENDOR
1	3	C1,C17,C18	C3225Y5V1C106Z	CAP, CER, 10 μF,10 V (Dist #: CC1210CY5V106Z)	TDK
ALT	0	Alt. part for item 1	TPSD107M010R0100	CAP, TANT, 100 μF, 10 V, D CASE	AVX
2	3	C2,C6,C15	STANDARD	CAP, CER, 0.1 μF, 1206, X7R	MULTI. SOURCE
3	1	C3	STANDARD	CAP, CER, 3300 pF, 0805, X7R	MULTI. SOURCE
4	1	C4	STANDARD	CAP, CER, 2200 pF, 0805, NPO	MULTI. SOURCE
5	1	C5	STANDARD	CAP, CER, 120 pF, 0805, NPO	MULTI. SOURCE
6	1	C7	ECS–T1CY155R	CAP, TANT, 1.5 μF, 16 V, A CASE	PANASONIC
7	1	C8	STANDARD	CAP, CER, 22 pF, 0805, NPO	MULTI. SOURCE
8	1	C9	STANDARD	CAP, CER, 1200 pF, 0805, X7R	MULTI. SOURCE
9	1	C10	STANDARD	CAP, CER, 1000 pF, 0805, X7R	MULTI. SOURCE
10	1	C11	STANDARD	CAP, CER, 1500 pF, 0805, X7R	MULTI. SOURCE
11	1	C12	THCR60E1E226Z	CAP, CER, 22 μF, 25 V, 2220, Y5V	MARCON/TOSHIBA
ALT	0	Alt. part for item 11	TPSE107M016R0100	CAP, TANT, 100 μF, 16 V, E CASE	AVX
12	1	C13	TPSD107M010R0100	CAP, TANT, 100 μF, 10 V, D CASE	AVX
13	1	C14	ECS-T1CY335R	CAP, TANT, 3.3 μF, 16 V, A CASE	PANASONIC
14	1	C16	STANDARD	CAP, CER, 0.47 μF, 1210, Z5U	MULTI. SOURCE
15	4	R1,R2,R9,R14	STANDARD	RES, 10 KΩ, 0805, 5%	MULTI. SOURCE
16	1	R3	STANDARD	RES, 47 KΩ, 0805, 5%	MULTI. SOURCE
17	1	R4	STANDARD	RES, 10.0 KΩ, 0805, 1%	MULTI. SOURCE
18	1	R5	STANDARD	RES, 11.0 KΩ, 0805, 1%	MULTI. SOURCE
19	1	R6	STANDARD	RES, 16.2 KΩ, 0805, 1%	MULTI. SOURCE
20	1	R7	STANDARD	RES, 95.3 KΩ, 0805, 1%	MULTI. SOURCE
21	1	R8	STANDARD	RES, 26.7 KΩ, 0805, 1%	MULTI. SOURCE
22	1	R11	STANDARD	RES, 2.7 Ω, 0805, 5%	MULTI. SOURCE
23	1	R10	STANDARD	RES, 10 Ω,, 0805, 5%	MULTI. SOURCE
24	1	R16	STANDARD	RES, 15 Ω,, 0805, 5%	MULTI. SOURCE
25	1	R12	STANDARD	RES, 3.01 KΩ, 0805, 1%	MULTI. SOURCE
26	1	R13	STANDARD	RES, 3.32 KΩ, 0805, 1%	MULTI. SOURCE
27	1	R15	STANDARD	RES, 91 KΩ, 0805, 5%	MULTI. SOURCE

Table 5–1. EVM Bill of Materials (Continued)

ITEM	QTY	REF. DES./COMM	PART NO.	PART DESCRIPTION	APPROVED VENDOR
28	4	R17A,R17B,R17C, R17D	STANDARD	(4 PARALLEL RES) RES, 1 Ω, 0805, 5%	MULTI. SOURCE
29	1	R18	STANDARD	RES, 1 Ω, 0805, 5%, See Item 28	MULTI. SOURCE
30	1	U1	TL1454CD	IC, DUAL PWM Controller, SOIC-16	TI
31	1	CR1	SS12	DIO, RECT, SCHOTTKY, 1A, 20 V, DO-214 AC	GI
ALT	0	Alt. part for item 31	SK12		DI
32	1	CR2	SS32	DIO, RECT, SCHOTTKY, 3A, 20 V, DO-214 AB	GI
ALT	0	Alt. part for item 32	SK32		DI
33	1	Q1	IRLL014	FET, MOS, N-Channel, 0.2 Ω 60 V, 2.7 A, SOT-223	IR
34	1	Q2	TPS1110D	FET, MOS, P-Channel, 0.06 Ω, 12 V, 6A, SOIC-8	TI
35	1	L1	CD43-2R7MC	IND, PWR, 2.7 μH, 0.052 Ω, 2.43 A	SUMIDA
36	1	L2	CD105-100MC	IND, PWR, 10 μH, 0.06 Ω, 2.6 A	SUMIDA
37	1	P1	TSW-104-14-G-S	HEADER, 4P, 0.100 Center, Straignt	SAMTEC
38	1	P2	TSW-105-14-G-S	HEADER, 5P, 0.100 Center, Straight	SAMTEC
39	1		STANDARD	FAB, PCB	MULTI. SOURCE
40	2	JMP1,JMP2		JUMPER, #22 Bus wire	MULTI. SOURCE

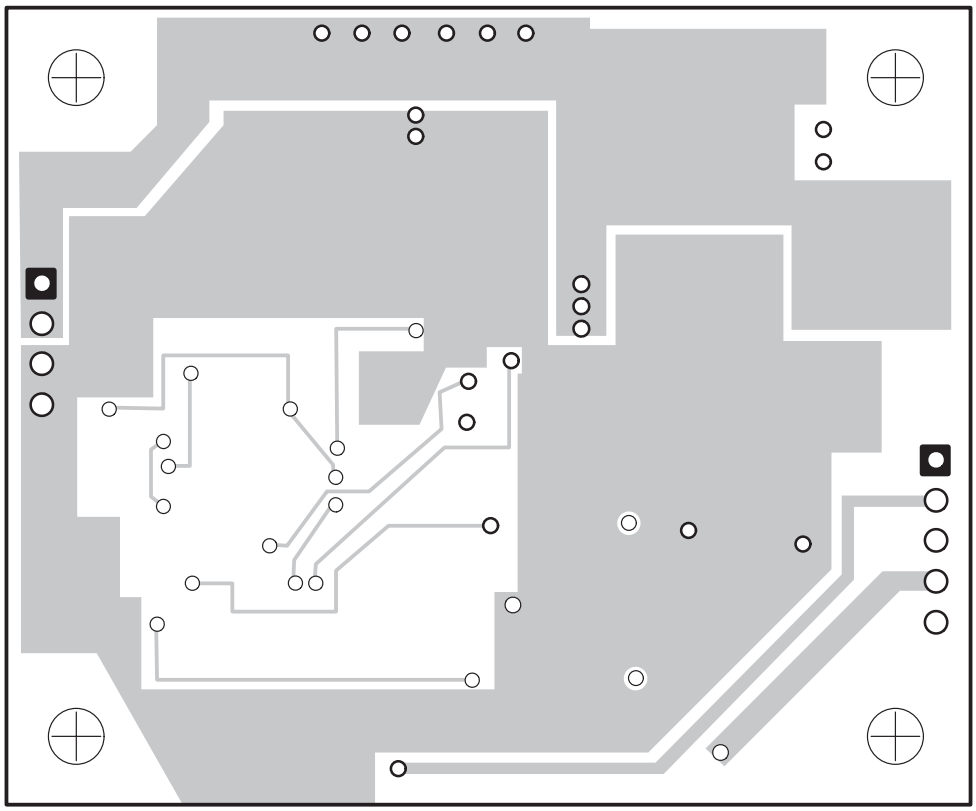
5.3 EVM Board Layout

Figure 5–2. EVM Board Layout Component Side



Component Side

Figure 5–3. EVM Board Layout Solder Side



Solder Side (Top View)