

TI Designs

Solid State Relay 24-V AC Switch With Galvanic Isolation



TI Designs

The solid state relay 24-V AC switch reference design is a single relay replacement that enables efficient power management for a low-power alternative to standard electromechanical relays. The OFF mode provides energy to the system controller, and the ON mode can switch fast enough to allow backup battery charging where electromechanical relays cannot. The transformer enables isolation and a voltage multiplier ensures enough voltage to safely turn on MOSFETs.

Design Resources

TIDA-00751	Design Folder
CSD19537Q3	Product Folder
SN74LVC1G19	Product Folder
SN74AUP1G74	Product Folder
SN74AUP3G14	Product Folder
LMC555	Product Folder

Design Features

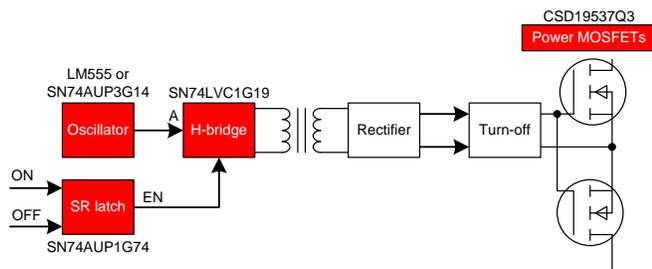
- Single Electromechanical Relay Replacement
- Low-Power Solid State Relay With Silent Operation
- No Clicking Noise
- <1- μ s Turn-on and Turn-off Switching Time
- In OFF Mode, 24-V AC Line Provides Energy to the System
- <200- μ A Consumption in OFF Mode
- Cost Efficient BOM

Featured Applications

- Building Automation
- HVAC Systems
- Thermostats



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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Logic input level range	3.3 V	Section 2.4
Max power input voltage	80 V	Section 2.1
Current range	2 to 6 A _{RMS}	Section 6.2
Isolation	Transformer (2500-V AC)	Section 3
Turn-on and turn-off time	< 1 μs	Section 7.2
On-state current consumption	1.2 mA	Section 7.1
Off-state current consumption	< 200 μA	Section 4.4.1
Operating temperature	-40°C to 85°C	
Working environment	Indoor building automation	

2 System Description

A solid-state relay (SSR) is an electronic switching device that switches on or off when a small external voltage is applied across its control terminals. SSRs consist of an input logic to respond to an appropriate input (control signal), a solid-state electronic switching device to switch power to the load circuitry, and a coupling mechanism to enable the control signal to activate this switch without mechanical parts. The SSR may be designed to switch either AC or DC to the load. It serves the same function as an electromechanical relay, but has no moving parts.

SSR use power semiconductor devices such as thyristors or transistors to switch currents up to a hundred amperes. SSRs have fast switching speeds compared with electromechanical relays and have no physical contacts to wear out. To apply an SSR, the user must consider their lower ability to withstand momentary overload, compared with electromechanical contacts, and their higher "on" state resistance. Unlike an electromechanical relay, an SSR provides only limited switching arrangements (single-pole, single-throw switching).

The control signal must be coupled to the controlled circuit in a way that provides galvanic isolation between the two circuits. SSRs can be coupled using a reed relay, transformer, or photocoupler. This design uses a transformer-coupled SSR, which permits to transfer signal and power over isolation barrier and at the same time to keep component number, footprint, and cost low.

2.1 N-Channel Power MOSFET

In residential as well as commercial building automation application, 24-V AC is used as standard power supply voltage. When SSR is used in thermostat applications as replacement for the mechanical relay, the maximum operating voltage of the power switch can be two times the nominal voltage. Taking into account the input voltage variations as well temporary overvoltage, the peak voltage for nominal 24-V AC power supply can rise up to 42 V. In the worst case, the power switch can operate at up to 84 V. For that reason, this design uses power MOSFETs with a breakdown voltage of 100 V.

2.2 Input Control Logic

In thermostat applications, power consumption is one of the main concerns. To ensure a long battery life, the control logic, in most cases a dedicated microcontroller, provides a control signal for a short period of time before it goes in a low power or sleep mode. Turn-on and turn-off signals are two different signals that active for short period of the time. For that reason, the input control logic uses the Texas Instruments low power AUP single-gate SR latch SN74AUP1G74. This circuit will set the output ENABLE signal (active LOW) on the short ON pulse and reset the signal when a short OFF signal is applied.

2.3 Oscillator

In this TI Design, two oscillator circuits are used. For the applications where cost is a main concern, the circuit is designed using Schmitt-trigger inverter gates. A second circuit using the LM555 is designed for applications where power consumption is a main concern. Both circuits will produce a 300-kHz signal used to turn on power MOSFETs. In some thermostat applications, multiple mechanical relays are used. For these applications, a signal-form single oscillator circuit can be used for multiple SSRs, additionally reducing cost and power consumption of the replacement.

2.4 Decoder and Demultiplexer

The SN74LVC1G19 was chosen as the decoder and demultiplexer device. In this reference design, the demultiplexer enables the oscillator output signal to be turned off when the high-frequency square wave is not needed at the primary side of the transformer. The demultiplexer also acts as an H-Bridge to create the AC square wave signal from the 3.3-V power supply. The SN74LVC1G19 was chosen because the wide range input voltage that goes up to 5 V and a ± 24 -mA output drive at 3.3 V. This reference design driver needs a maximum output of 4 mA from the H-Bridge to drive the transformer; therefore, this part has significant robustness to run for long periods. The SN74LVC1G19 was also chosen because of its low propagation delay and offers live insertion, partial power-down mode, and, most importantly, back drive protection.

3 Block Diagram

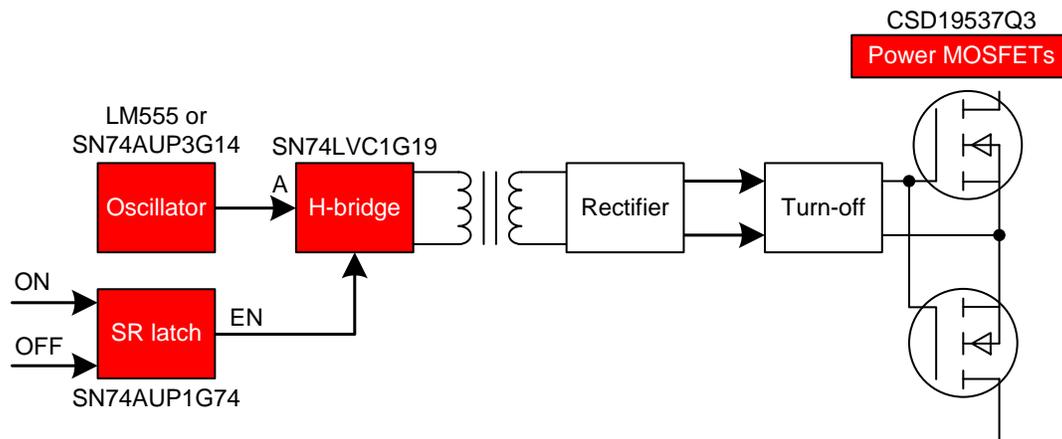


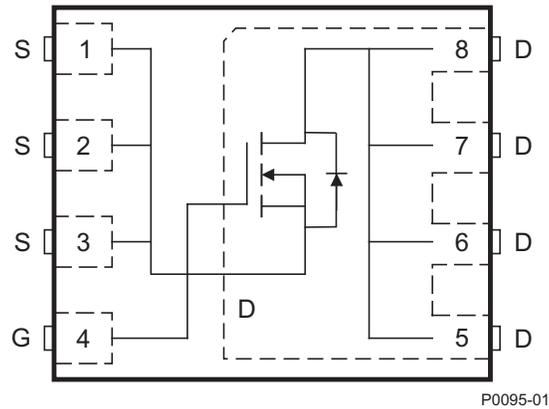
Figure 1. TIDA-00751 Block Diagram

3.1 Highlighted Products

The solid state relay reference design features the following devices:

- CSD19537Q3: 100-V N-channel NexFET power MOSFET
- SN74LVC1G19: 1-of-2 decoder and demultiplexer
- SN74AUP3G14: Schmitt-trigger inverter gate
- LM555: Low-power CMOS timer
- SN74AUP1G74: Single positive-edge-triggered D flip-flop

3.1.1 CSD19537Q3

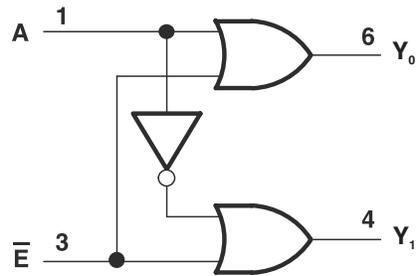


P0095-01

Figure 2. CSD19537Q3 Block Diagram (Top View)

Features:

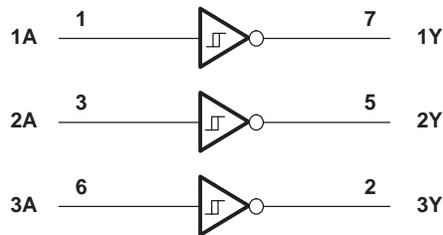
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- SON 3.3x3.3-mm plastic package

3.1.2 SN74LVC1G19

Figure 3. SN74LVC1G19 Functional Block Diagram
Features:

- Available in the Texas Instruments NanoFree™ package
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 4 ns at 3.3 V
- Low power consumption, 10- μ A maximum I_{CC}
- ± 24 -mA output drive at 3.3 V
- V_{OLP} (output ground bounce) < 0.8 V typical at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- V_{OHV} (output V_{OH} undershoot) > 2 V typical at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{OFF} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
 - 2000-V human-body model (A114-A)
 - 200-V machine model (A115-A)
 - 1000-V charged-device model (C101)

3.1.3 SN74AUP3G14
Table 2. Function Table

INPUT	OUTPUT
A	Y
High	Low
Low	High


Figure 4. SN74AUP3G14 Logic Diagram (Positive Logic)
Features:

- Available in the Texas Instruments NanoStar™ package
- Low static-power consumption ($I_{CC} = 0.9 \mu\text{A}$ maximum)
- Low dynamic-power consumption ($C_{PD} = 4.3 \text{ pF}$ typical at 3.3 V)
- Low input capacitance ($C_I = 1.5 \text{ pF}$ typical)
- Low noise: overshoot and undershoot $<10\%$ of V_{CC}
- I_{OFF} supports partial-power-down mode operation
- Wide operating V_{CC} range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O tolerant to support mixed-mode signal operation
- $t_{PD} = 4.3 \text{ ns}$ maximum at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22:
 - 2000-V human-body model (A114-B, Class II)
 - 1000-V charged-device model (C101)

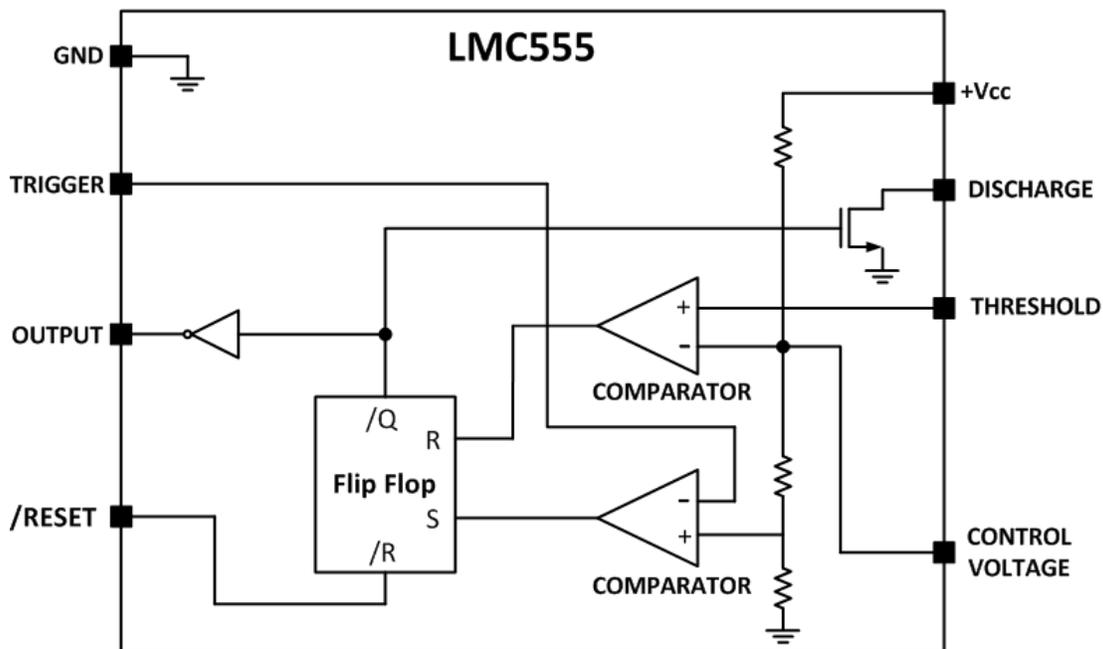
3.1.4 LMC555


Figure 5. LMC555 Functional Block Diagram

Features:

- Less than 1-mW typical power dissipation at 5-V supply
- 3-MHz astable frequency capability
- 1.5-V supply operating voltage ensured
- Output fully compatible with TTL and CMOS logic at 5-V supply
- Tested to -10-mA, 50-mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers
- Available in 8-pin VSSOP package and 8-bump DSBGA package

3.1.5 SN74AUP1G74

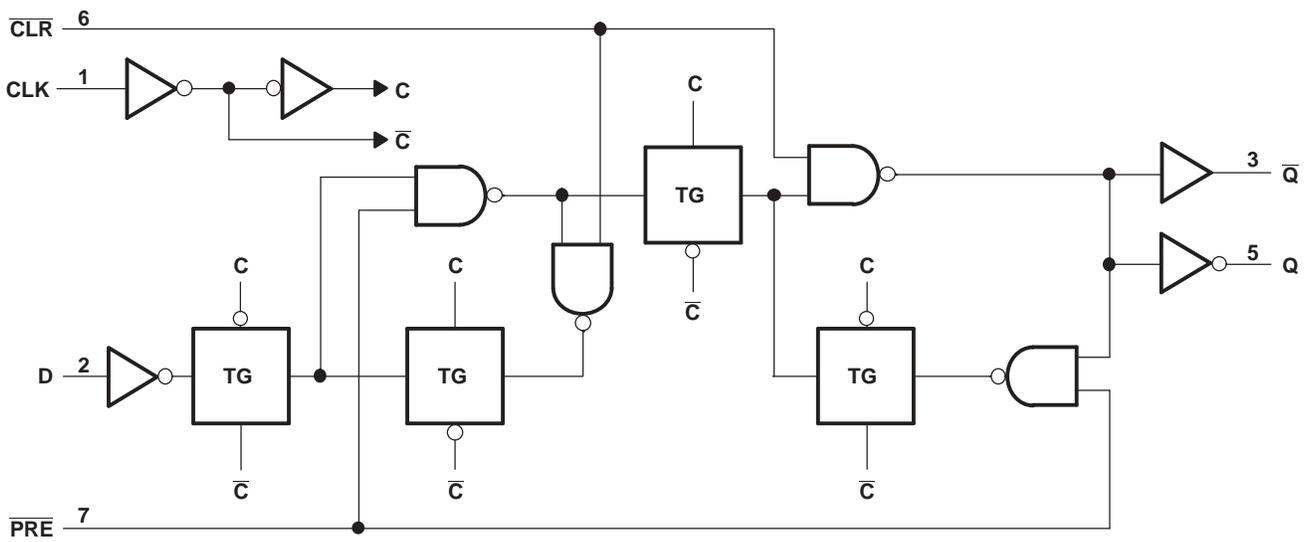


Figure 6. SN74AUP1G74 Functional Block Diagram

Features:

- Available in the Texas Instruments NanoStar package
- Low static-power consumption: $I_{CC} = 0.9 \mu\text{A}$ maximum
- Low dynamic-power consumption: $C_{pd} = 5.5 \text{ pF}$ typical at 3.3 V
- Low input capacitance: $C_i = 1.5 \text{ pF}$ typical
- Low noise: overshoot and undershoot $< 10\%$ of V_{CC}
- I_{OFF} supports partial-power-down mode operation
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the input ($V_{HYS} = 250 \text{ mV}$ typical at 3.3 V)
- Wide operating V_{CC} range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O tolerant to support mixed-mode signal operation
- $t_{PD} = 5 \text{ ns}$ maximum at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22
 - 2000-V human-body model (A114-B, Class II)
 - 1000-V charged-device model (C101)

4 System Design Theory

4.1 Basic SSR Theory

SSRs are integrated electrical circuits that act as a mechanical switch. SSRs have no moving parts, hence the device name. The relays can be switched much faster and are not prone to wear because of the absence of moving parts. Another advantage is that less current and voltage is needed for SSRs to control high-voltage AC loads.

Electric isolation is still achieved in SSRs as with other electromechanical relays. Both SSRs and electromechanical relays use two different circuits: a control circuit and a separate circuit for switching the load. Transformers or optocouplers are used to isolate the control side from the high-voltage switching side of the relay. This reference design implements isolation with a transformer.

4.2 Power Management Theory

The solid state relay 24-V AC switch reference design power is used to charge either the battery or capacitor the thermostat runs off of. A normal wiring of such a system is shown in Figure 7. In order to charge the battery or capacitor from the 24-V AC line, a bridge rectifier turns the AC signal into a DC voltage.

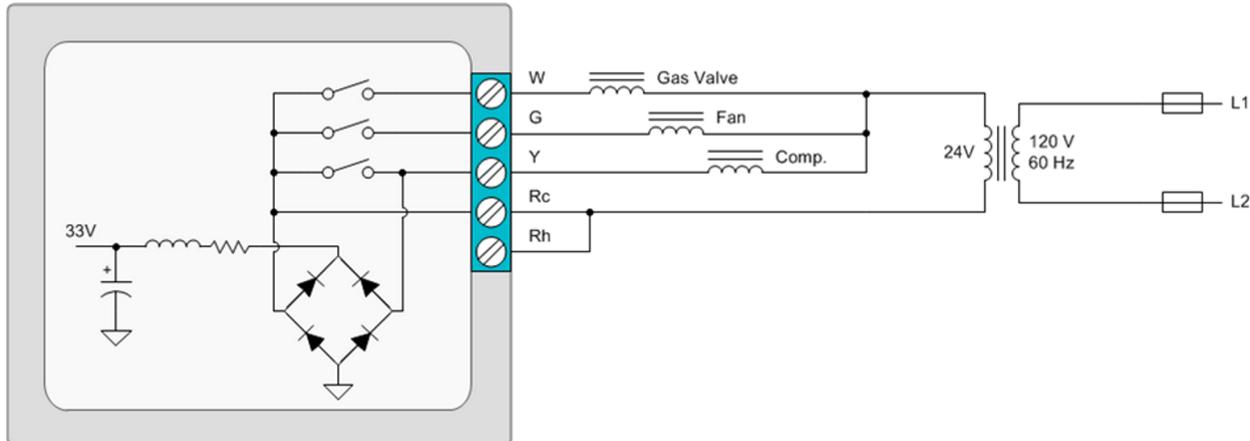


Figure 7. Standard Wiring of Thermostat

The rectifier allows charging of the battery or capacitor when the low-voltage relay is open, or when the HVAC system is not powering the gas valve, fan, or compressor. The high-voltage electromechanical relay that switches on each of the main high-voltage systems is controlled by the low-voltage relay. **Figure 8** shows the charging of the battery during HVAC inactive mode.

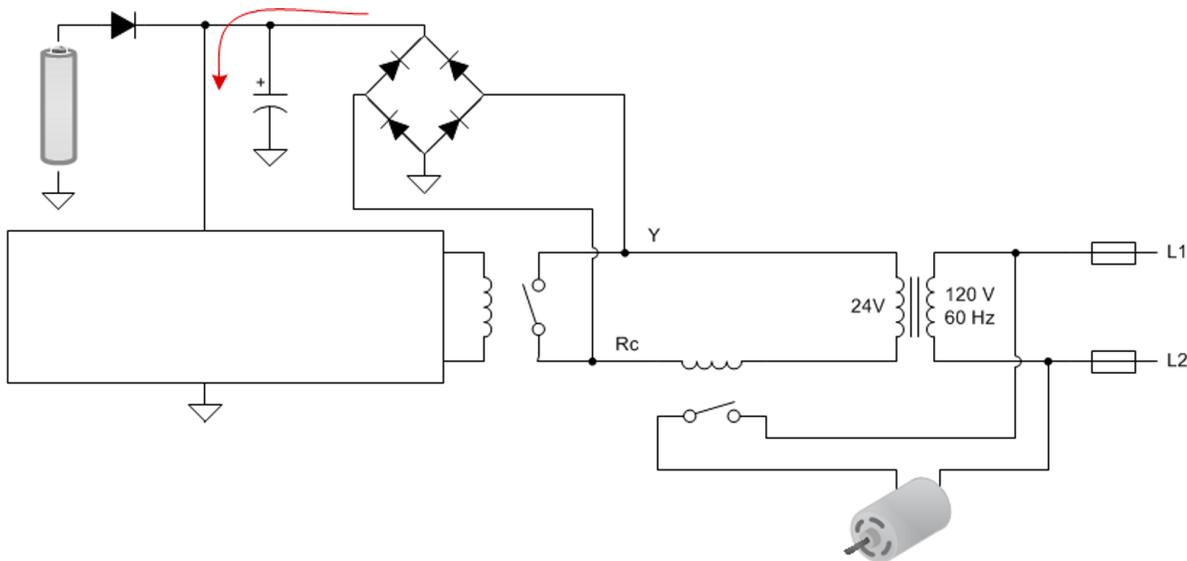


Figure 8. Battery Charging During HVAC Inactive Mode

During active heating and cooling the thermostat must be powered off of the battery. The circuit configuration during active mode is shown in **Figure 9**.

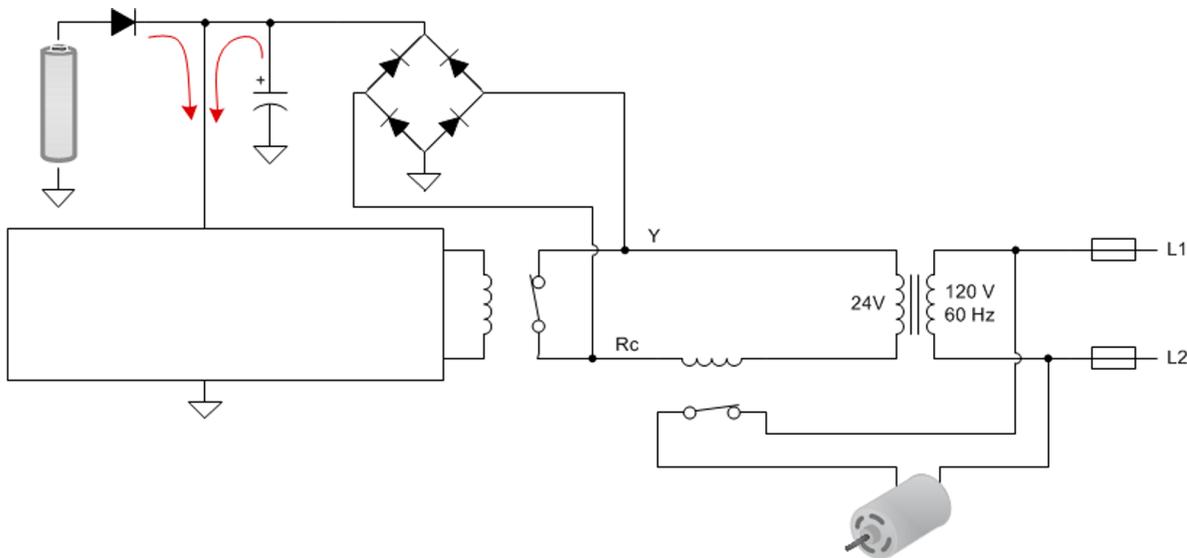


Figure 9. HVAC Active Mode, Thermostat Running off Battery

An adjustment to the power implementation must be made if the battery or capacitor is not large enough to power the control board during a long active mode heating or cooling. By quickly turning off and on the low-voltage relay, a charge can be added to the battery while in "active" mode. Using an SSR in place of the low-voltage electromechanical switch is one way to accomplish the active mode power management. The SSR switch much faster than the electromechanical relays. The switching frequency of the SSR must be high enough to not interrupt the power to the heater, fan, or compressor.

4.3 MOSFET Selection

When SSR is used to turn on and off inductive load, take care to limit overvoltage spikes during the turn-off process. In some thermostat applications where the load power supply also provides additional power to the thermostat, a rectifier bridge and a capacitor will act as snubber circuit absorbing energy from inductive load during turn off. When this circuit is missing from the application, an additional transient voltage suppression (TVS) diode needs to be added. For the DC application unidirectional TVS is sufficient, where for AC application a bidirectional TVS is needed.

4.4 Oscillator Design Theory

The oscillator circuitry generates a 3.3-V, 50% duty cycle square wave that is fed into the H-bridge. Two astable multivibrator circuits are included in this reference design for the implementation of the oscillator function. The first circuit uses the LMC555 timer to implement a low supply current oscillator version. The second circuit uses the SN74AUP3G14 Schmitt-trigger inverter to implement a low-cost oscillator version. The design of these oscillator circuits are discussed in the following sections. The H-bridge design is discussed in the next section of this document.

4.4.1 Timer-Based Oscillator Design

The timer-based oscillator design uses a modified oscillator topology based on the 555 timer circuit. The modification compared to traditional implementations uses the output signal to charge and discharge the timing capacitor instead of using the discharge output of the timer circuit. This modification forces the charge and discharge current to flow through a single resistor, thereby producing a 50% duty cycle oscillator output. A simplified schematic of this oscillator circuit is shown in [Figure 10](#).

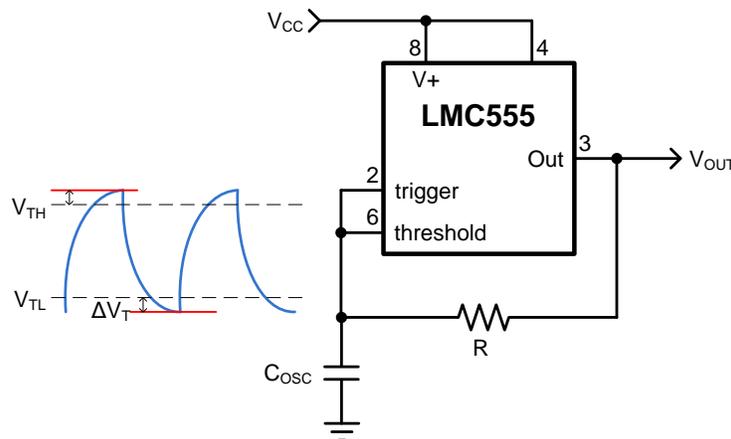


Figure 10. LMC555 Timer-Based Oscillator Schematic

Based on the capacitor voltage waveform shown in [Figure 10](#), the following equations can be used to describe the behavior of the circuit and to make adjustments to the component values. As shown in the waveform, the propagation delay of the timer circuit needs to be taken into account to accurately predict the output frequency and supply current. The finite propagation delay causes the capacitor voltage to be larger than what is predicted by the DC thresholds of the timing circuit. Because of this, there is additional charge that needs to be added or removed before reaching the next threshold. This additional charge or discharge time plus the finite prop delay adds to the time needed to complete each oscillator half cycle.

The excess voltage is given by the following:

$$V_{\text{EXTRA}} = V_{\text{CC}} \left(1 - e^{-\frac{t_{\text{PD}}}{\text{RC}}} \right) \cong \frac{t_{\text{PD}}}{\text{RC}} \times V_{\text{CC}}, \quad \text{since } e^{-\frac{t_{\text{PD}}}{\text{RC}}} \approx 1 - \frac{t_{\text{PD}}}{\text{RC}} \quad (1)$$

with $\text{RC} \gg t_{\text{PD}}$

With the excess voltage defined, the charge and discharge times and therefore the output frequency is given by the following:

$$t_{\text{D}} = -\text{RC} \left[\ln \frac{V_{\text{TL}}}{V_{\text{CC}}} - \ln \frac{V_{\text{INIT}}}{V_{\text{CC}}} \right] + t_{\text{PD}} = -\text{RC} \left[\ln \frac{1}{3} - \ln \left(\frac{2}{3} + \frac{t_{\text{PD}}}{\text{RC}} \right) \right] + t_{\text{PD}} = \text{RC} \left[\ln \left(2 + \frac{3 \times t_{\text{PD}}}{\text{RC}} \right) \right] + t_{\text{PD}} \quad (2)$$

$$\begin{aligned} t_{\text{C}} &= -\text{RC} \left[\ln \left(1 - \frac{V_{\text{TH}}}{V_{\text{CC}}} \right) - \ln \left(1 - \frac{V_{\text{INIT}}}{V_{\text{CC}}} \right) \right] + t_{\text{PD}} = -\text{RC} \left[\ln \left(\frac{1}{3} \right) - \ln \left(\frac{2}{3} + \frac{t_{\text{PD}}}{\text{RC}} \right) \right] + t_{\text{PD}} \\ &= \text{RC} \left[\ln \left(2 + \frac{3 \times t_{\text{PD}}}{\text{RC}} \right) \right] + t_{\text{PD}} \end{aligned} \quad (3)$$

$$T_{\text{OSC}} = t_{\text{C}} + t_{\text{D}} = 2 \left\{ \text{R} \times (\text{C}_{\text{OSC}} + \text{C}_{\text{IN}}) \left[\ln \left(2 + \frac{3 \times t_{\text{PD}}}{\text{R}(\text{C}_{\text{OSC}} + \text{C}_{\text{IN}})} \right) \right] + t_{\text{PD}} \right\}, \quad f_{\text{OSC}} = \frac{1}{T_{\text{OSC}}} \quad (4)$$

Using typical datasheet values of 100 ns for t_{PD} , thresholds of $V_{\text{CC}}/3$ and $2V_{\text{CC}}/3$ for V_{TL} and V_{TH} , respectively, a measured nominal value of 15 pF for C_{IN} , and a nominal value of 100 pF for C_{OSC} , the value of the resistor needed to produce an output frequency of 300 kHz as an example is 17.83 kΩ, or 17.8k in a 1% standard value resistor. Because the output frequency is dependent on timer circuit parameters, which will vary from part to part, it may be necessary to adjust the resistor value slightly if the output frequency needs to have a tight tolerance across multiple boards. Also note that observing Equation 4, assuming a negligible timer circuit propagation delay, will yield the more commonly quoted equation for astable operation of the timer circuit, which is:

$$f_{\text{OSC}} = \frac{1}{2 \times 0.693 \times \text{R} \times \text{C}_{\text{OSC}}} \quad (5)$$

Making use of this analysis, the equation for power supply current is derived as follows:

$$\begin{aligned} I_{\text{CC}} &= I_{\text{Q}} + \text{C}_{\text{T}} \times V_{\text{OSC}} \times f_{\text{OSC}} + \text{C}_{\text{PD}} \times V_{\text{CC}} \times f_{\text{OSC}} = I_{\text{Q}} + (\text{C}_{\text{OSC}} + \text{C}_{\text{IN}}) \left[\frac{t_{\text{PD}}}{\text{R}(\text{C}_{\text{OSC}} + \text{C}_{\text{IN}})} \times V_{\text{CC}} + \frac{V_{\text{CC}}}{3} \right] \times f_{\text{OSC}} + \text{C}_{\text{PD}} \times V_{\text{CC}} \times f_{\text{OSC}} \\ &= I_{\text{Q}} + V_{\text{CC}} \times f_{\text{OSC}} \left[\frac{t_{\text{PD}}}{\text{R}} + \frac{(\text{C}_{\text{OSC}} + \text{C}_{\text{IN}})}{3} + \text{C}_{\text{PD}} \right] \end{aligned} \quad (6)$$

The variables I_{Q} and t_{PD} can be taken directly from the LMC555 datasheet for the timer circuit and are 80 μA and 100 ns typical, respectively. The input capacitance, C_{IN} , was measured to be ~15 pF on average for a small sample size. The internal dynamic switching current of the timer circuit power supply is not given in the datasheet but can be approximated, and represented as C_{PD} in equation 6, from measured supply current data over multiple frequencies with a fixed power supply voltage. The resulting value of C_{PD} is estimated to be ~55 pF. Figure 11 shows the measured supply current compared to the calculated data using Equation 6.

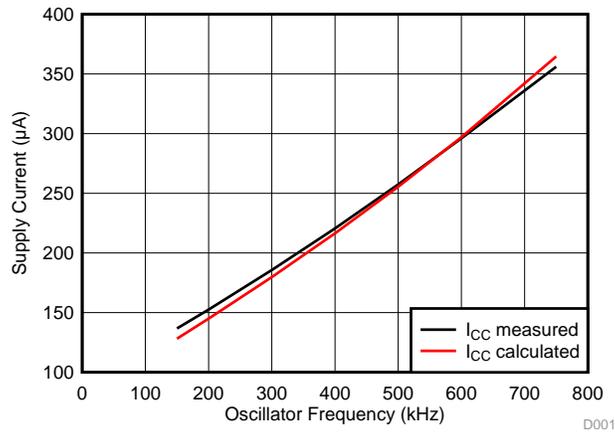


Figure 11. LMC555 Timer-Based Oscillator Supply Current Comparison

For more information on C_{PD} and calculating power dissipation in CMOS logic circuits, please see *CMOS Power Consumption and Cpd Calculation* ([SCAA035](#)).

4.4.2 Schmitt-Trigger Inverter-Based Oscillator Design

The inverter-based oscillator design uses a ring-of-three astable multivibrator architecture. A simplified schematic of this oscillator circuit is shown in [Figure 12](#).

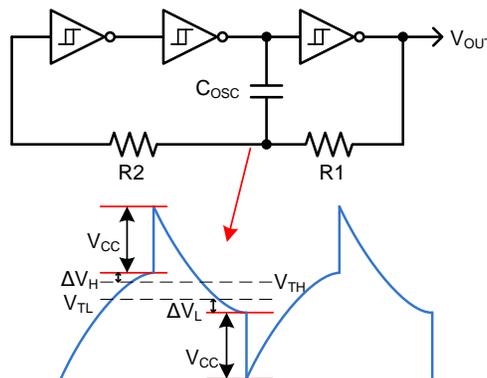


Figure 12. Schmitt-Trigger Inverter-Based Oscillator Schematic

There are inverter-based oscillator designs that only require two inverters; however, these architectures are known to have problems with startup when using small values of C_{OSC} . Using the smallest possible value of C_{OSC} in this circuit is important in minimizing the supply current because of the large voltage appearing across this capacitor. The lower limit for the value of C_{OSC} should be the constraint that C_{OSC} is much greater than the sum of the parasitic and stray capacitances which are present in the circuit in the absence of C_{OSC} . The resistor R2 is added to limit voltage excursions above and below the supply rails at the input of the first inverter. Depending on the oscillator frequency and stray capacitance across R2, there is still a possibility that the voltage at the input of the first inverter can exceed the supply rails, in which case R2 will also serve to limit the parasitic current to prevent damage to the inverter IC. Schmitt-trigger devices are preferred in this architecture because the input to the first inverter can have slow transitions. Use of Schmitt-trigger devices will prevent large shoot-through currents in the first stage as well as providing robustness to coupled noise by providing hysteresis in the switching threshold voltage.

Based on the capacitor voltage waveform shown in [Figure 12](#), the following equations can be used to describe the behavior of the circuit and to make adjustments to the component values. As shown in the waveform, the propagation delay of the inverters and of the R2, C_{IN} combination need to be taken into account in order to accurately predict the output frequency and supply current. The finite propagation delay causes the capacitor voltage to be larger than what is predicted by the DC thresholds of the Schmitt-trigger inverters and because of this, there is additional charge that needs to be added or removed before reaching the next threshold. This additional charge or discharge time plus the finite prop delay adds to the time needed to complete each oscillator half cycle. Further complicating the analysis of this circuit is the fact that C_{IN} is non-linear with input voltage. The non-linearity of this capacitance has been approximated for this analysis as will be described in this section. More importantly, depending on the value chosen for R2, this capacitance will cause a difference in the excess voltage on charge and discharge cycles; this ultimately leads to a duty cycle that is not the ideal 50% that is expected. The excess voltages are given by the following:

$$\Delta V_H = V_{CC} \left(1 - e^{-\frac{-(t_{del} + 0.693 \times R2 \times C_{IN_CH})}{R1 \times C_{OSC}}} \right) \quad (7)$$

$$\Delta V_L = (V_{CC} + V_{TH} + \Delta V_H) \left(1 - e^{-\frac{-(t_{del} + 0.693 \times R2 \times C_{IN_CL})}{R1 \times C_{OSC}}} \right) \quad (8)$$

The variable t_{del} is the sum of the propagation delays due to the first two inverter stages and was measured to be ~12 ns in this design. The variable V_{TH} is the positive going trip point taken from the datasheet for the Schmitt-trigger inverters. The input capacitance estimate based on voltage measurements in the circuit are $C_{IN_CH} \sim 2.39$ pF and $C_{IN_CL} \sim 1.42$ pF. With the excess voltage defined, the charge and discharge times, and therefore the output frequency, is given by the following:

$$t_D = -R1 \times C_{OSC} \times \ln \left(\frac{V_{TL} - \Delta V_L}{V_{CC} + V_{TH} + \Delta V_H} \right) = R1 \times C_{OSC} \times \ln \left(\frac{V_{CC} + V_{TH} + \Delta V_H}{V_{TL} - \Delta V_L} \right) \quad (9)$$

$$t_C = -R1 \times C_{OSC} \left[\ln \left(1 - \frac{V_{TH} + \Delta V_H}{V_{CC}} \right) - \ln \left(1 - \frac{V_{TL} - \Delta V_L - V_{CC}}{V_{CC}} \right) \right] = R1 \times C_{OSC} \left[\ln \left(\frac{2 \times V_{CC} - V_{TL} + \Delta V_L}{V_{CC} - V_{TH} - \Delta V_H} \right) \right] \quad (10)$$

$$\begin{aligned} T_{OSC} &= t_C + t_D = R1 \times C_{OSC} \left[\ln \left(\frac{2 \times V_{CC} - V_{TL} + \Delta V_L}{V_{CC} - V_{TH} - \Delta V_H} \right) + \ln \left(\frac{V_{CC} + V_{TH} + \Delta V_H}{V_{TL} - \Delta V_L} \right) \right] \\ &= R1 \times C_{OSC} \times \ln \left[\left(\frac{2 \times V_{CC} - V_{TL} + \Delta V_L}{V_{CC} - V_{TH} - \Delta V_H} \right) \left(\frac{V_{CC} + V_{TH} + \Delta V_H}{V_{TL} - \Delta V_L} \right) \right], \quad f_{OSC} = \frac{1}{T_{OSC}} \end{aligned} \quad (11)$$

The variable V_{TL} is the negative going trip point taken from the datasheet for the Schmitt-trigger inverters. Observing the previous equations, there are a couple of important points to be considered. First, ΔV_L will be larger than ΔV_H . Secondly, in applying this point to equation 11, the denominator of the second term in the natural log function is at risk of going to zero for frequencies where the sum of the circuit delays and the delay due to the combination of R2, C_{IN} becomes a large percentage of the intended delay due to R1 and C_{OSC}. In reality, the oscillator capacitor will discharge to a value equal to the C_{IN} discharge current times R2 and remain at that level until the lower threshold of the input inverter is reached. While this behavior is not comprehended by these equations, the saturation of the output frequency for a fixed value of R2 is reached at frequencies much lower than the frequency where the predicted ΔV_L approaches V_{TL} . Along this same line of reasoning, R2 will ultimately limit the upper frequency of the oscillator. This is correctly predicted by the above equations, albeit erring on the conservative side.

In order to limit the effect of the non-linear C_{IN} and to achieve a duty cycle that is as close as possible to 50% while still providing a reasonable limit to parasitic currents due to voltage excursions exceeding the supply rails at the input of the first inverter, this design chose to make R1 and R2 equal. Using Equation 11, the value of R1 can be calculated for a 300-kHz operating frequency using the following values for the other variables: $V_{TL} = 1\text{ V}$, $V_{TH} = 2\text{ V}$, $C_{OSC} = 100\text{ pF}$, $t_{del} = 12\text{ ns}$, $C_{IN,CH} = 2.39\text{ pF}$, $C_{IN,CL} = 1.42\text{ pF}$, and $V_{CC} = 3.3\text{ V}$. This results in the following calculated values: $f_{OSC} = 300.146\text{ kHz}$, $R1 = R2 = 9.9\text{ k}\Omega$.

Making use of this analysis, the equation for power supply current is derived as follows:

$$I_{CC} = I_Q + 3C_{PD} \times V_{CC} \times f_{OSC} + V_{CC} \times f_{OSC} \sum C_L + C_{OSC} \times V_{CC} \times f_{OSC} + I_{PARA}$$

$$= I_Q + f_{OSC} \left[V_{CC} \left(3C_{PD} + \sum C_L \right) + C_{OSC} \times V_{CC} \right] + I_{PARA} \tag{12}$$

where $V_{OSC} = 2V_{CC} + [V_{TH} + \Delta V_H - (V_{TL} - \Delta V_L)]$

The variables I_Q and C_{PD} can be taken directly from the datasheet for the Schmitt-trigger inverters and are $0.9\text{ }\mu\text{A}$ and 4.5 pF typical, respectively. The $\sum C_L$ term represents the sum of the capacitances found on the internal nodes of the oscillator circuit. For the input capacitance, an average of the $C_{IN,CH}$ and $C_{IN,CL}$ values is used for this calculation and is $\sim 2\text{ pF}$. The output capacitance is shown in the inverter datasheet to be 3 pF typical. In this analysis, an additional 2 pF was included to account for stray capacitances at the output nodes, with an additional 5 pF estimated for the inverter node connected to C_{OSC} . Capacitance measurements were performed on a standalone PCB to confirm these estimates. Referring to Figure 12, moving from left to right through the inverter string, $\sum C_L = 2\text{ pF} + 7\text{ pF} + 12\text{ pF} + 5\text{ pF} \approx 26\text{ pF}$. I_{PARA} is an error term that is independent of frequency. The exact source of I_{PARA} was not thoroughly investigated as part of this reference design, but it is suspected that this term is due to a combination of shoot-through current in the inverters along with voltage spikes appearing at the oscillator output, which exceed the supply rails at the state transitions due to coupling from the summing junction (node connecting R1, R2, and C_{OSC}) through the stray capacitance of R1. The value of this current is derived to be $\sim 84\text{ }\mu\text{A}$.

Figure 13 shows the measured supply current compared to the calculated data using Equation 12.

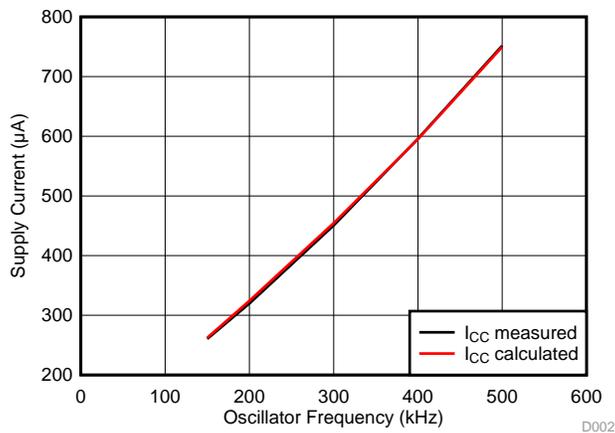


Figure 13. Schmitt-Trigger Inverter-Based Oscillator Supply Current Comparison

4.5 H-Bridge Design

When a 3.3-V square wave is put on the input of the H-bridge, the H-bridge outputs an AC signal. This 3.3-V AC signal drives the primary side of the transformer, enabling the transformer to operate. The SN74LVC1G19 is rated for approximately a 24-mA maximum output and gives enough robustness because the expected output peak current is 4 mA.

The SN74LVC1G19 is actually a demultiplexer, but it also works as an H-bridge. The device "decodes" the bit on input A and places a logic low on the matching address output, Y₀ or Y₁, when the enable pin (\bar{E}) is pulled low. The each output pin toggles (0 and 3.3 V) out of phase from each other when a square wave signal is input on the input 'A' pin of the SN74LVC part. [Table 3](#) demonstrates what is happening at logic level.

Table 3. H-Bridge Logic Table

INPUTS		OUTPUTS	
\bar{E}	A	Y ₀	Y ₁
Low	Low	Low	High
Low	High	High	Low
High	X	High	High

This part is ideal for driving the transformer because of its high-current output capability.

4.6 Choosing a Transformer

The transformer serves multiple purposes in the SSR reference design; it is used for electrical isolation and as a voltage multiplier. To ensure the power MOSFETs are in saturation at least 6.0 V is required. With only 3.3 V on the primary side of the transformer more voltage is required on the secondary side. Therefore, a higher secondary turn ratio is preferred on the transformer. This reference design's transformer has a turns ratio of 1:3.2. With a turn ratio of 3.2, the transformer outputs approximately 10 V on the secondary side when 3.3-V AC is applied on primary. When the power MOSFETs are in saturation there will be plenty of current to turn on the high-voltage electromechanical relays.

A suitable transformer for this type of design requires the ability to operate at high frequencies with low current losses. Low losses are key to enable direct switching between older electromechanical relays and a newer SSR because the electromechanical relays do not use much current. The losses can be adjusted by trying different transformer cores and controlling leakage flux.

5 Getting Started Hardware

5.1 Board Overview

For ease of use, all of the components, jumpers, and test points are located on the top side of the board. The signal chain starts on the left side of the board and moves to the right side of the board in a linear fashion. The terminal block (J3) located on the left edge of the board has connection points for the 3.3-V supply voltage and ground. Moving right, the first jumper (J1) selects which oscillator receives the supply voltage, and the next jumper (J2) selects which oscillator output is sent to the H-bridge. Colored test points denote signal chain test points and black test points are for ground connections.



Figure 14. TIDA-00751 Reference Design Hardware

The control signal pins are located just below the leftmost terminal block.

A visible blank area in the ground fill can be seen in the middle of the board. The blank area is added to the isolated properties of this design. The transformer is the only component that connects the two different ground planes or each side of the design, which are primary and secondary sides of the transformer.

5.2 Operating the Circuit

When the board is first powered on, the oscillator that is selected with the jumpers will start oscillating and the H-bridge will be enabled, allowing the power MOSFETs to turn on. To turn off MOSFETs, a short OFF pulse is sent. Since both inputs are active low and have pullup resistors, the pulse must pull down the signal to logic zero. The simplest way to do this is to short the pin to ground for a short time. The same method goes for the ON signal, shorting the #ON pin to ground will turn on the power MOSFETs.

6 Test Setup

The transformer's primary and secondary sides of the circuit are tested separately and the test setup for each are outlined in this section.

6.1 Primary Side Functional Test Setup

Two independent power supplies were needed for testing: one supply to power the 3.3-V rail and another to be a high-power load that the MOSFETs could control. A power supply that can source 3 A and drive at least 27 V at the same time was used as the load that the power MOSFETs were controlling. The secondary side of the transformer was connected to a constant 24-V, 3-A load at terminal block J5. A TVS diode was also inserted between the load connection points as a safety measure.

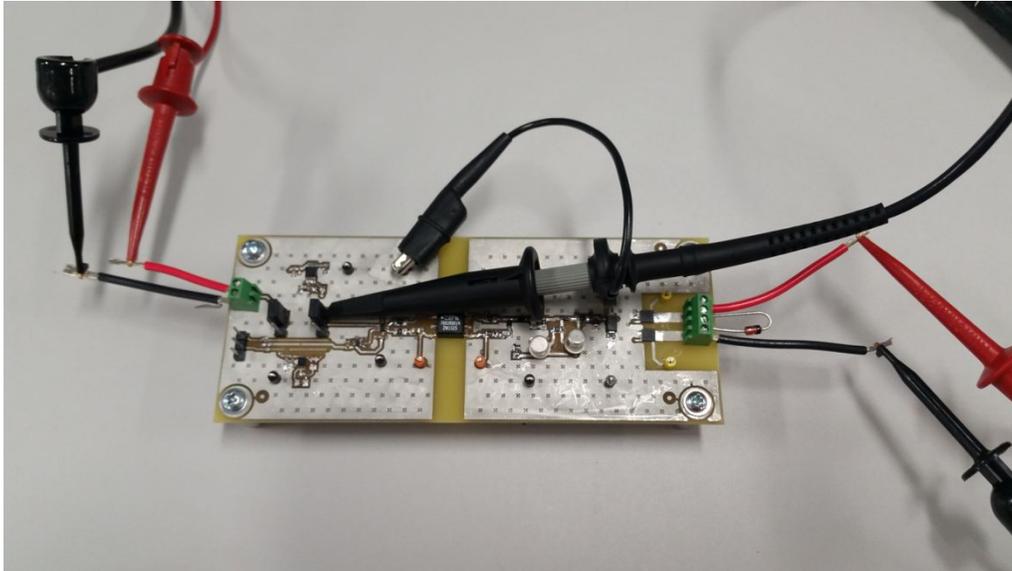


Figure 15. Prototype With Probes and Power Supplies Connected

In [Figure 15](#), the oscilloscope probe is set up to probe the output of Oscillator 1, and the TVS diode is connected between the load connection points. Header J2 has output pins for both oscillators, making probing easy.

To create the high-power load, a BK precision high-current DC regulated power supply is in series with a resistor decade box rated for 5 A was connected across the terminal block J5. The test setup with the power supplies, decade box, and temperature chamber is shown in Figure 16. The high-current power supply has the decade box connected to the positive terminal and the output of the decade box is the new positive terminal of the high-power load, the output is seen running into the temperature chamber in Figure 16.

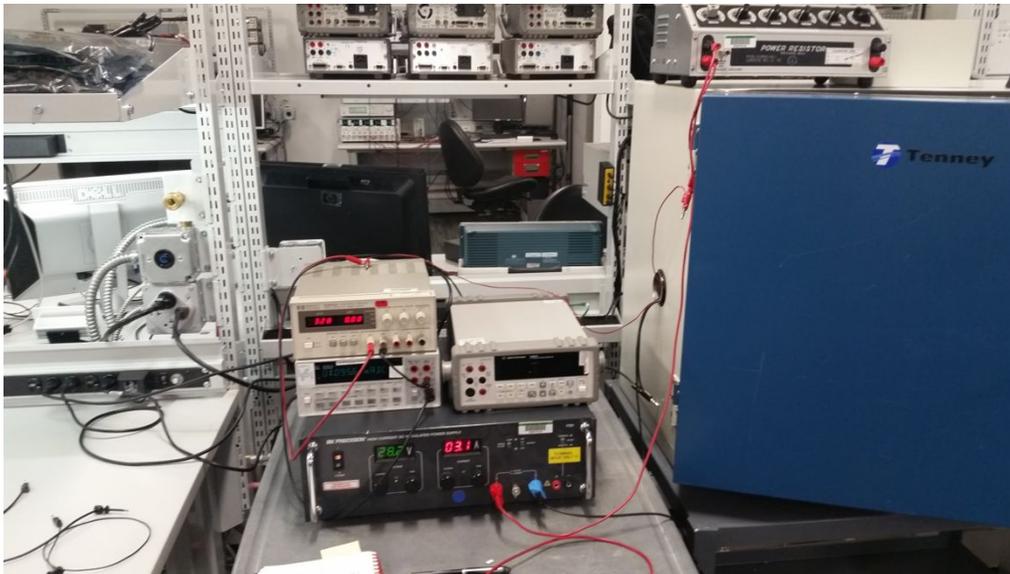


Figure 16. Primary Side Functional Test Setup

Inside the temperature chamber, each power connection has its own independent positive and negative connections.

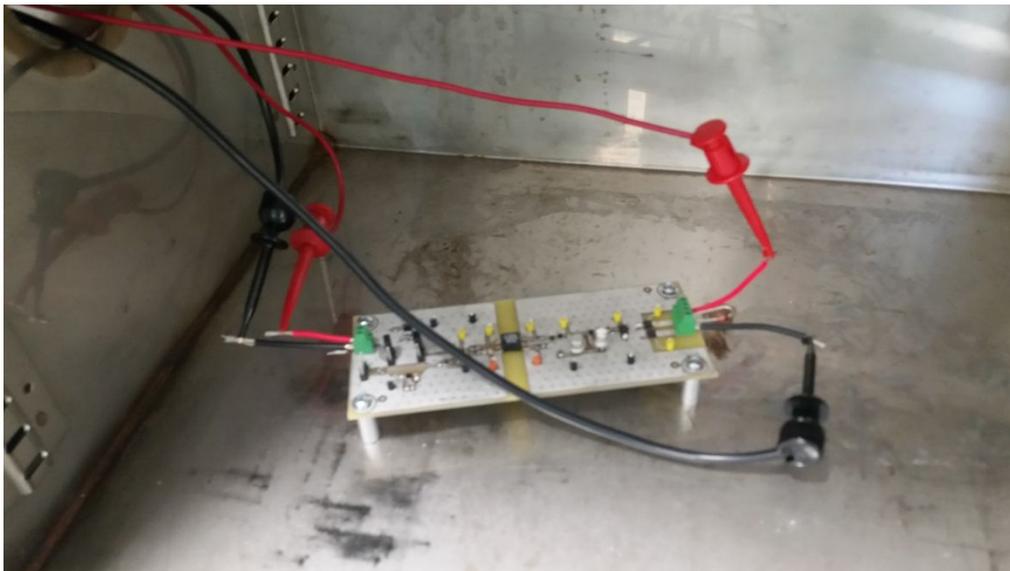


Figure 17. Inside Temperature Chamber

6.2 Transformer Secondary Side Test Setup

The secondary side test is to collect data of the amount of time for the turn on and off signal to propagate through the control circuit and to get waveform captures. The setup includes connecting power supplies as done in the primary side test, with one supply for the 3.3-V rail and the other high-power supply to act as the load supply. For this test, the power load was set to approximately 34 V with a current of 3.1 A. The temperature chamber was not used for this round of testing. [Figure 18](#) shows the connection points of several probe locations used to collect data.

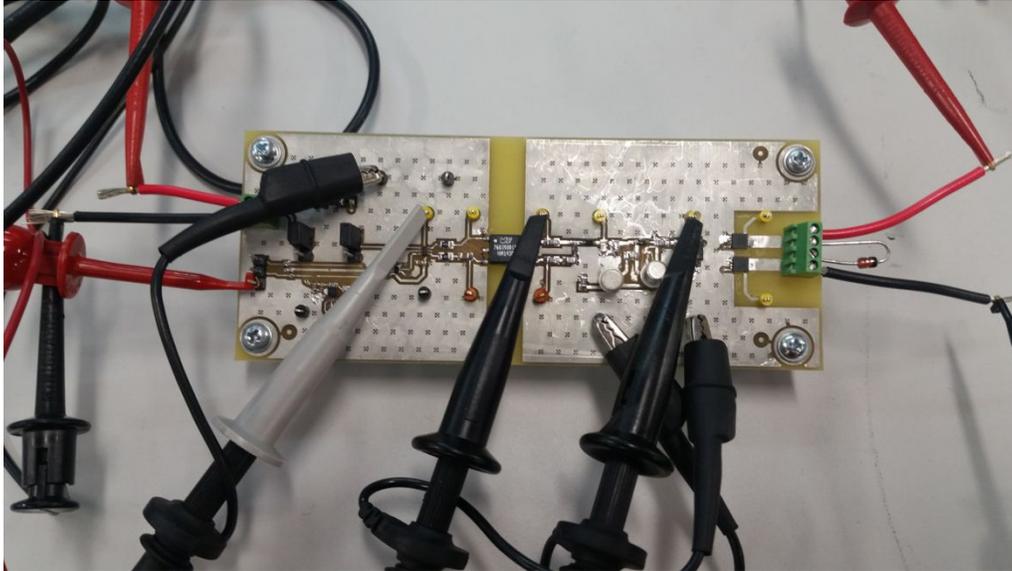


Figure 18. Probe Connections for Signal Chain Waveforms

To toggle the system on, the "#on" pin on jumper J4 was grounded, and grounding "#OFF" on J4 turns off the oscillator output, thus turning off the power MOSFETs.

7 Test Data

The transformer's primary and secondary sides of the circuit are tested separately, and the results are outlined in this section.

7.1 Primary Side Temperature Functional Test

This test varied temperature and supply voltage to characterize the supply current and oscillator frequency. The secondary side was connected to a constant 28-V, 3-A load.

Table 4. Oscillator and H-Bridge Temperature Functional Test

PARAMETER	TEMP 1 (0°C)			TEMP 2 (25°C)			TEMP 3 (50°C)		
	3 V	3.3 V	3.6 V	3 V	3.3 V	3.6 V	3 V	3.3 V	3.6 V
I _{CC1} (OC1) mA	1.501	1.68	1.857	1.249	1.395	1.543	1.432	1.606	1.777
Freq (OC1) kHz	305.2	308.1	310.4	300.4	303.4	305.8	296.1	299	301.6
I _{CC2} (OC2) mA	1.666	1.871	2.089	1.422	1.588	1.768	1.576	1.774	1.969
Freq (OC2) kHz	290.6	287.3	284.5	291.7	288.6	285.6	292.7	289.3	286.3

Both oscillators operating current react in a similar way to changing temperature and supply voltage, which is to be expected. The temperature on the outer ends of the temperature spectrum does increase the operating current as seen in [Figure 19](#). This could be because the passive component values have shifted slightly due to temperature.

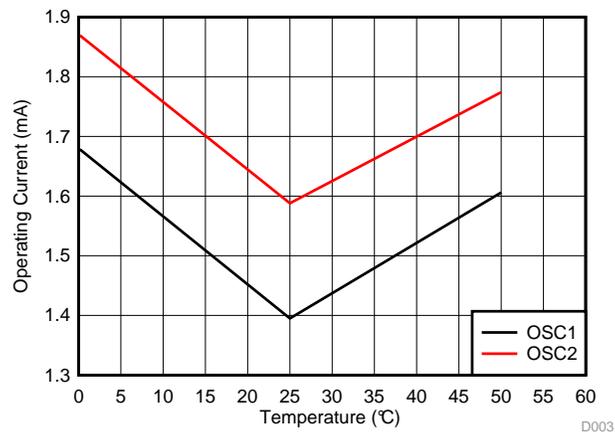


Figure 19. Operating Current versus Temperature

As the supply voltage increases, so does the supply current, which is to be expected. The results are shown in Figure 20.

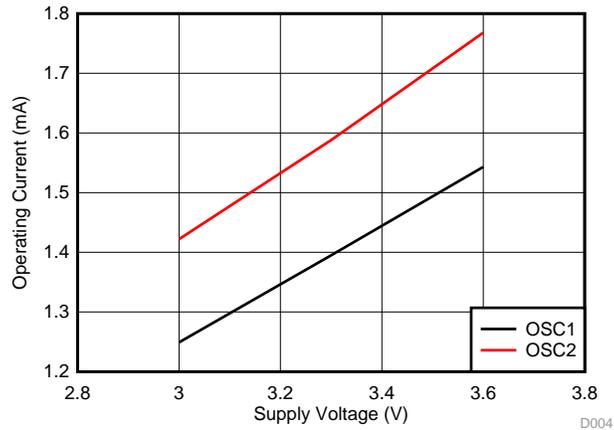


Figure 20. Operating Current versus Supply Voltage

The oscillator using the LM555 timer varies more over temperature than the cheaper alternative oscillator made with the triple Schmitt-trigger inverter. The following graphs show oscillator frequency in reaction to varying temperature and supply voltage.

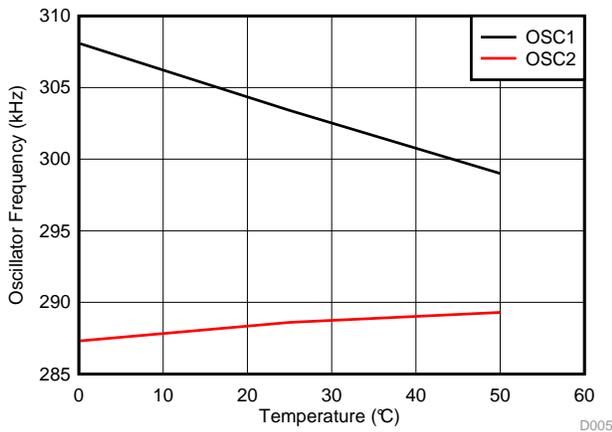


Figure 21. Oscillator Frequency versus Temperature

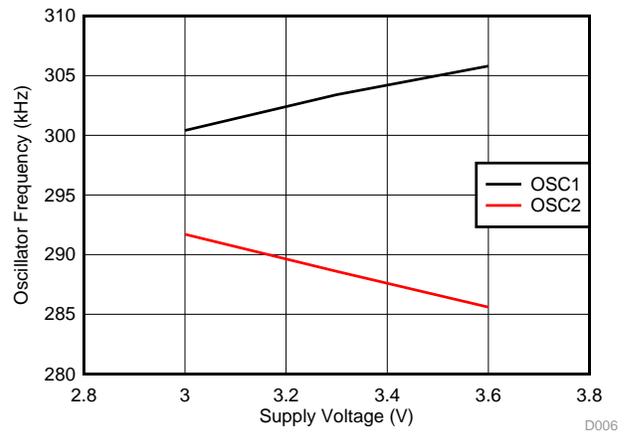


Figure 22. Oscillator Frequency versus Supply Voltage

7.2 Secondary Side Test

The first waveform capture is of enable signal at test point 10 (TP10), H-bridge output (TP7), and gate voltage on output (TP6). The H-bridge output is the result of the 300-kHz signal from the oscillator and the H-bridge device. The gate voltage ramps up to about 11.4 V before evening out.

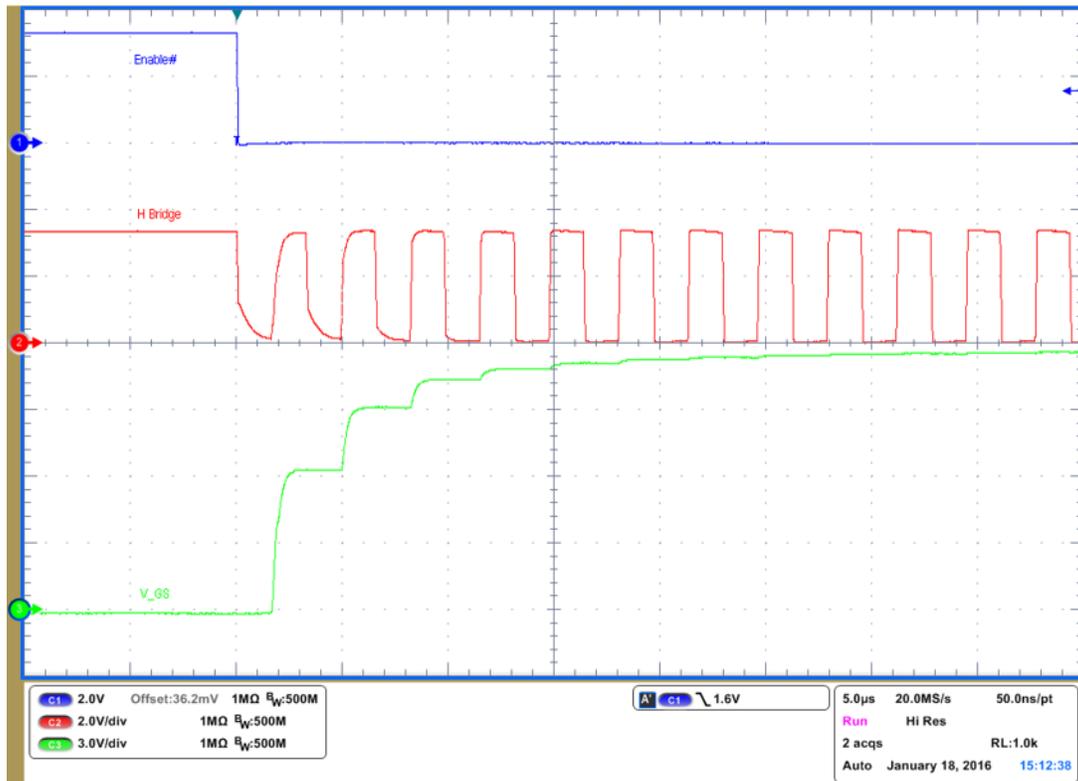


Figure 23. Gate Voltage Ramp-up

The next waveform collected demonstrates the propagation time of the signal (T_{delay}). The approximate time from "enable" dropping low to voltage of drain source dropping to zero. V_{DS} is the voltage difference between TP2 and TP13 ($V_{\text{GS}} = \text{TP6} - \text{TP13}$). The approximate "on" delay time is $\sim 2 \mu\text{s}$. The actual time to turn on the MOSFET, is $T_{\text{ON}} = \sim 100 \text{ ns}$ as seen in Figure 24. This is the time between V_{DS} starting to drop and load current, I_{D} , starting to ramp up. The load current waveform was also captured and can be seen in Figure 24.

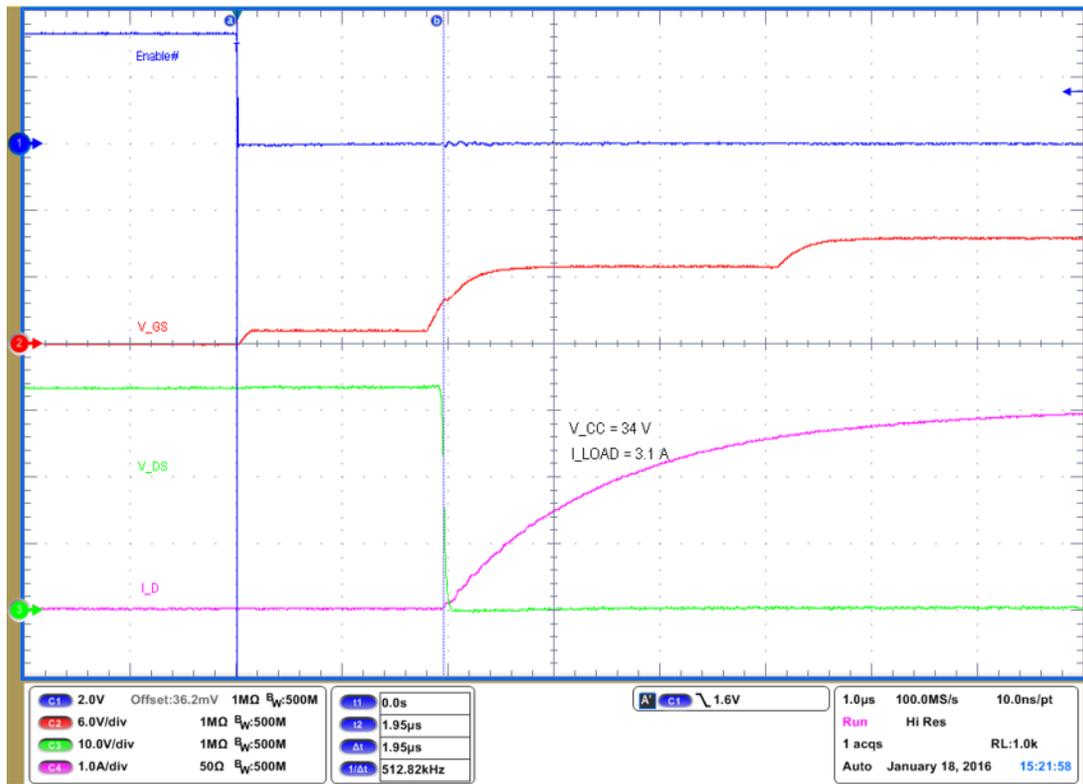


Figure 24. ON Delay Time Waveforms

The turn-off delay is also important in power control systems. Waveforms during turn-off were collected in the same fashion as the turn-on signals. Enable (T10), $V_{GS} = TP6 - TP13$, $V_{DS} = TP2 - TP13$. I_D was measured with a current probe on load wire connected to J5. The "off" delay time is around $5.5 \mu s$. The time to turn off MOSFET, is $T_{OFF} = 200 ns$. The extra voltage spike and ripple on V_{DS} is caused by the TVS diode installed across the terminal block J5 for protection during testing. The TVS diode also makes the load current drop slower. See Figure 25 for waveforms of T_{OFF} and off delay time.

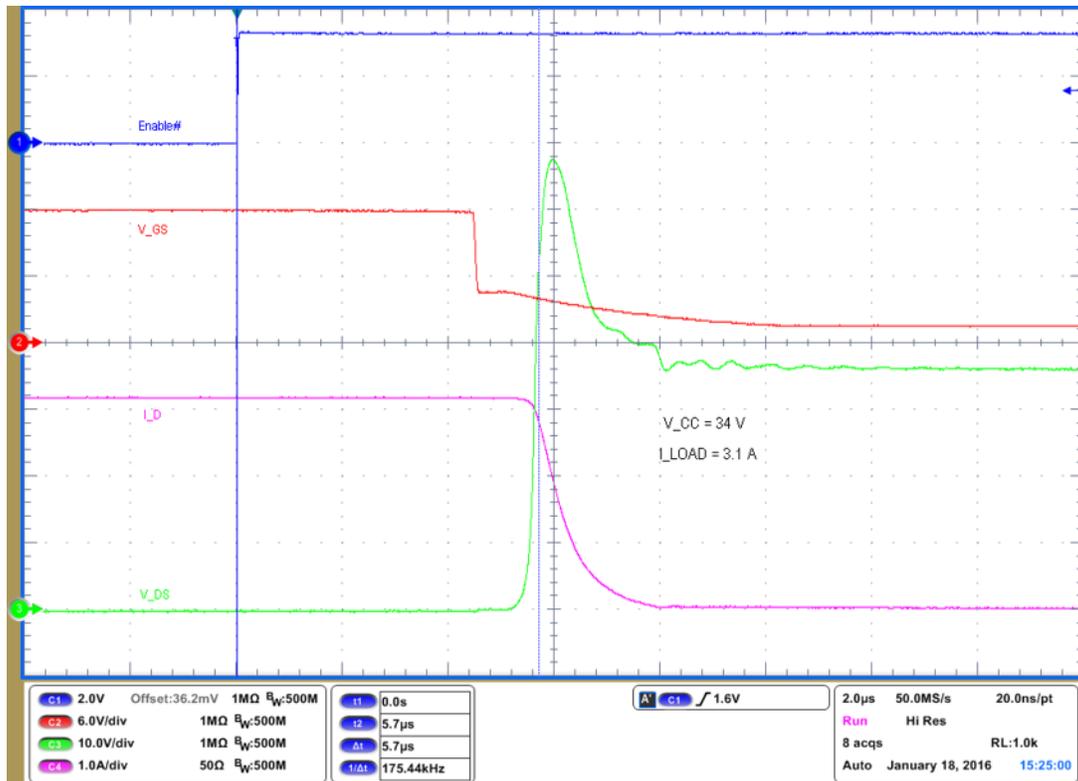


Figure 25. OFF Delay Time Waveforms

7.3 Summary

To sum up the results of testing, at room temperature the reference design uses approximately 1.4 mA with Oscillator 1 running at 300 kHz and a supply voltage of 3.3 V. T_{ON} is around 100 ns with a propagation delay of about 2 μs . T_{OFF} is around 200 ns with a propagation delay of about 5.5 μs .

8 Design Files

8.1 Schematics

To download the schematics, see the design files at [TIDA-00751](#).

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00751](#).

8.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting later on. Also, keep grounds separate.

8.3.1 Layout Prints

To download the layout prints, see the design files at [TIDA-00751](#).

8.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00751](#).

8.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00751](#).

8.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00751](#).

9 References

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report ([SLVA043](#))
2. Texas Instruments, *CMOS Power Consumption and Cpd Calculation*, Application Report ([SCAA035](#))
3. Texas Instruments, WEBENCH® Design Center, <http://www.ti.com/webench>

10 About the Author

JARROD KREBS is a systems designer at Texas Instruments, where he is responsible for developing reference designs in the industrial segment. Jarrod has experience with software and embedded applications implemented on ARM-based microcontrollers and TI's MSP430 platforms. Jarrod earned his bachelor of science in computer engineering from Kansas State University in Manhattan, KS. Jarrod is also a member of the Institute of Electrical and Electronics Engineers (IEEE).

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Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (February 2016) to B Revision	Page
• Added feature "No Clicking Noise"	1
• Changed the general "Fast" to specific "<1- μ s"	1
• Changed "Zero Power" to "<200- μ A"	1
• Added DETAILS column to Table 1	2
• Added 2500-V AC measurement.....	2
• Added row for turn-on and turn-off time in Table 1	2
• Added row for off-state current consumption in Table 1	2

Revision A History

Changes from Original (December 2015) to A Revision	Page
• Changed from preview page.....	1

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