INFOTAINMENT EXPANSION BOARD

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REVISION	E3A
VERSION	0.1

Project : J7 EVM

TEXAS INSTRUMENTS

Title: TABLE OF CONTENTS

Size: C | PROC086 001 J7EXPE01EVM | Rev: E3A

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	21 NOV 2019	Drafted from "PROC086E3_SCH, VER: 1.1" Hardware Schematic page Updated	Mistral Design Team		

Project :

J7 EVM

TEXAS INSTRUMENTS

Title: REVISION HISTORY

Size	PROC086 001 J7EXPE01EVM	Rev
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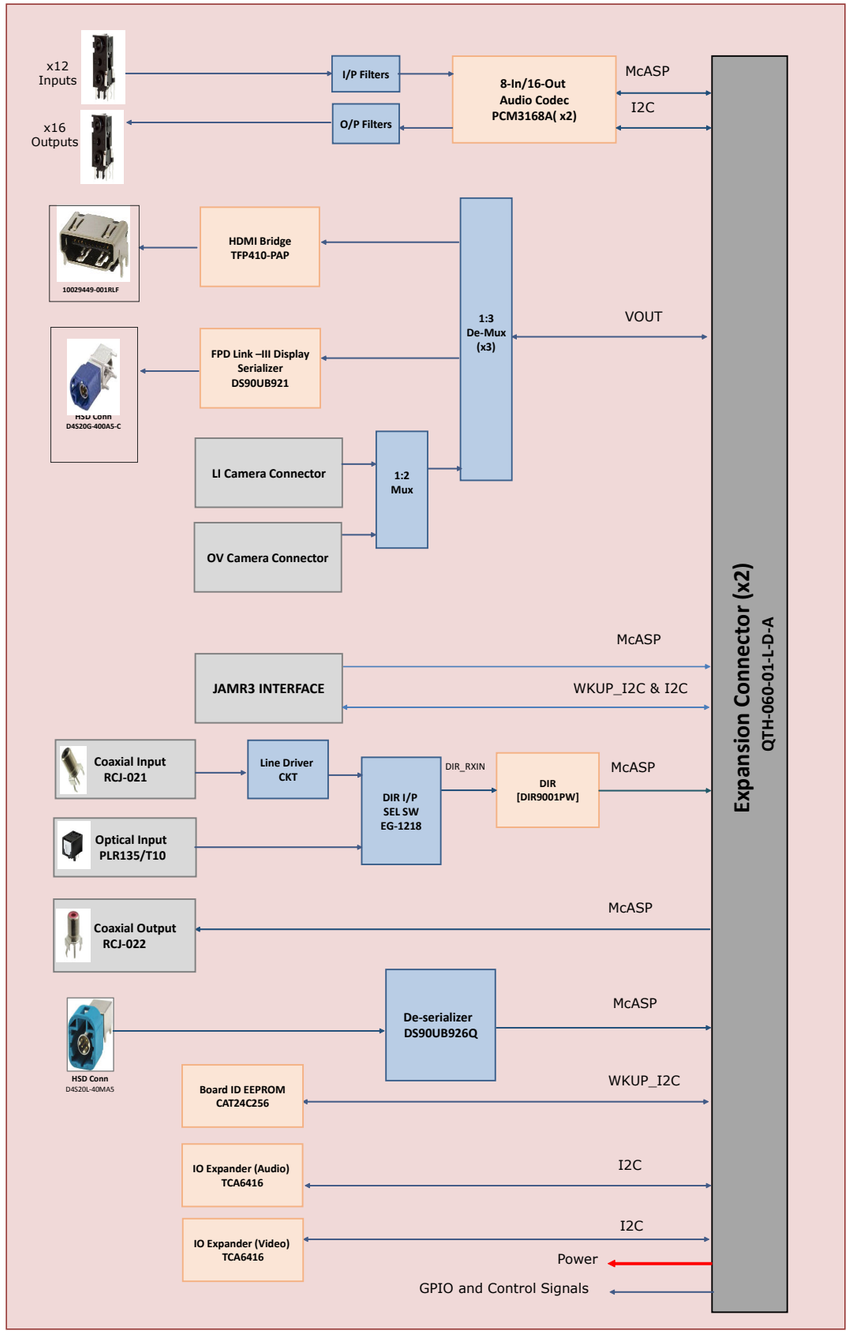
BLOCK DIAGRAM

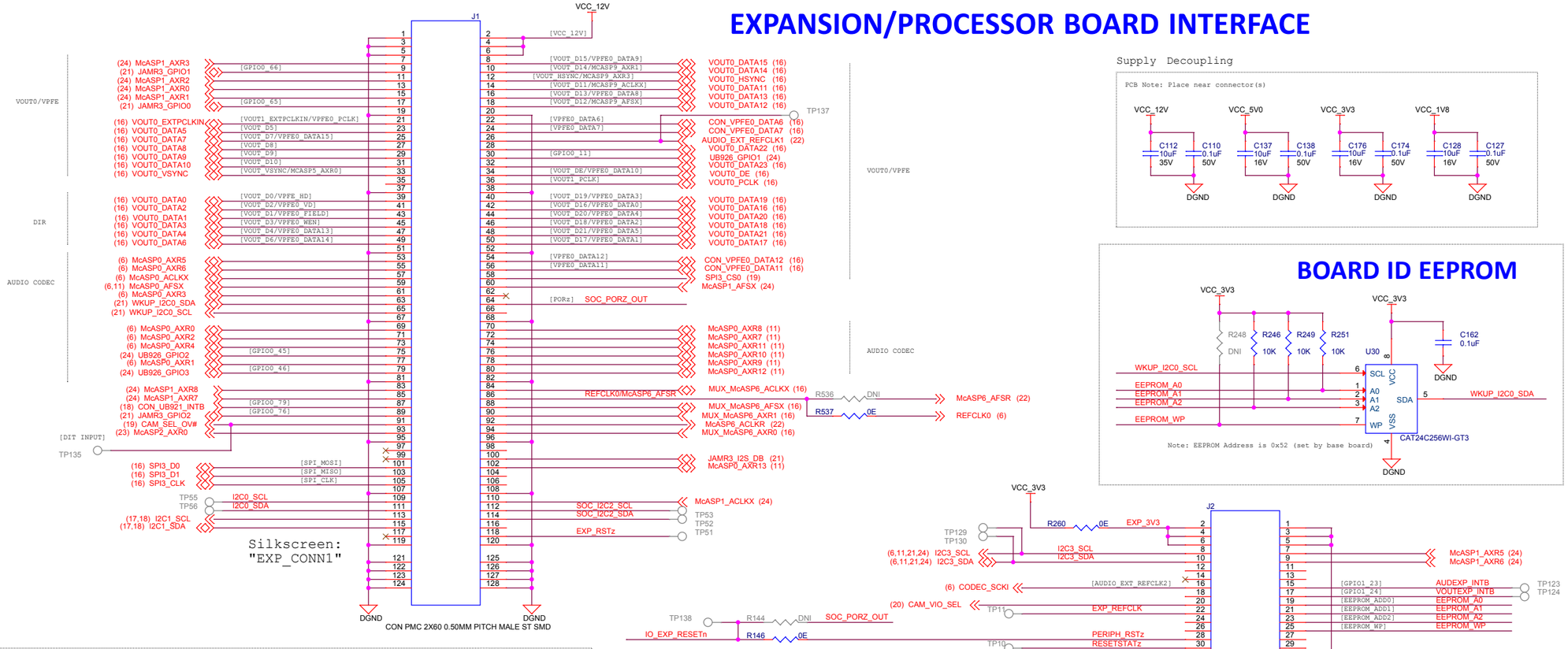


Project : J7 EVM	TEXAS INSTRUMENTS	Title: BLOCK DIAGRAM
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 3 of 25

GPIO EXPANDER MAP/TABLE

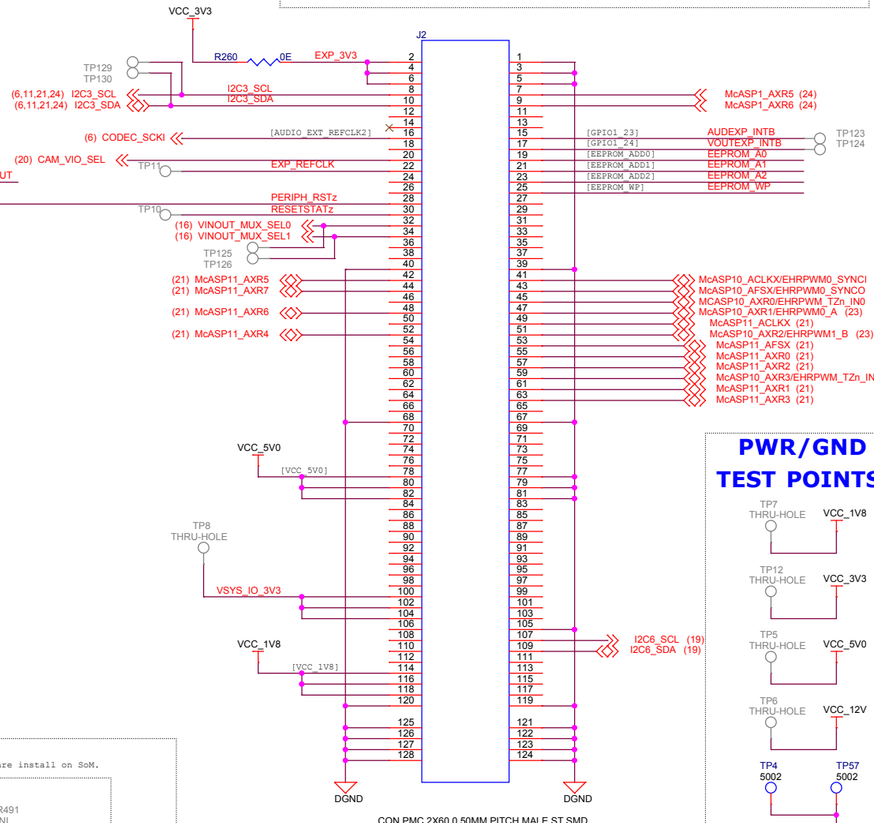
Jacinto7 EVM - Infotainment Expansion Board GPIO Expander						
I2C Bus/ Address	GPIO Port	Net name in INFO Board	Direction WRT CTRL	Default state	Active state	Remarks
INFO GPIO Expander - 1 Part# TCA6416ARTWR (AUDIO IO EXPANSION)						
I2C3/0x21	P00	CODEC_RESETn	Output	PD	Active Low	Used as a Reset signal for Audio Codecs A & B
	P01	JAMR3_RESETn	Output	PD	Active Low	Used as a Reset signal for JAMR3 Interface
	P02	JAMR3_PWR_CTRL	Output	NA	Active High	Power EN for JAMR3 Interface
	P03	UB926_RESETn	Output	PD	Active Low	Used as a Reset signal for FPD Audio De-Serializer
	P04	PWR_SW_UB926	Output	PD	Active High	Used as a Power Enable signal for Audio/FPD connector
	P05	UB926_TUNER_RESET	Output	PD	Active Low	Used as a Reset signal for FPD Tuner
	P06	UB926_GPIO_SPARE	Output	NA	NA	SPARE GPIO for Tuner
	P07	UB926_LOCK	Input	NA	NA	Lock Input from Tuner
	P10	DIR_RESETn	Output	PD	Active Low	Used as a Reset signal for DIR interface
	P11	DIR_CKSEL	Output	PU	NA	Used for DIR System clock source selection Low: PLL (VCO) clock, High: XTI clock
	P12	DIR_FMT0	Output	PU	NA	DOUT Audio Data output format - 24-bit, MSB-first, I2S (Default)
	P13	DIR_FMT1	Output	PU	NA	
	P14	DIR_PSCK0	Output	PD	NA	System clock of PLL selection
	P15	DIR_PSCK1	Output	PD	NA	
	P16	AUDEXP_P16	NA	NA	NA	Reserved GPIO
	P17	McASP6_MUX_SEL	Output	PD	NA	User for Mux selection b/w DIR or Tuner
INFO GPIO Expander – 2 Part# TCA6416ARTWR (VIDEO IN/OUT IO EXPANSION)						
I2C1/0x21	P00	NC	NA	NA	NA	Not used
	P01	NC	NA	NA	NA	Not used
	P02	NC	NA	NA	NA	Not used
	P03	NC	NA	NA	NA	Not used
	P04	NC	NA	NA	NA	Not used
	P05	VOUTEXP_P04	NA	NA	NA	Terminated with Test point
	P06	VOUTEXP_P05	NA	NA	NA	Terminated with Test point
	P07	NC	NA	NA	NA	Not used
	P10	HDMI_PDn	Output	PD	Active Low	Used as a Power Down signal for HDMI Transmitter
	P11	HDMI_DDC_OE	Output	PD	Active High	Used for HDMI I2C Translator Enable logic
	P12	HDMI_HPD	Input	NA	NA	Used for detection of HDMI cable Hot plug
	P13	UB921_RESETn	Output	PD	Active Low	Used as a Reset signal for FPD III Display Serializer
	P14	PWR_SW_UB921	Output	PD	Active High	Used as a Power Enable signal for Audio/FPD connector
	P15	UB921_INTB	Input	NA	Active High	FPD III Display Serializer INTB = H, normal INTB = L, Interrupt request
	P16	VOUTEXP_P16	NA	NA	NA	Terminated with Test point
	P17	VOUTEXP_P17	NA	NA	NA	Terminated with Test point

EXPANSION/PROCESSOR BOARD INTERFACE



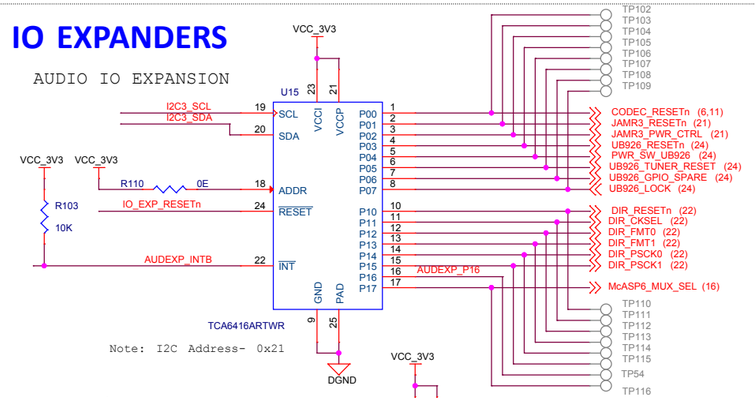
Supply Decoupling

BOARD ID EEPROM

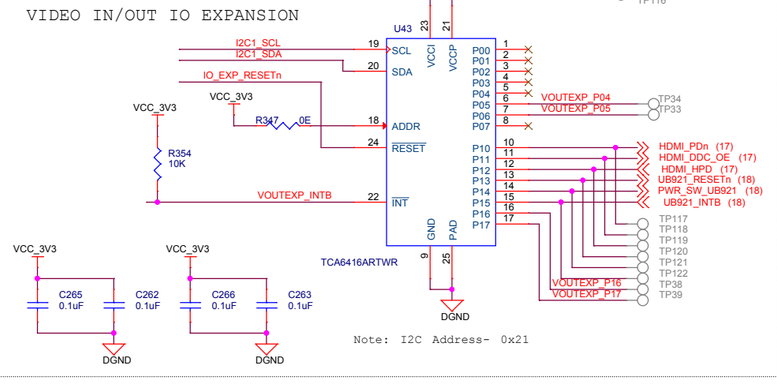


IO EXPANDERS

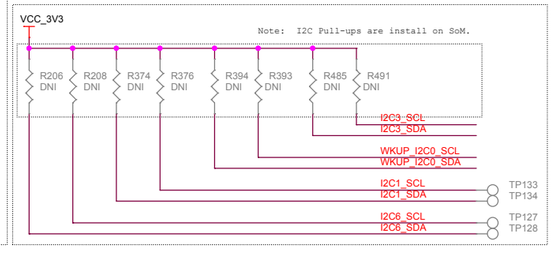
AUDIO IO EXPANSION



VIDEO IN/OUT IO EXPANSION



I2C Bus Pull-up Resistor Options



PWR/GND TEST POINTS

Project : J7 EVM	TEXAS INSTRUMENTS	Title: EXPANSION CONNECTORS
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 5 of 25

AUDIO I/F CODEC - A

Resistor Isolation option provided for Debug purpose

2x STEREO MIC-IN

1x STEREO LINE-IN

From Expansion Connector

4x STEREO LINE-OUT

To Expansion connector

U32 PCM3168APAP

PCB Note: Short CODEC_AGND and DGND at single point

Note: Use for input signal conditioning.

Note: MODE tied to DGND with 0E Resistor for Software Control (default)

Codec1 I2C Address SEL

7b' I2C Address 0x47 (default)

1-to-2 Clock Fanout Buffer

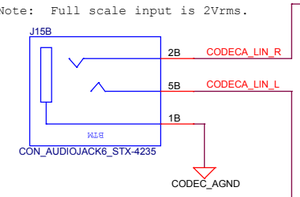
1-to-2 Clock Fanout Buffer

Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F CODEC - A	
		Size: C	PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019	Sheet 6 of 25

CODEC-A STEREO LINE IN

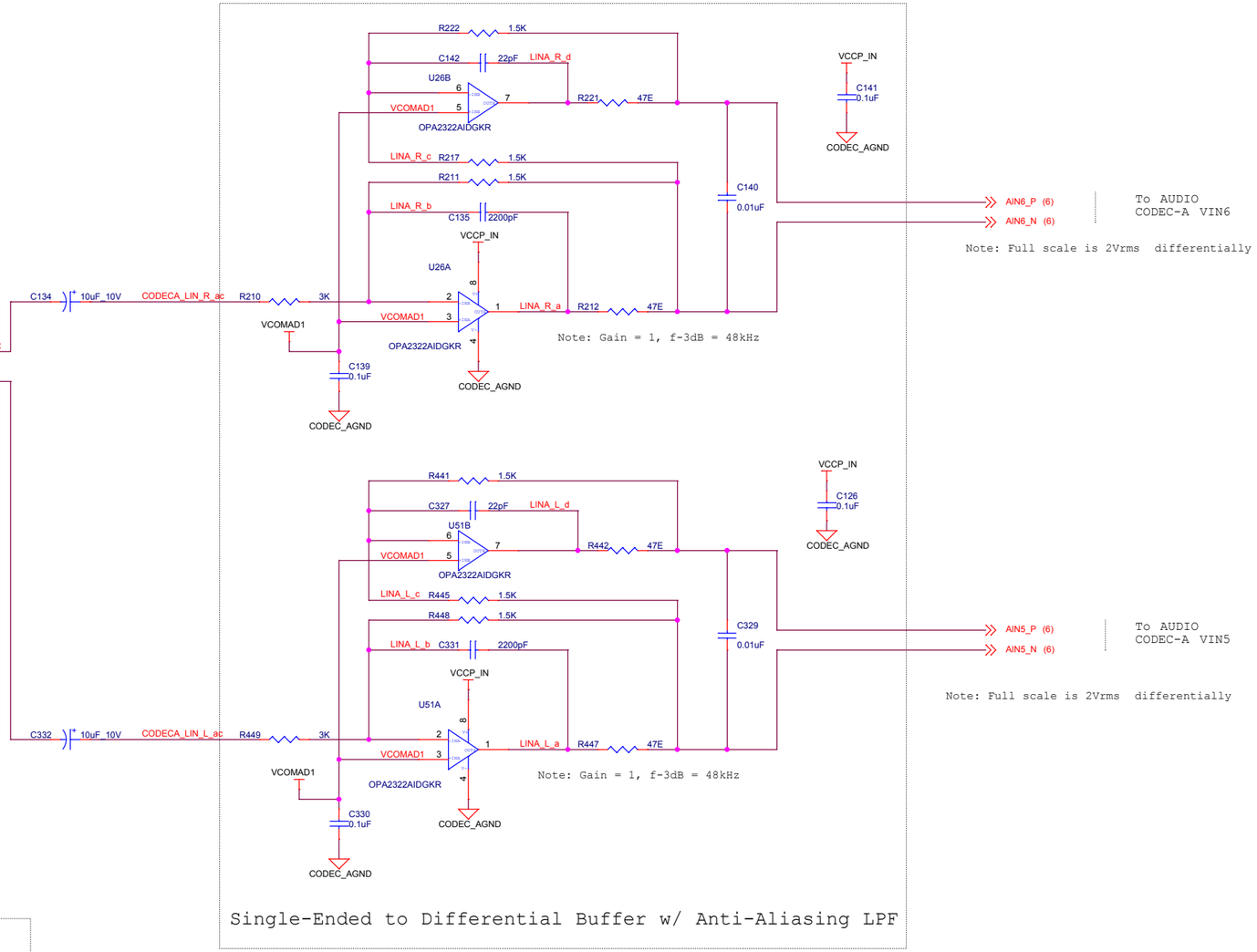
J15-BOTTOM JACK
LIN L CODEC-A VIN5
LIN R CODEC-A VIN6

Note: Full scale input is 2Vrms.



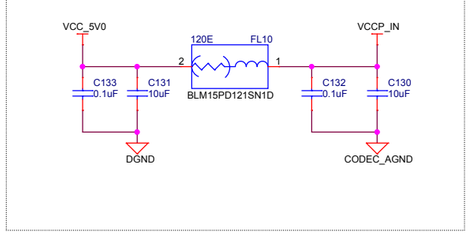
CON AUDIO JACK DUAL 6POS 3.50MM FEMALE RT TH

Silkscreen:
"CODEC-A LIN"



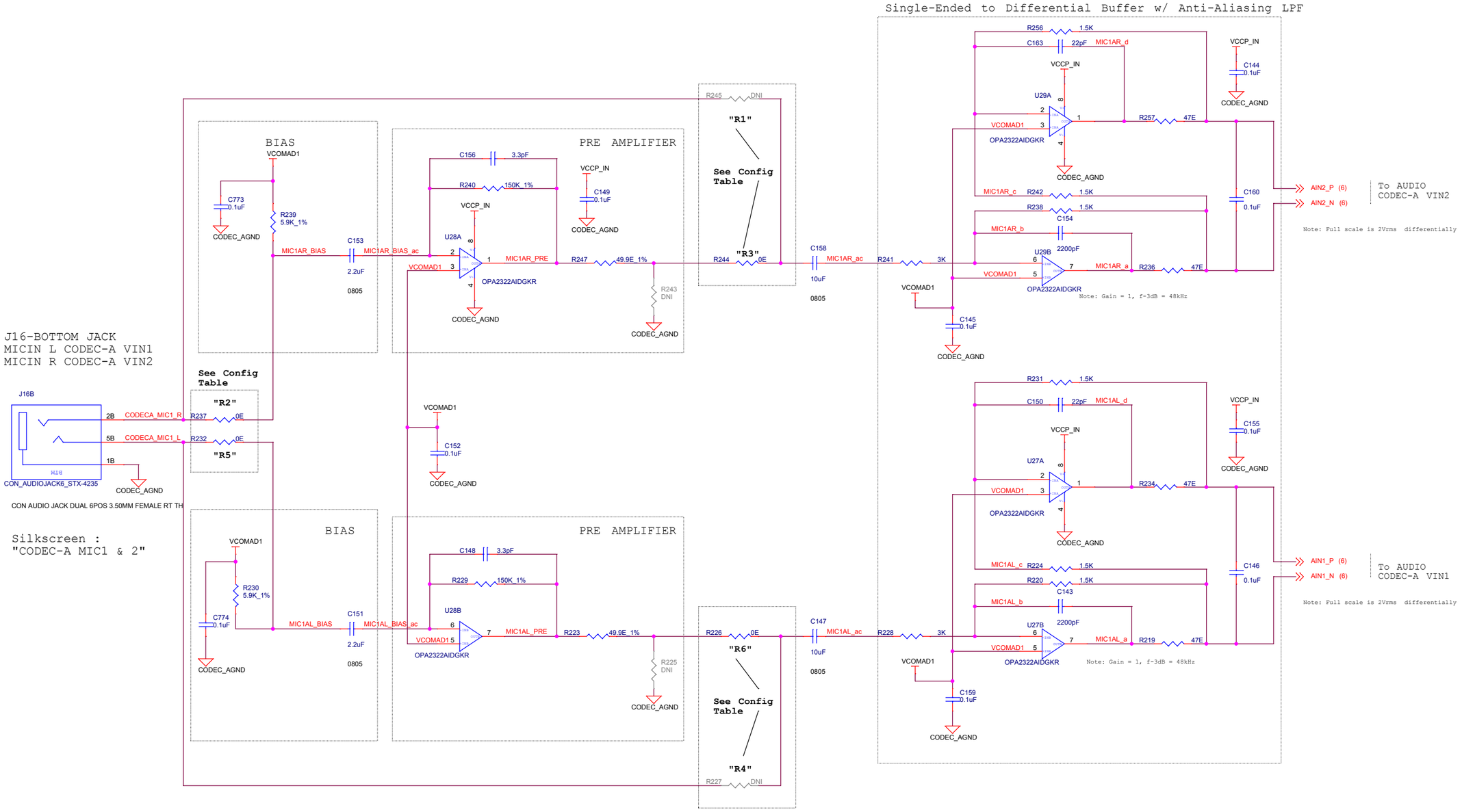
Single-Ended to Differential Buffer w/ Anti-Aliasing LPF

Audio Op-Amp Supply Filter



Project : J7 EVM	Title: CODEC-A STEREO LINE IN	
	Size: C — PROC086 001 J7EXPE01EVM	Rev: E3A
	Date: Thursday, November 21, 2019	Sheet 7 of 25

CODEC-A STEREO MICROPHONE 1



Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

Project : J7 EVM

TEXAS INSTRUMENTS

Title: CODEC-A STEREO MIC 1

Size	PROC086 001 J7EXPE01EVM	Rev
C		E3A

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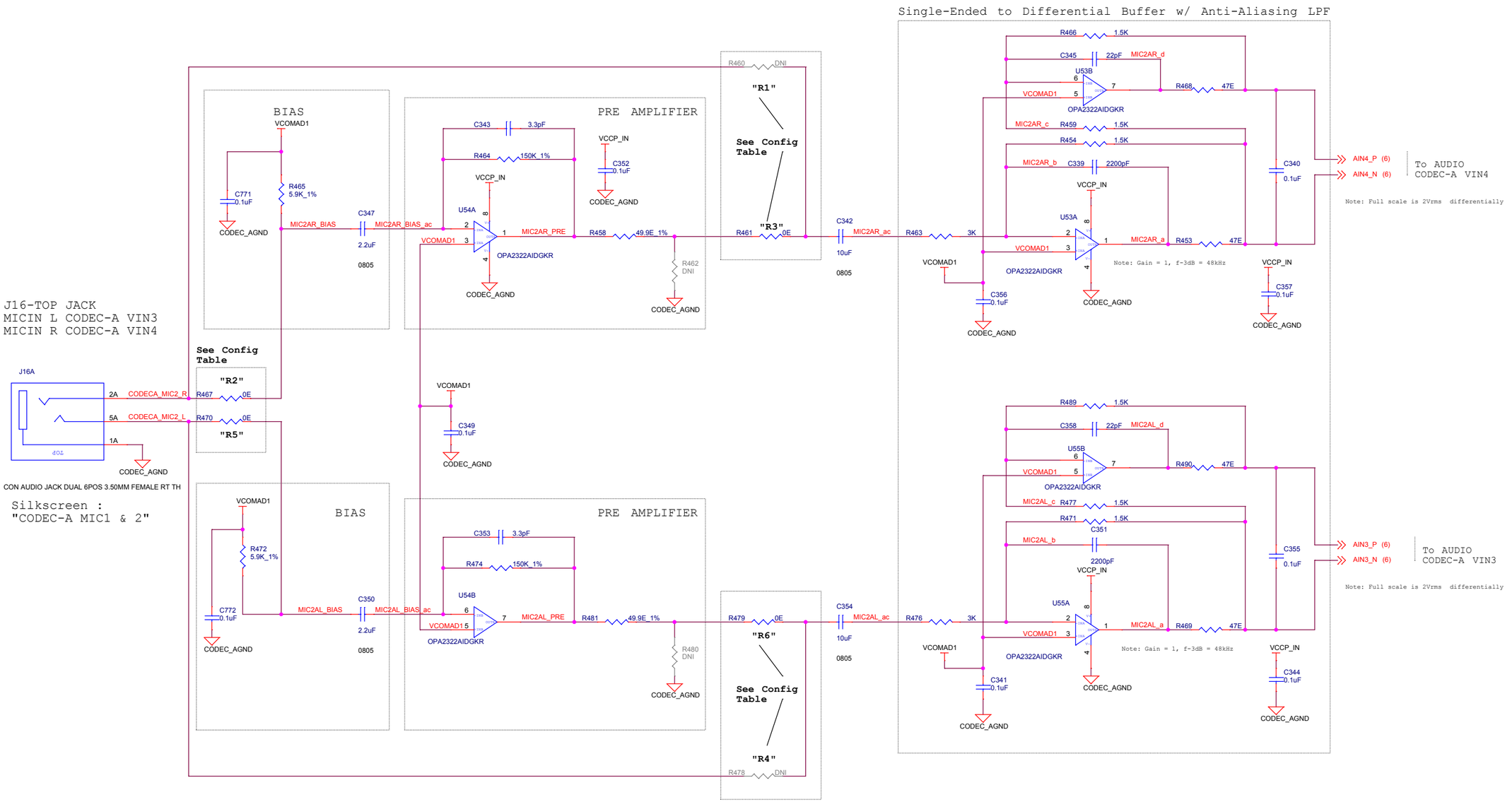
CODEC-A STEREO MICROPHONE 2

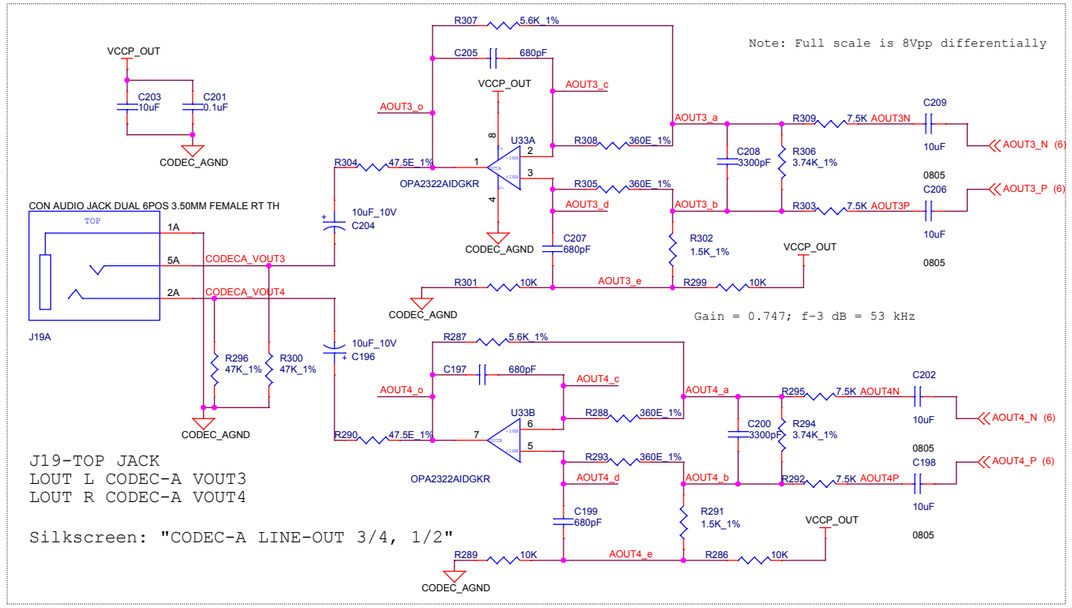


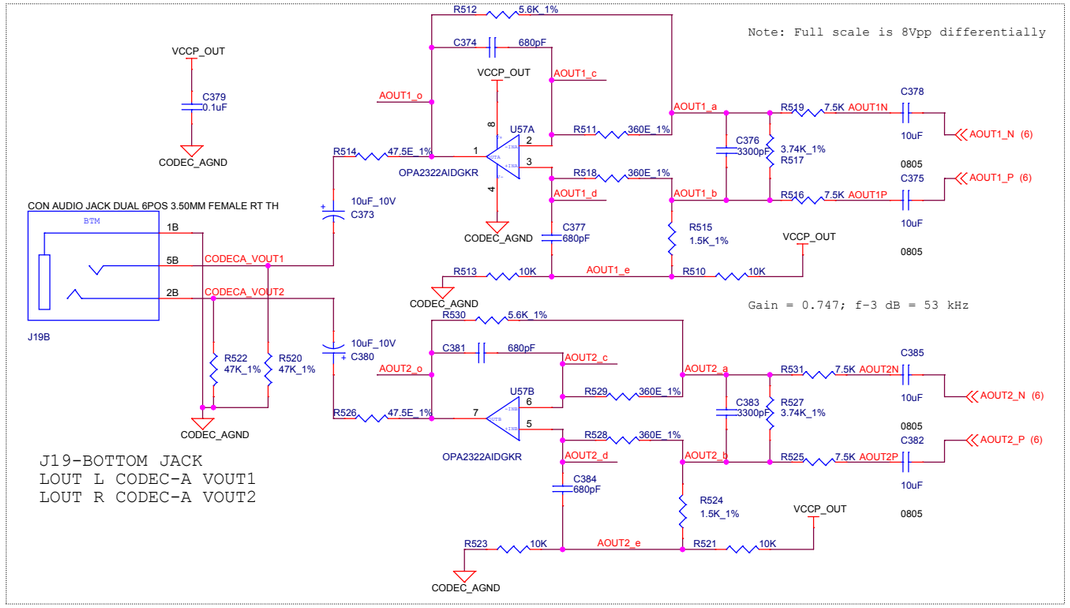
Config Table

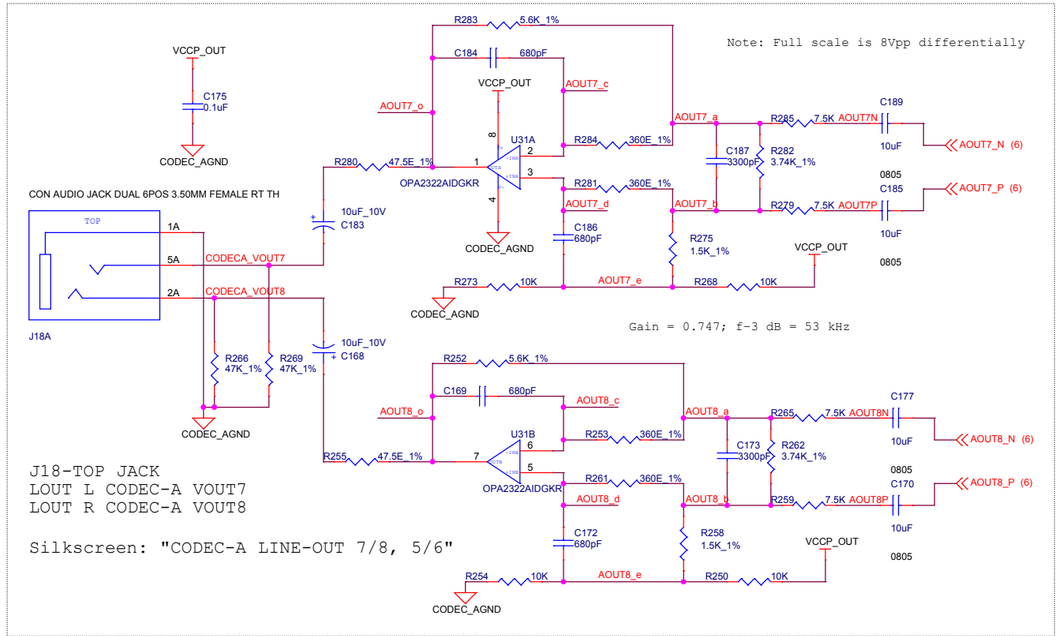
		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

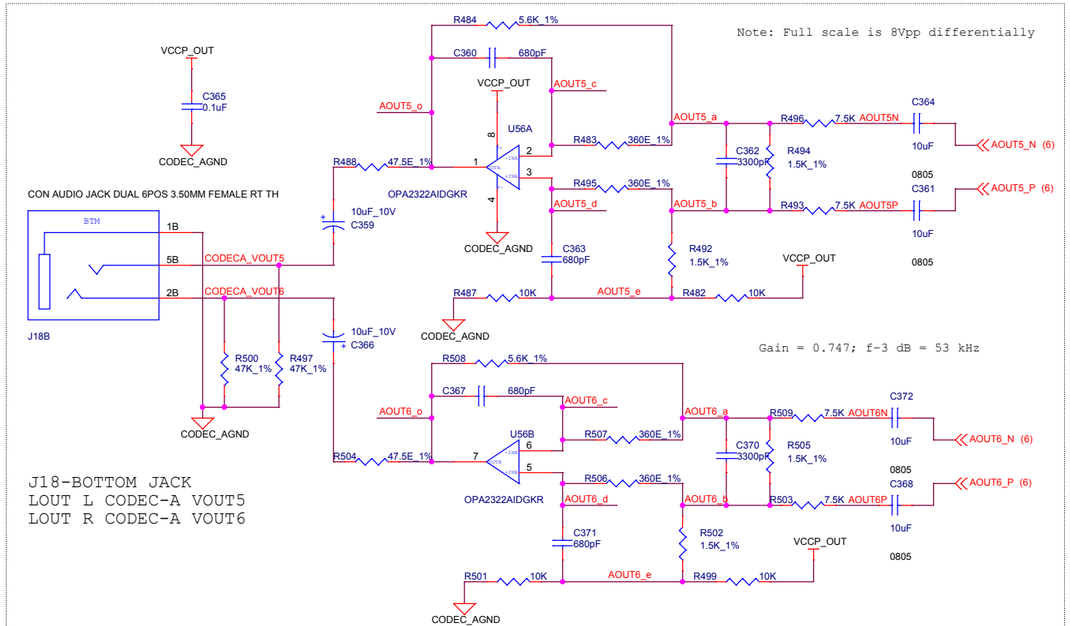
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CODEC-A STEREO MIC 2	
		Size: C	PROC086 001 J7EXPE01EVM
		Date: Thursday, November 21, 2019	Sheet 9 of 25
			Rev: E3A

CODEC-A STEREO LINE OUT

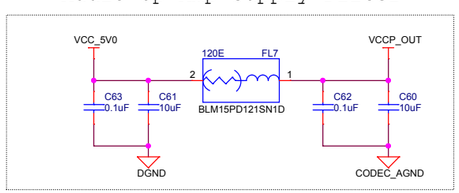








Audio Op-Amp Supply Filter



Project : J7 EVM	Title: CODEC-A STEREO LINE OUT	
	Size: C	PROC086 001 J7EXPE01EVM — Rev: E3A
	Date: Thursday, November 21, 2019	Sheet 10 of 25

AUDIO I/F CODEC-B

Resistor Isolation option provided for Debug purpose

2x STEREO MIC-IN

1x STEREO LINE-IN

From Expansion Connector

4x STEREO LINE-OUT

To Expansion connector

PCB Note: Short at single point or segment signals/plane to isolate analog from digital signals

Note: Use for input signal conditioning.

Note: MODE tied to DGND with 0E Resistor for Software Control (default)

Codec2 I2C Address SEL

7b' I2C Address 0x46 (default)

Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F CODEC - B	
		Size: C	PROC086 001 J7EXPE01EVM — Rev: E3A
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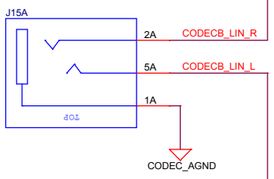
CODEC-B STEREO LINE IN

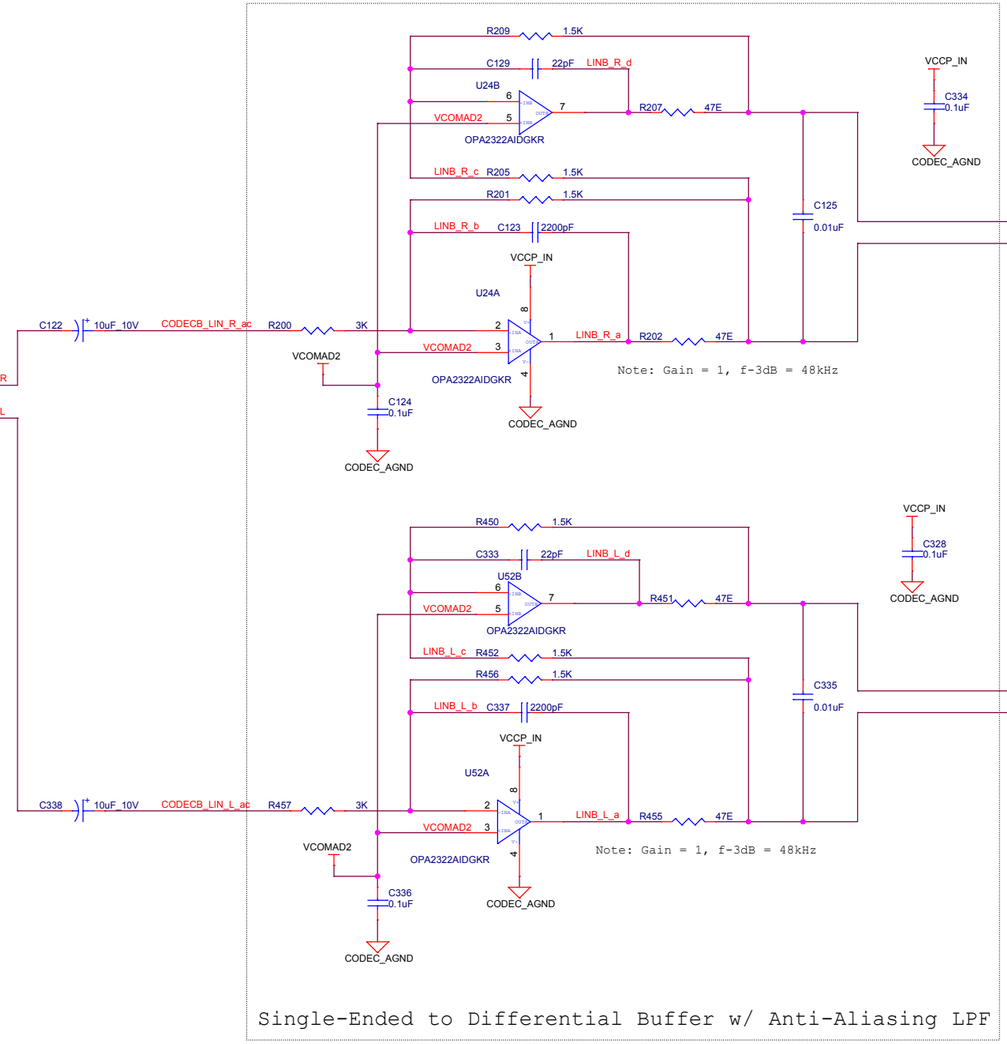
J15-TOP JACK
LIN L CODEC-B VIN5
LIN R CODEC-B VIN6

Note: Full scale input is 2Vrms.



CON AUDIO JACK DUAL 6POS 3.50MM FEMALE RT TH

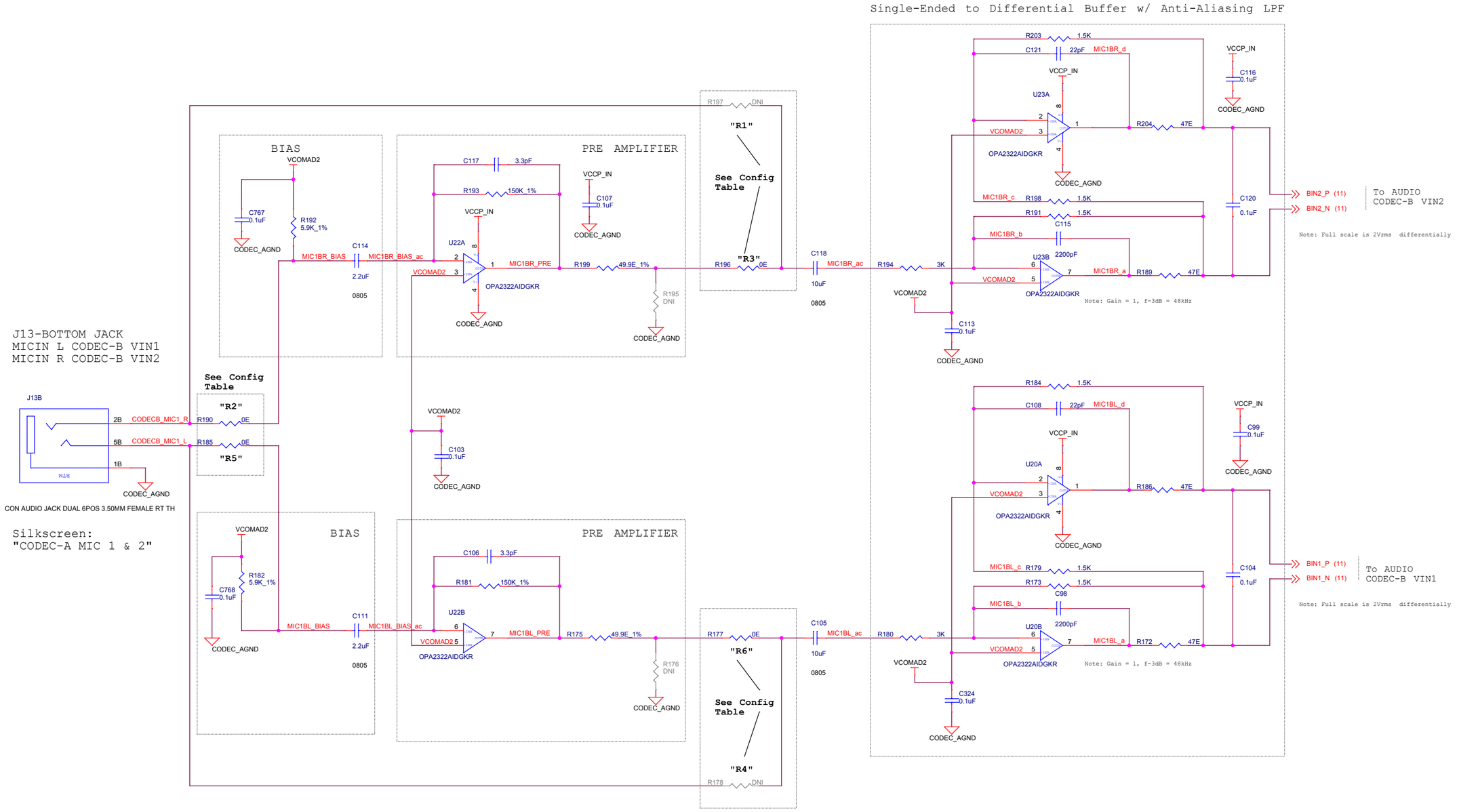
Silkscreen:
"CODEC-B LIN"



Single-Ended to Differential Buffer w/ Anti-Aliasing LPF

Project : J7 EVM	TEXAS INSTRUMENTS	Title: CODEC-B STEREO LINE IN
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 12 of 25

CODEC-B STEREO MICROPHONE 1



Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

Project : J7 EVM	TEXAS INSTRUMENTS	Title: CODEC-B STEREO MIC 1
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
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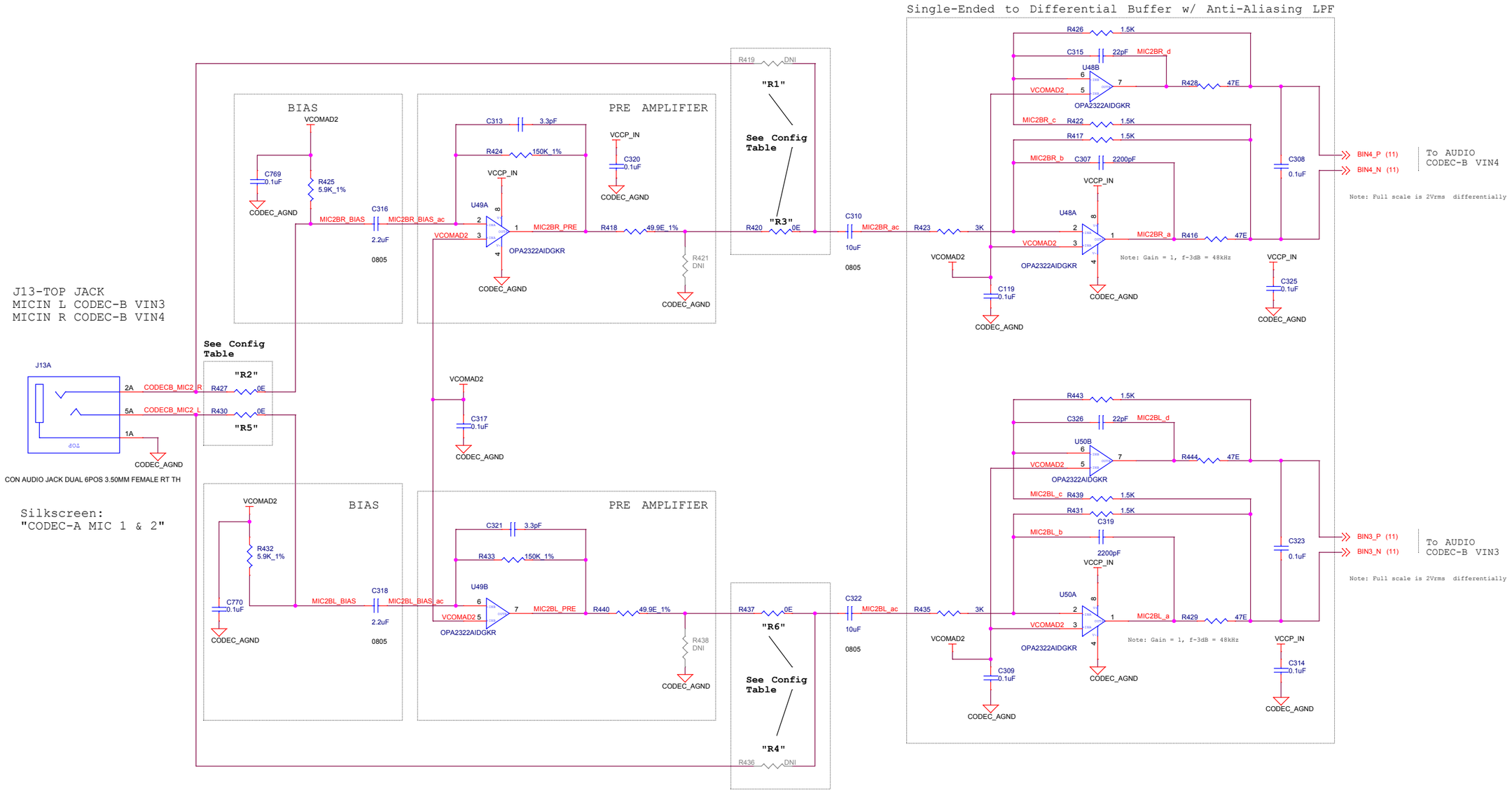
CODEC-B STEREO MICROPHONE 2



Silkscreen:
"CODEC-A MIC 1 & 2"

Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

Project : J7 EVM	TEXAS INSTRUMENTS	Title: CODEC-B STEREO MIC 2	
		Size: C — PROC086 001 J7EXPE01EVM	Rev: E3A
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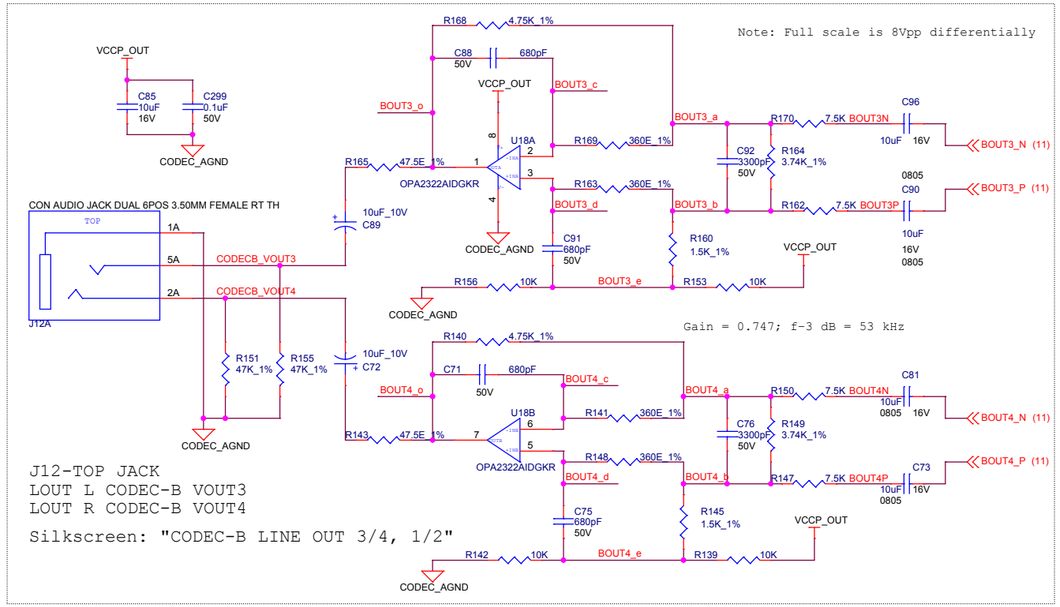
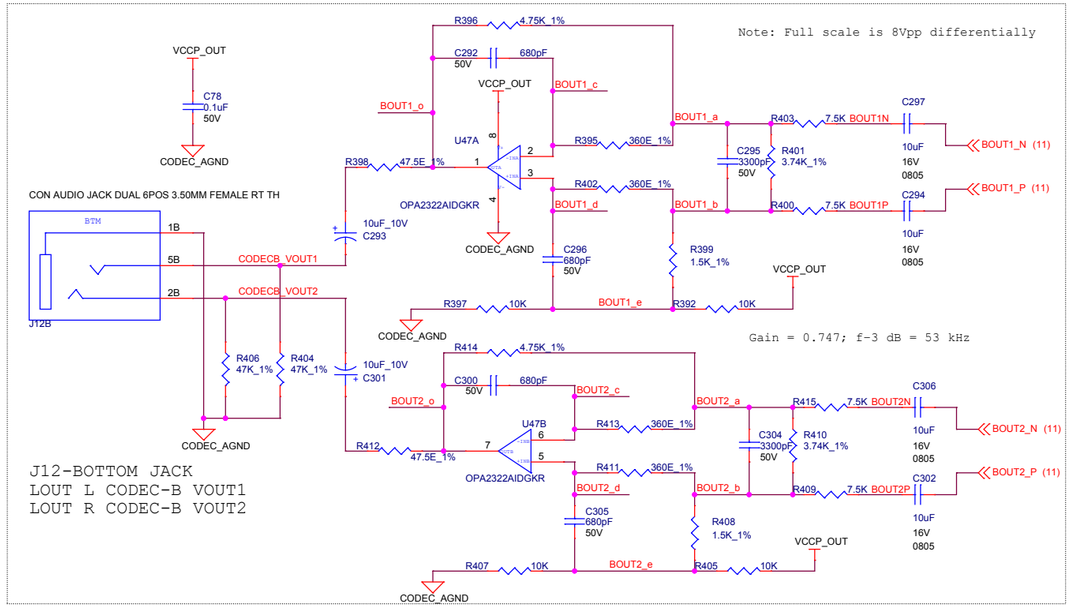
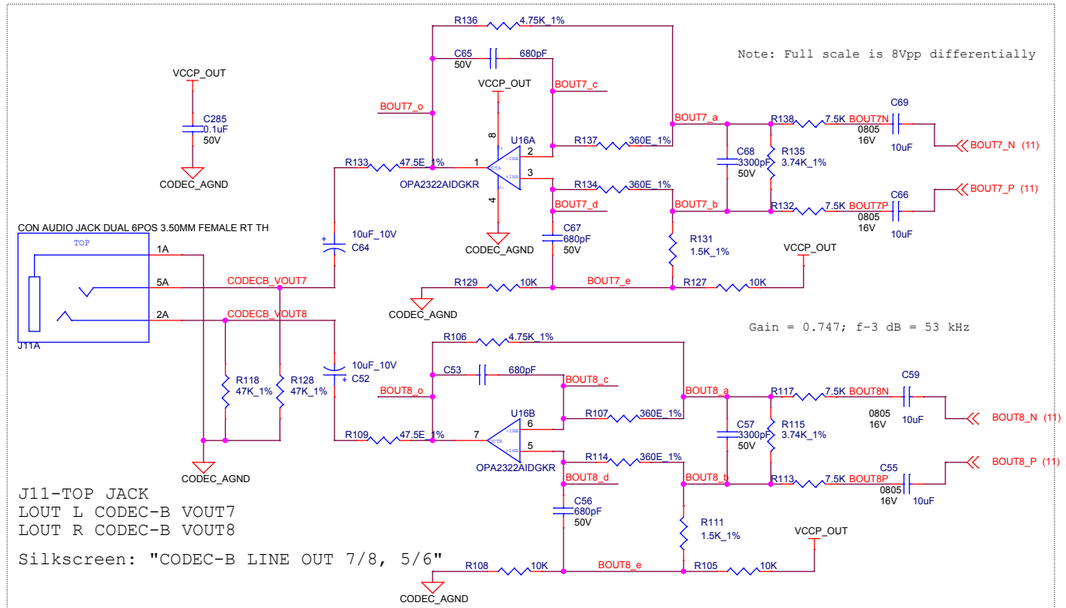
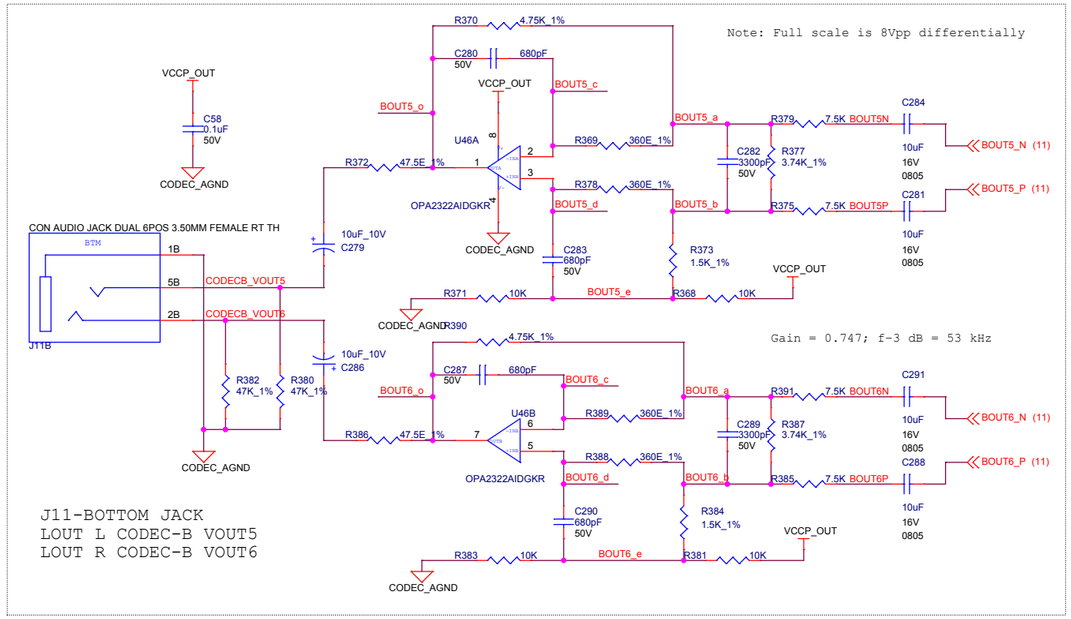
CODEC-B STEREO LINE OUT



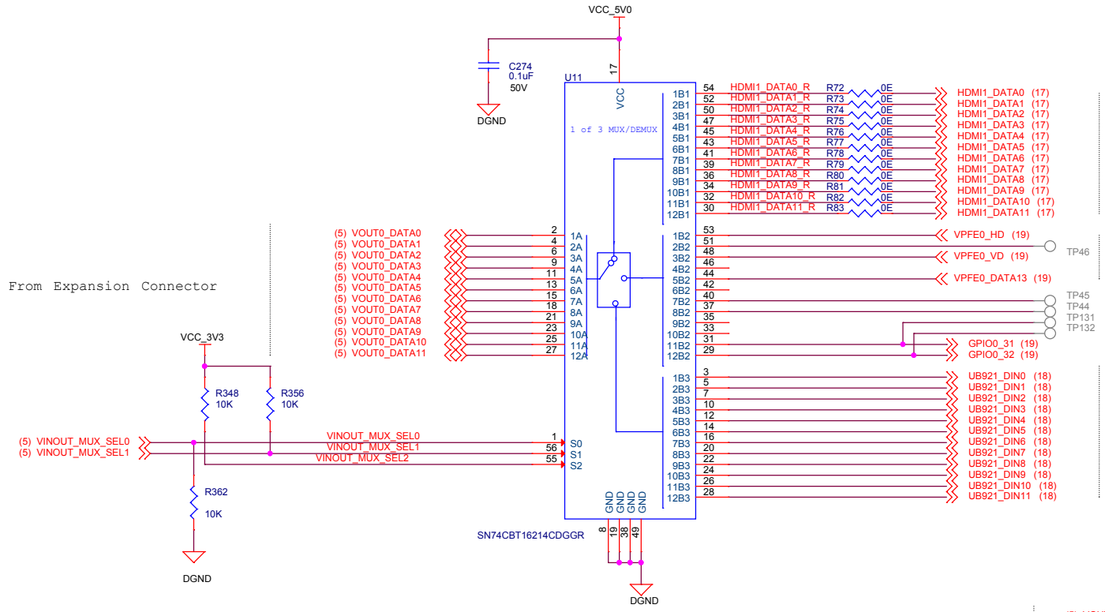






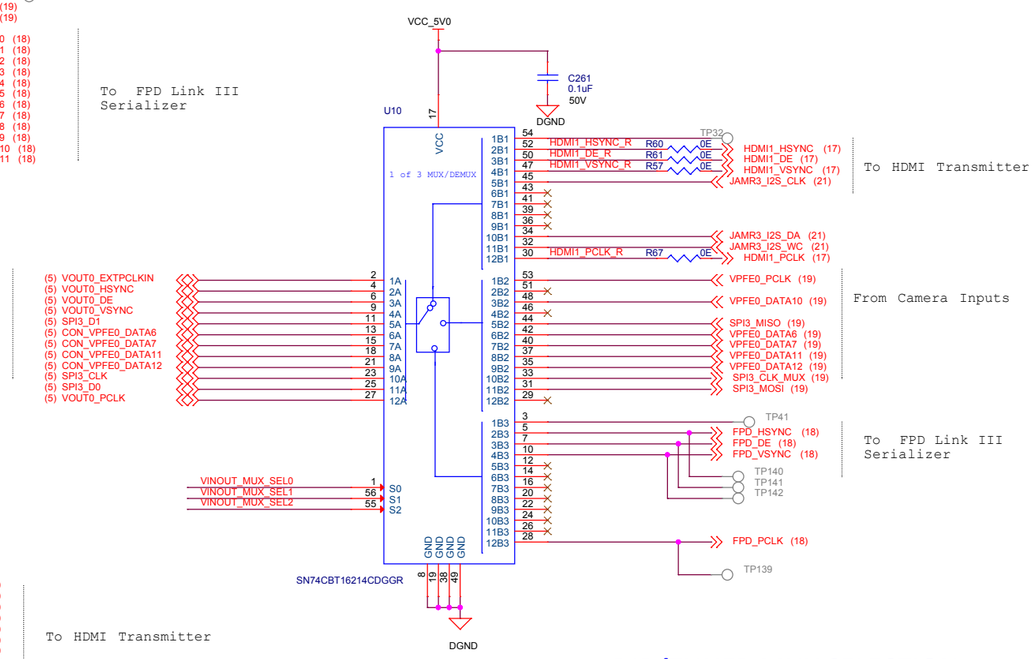
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CODEC-B STEREO LINE OUT
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 15 of 25

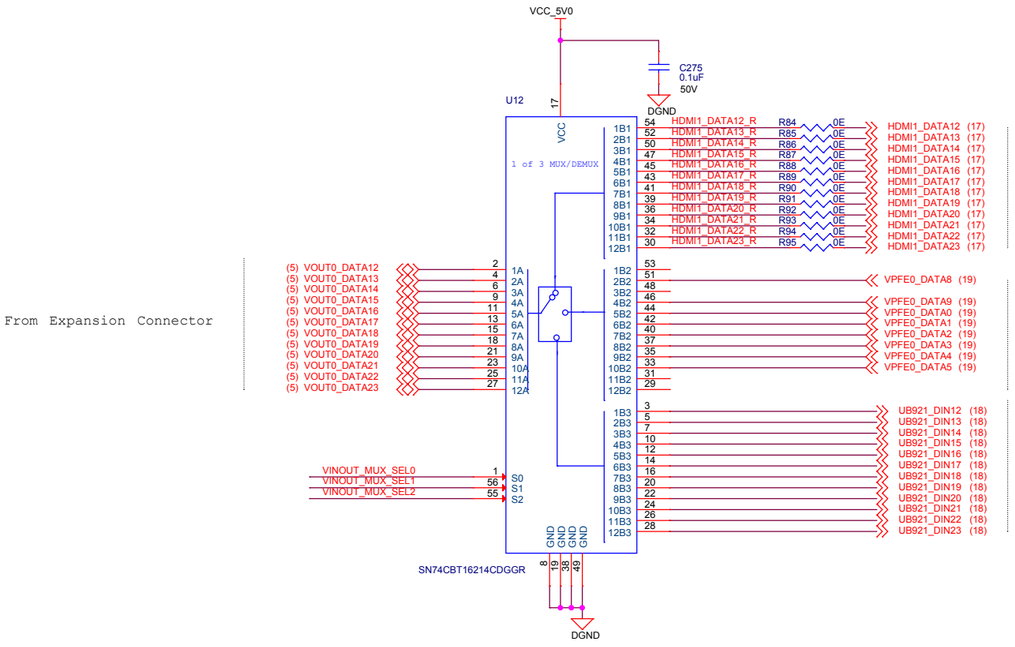
VIN/VOUT MUX SELECTION



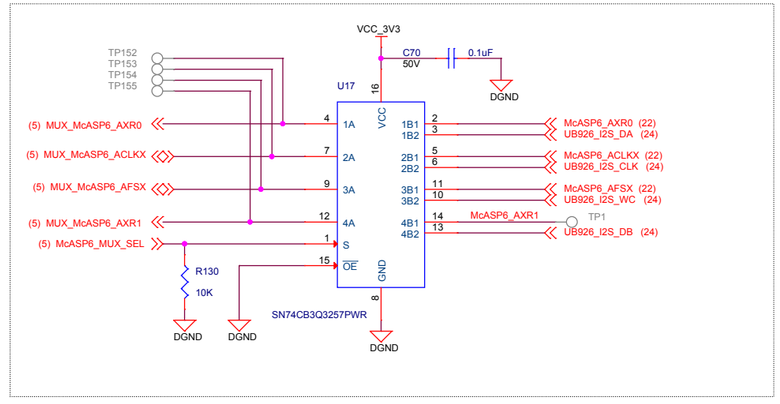
MUX Control/Selection Table

MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION	INTERFACE SELECTED
HIGH	HIGH	LOW	A port = B1 port	HDMI (default)
HIGH	HIGH	HIGH	A port = B2 port	CAMERA
HIGH	LOW	HIGH	A port = B3 port	FPD





DIR/TUNER MUX SELECTION



Project : J7 EVM	TEXAS INSTRUMENTS	Title: VIN/VOUT MUX SELECTION	
		Size: C	PROC086 001 J7EXPE01EVM — Rev: E3A
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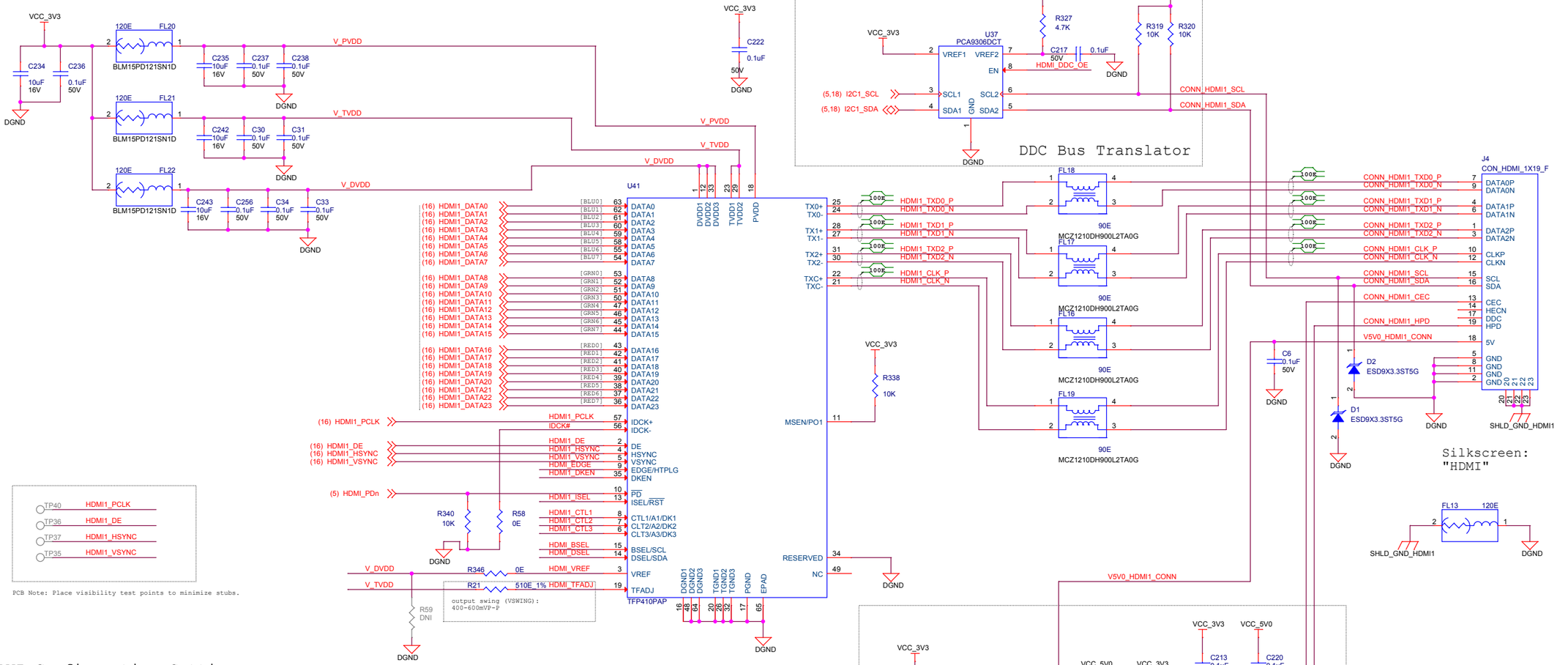
DVI/HDMI TRANSMITTER



VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	0	0	0	12-bit	Dual-edge	Falling	Differential
	0	0	1	12-bit	Dual-edge	Falling	Single-ended
	0	1	0	12-bit	Dual-edge	Raising	Differential
	0	1	1	12-bit	Dual-edge	Raising	Single-ended
	1	0	0	24-bit	Single-ended	Falling	Single-ended
	1	0	1	24-bit	Single-ended	Falling	Differential
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended
	1	1	1	24-bit	Single-ended	Raising	Differential

ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins

When ISEL: L, DSEL-H- enables de-skew function (default)

Project : J7 EVM

Title: HDMI BRIDGE

Size: C | PROC086 001 J7EXPE01EVM | Rev: E3A

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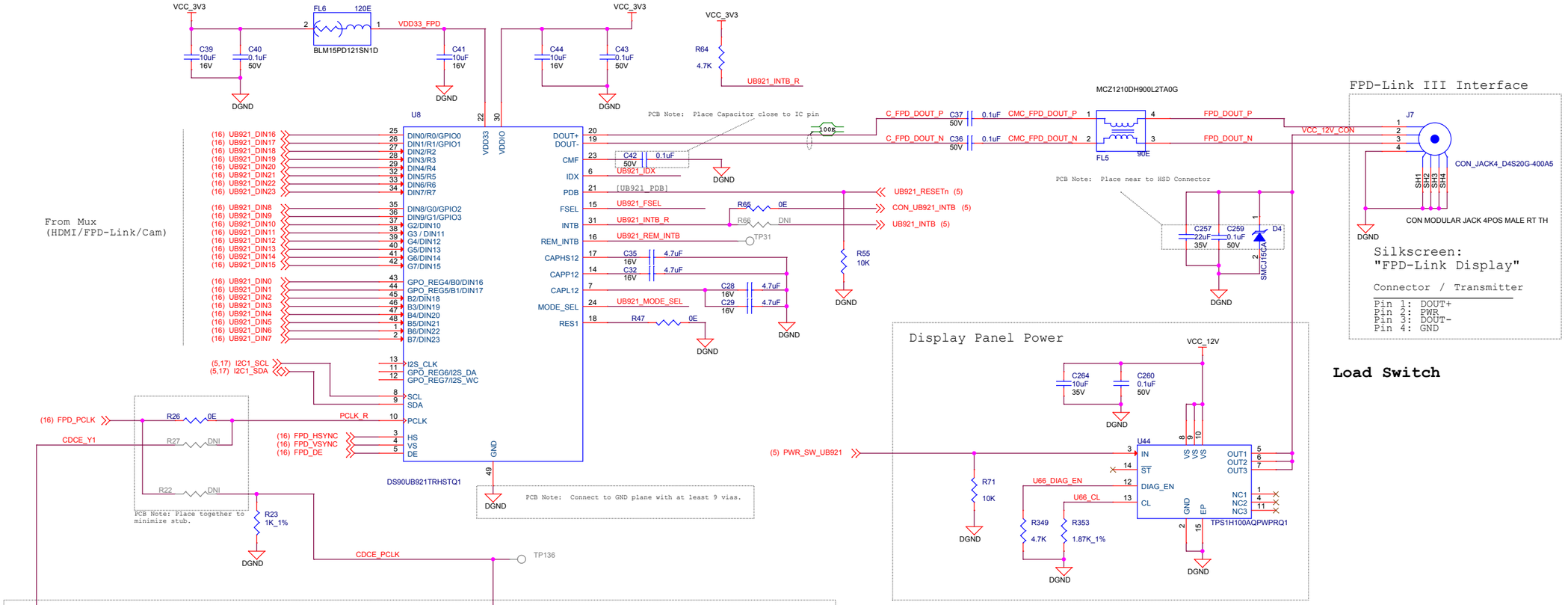
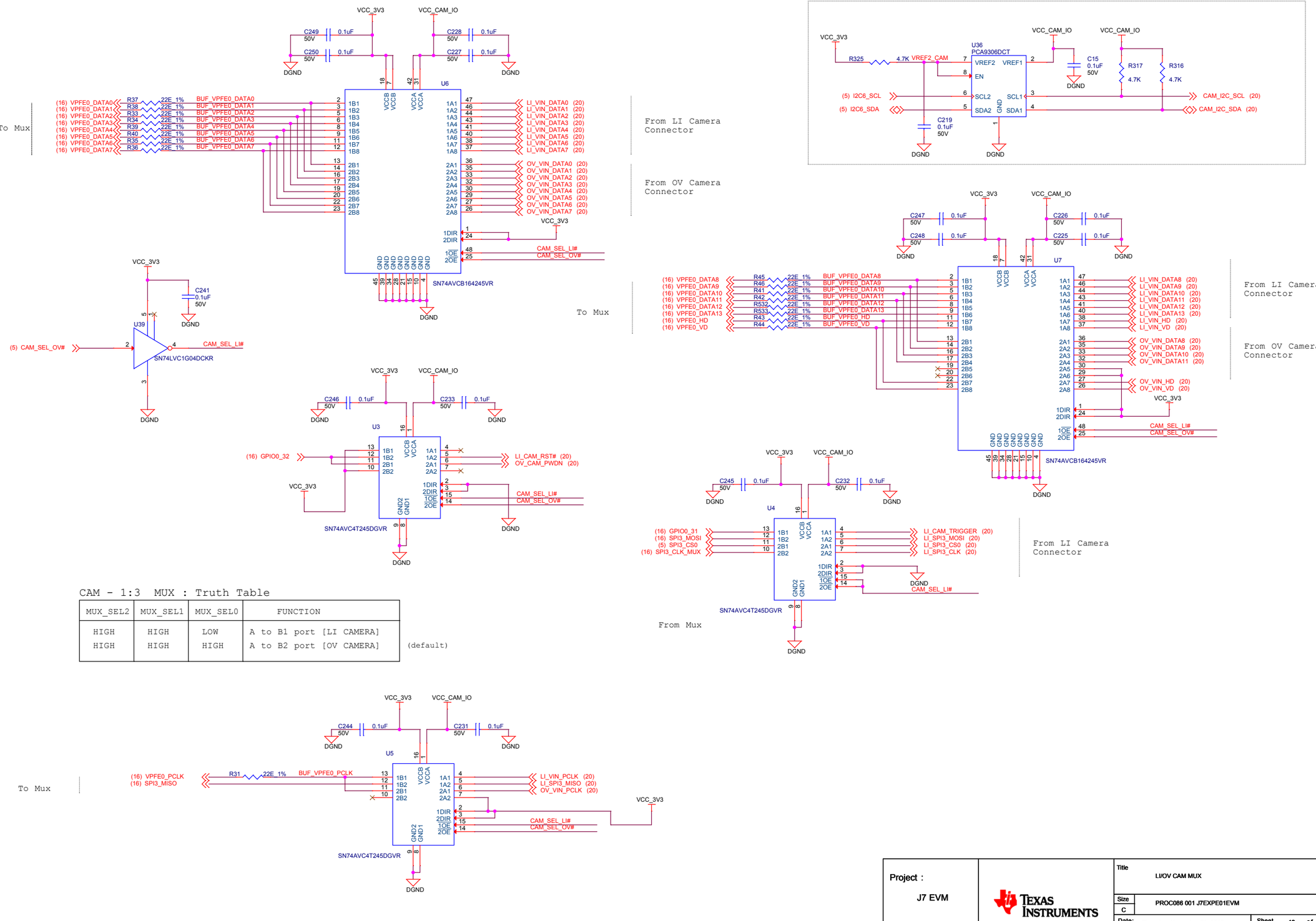
FPD LINK-III DISPLAY SERIALIZER



7b' I2C Address	R20	R24
0x1A (default)	30.9K	95.3K
(other - see DM)		

Project : J7 EVM	TEXAS INSTRUMENTS	Title: FPD LINK-III SERIALIZER
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 18 of 25

LI/OV CAM SELECTION MUX

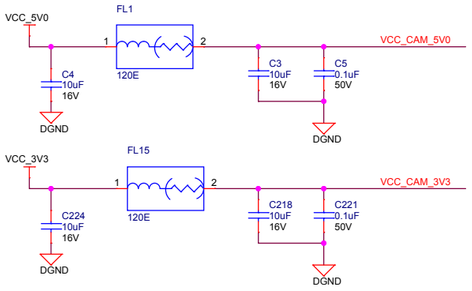


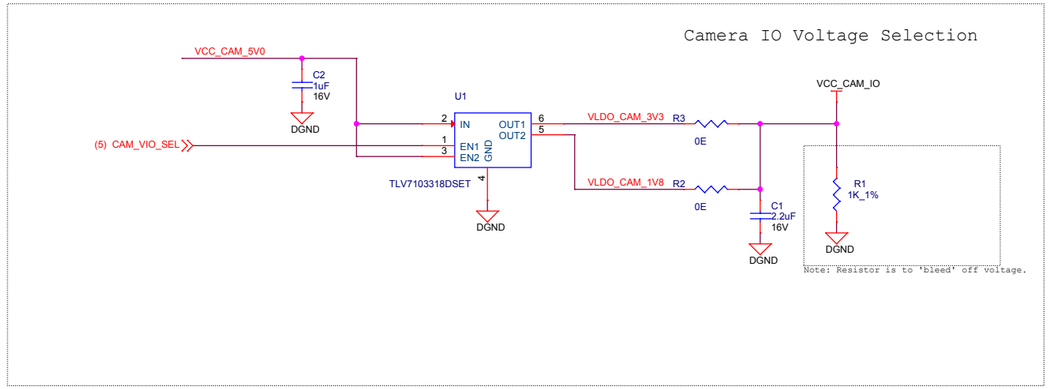
CAM - 1:3 MUX : Truth Table

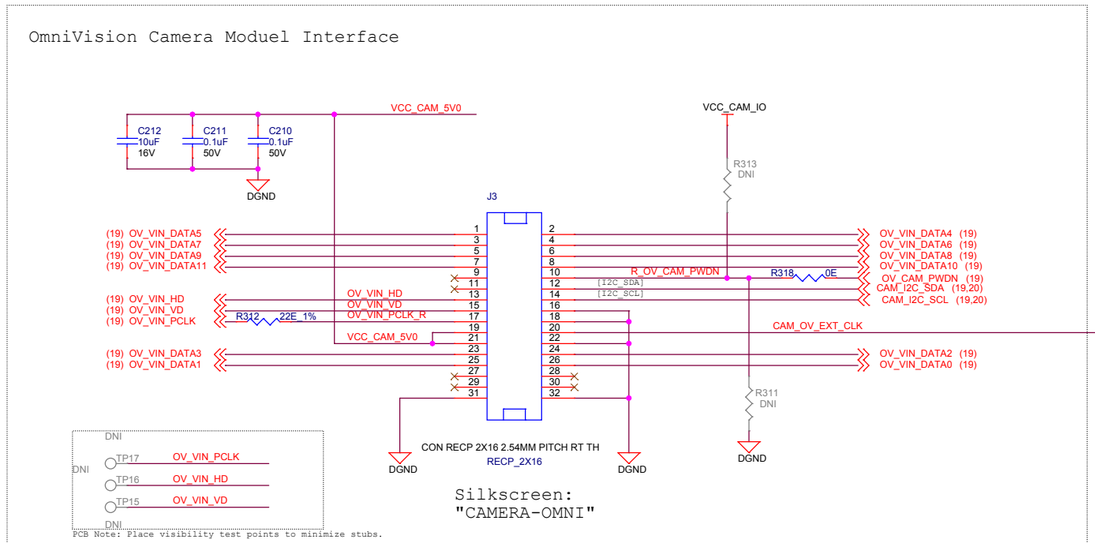
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION	
HIGH	HIGH	LOW	A to B1 port [LI CAMERA]	
HIGH	HIGH	HIGH	A to B2 port [OV CAMERA]	(default)

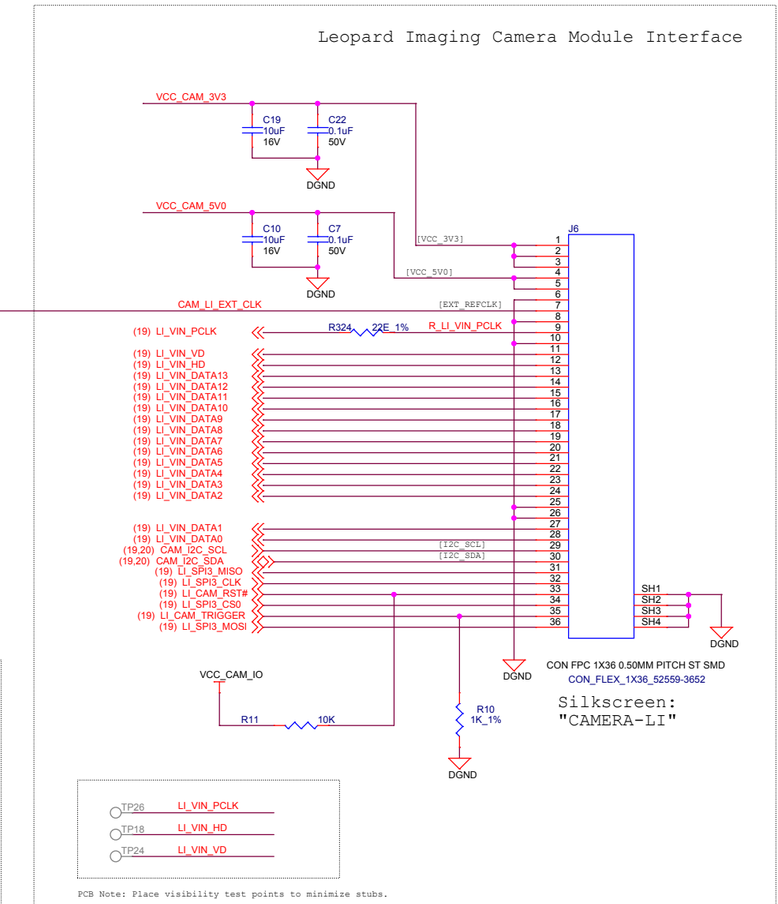
Project : J7 EVM	Title: LI/OV CAM MUX	
	Size: C	PROC086 001 J7EXPE01EVM — Rev: E3A
	Date: Thursday, November 21, 2019	Sheet 19 of 25

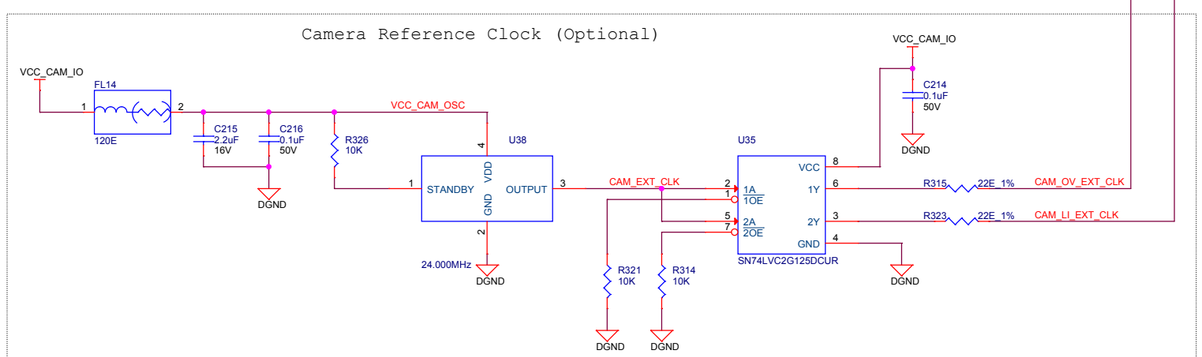
CAMERA MODULE INTERFACES







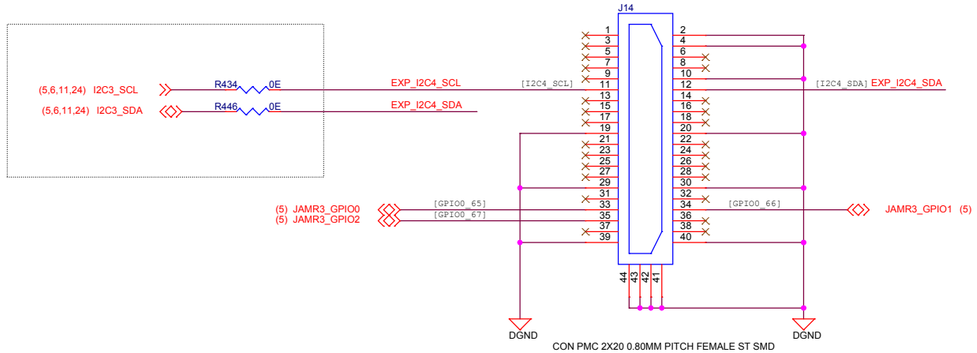


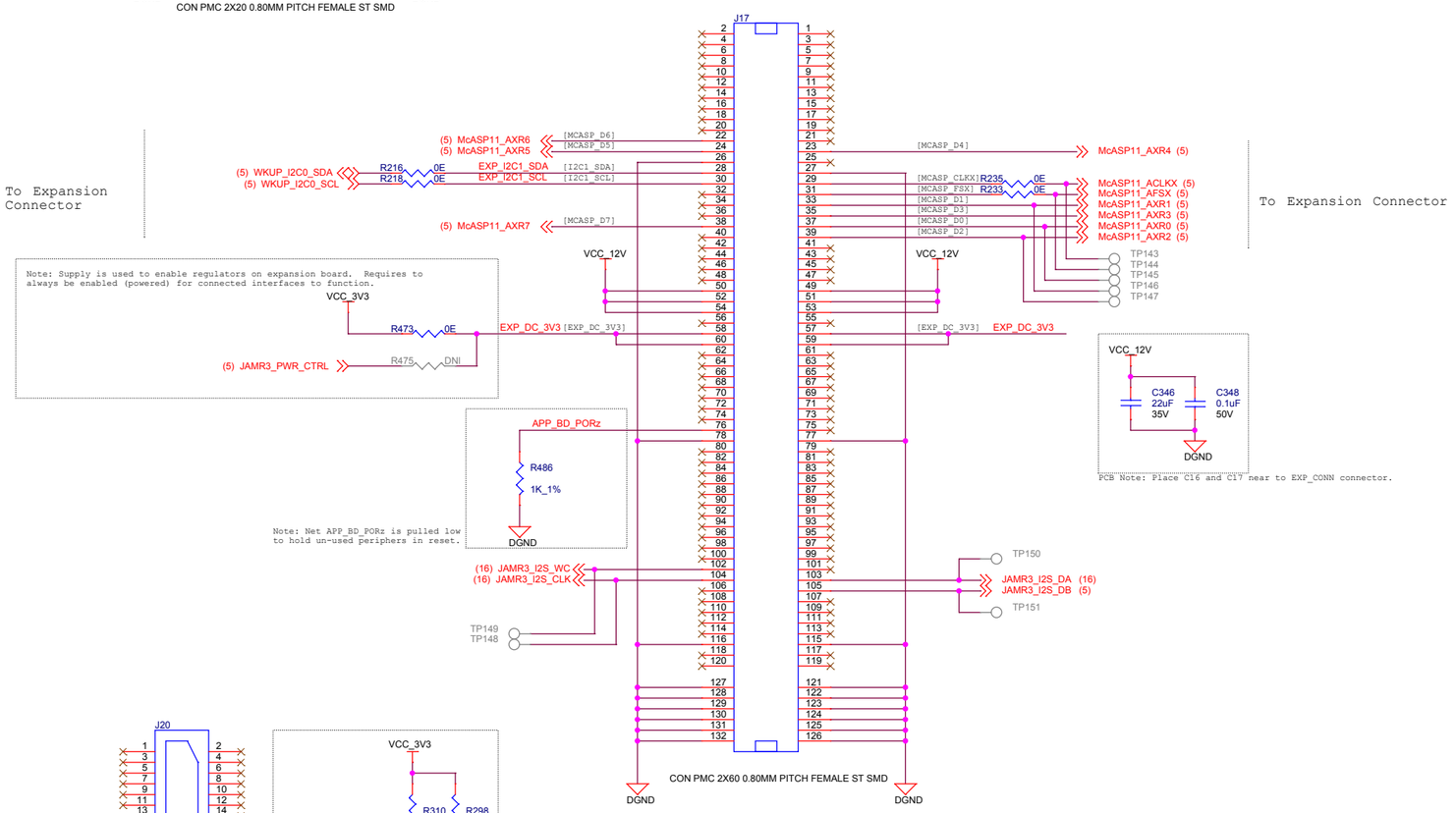


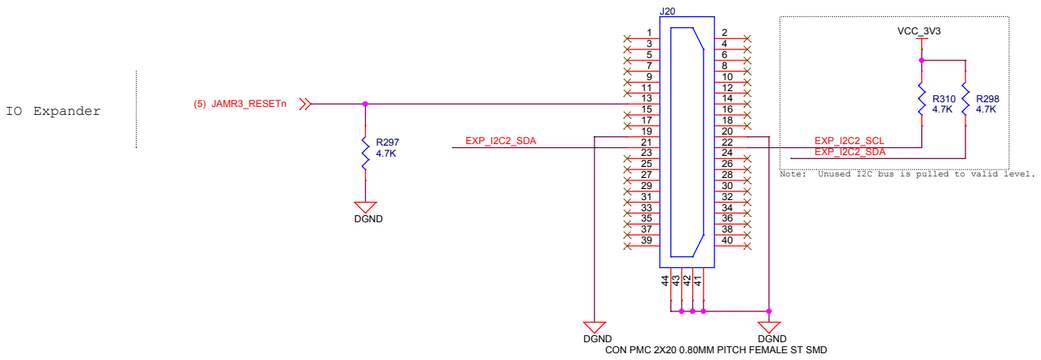
Project : J7 EVM	TEXAS INSTRUMENTS	Title: OV CAMERA INTERFACE
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 20 of 25

JAMR3/TUNER INTERFACE

Silkscreen "JAMR3/TUNER INTERFACE"

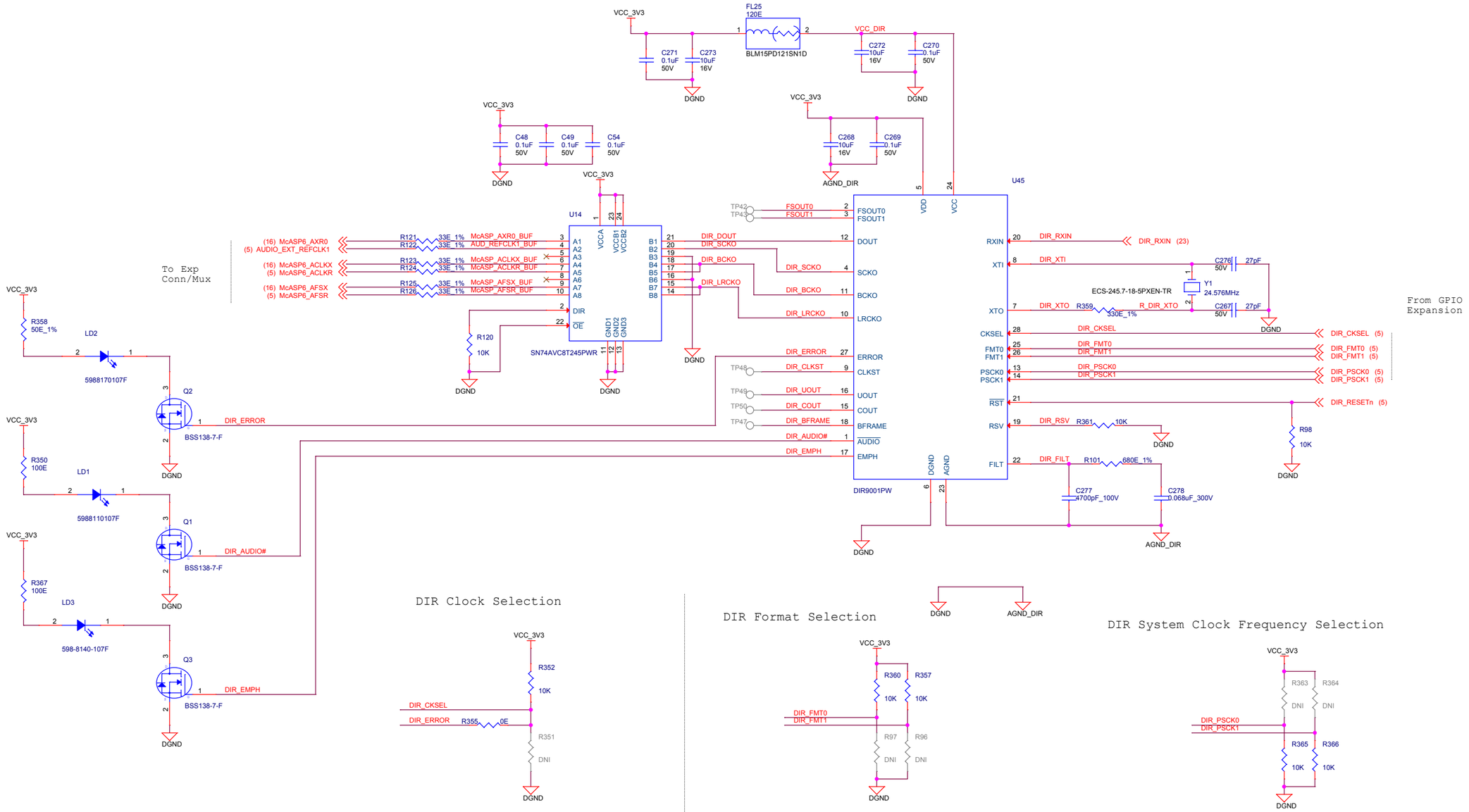






Project : J7 EVM	TEXAS INSTRUMENTS	Title: JAMR3 INTERFACE
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 21 of 25

Digital Audio Interface Receiver (DIR)



DIR Operation Mode and Clock Source

OPERATION MODE	CKSEL	ERROR Pin Status	SCKO, BCKO, LRCKO CLOCK SOURCE
PLL	L	H	PLL (VCO) free-running Clock
		L	PLL recovered clock
XTAL	H	H	XTAL clock
		L	XTAL clock
AUTO	Connected to ERROR Pin	H	XTAL clock
		L	PLL recovered clock (default)

SERIAL AUDIO DATA OUTPUT FORMAT SELECTION

FMT[1:0] SETTING		DOUT SERIAL AUDIO DATA OUTPUT FORMAT
FMT1	FMT0	
L	L	16-bit, MSB-first, Right-justified
L	H	24-bit, MSB-first, Right-justified
H	L	24-bit, MSB-first, Left-justified
H	H	24-bit, MSB-first, I2S (default)

SYSTEM CLK FREQUENCY OF PLL SELECTION

PSCK[1:0] SETTING		OUTPUT CLOCK FROM PLL SOURCE			
PSCK1	PSCK0	SCKO	BCKO	LRCKO	
L	L	128 fs	64 fs	fs	(default)
L	H	256 fs	64 fs	fs	
H	L	384 fs	64 fs	fs	
H	H	512 fs	64 fs	fs	

Project : J7 EVM

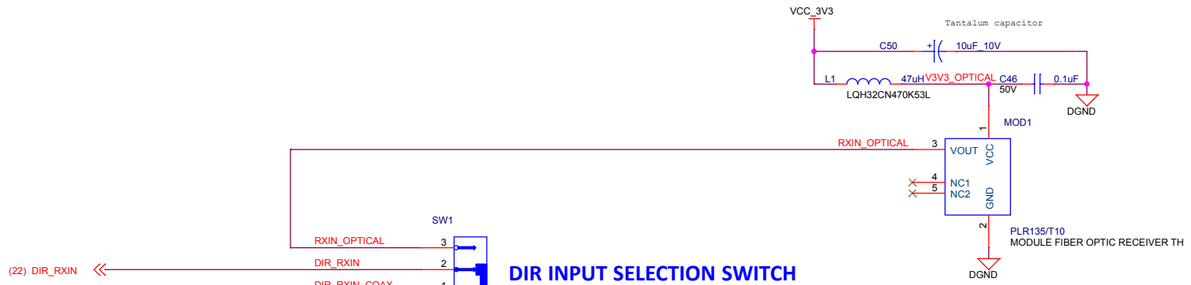
Title: DIR INTERFACE

Size: C | PROC086 001 J7EXPE01EVM | Rev: E3A

Date: Thursday, November 21, 2019 | Sheet 22 of 25

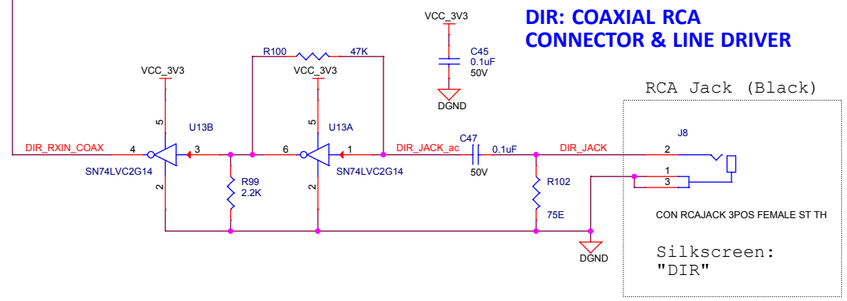
Digital Audio Interface Receiver (DIR) INPUT

DIR: FIBER OPTIC RECEIVER MODULE

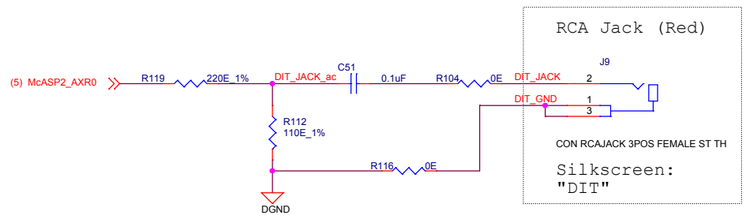


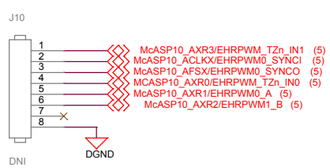
DIR INPUT SELECTION SWITCH

DIR: COAXIAL RCA CONNECTOR & LINE DRIVER



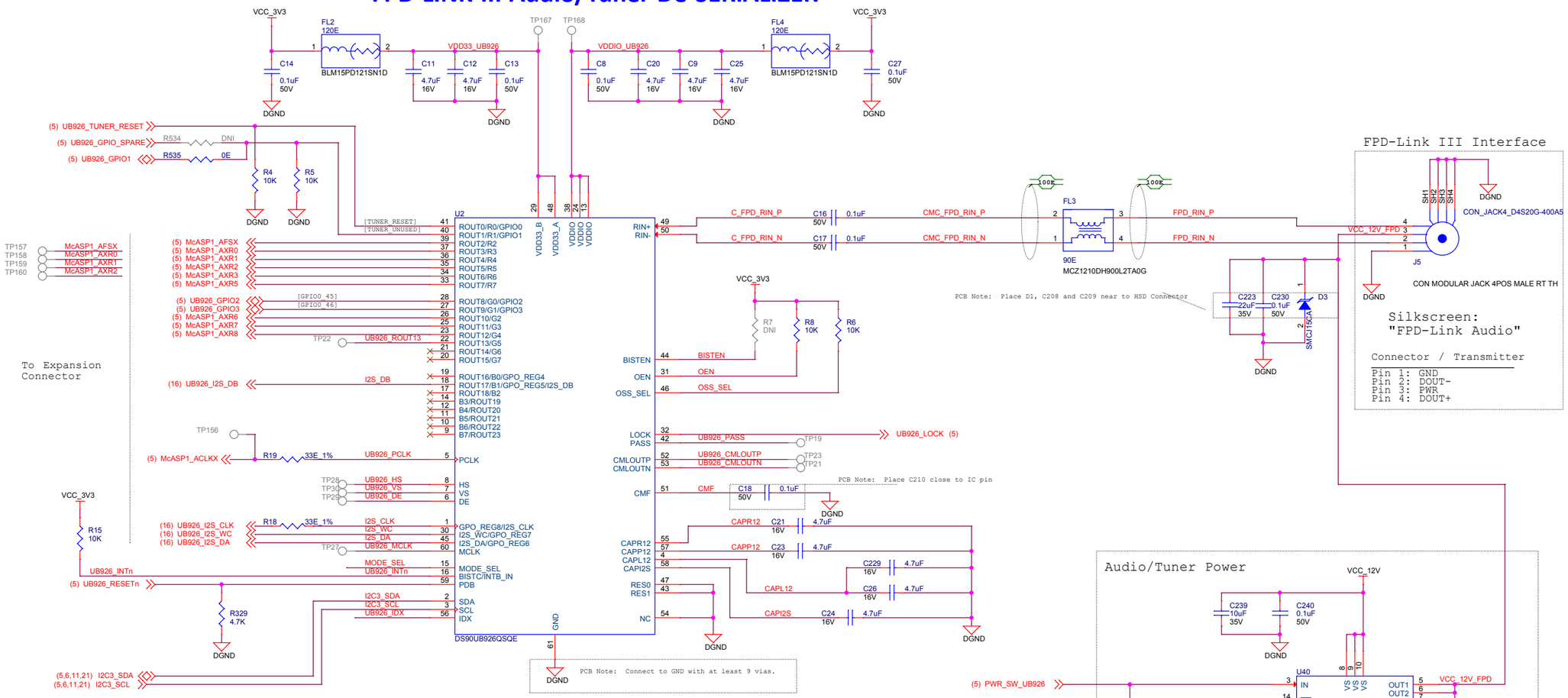
Digital Audio Interface Transmit (DIT)



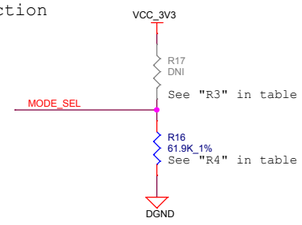


Project : J7 EVM	TEXAS INSTRUMENTS	Title: DIR INPUT SELECTION
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019 — Sheet 23 of 25

FPD LINK-III Audio/Tuner De-SERIALIZER

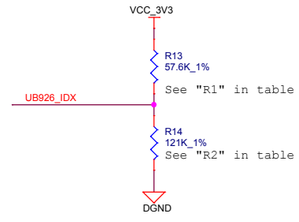


MODE Selection



Selected Mode: 0 (Default)	Software Config Only
LFMODE (15 - <85 MHz) REPEATER (OFF) BACK-COMPATIBLE (OFF) I2S-B OFF. 24B RGB	LFMODE (15 - <85 MHz) REPEATER (OFF) BACK-COMPATIBLE (OFF) I2S-B ON. 18B RGB
R3 = <open> R4 = 40.2K, 1% (or any)	R3 = <open> R4 = 40.2K, 1% (or any)

DEVICE ALIAS ID



7b' I2C Address	R1	R2
0x3B (default)	57.6K	121K
(other - see DM)		

Project : J7 EVM	TEXAS INSTRUMENTS	Title: FPD LINK-III De-SERIALIZER	
		Size: C	PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Thursday, November 21, 2019	Sheet 24 of 25

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

WASHERS

MH1 RWM100A

MH2 RWM100A

MH3 RWM100A

MH4 RWM100A

FIDUCIALS

FID1 DNI

FID2 DNI

FID3 DNI

FID4 DNI

FID5 DNI

FID6 DNI

LABELS

Board Serial No.

LBL1

PCB LABEL

THT-103-423-10

Assembly Revision.

LBL2

PCB LABEL

THT-103-423-10

BARE PCB

PCB1

PROC086E3

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

Project : J7 EVM	TEXAS INSTRUMENTS	Title: HARDWARE SCHEMATICS
		Size: C — PROC086 001 J7EXPE01EVM — Rev: E3A
		Date: Friday, November 22, 2019 — Sheet 25 of 25