STACKUP TABLE:

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.80mil	3.5	
3	L1 TOP	Copper	1.60mil		
4	Dielectric 1	R03003	5.00mil	3	
5	L2 GND	Copper	0.80mil		
6	Dielectric2	R04450F	3.62mil	3.52	
7	L3 SIGNAL 1	Copper	0.60mil		
8	Dielectric3	R04835 LOPRO	10.70mil	3.66	
9	L4 GND	Copper	0.60mil		
10	Dielectric4	370HR	8.02mil	4.02	
11	L5 SIGNAL 2	Copper	1.20mil		
12	Dielectric5	370HR	10.00mil	4.34	
13	L6 SIGNAL 3	Copper	0.60mil		
14	Dielectric6	370HR	4.82mil	4.06	
15	L7 GND	Copper	0.80mil		
16	Dielectric7	370HR	5.00mil	4.34	
17	L8 BOTTOM	Copper	1.60mil		
18	Bottom Solder	Solder Resist	0.80mil	3.5	
19	Bottom Overlay				

(L1-L8)
(L1-L2)

THIS IS AN IMPEDANCE CONTROLLED BOARD

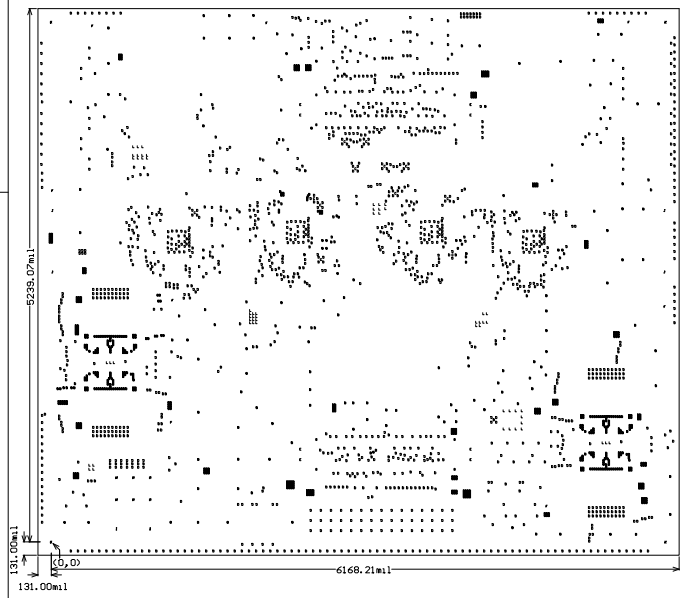
NOTE:
1. EXTERNAL LAYER CU THICKNESS ARE FINISHED THICKNESS AFTER PLATING.

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
2. THE SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED AS PER THE MANUFACTURING CAPABILITIES BUT NOT BEYOND 0.08MM PER SIDE OR 0.15MM OVERALL. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE MODIFIED.
3. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL FOR ETCHING ACCURACY NEAR THE ANTENNA REFER "ANTENNA_ETCHING_REQUIREMENTS" DOCUMENT
4. 5.9MIL VIA ONLY ON PAD SHOULD BE FILLED WITH CONDUCTIVE COPPER AND SURFACE SHOULD BE FLAT. FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON TOP SIDE.
5. BACKDRILLING INFO: 12 MIL DRILL AND 24 MIL PAD NEED TO BE REMOVED FROM THE BOTTOM TO LAYER 4 USE 24MIL DRILL BIT FOR BACKDRILLING ABOVE MENTIONED DRILLS. VENDOR MUST CUT L4 AND MUST NOT CUT L3.
6. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
7. BOW AND TWIST SHALL NOT EXCEED 0.7% OF LONGEST SIDE

IMPEDANCE TABLE

LAYER	TRACE WIDTH (mil)	TRACE SPACING (mil)	IMPEDANCE
1	10.5	-	50 OHM +/-10%
1	6.5	5.5	100 OHM +/-10%
3	5.1	-	50 OHM +/-10%
5	12	-	50 OHM +/-10%
6	6.9	-	50 OHM +/-10%
6	5	7	100 OHM +/-10%
8	7.75	-	50 OHM +/-10%
8	5.25	6.75	100 OHM +/-10%



Symbol	Count	Hole Size	Drill Layer Pair	Plated	Hole Tolerance(mil)
L	60	7.87mil (0.200mm)	L1 TOP - L8 BOTTOM	PTH	+0/-7.87
B	727	8.00mil (0.203mm)	L1 TOP - L8 BOTTOM	PTH	+0/-8
C	13	12.00mil (0.305mm)	L1 TOP - L8 BOTTOM	PTH	+0/-12
D	1522	12.20mil (0.310mm)	L1 TOP - L8 BOTTOM	PTH	+0/-12.2
E	8	39.37mil (1.000mm)	L1 TOP - L8 BOTTOM	PTH	+4/-0
F	8	40.00mil (1.016mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
G	8	47.24mil (1.200mm)	L1 TOP - L8 BOTTOM	PTH	+4/-0
H	6	70.87mil (1.800mm)	L1 TOP - L8 BOTTOM	PTH	+/-2
I	2	118.11mil (3.000mm)	L1 TOP - L8 BOTTOM	NPTH	+/-2
J	4	118.11mil (3.000mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
K	4	160.00mil (4.064mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
	2362 Total				

[5]

DRILL TABLE: (L1-L8)

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4 MIL
MIN. VIA PAD SIZE:	13.77MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 2 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER REFER STACKUP
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER 55MIL +/-10%
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [ ] ANSI IPC-6012 TYPE 3 CLASS 2
[X] OTHER +/- REFER NOTE 7

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC054	REV: C	SUN REV: Not In VersionControl
LAYER NAME = FAB1			
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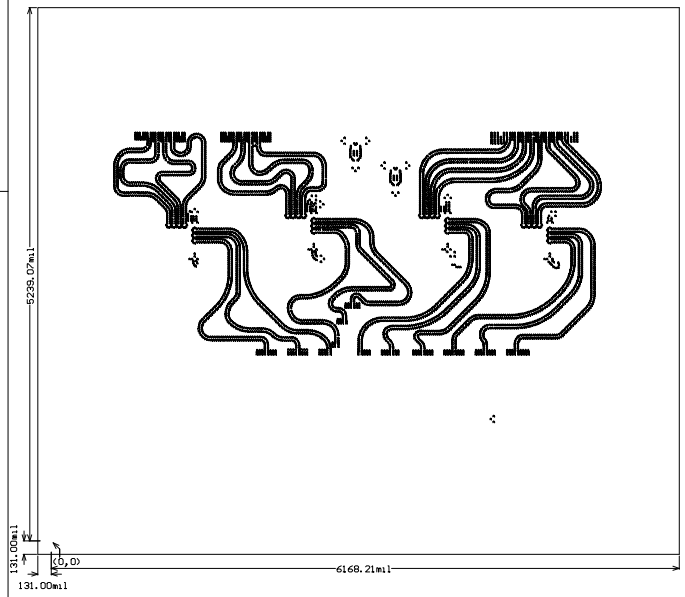
PROJECT TITLE:	MMW_CAS_RF_EVM
DESIGNED FOR:	Public Release
FILE NAME:	PROC054C_MMWCAS_RF_EVM.PcbDoc
ENGINEER:	a0271760
LAYOUT BY:	Tessolve
SCALE:	1.00
ALTIUM DESIGNER VERSION:	17.1.9.592

WO#307308-7306-D



Symbol	Count	Hole Size	Drill Layer Pair	Plated	Hole Tolerance(mil)
A	5523	5.90mil (0.150mm)	L1 TOP - L2 GND	PTH	+0/-5.9
	5523 Total				

DRILL TABLE: (L1-L2)

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC054	REV: C	SUN REV: Not In VersionControl
LAYER NAME = FAB2			
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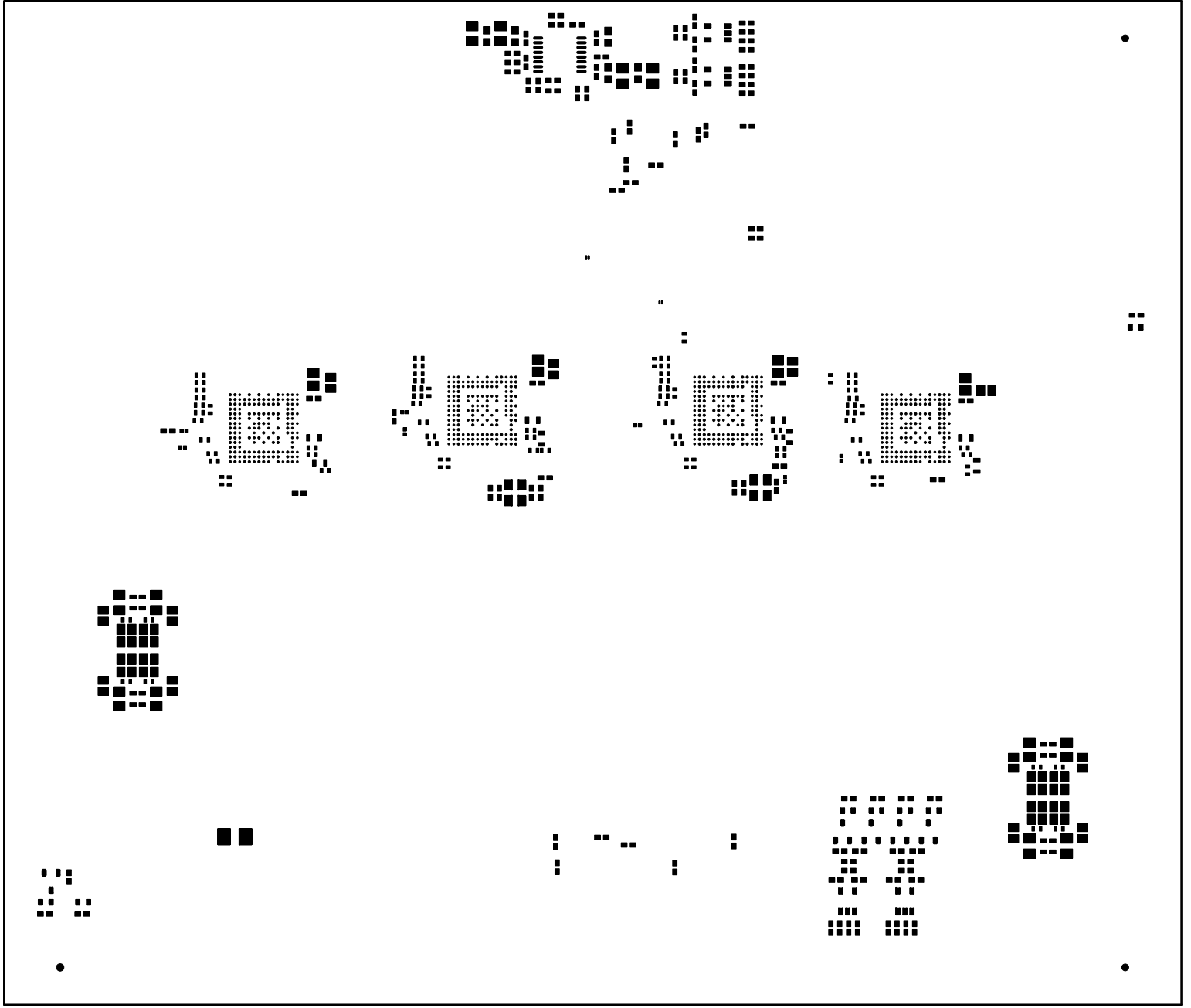
PROJECT TITLE: MMW_CAS_RF_EVM	
DESIGNED FOR: Public Release	
FILE NAME: PROC054C_MMWCAS_RF_EVM.PcbDoc	
ENGINEER: a0271760	LAYOUT BY: Tessolve
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.9.592



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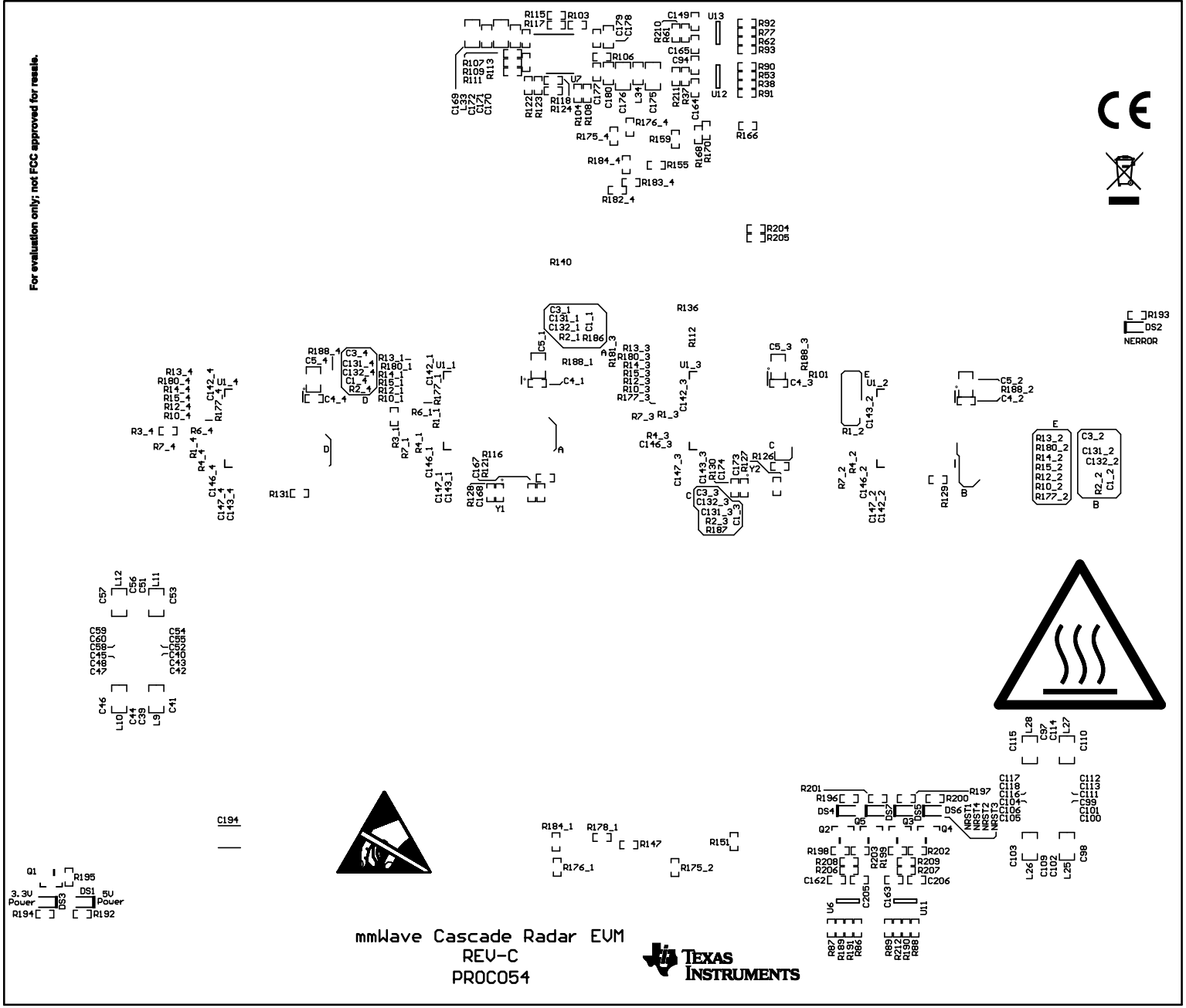

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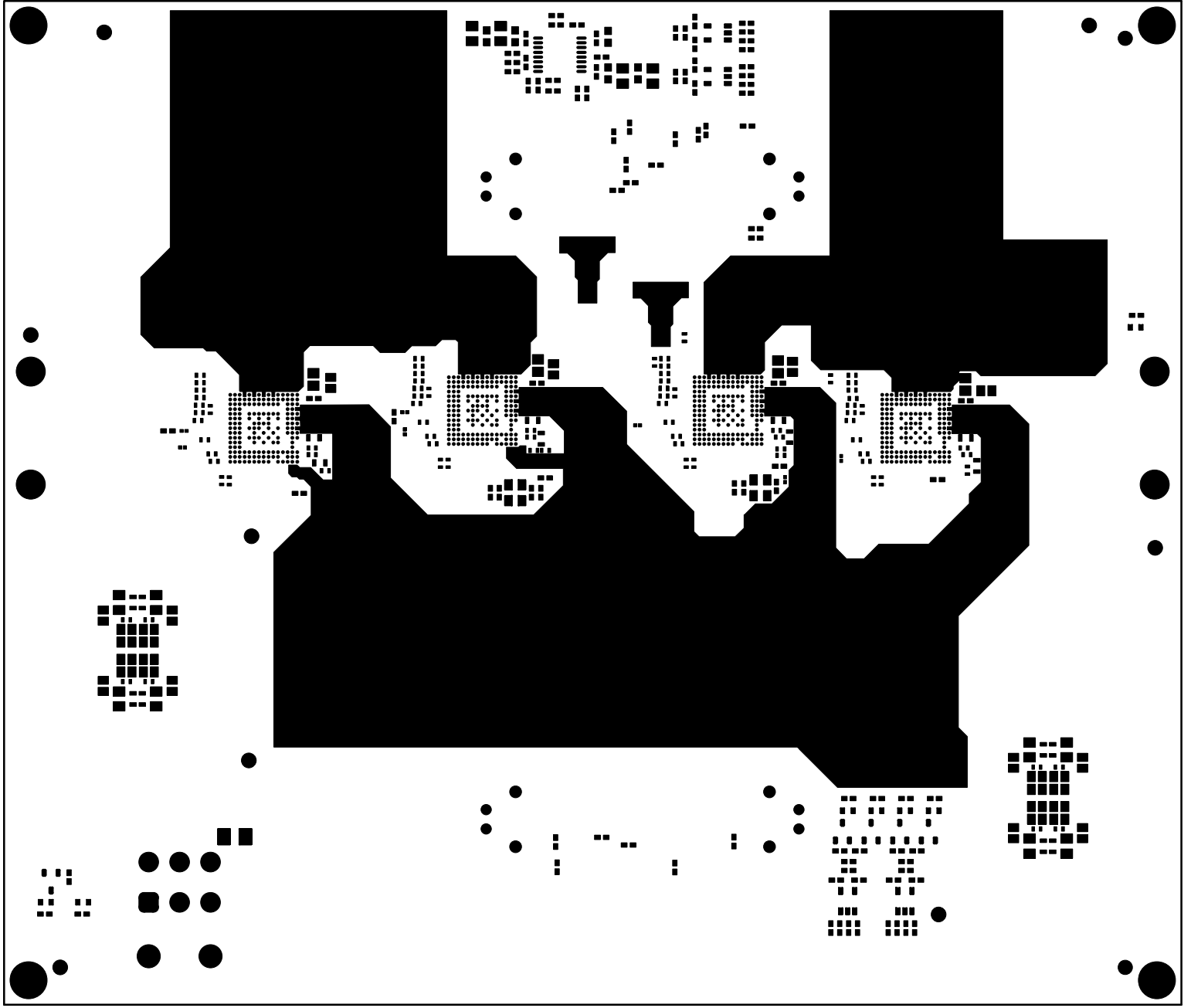

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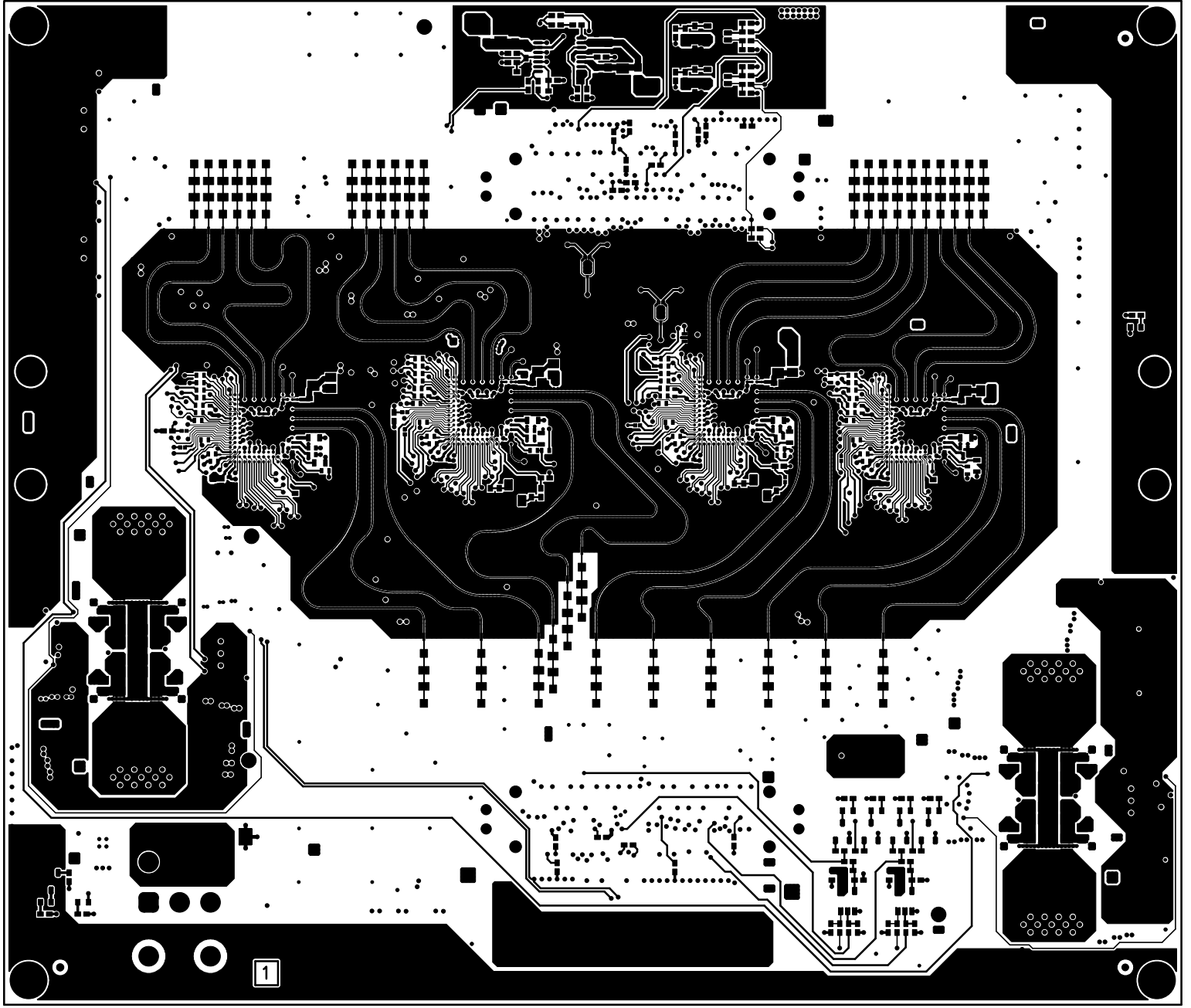

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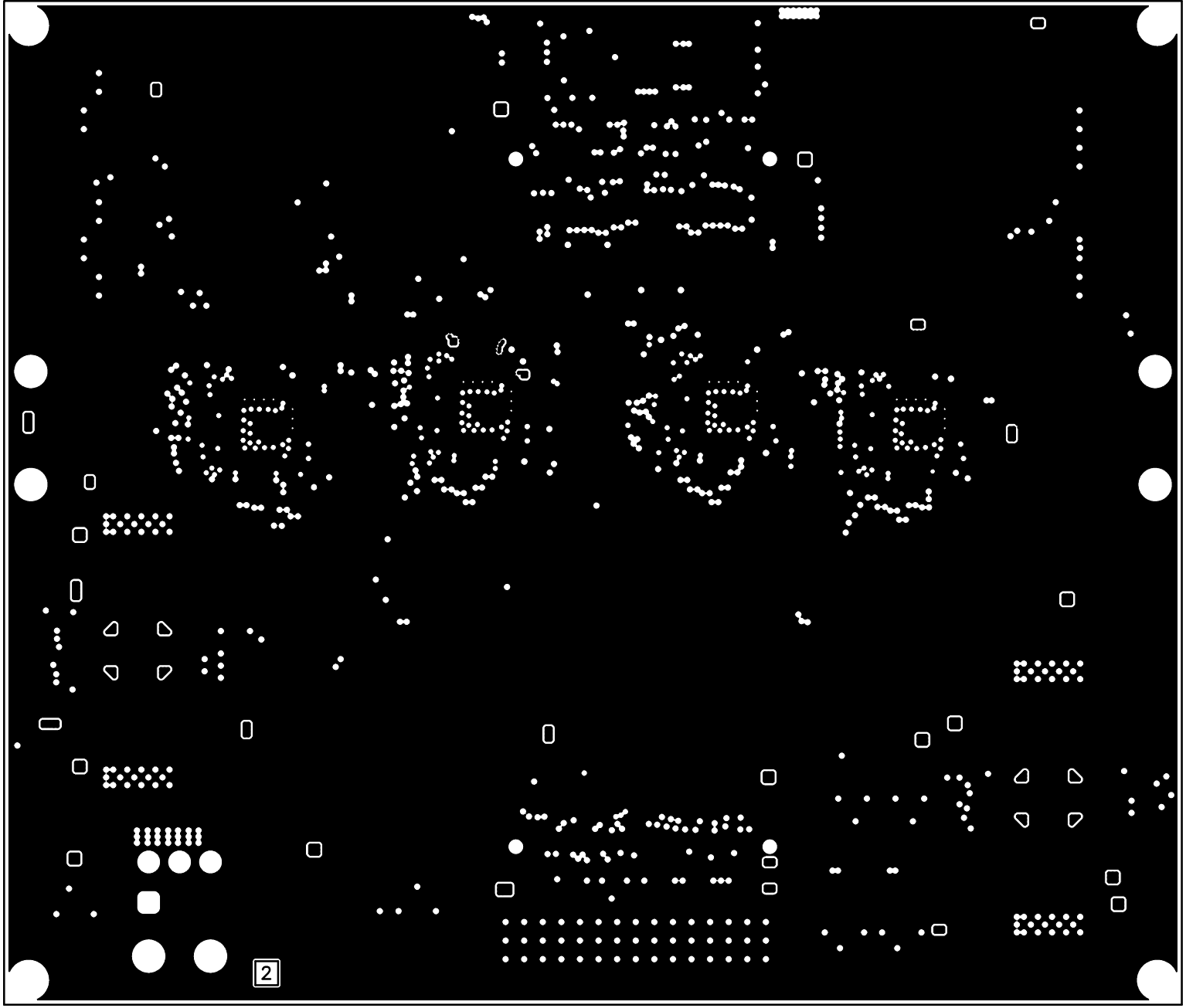

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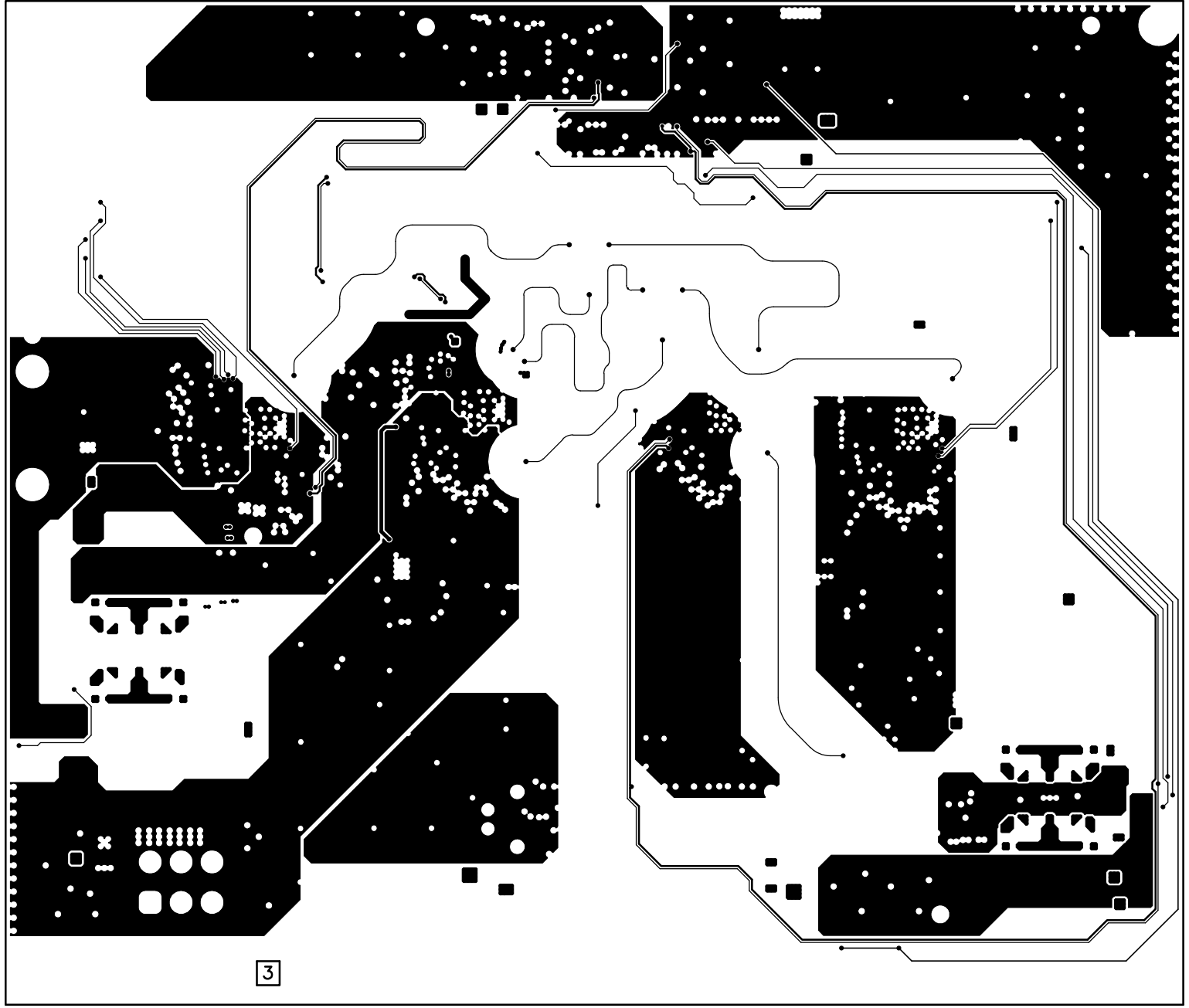

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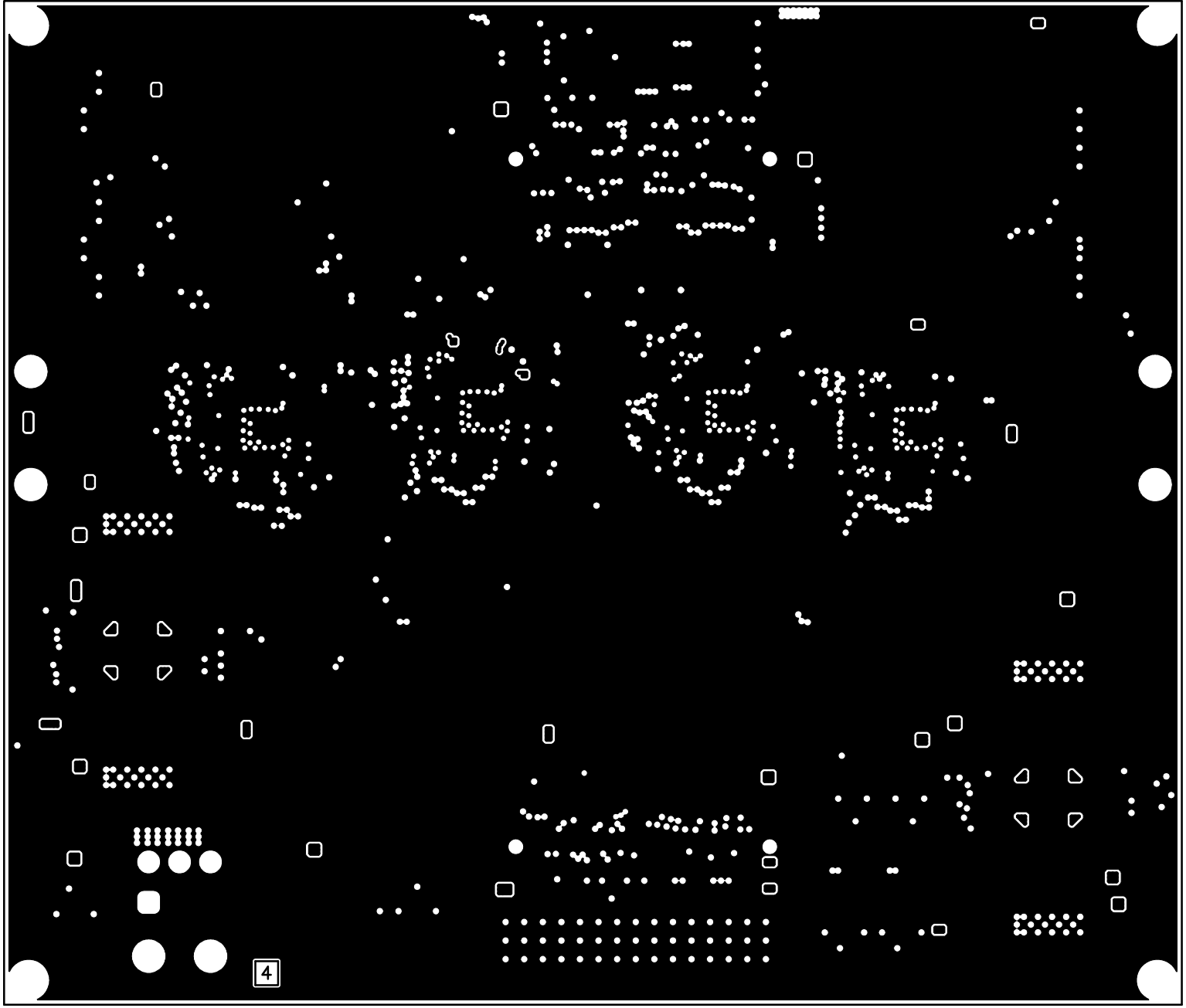

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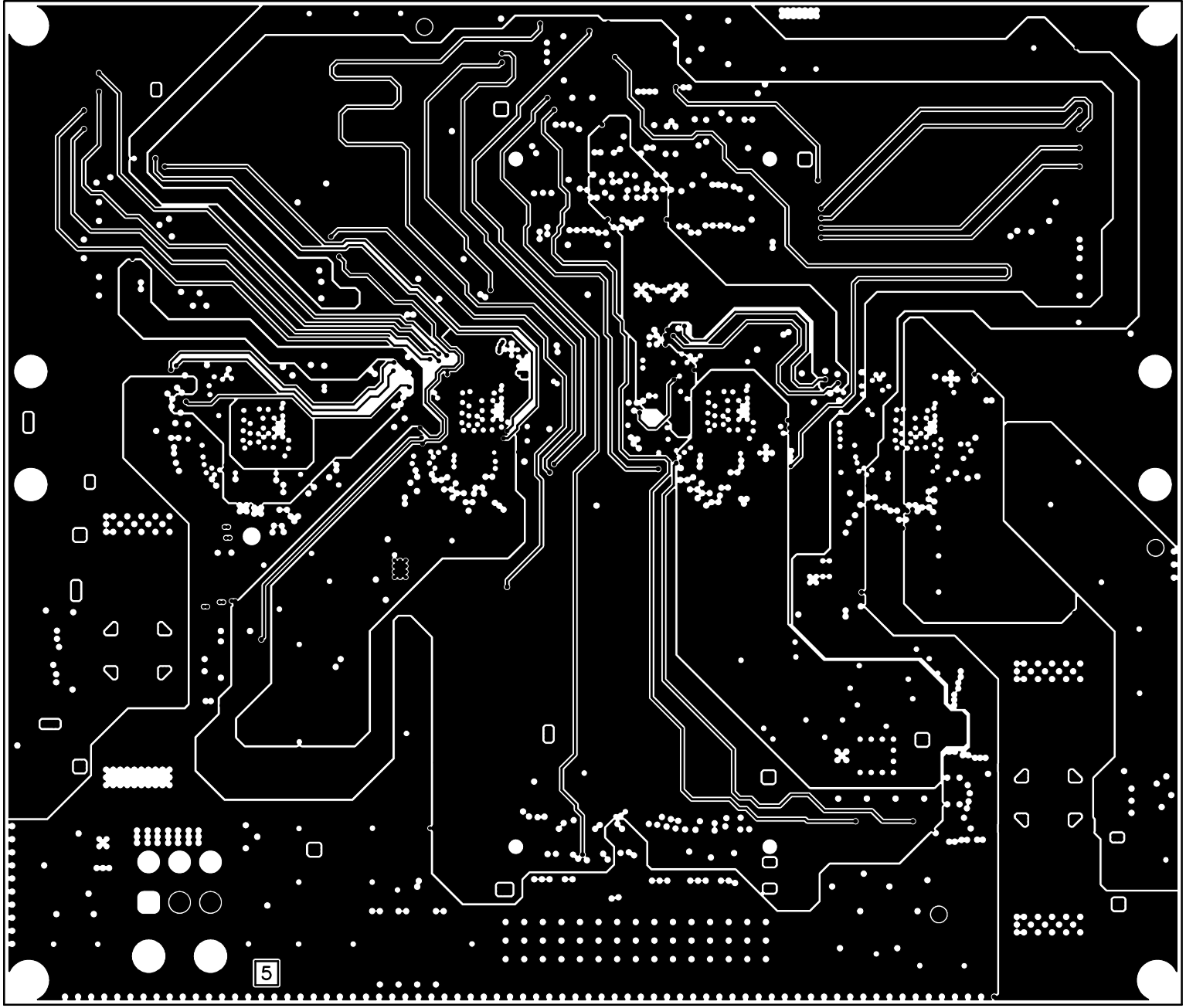

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LAYER NAME = L5 SIGNAL 2			
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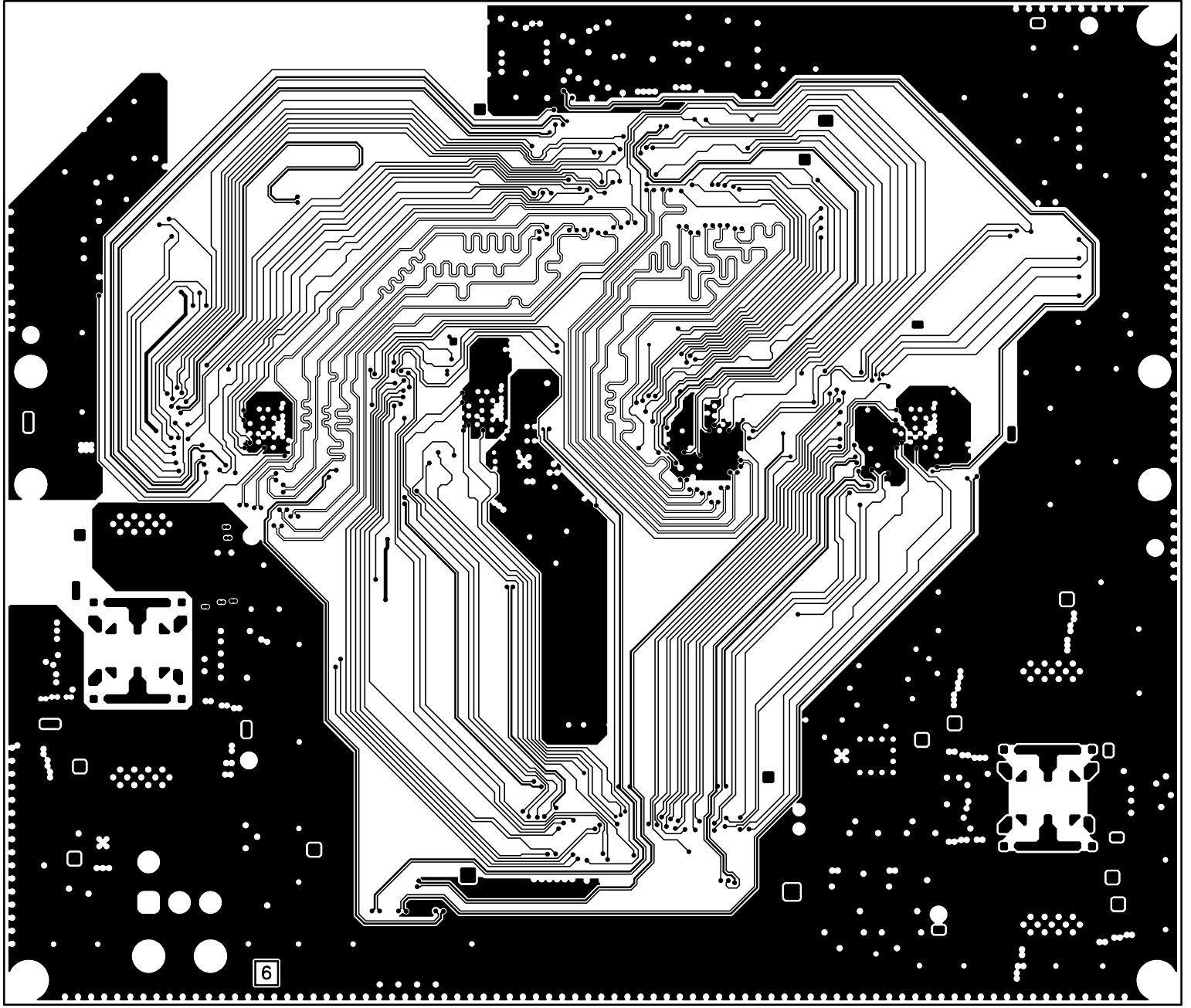

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LAYER NAME = L6 SIGNAL 3			
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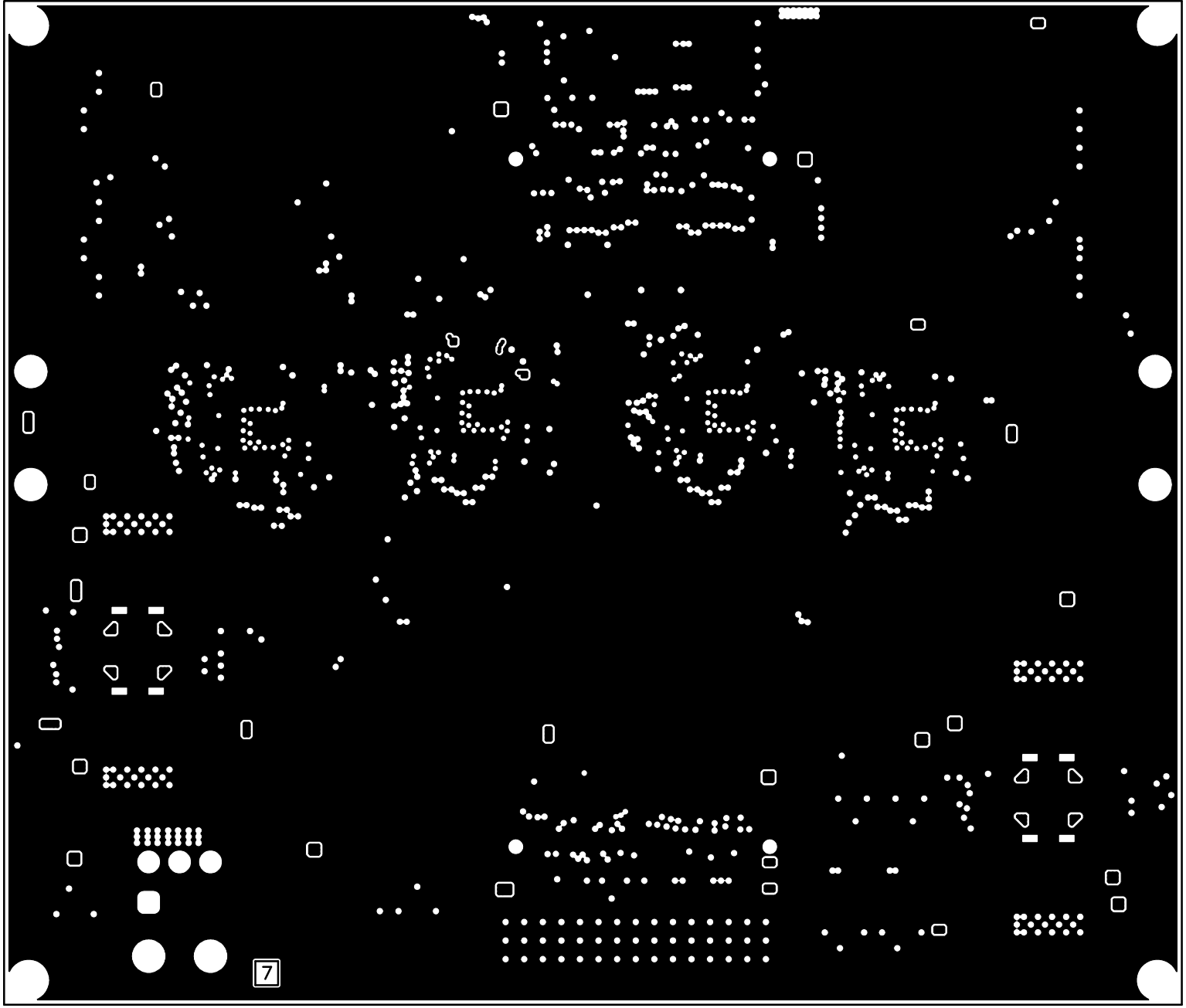

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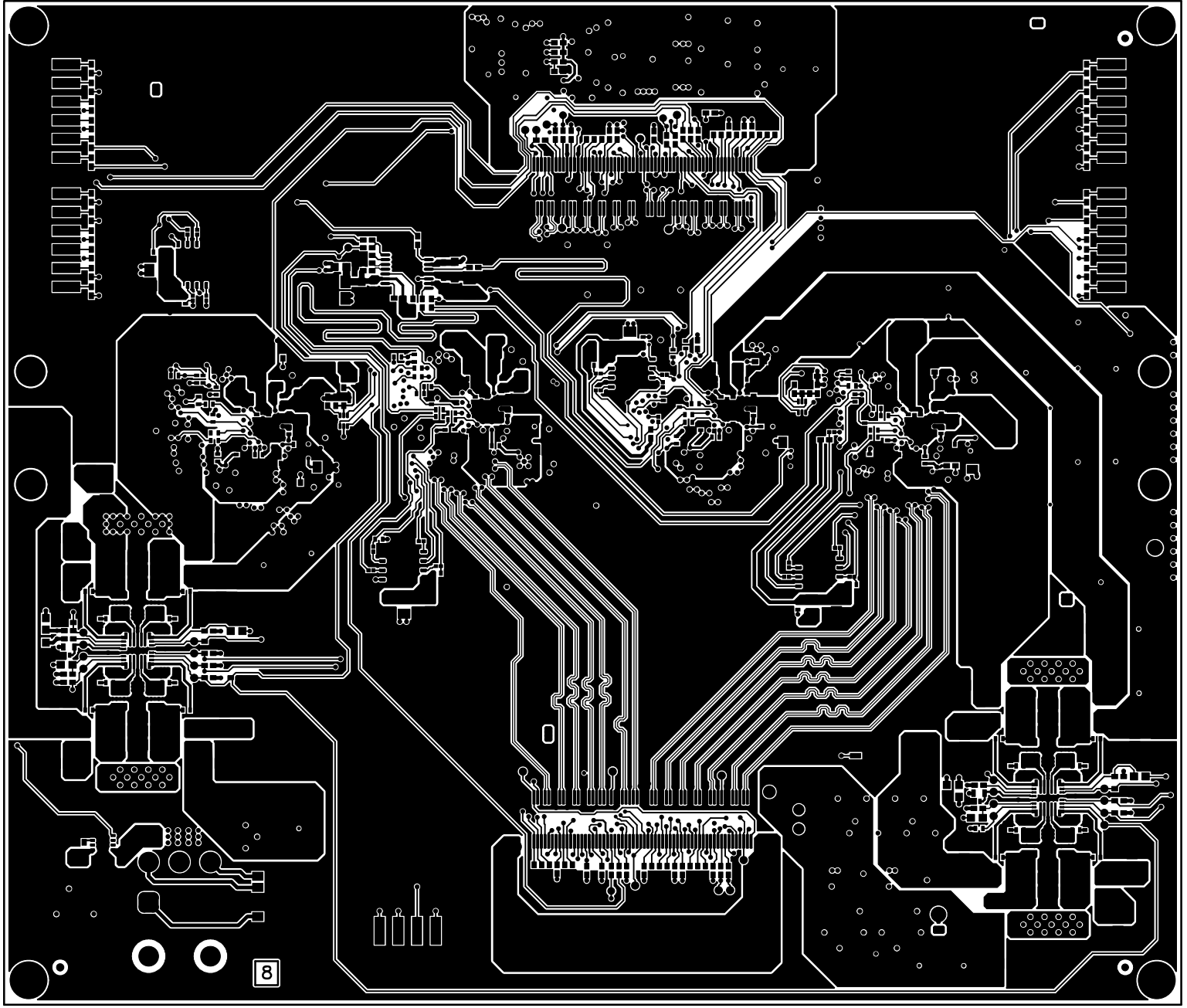

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC054	REV: C	SVN REV: Not In VersionControl
LAYER NAME = L8 BOTTOM			
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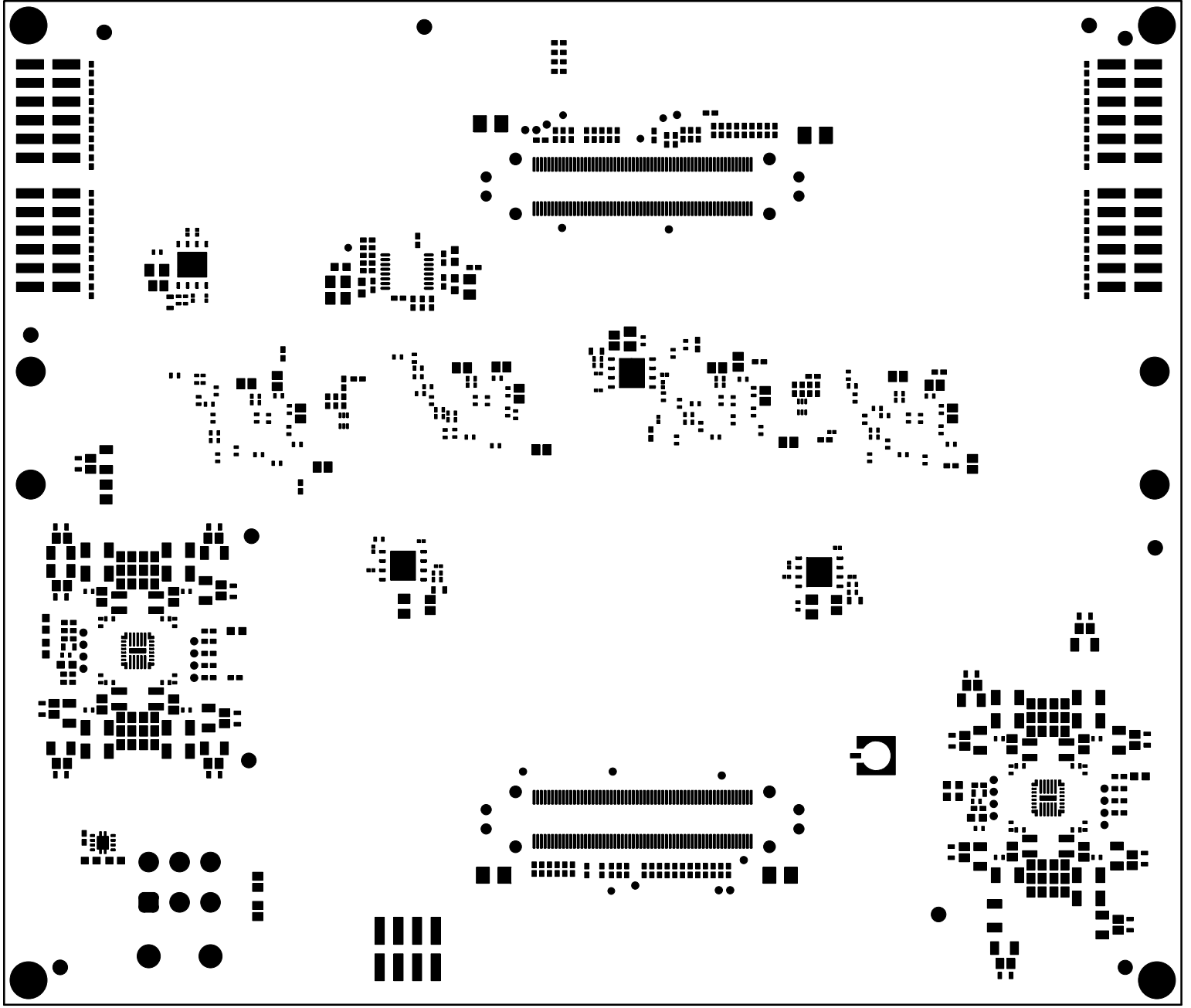

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC054	REV: C	SVN REV: Not In VersionControl
LAYER NAME = Bottom Solder			
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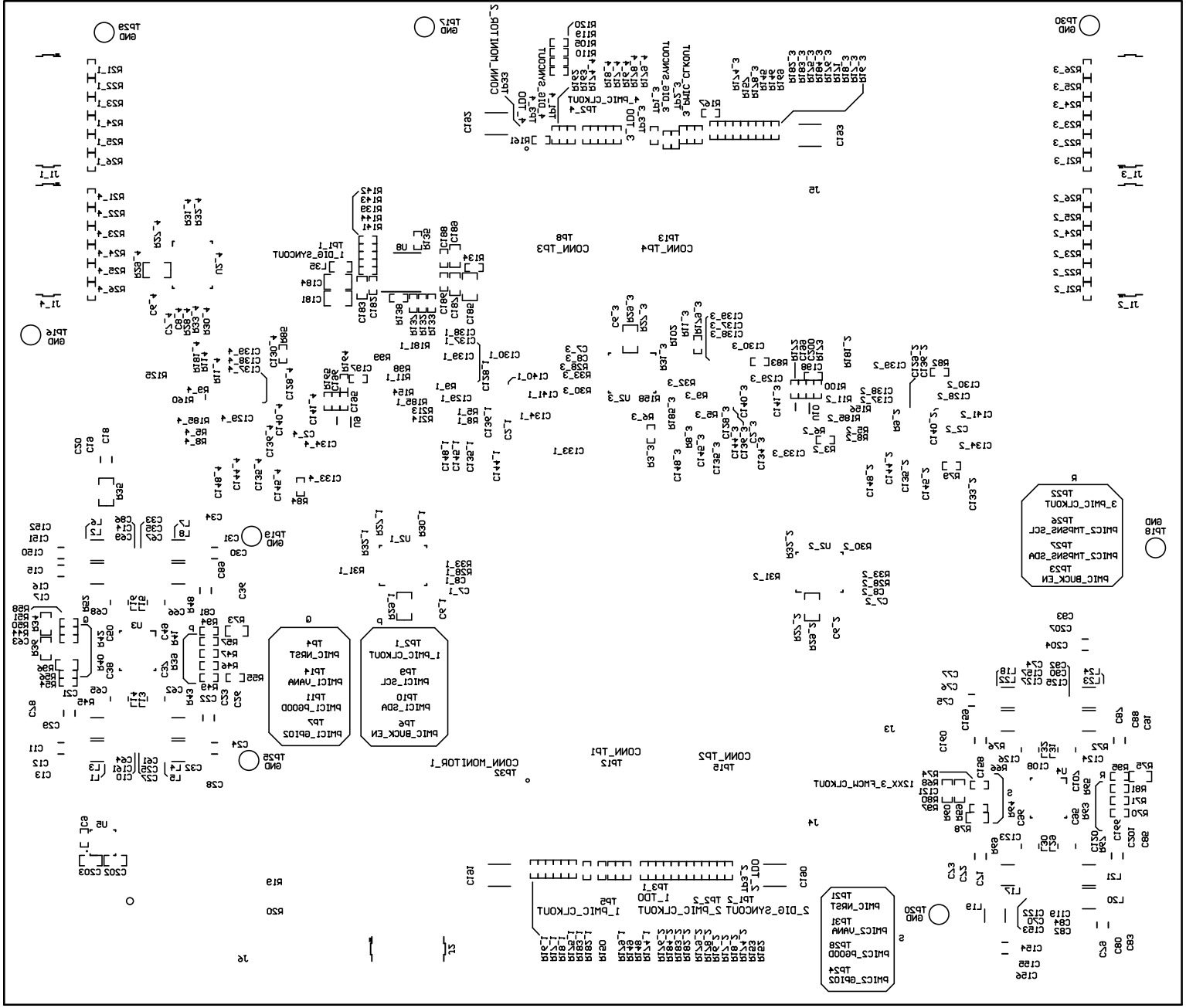

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC054	REV: C	SVN REV: Not In VersionControl
LAYER NAME = Bottom Overlay			
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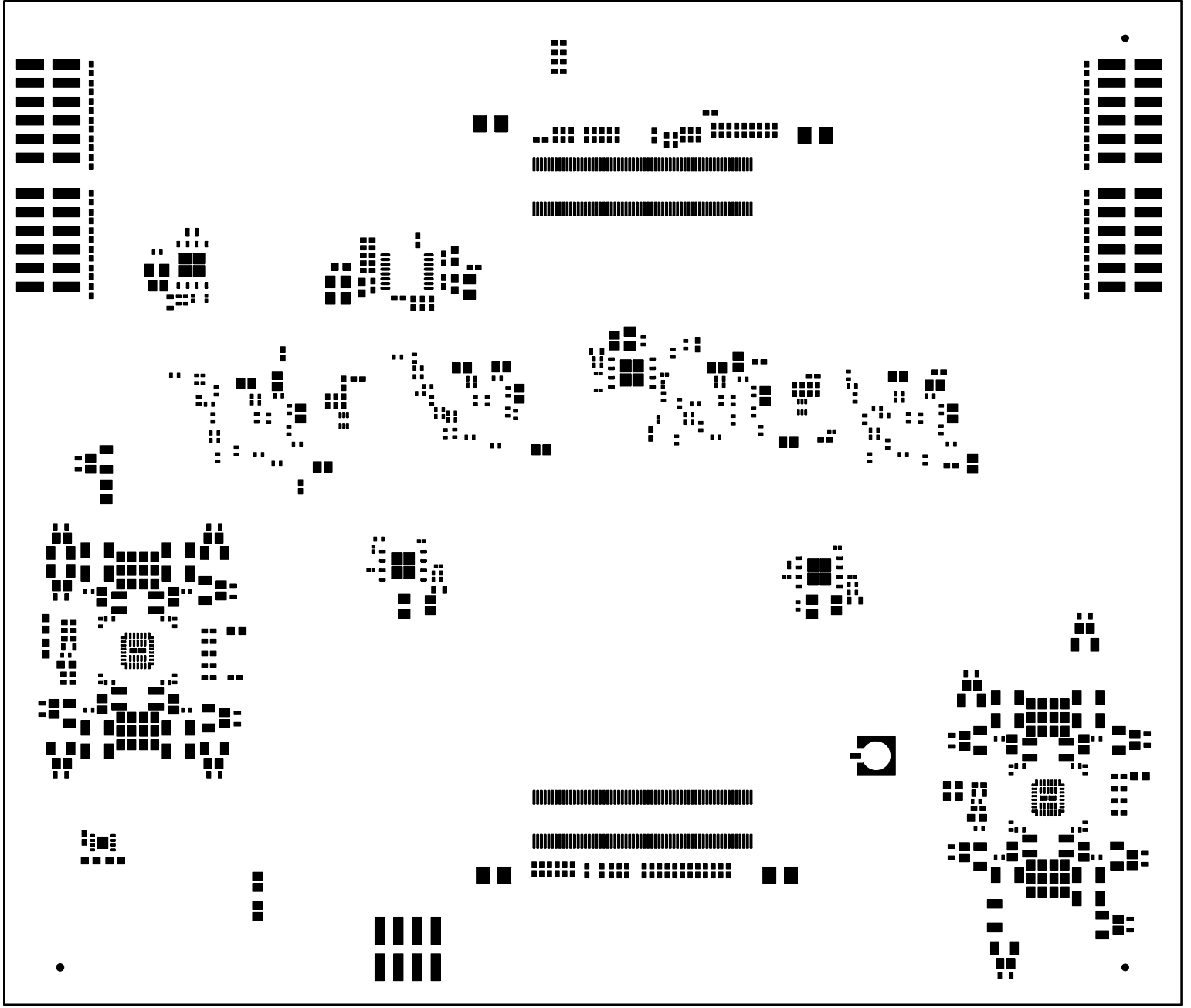

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