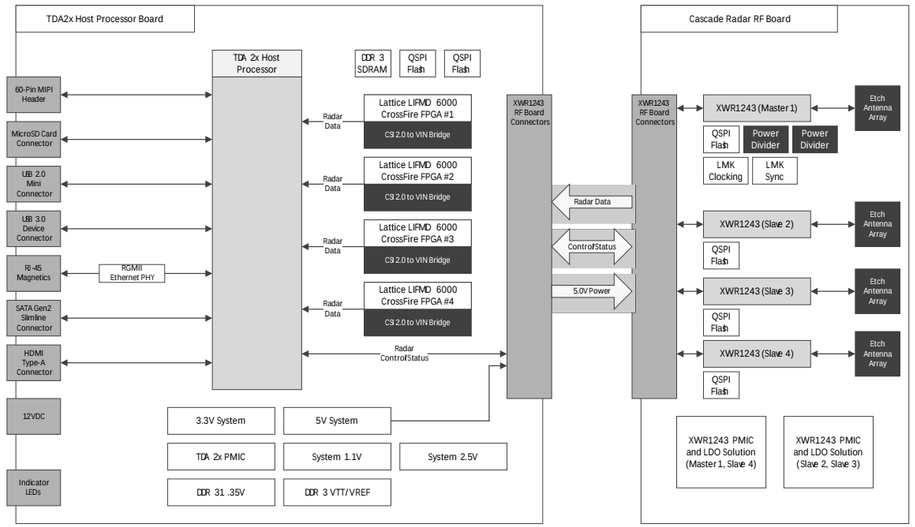
mmWave Cascade Radar RF Board

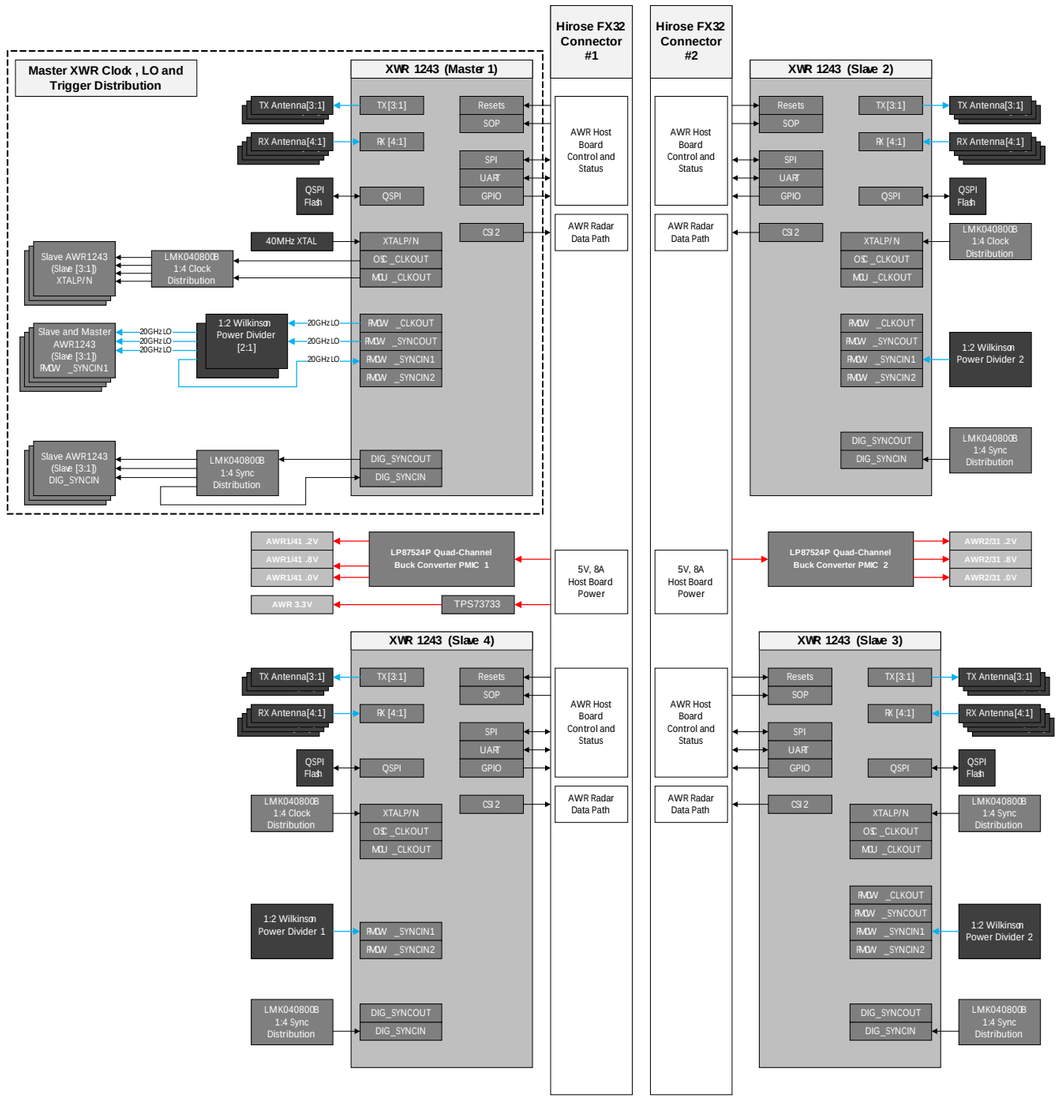
System Description

	Cascade Radar RF Board
4x AWR1243P 76-81GHz Radar SoC	Integrated VCO, LO distribution, PA, LNA, ADC, 3 TX and 4 RX ARM MCU R4 Controller
AWR RF Peripherals	
12x TX, 16x RX Antennas	12 total transmitters across all 4 AWR1243 P devices 16 total receivers across all 4x AWR1243P devices
Embedded Antenna	4-element series-fed patch antenna
20 GHz LO Star Distribution	2x Wilkinson Power dividers fed by the Master AWR12x device LO output to Slave AWR12x devices
AWR Digital Peripherals	
CSI2.0 4-lane	600Mbps/Lane for 2.4Gbps ADC IF data per device
QSPI Flash	16Mbit QSPI flash for AWR firmware updates
Serial Peripherals	SPI, I2C, UART, GPIO
System Temperature	TMP112 I2C Temperature Sensors
Power	
Radar Power Management IC (PMIC) Solution	2x LP87524P Quad-Channel, Integrated FET, Buck Converters and LC filtering solution

Cascade Radar Evaluation Kit Diagram



Cascade Radar RF System Diagram



PROC054C_System_Top.SchDoc
CASCADE_RF_BOARD

PROC054C_EVM_Hardware.SchDoc
EVM_HARDWARE

PROC054C_Revision_History.SchDoc
REVISION_HISTORY

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: Coversheet	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 19
Drawn By: a0271760		File: PROC054C_Coversheet.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

TEXAS INSTRUMENTS
http://www.ti.com

Cascade Radar RF Board - Top Level Schematic

References

12XX_1243 Cascade Radar Application Note

12XX_1 (Master)

12XX_1
PROC054C_12XX_1.SchDoc

12XX_1
PROC054C_PULL_UP_DOWN_1.SchDoc

12XX_1
PROC054C_12XX_DECOUPLING_CAPS_1.SchDoc

12XX_3 (Slave)

12XX_3
PROC054C_12XX_1.SchDoc

12XX_3
PROC054C_PULL_UP_DOWN_1.SchDoc

12XX_3
PROC054C_12XX_DECOUPLING_CAPS_1.SchDoc

HOST_CONNECTORS
PROC054C_HOST_CONNECTOR.SchDoc

System Power/Reset

SYSTEM_POWER
PROC054C_System_Power.SchDoc

40MHz Generation/Distribution

40MHZ_CLOCK
PROC054C_40MHZ_CLOCK_1.SchDoc

Digital Sync and 20GHZ LO

DIG_SYNC_LO_20GHZ
PROC054C_FMCW_SYNC.SchDoc

12XX_2 (Slave)

12XX_2
PROC054C_12XX_1.SchDoc

12XX_2
PROC054C_PULL_UP_DOWN_1.SchDoc

12XX_2
PROC054C_12XX_DECOUPLING_CAPS_1.SchDoc

12XX_4 (Slave)

12XX_4
PROC054C_12XX_1.SchDoc

12XX_4
PROC054C_PULL_UP_DOWN_1.SchDoc

12XX_4
PROC054C_12XX_DECOUPLING_CAPS_1.SchDoc

System LED Indicators

SYSTEM_LED_INDICATORS
PROC054C_SYSTEM_LED.SchDoc

System Temperature Sensors

SYSTEM_TEMP_SENSORS
PROC054C_ON_BRD_TEMP_SENSOR.SchDoc

System Test Connectors And Termination

SYSTEM_TEST_CONN_TERMINATION
PROC054C_SMA_SMP_CONNECTORS.SchDoc

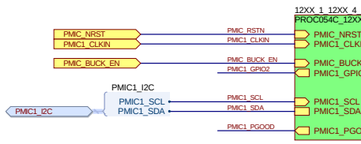
Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: System Top	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 19
Drawn By: a0271760		File: PROC054C_System_Top.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

Cascade RF System Power

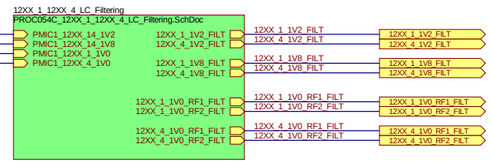
References

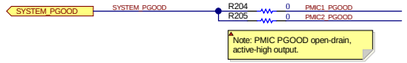
4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC #1 - Master 12XX_1 and Slave 12XX_4

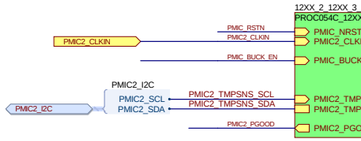


LC Filtering, Ferrite Filtering 12XX_1 and 12XX_4

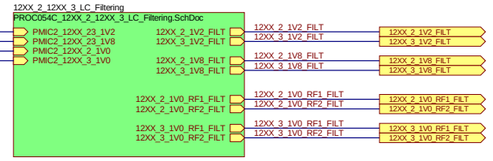




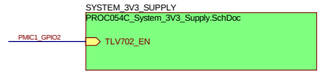
PMIC #2 - Master 12XX_2 and Slave 12XX_3



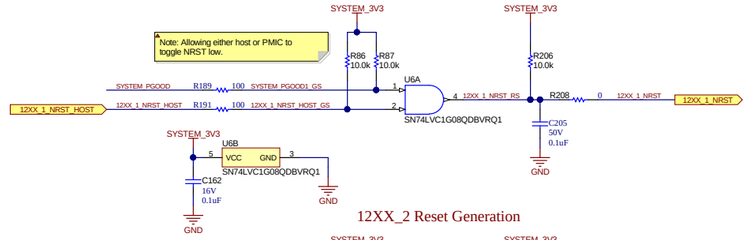
LC Filtering, Ferrite Filtering 12XX_2 and 12XX_3



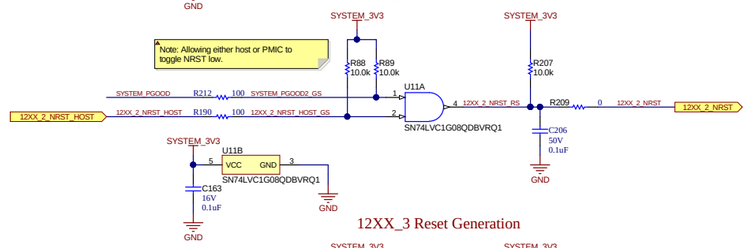
3.3V System LDO



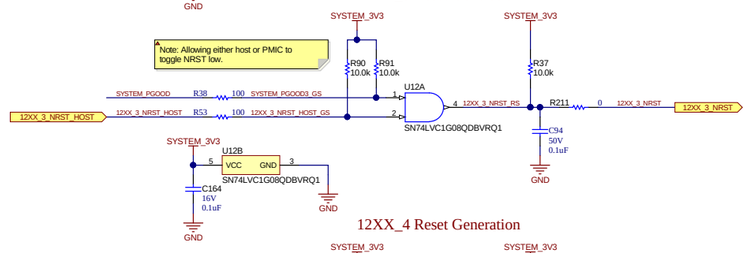
12XX_1 Reset Generation



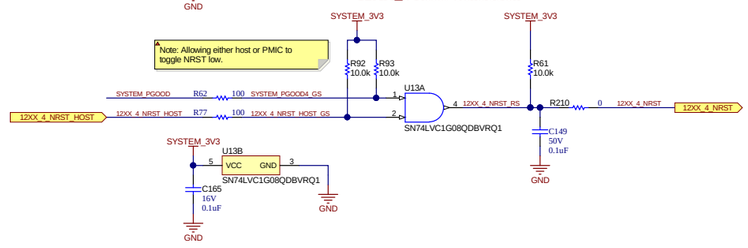
12XX_2 Reset Generation



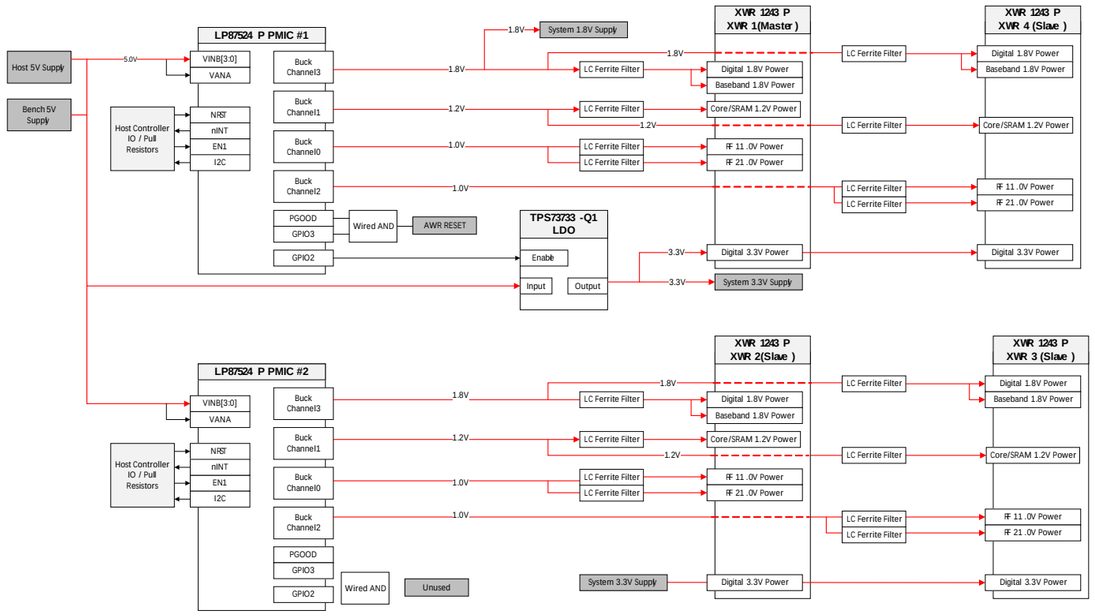
12XX_3 Reset Generation

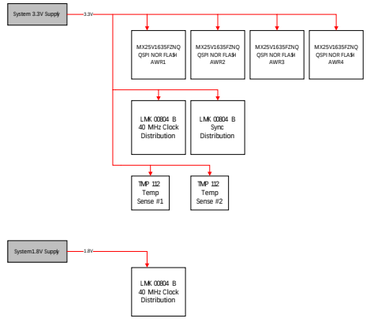


12XX_4 Reset Generation

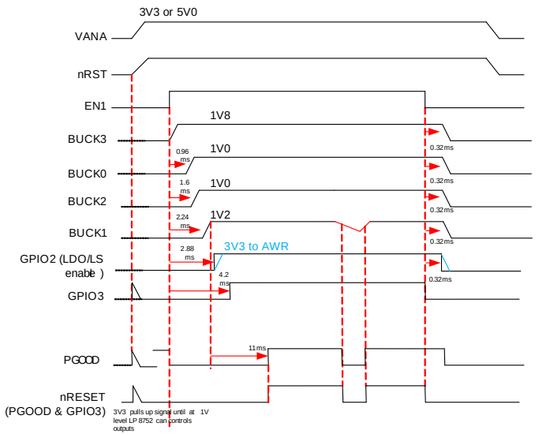


XWR1243 Cascade System Power Diagram





XWR1243 Cascade System Power Sequence Diagram



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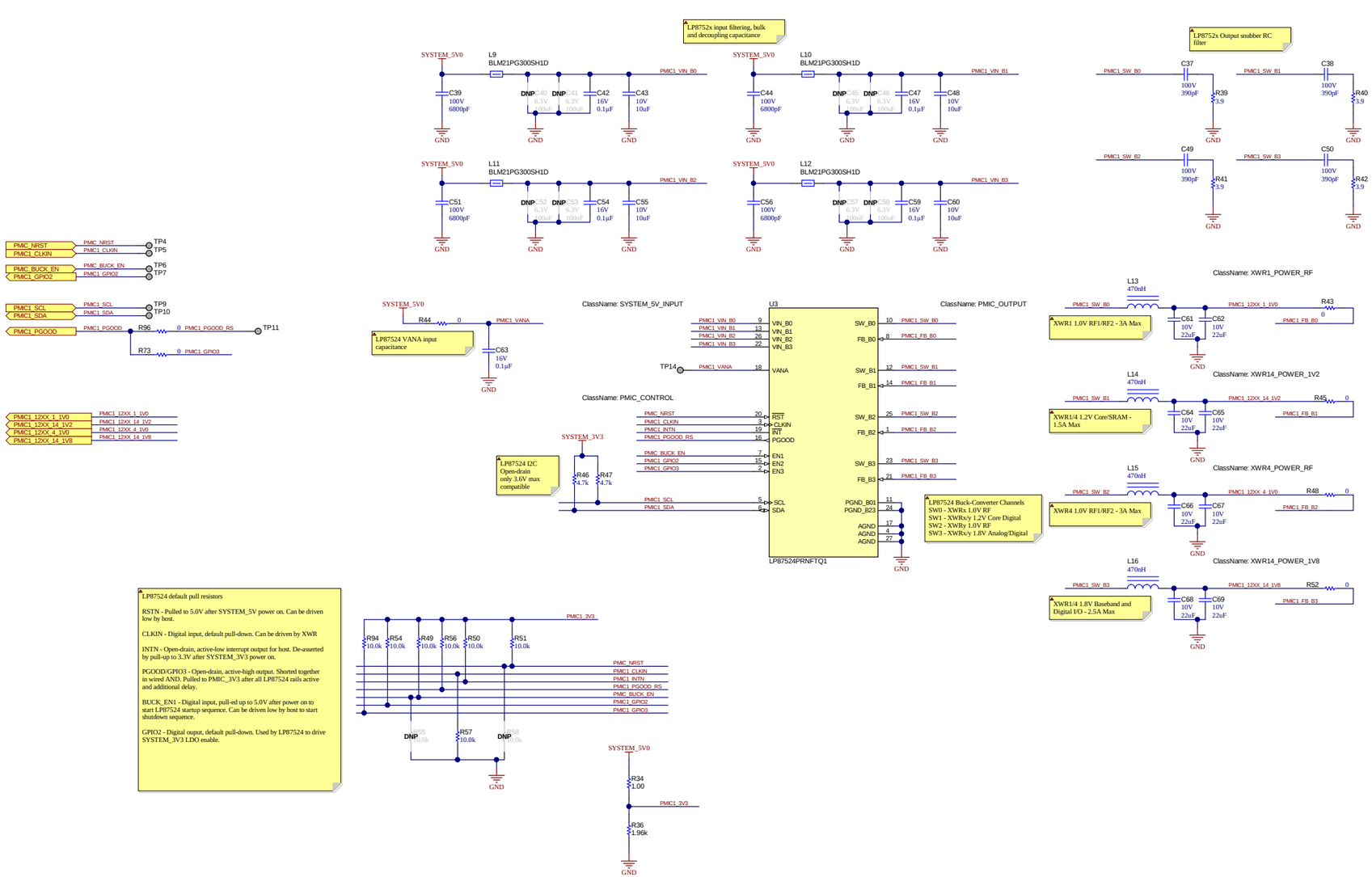
Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: System Power	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 19
Drawn By: a0271760		File: PROC054C_System_Power.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

LP87524P Quad-Channel Synchronous Buck PMIC - Master 12XX_1 and Slave 12XX_4

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 12XX_1_12XX_4_LP87524P	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 19
Drawn By: a0271760		File: PROC054C_12XX_1_12XX_4_LP87524P.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

LP87524P Quad-Channel Synchronous Buck PMIC - Slave 12XX_2 and Slave 12XX_3

References

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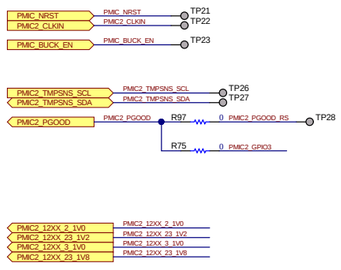

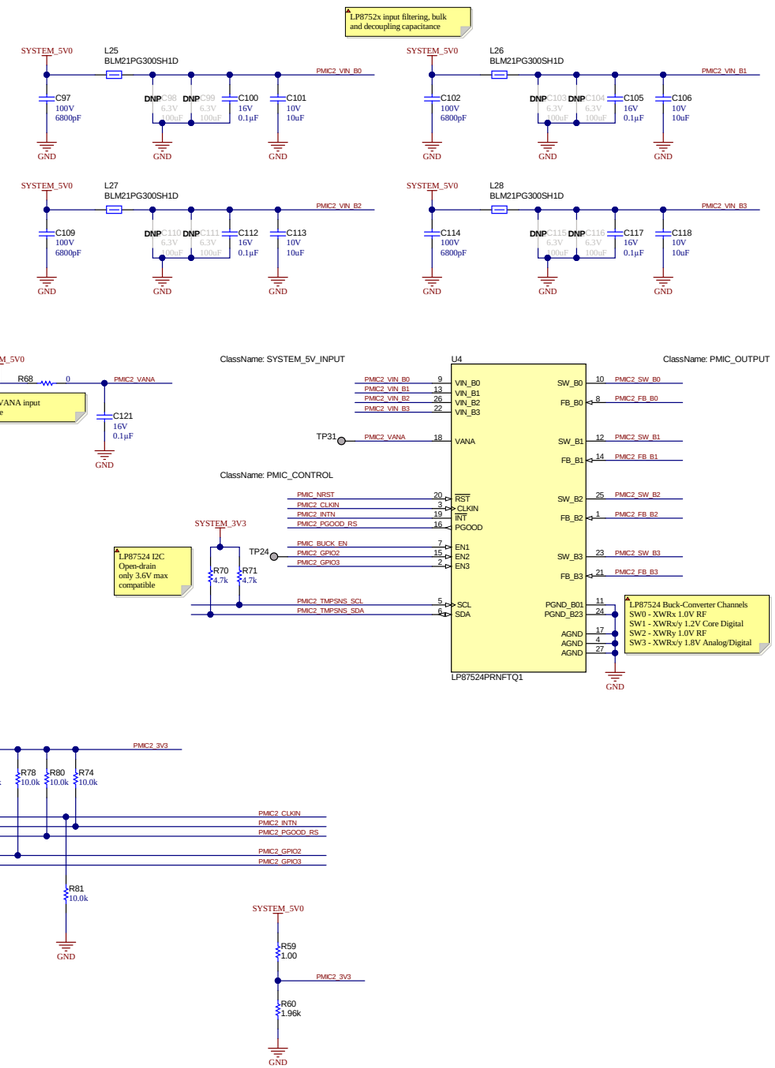

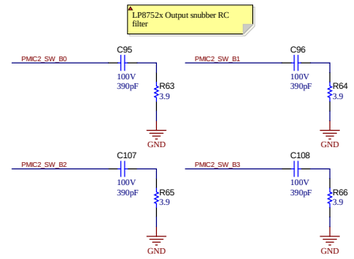

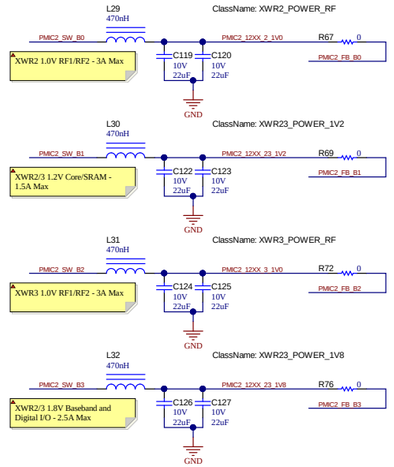

LP87524 default pull resistors

RSTN - Pulled to 5.0V after SYSTEM_5V power on. Can be driven low by host.

CLKIN - Digital input, default pull-down. Can be driven by XWR

INTN - Open-drain, active-low interrupt output for host. De-asserted by pull-up to 3.3V after SYSTEM_3V3 power on.

PGOOD/GPIO3 - Open-drain, active-high output. Shorted together in wired AND. Pulled to SYSTEM_3V3 after all LP87524 rails active and additional delay.

BUCK_EN1 - Digital input, pull-ed up to 5.0V after power on to start LP87524 startup sequence. Can be driven low by host to start shutdown sequence.

GPIO2 - Digital ouput, default pull-down.

GPIO3 - Digitial output, default pull-down. After PMIC power on sequence - used to create delayed NRESET with PGOOD.

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Number: PROC054	Rev: C	Sheet Title: 12XX_2_12XX_3_LP87524P	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 19
Drawn By: a0271760		File: PROC054C_12XX_2_12XX_3_LP87524P.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

XWR1243 Power Filtering and Decoupling - Master 12XX_1 and Slave12XX_4

PMIC1_12XX_14_1V2 → PMIC1_12XX_14_1V2
PMIC1_12XX_14_1V8 → PMIC1_12XX_14_1V8
PMIC1_12XX_1_1V0 → PMIC1_12XX_1_1V0
PMIC1_12XX_4_1V0 → PMIC1_12XX_4_1V0

12XX_1_1V2_FILT → 12XX_1_1V2_FILT
12XX_4_1V2_FILT → 12XX_4_1V2_FILT
12XX_1_1V8_FILT → 12XX_1_1V8_FILT
12XX_4_1V8_FILT → 12XX_4_1V8_FILT
12XX_1_1V0_RF1_FILT → 12XX_1_1V0_RF1_FILT
12XX_1_1V0_RF2_FILT → 12XX_1_1V0_RF2_FILT
12XX_4_1V0_RF1_FILT → 12XX_4_1V0_RF1_FILT
12XX_4_1V0_RF2_FILT → 12XX_4_1V0_RF2_FILT

LP87524P PMIC switcher LC ripple filtering and decoupling for XWR1 and XWR4

L1 NLCV32T-R10M-EFRD 100nH
PMIC1_12XX_14_1V2 → 12XX_1_1V2_FILT
ClassName: 12XX_1_POWER_1V2
1.2V Digital Core/SRAM XWR1/XWR4
C10 10V 10uF
C11 10V 22uF
C12 10V 10uF
C13 16V 1µF
GND

L3 NLCV32T-R10M-EFRD 100nH
PMIC1_12XX_14_1V2 → 12XX_4_1V2_FILT
ClassName: 12XX_4_POWER_1V2
1.2V Digital Core/SRAM XWR1/XWR4
C161 10V 10uF
C21 10V 22uF
C29 10V 10uF
C78 16V 1µF
GND

L2 NLCV32T-R10M-EFRD 100nH
PMIC1_12XX_14_1V8 → 12XX_1_1V8_FILT
ClassName: 12XX_1_POWER_1V8
1.8V Digitial I/O and Analog Baseband XWR1/XWR4
C14 10V 10uF
C15 10V 22uF
C16 10V 10uF
C17 16V 1µF
GND

L6 NLCV32T-R10M-EFRD 100nH
PMIC1_12XX_14_1V8 → 12XX_4_1V8_FILT
ClassName: 12XX_4_POWER_1V8
1.8V Digitial I/O and Analog Baseband XWR1/XWR4
C86 10V 10uF
C150 10V 22uF
C151 10V 10uF
C152 16V 1µF
GND

L4 NLCV32T-R10M-EFRD 100nH
PMIC1_12XX_1_1V0 → 12XX_1_1V0_RF1_FILT
ClassName: 12XX_1_POWER_1V0_RF
1.0V Analog RF XWR1
C25 10V 10uF
C22 10V 22uF
C23 10V 10uF
C26 16V 1µF
GND

L5 NLCV32T-R10M-EFRD 100nH
12XX_1_1V0_RF2_FILT
ClassName: 12XX_1_POWER_1V0_RF
C27 10V 10uF
C24 10V 22uF
C32 10V 10uF
C28 16V 1µF
GND

L7 NLCV32T-R10M-EFRD 100nH
PMIC1_12XX_4_1V0 → 12XX_4_1V0_RF1_FILT
ClassName: 12XX_4_POWER_RF
1.0V Analog RF XWR4
C33 10V 10uF
C30 10V 22uF
C31 10V 10uF
C34 16V 1µF
GND

L8 NLCV32T-R10M-EFRD 100nH
12XX_4_1V0_RF2_FILT
ClassName: 12XX_4_POWER_RF
C35 10V 10uF
C81 10V 22uF
C89 10V 10uF
C36 16V 1µF
GND

ClassName: SYSTEM_1V8
PMIC1_12XX_14_1V8 → R35 0 → SYSTEM_1V8
C18 10V 22uF
C19 10V 10uF
C20 16V 1µF
GND
12XX_1 1.8V supply also generates SYSTEM_1V8
- LMK00804B clock distribution
- LMK00804B sync distribution

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Number: PROC054	Rev: C	Sheet Title: 12XX_1_12XX_4_LC_Filtering	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 19
Drawn By: a0271760		File: PROC054C_12XX_1_12XX_4_LC_Filtering.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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http://www.ti.com

XWR1243 Power Filtering and Decoupling - Master 12XX_2 and Slave 12XX_3

References

4-A + 2.5-A + Two 1.5-A BLP87524J-Q1 Buck Converters With Integrated Switches
LP87524-Q1 Quad Output, Single-Phase Buck Converter Evaluation Module
XWR1xxx Power Management Optimizations- Low Cost LC Filter Solution

PMIC2_12XX_23_1V2 → PMIC2_12XX_23_1V2
PMIC2_12XX_23_1V8 → PMIC2_12XX_23_1V8
PMIC2_12XX_2_1V0 → PMIC2_12XX_2_1V0
PMIC2_12XX_3_1V0 → PMIC2_12XX_3_1V0

12XX_2_1V2_FILT → 12XX_2_1V2_FILT
12XX_3_1V2_FILT → 12XX_3_1V2_FILT
12XX_2_1V8_FILT → 12XX_2_1V8_FILT
12XX_3_1V8_FILT → 12XX_3_1V8_FILT
12XX_2_1V0_RF1_FILT → 12XX_2_1V0_RF1_FILT
12XX_2_1V0_RF2_FILT → 12XX_2_1V0_RF2_FILT
12XX_3_1V0_RF1_FILT → 12XX_3_1V0_RF1_FILT
12XX_3_1V0_RF2_FILT → 12XX_3_1V0_RF2_FILT

LP87524P PMIC switcher LC ripple filtering and decoupling for XWR2

PMIC2_12XX_23_1V2 → L17 NLCV32T-R10M-EFRD 100nH → 12XX_2_1V2_FILT
ClassName: 12XX_2_POWER_1V2
1.2V Digital Core/SRAM XWR2
C70 10V 10uF
C71 10V 22uF
C72 10V 10uF
C73 16V 1µF
GND

LP87524P PMIC switcher LC ripple filtering and decoupling for XWR3

PMIC2_12XX_23_1V2 → L19 NLCV32T-R10M-EFRD 100nH → 12XX_3_1V2_FILT
ClassName: 12XX_3_POWER_1V2
1.2V Digital Core/SRAM XWR3
C153 10V 10uF
C154 10V 22uF
C155 10V 10uF
C156 16V 1µF
GND

PMIC2_12XX_23_1V8 → L18 NLCV32T-R10M-EFRD 100nH → 12XX_2_1V8_FILT
ClassName: 12XX_3_POWER_1V8
1.8V Digitial I/O and Analog Baseband XWR2
C74 10V 10uF
C75 10V 22uF
C76 10V 10uF
C77 16V 1µF
GND

PMIC2_12XX_23_1V8 → L22 NLCV32T-R10M-EFRD 100nH → 12XX_3_1V8_FILT
ClassName: 12XX_3_POWER_1V8
1.8V Digitial I/O and Analog Baseband XWR3
C157 10V 10uF
C158 10V 22uF
C159 10V 10uF
C160 16V 1µF
GND

PMIC2_12XX_2_1V0 → L20 NLCV32T-R10M-EFRD 100nH → 12XX_2_1V0_RF1_FILT
ClassName: 12XX_2_POWER_1V0_RF
1.0V Analog RF XWR2
C82 10V 10uF
C79 10V 22uF
C80 10V 10uF
C83 16V 1µF
GND

L21 NLCV32T-R10M-EFRD 100nH → 12XX_2_1V0_RF2_FILT
ClassName: 12XX_2_POWER_1V0_RF
C84 10V 10uF
C166 10V 22uF
C201 10V 10uF
C85 16V 1µF
GND

PMIC2_12XX_3_1V0 → L23 NLCV32T-R10M-EFRD 100nH → 12XX_3_1V0_RF1_FILT
ClassName: 12XX_3_POWER_RF
1.0V Analog RF XWR3
C90 10V 10uF
C87 10V 22uF
C88 10V 10uF
C91 16V 1µF
GND

L24 NLCV32T-R10M-EFRD 100nH → 12XX_3_1V0_RF2_FILT
ClassName: 12XX_3_POWER_RF
C92 10V 10uF
C204 10V 22uF
C207 10V 10uF
C93 16V 1µF
GND

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 12XX_2_12XX_3 LC_Filtering	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 7 of 19
Drawn By: a0271760		File: PROC054C_12XX_2_12XX_3 LC_Filtering.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

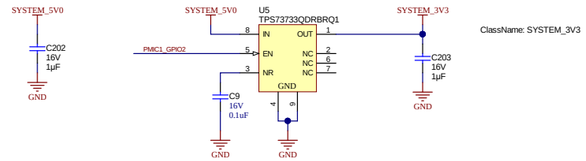
System 3.3V Supply

References

TLV70028EVM-463 Evaluation Module
TPS22965 Evaluation Module

REPLACE WITH higher current TPS73733-Q1

TPS73733-Q1 5.0V to 3.3V LDO - System 3.3V Power



ClassName: SYSTEM_3V3

TLV702_EN — PMIC1_GPIO2

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: System_3V3_Supply	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 8 of 19
Drawn By: a0271760		File: PROC054C_System_3V3_Supply.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

Host to RF Board Connectors

ClassName: 12XX_1_GENERAL

12XX_1_GPIO_0
12XX_1_GPIO_1
12XX_1_GPIO_2

12XX_1_SPI_MISO1
12XX_1_SPI_HOST_INTR1
12XX_1_SPI_CS1
12XX_1_SPI_MOSI1
12XX_1_SPI_CLK1

12XX_1_UART_RX
12XX_1_UART_TX
12XX_1_MSS_LOGGER
12XX_1_BSS_LOGGER

ClassName: 12XX_1_SOP_RESET

12XX_1_SOP2_PMICCLKOUT
12XX_1_SOP1_SYNCOUT
12XX_1_SOP0_TDO
12XX_1_NRST
12XX_1_WARM_RST

ClassName: 12XX_1_JTAG

12XX_1_TCK
12XX_1_TMS
12XX_1_TDO
12XX_1_TDI

ClassName: 12XX_2_GENERAL

12XX_2_GPIO_0
12XX_2_GPIO_1
12XX_2_GPIO_2

12XX_2_SPI_MISO1
12XX_2_SPI_HOST_INTR1
12XX_2_SPI_CS1
12XX_2_SPI_MOSI1
12XX_2_SPI_CLK1

12XX_2_UART_RX
12XX_2_UART_TX
12XX_2_MSS_LOGGER
12XX_2_BSS_LOGGER

ClassName: 12XX2_SOP_RESET

12XX_2_SOP2_PMICCLKOUT
12XX_2_SOP1_SYNCOUT
12XX_2_SOP0_TDO
12XX_2_NRST
12XX_2_WARM_RST

ClassName: 12XX_2_JTAG

12XX_2_TCK
12XX_2_TMS
12XX_2_TDO
12XX_2_TDI

ClassName: 12XX_SYNC

EXT_DIG_SYNC

ClassName: 12XX_CLOCK

EXT_40MHZ_CLK_1V8

ClassName: PMIC_CONTROL

PMIC_NRST
PMIC1_SCL
PMIC1_SDA
PMIC2_TMPSNS_SDA
PMIC2_TMPSNS_SCL

ClassName: 12XX_SAFETY

NERROR_OUT
TMPSNS_ALERT

ClassName: 12XX_3_GENERAL

12XX_3_GPIO_2
12XX_3_GPIO_1
12XX_3_GPIO_0

12XX_3_SPI_CLK1
12XX_3_SPI_MOSI1
12XX_3_SPI_CS1
12XX_3_SPI_HOST_INTR1
12XX_3_SPI_MISO1

12XX_3_UART_TX
12XX_3_UART_RX
12XX_3_BSS_LOGGER
12XX_3_MSS_LOGGER

ClassName: 12XX_3_SOP_RESET

12XX_3_SOP2_PMICCLKOUT
12XX_3_SOP1_SYNCOUT
12XX_3_SOP0_TDO
12XX_3_NRST
12XX_3_WARM_RST

ClassName: 12XX_3_JTAG

12XX_3_TDI
12XX_3_TDO
12XX_3_TMS
12XX_3_TCK

ClassName: 12XX_4_GENERAL

12XX_4_GPIO_2
12XX_4_GPIO_1
12XX_4_GPIO_0

12XX_4_SPI_CLK1
12XX_4_SPI_MOSI1
12XX_4_SPI_CS1
12XX_4_SPI_HOST_INTR1
12XX_4_SPI_MISO1

12XX_4_UART_TX
12XX_4_UART_RX
12XX_4_BSS_LOGGER
12XX_4_MSS_LOGGER

ClassName: 12XX_4_SOP_RESET

12XX_4_SOP2_PMICCLKOUT
12XX_4_SOP1_SYNCOUT
12XX_4_SOP0_TDO
12XX_4_NRST
12XX_4_WARM_RST

ClassName: 12XX_4_JTAG

12XX_4_TDI
12XX_4_TDO
12XX_4_TMS
12XX_4_TCK

Host Board Connector 1

ClassName: 12XX_1_CSI_LVDS

12XX_1_LVDS_VALID_P
12XX_1_LVDS_VALID_N
12XX_1_LVDS_FRCLK_P
12XX_1_LVDS_FRCLK_N
12XX_1_CSI2_TX3_P
12XX_1_CSI2_TX3_N
12XX_1_CSI2_TX2_P
12XX_1_CSI2_TX2_N
12XX_1_CSI2_CLK_P
12XX_1_CSI2_CLK_N

ClassName: 12XX_2_CSI_LVDS

12XX_2_LVDS_VALID_P
12XX_2_LVDS_VALID_N
12XX_2_LVDS_FRCLK_P
12XX_2_LVDS_FRCLK_N
12XX_2_CSI2_TX3_P
12XX_2_CSI2_TX3_N
12XX_2_CSI2_TX2_P
12XX_2_CSI2_TX2_N
12XX_2_CSI2_CLK_P
12XX_2_CSI2_CLK_N

TP32 CONN_MONITOR_1
12XX_1_MCU_CLKOUT
12XX_1_MCU_CLKOUT_CONN

TP12 XWR_CONN_TP1
12XX_1_CSI2_TX1_P
12XX_1_CSI2_TX1_N
12XX_1_CSI2_TX0_P
12XX_1_CSI2_TX0_N

TP15 XWR_CONN_TP2
12XX_2_CSI2_TX1_P
12XX_2_CSI2_TX1_N
12XX_2_CSI2_TX0_P
12XX_2_CSI2_TX0_N

J4 — FX23-120P-0.5SV15

1	12XX_1_GPIO_0	61	12XX_1_GPIO_0
2	12XX_1_GPIO_1	62	12XX_1_GPIO_1
3	12XX_1_GPIO_2	63	12XX_1_GPIO_2
4	12XX_1_LVDS_VALID_P	64	EXT_DIG_SYNC
5	12XX_1_LVDS_VALID_N	65	
6		66	12XX_1_SPI_MISO1
7	12XX_1_LVDS_FRCLK_P	67	12XX_1_SPI_HOST_INTR1
8	12XX_1_LVDS_FRCLK_N	68	12XX_1_SPI_CS1
9		69	12XX_1_SPI_MOSI1
10	12XX_1_CSI2_TX3_P	70	12XX_1_SPI_CLK1
11	12XX_1_CSI2_TX3_N	71	
12		72	PMIC1_SCL
13	12XX_1_CSI2_TX2_P	73	PMIC1_SDA
14	12XX_1_CSI2_TX2_N	74	EXT_40MHZ_CLK_1V8
15		75	NERROR_OUT
16	12XX_1_CSI2_CLK_P	76	
17	12XX_1_CSI2_CLK_N	77	12XX_1_UART_RX
18		78	12XX_1_UART_TX
19	12XX_1_CSI2_TX1_P	79	12XX_1_MSS_LOGGER
20	12XX_1_CSI2_TX1_N	80	12XX_1_BSS_LOGGER
21		81	
22	12XX_1_CSI2_TX0_P	82	12XX_1_SOP2_PMICCLKOUT
23	12XX_1_CSI2_TX0_N	83	12XX_1_SOP1_SYNCOUT
24		84	12XX_1_SOP0_TDO
25	12XX_2_LVDS_VALID_P	85	12XX_1_NRST
26	12XX_2_LVDS_VALID_N	86	12XX_1_WARM_RST
27		87	
28	12XX_2_LVDS_FRCLK_P	88	12XX_1_TCK
29	12XX_2_LVDS_FRCLK_N	89	12XX_1_TMS
30		90	12XX_1_TDO
31	12XX_2_CSI2_TX3_P	91	12XX_1_TDI
32	12XX_2_CSI2_TX3_N	92	
33		93	12XX_2_SPI_MISO1
34	12XX_2_CSI2_TX2_P	94	12XX_2_SPI_HOST_INTR1
35	12XX_2_CSI2_TX2_N	95	
36		96	12XX_2_SPI_CS1
37	12XX_2_CSI2_CLK_P	97	12XX_2_SPI_MOSI1
38	12XX_2_CSI2_CLK_N	98	12XX_2_SPI_CLK1
39		99	
40	12XX_2_CSI2_TX1_P	100	12XX_2_UART_RX
41	12XX_2_CSI2_TX1_N	101	12XX_2_UART_TX
42		102	12XX_2_MSS_LOGGER
43	12XX_2_CSI2_TX0_P	103	12XX_2_BSS_LOGGER
44	12XX_2_CSI2_TX0_N	104	
45		105	12XX_2_GPIO_0
46		106	12XX_2_GPIO_1
47		107	12XX_2_GPIO_2
48		108	
49		109	12XX_2_NRST
50		110	12XX_2_WARM_RST
51		111	
52		112	12XX_2_SOP2_PMICCLKOUT
53		113	12XX_2_SOP1_SYNCOUT
54		114	12XX_2_SOP0_TDO
55		115	
56		116	12XX_2_TCK
57		117	12XX_2_TMS
58		118	12XX_2_TDO
59		119	12XX_2_TDI
60		120	CONN_MONITOR_1
P1		P3	SYSTEM_5V0
P2		P4	
MH1		MH2	

C190 10V 47µF
C191 10V 47µF
ClassName: SYSTEM_5V

Bench 5.0V Supply

J6 — 0039300060 Molex

GND_SENSE — SYSTEM_5V0_SENSE
SYSTEM_5V0
C194 10V 47µF

5.0V Supply Sense

SYSTEM_5V0
R19 0 SYSTEM_5V0_SENSE DNP
R20 0 GND_SENSE DNP

GROUND TEST POINTS

TP16 TP17 TP18 TP19 TP20 TP25 TP29 TP30 — 5001

Ground test points should be distributed across board near major IC

SOP Mode / Functional Mode Signals

12XX_1_TDO	12XX_1_TDO	R147	10.0k	12XX_1_SOP0_TDO
12XX_1_DIG_SYNCOUT	12XX_1_DIG_SYNCOUT	R148	10.0k	12XX_1_SOP1_SYNCOUT
12XX_1_PMIC_CLKOUT	12XX_1_PMIC_CLKOUT	R149	10.0k	12XX_1_SOP2_PMICCLKOUT
12XX_2_TDO	12XX_2_TDO	R151	10.0k	12XX_2_SOP0_TDO
12XX_2_DIG_SYNCOUT	12XX_2_DIG_SYNCOUT	R152	10.0k	12XX_2_SOP1_SYNCOUT
12XX_2_PMIC_CLKOUT	12XX_2_PMIC_CLKOUT	R153	10.0k	12XX_2_SOP2_PMICCLKOUT
12XX_3_TDO	12XX_3_TDO	R155	10.0k	12XX_3_SOP0_TDO
12XX_3_DIG_SYNCOUT	12XX_3_DIG_SYNCOUT	R157	10.0k	12XX_3_SOP1_SYNCOUT
12XX_3_PMIC_CLKOUT	12XX_3_PMIC_CLKOUT	R159	10.0k	12XX_3_SOP2_PMICCLKOUT
12XX_4_TDO	12XX_4_TDO	R161	10.0k	12XX_4_SOP0_TDO
12XX_4_DIG_SYNCOUT	12XX_4_DIG_SYNCOUT	R162	10.0k	12XX_4_SOP1_SYNCOUT
12XX_4_PMIC_CLKOUT	12XX_4_PMIC_CLKOUT	R163	10.0k	12XX_4_SOP2_PMICCLKOUT

Note: Both functional mode and SOP modes of these pins are provided at the RF Host Interface connector.

Host device should not simultaneously drive the SOP mode pin and functional pin.

Host Board Connector 2

ClassName: 12XX_4_CSI_LVDS

12XX_4_CSI2_TX0_N
12XX_4_CSI2_TX0_P
12XX_4_CSI2_TX1_N
12XX_4_CSI2_TX1_P

ClassName: 12XX_4_CSI_LVDS

12XX_4_CSI2_CLK_N
12XX_4_CSI2_CLK_P
12XX_4_CSI2_TX2_N
12XX_4_CSI2_TX2_P
12XX_4_CSI2_TX3_N
12XX_4_CSI2_TX3_P
12XX_4_LVDS_FRCLK_N
12XX_4_LVDS_FRCLK_P
12XX_4_LVDS_VALID_N
12XX_4_LVDS_VALID_P

ClassName: 12XX_3_CSI_LVDS

12XX_3_CSI2_TX0_N
12XX_3_CSI2_TX0_P
12XX_3_CSI2_TX1_N
12XX_3_CSI2_TX1_P

ClassName: 12XX_3_CSI_LVDS

12XX_3_CSI2_CLK_N
12XX_3_CSI2_CLK_P
12XX_3_CSI2_TX2_N
12XX_3_CSI2_TX2_P
12XX_3_CSI2_TX3_N
12XX_3_CSI2_TX3_P
12XX_3_LVDS_FRCLK_N
12XX_3_LVDS_FRCLK_P
12XX_3_LVDS_VALID_N
12XX_3_LVDS_VALID_P

TP33 CONN_MONITOR_2
12XX_4_TDI
12XX_4_TDO
12XX_4_TMS
12XX_4_TCK

XWR_CONN_TP3 TP8
12XX_4_WARM_RST
12XX_4_NRST
12XX_4_GPIO_2
12XX_4_GPIO_1
12XX_4_GPIO_0

XWR_CONN_TP4 TP13
12XX_3_TDI
12XX_3_TMS
12XX_3_TCK
12XX_3_WARM_RST
12XX_3_NRST

J5 — FX23-120P-0.5SV15

1	12XX_4_TDI	61	
2	12XX_4_TDO	62	12XX_4_CSI2_TX0_N
3	12XX_4_TMS	63	12XX_4_CSI2_TX0_P
4	12XX_4_TCK	64	
5		65	12XX_4_CSI2_TX1_N
6		66	12XX_4_CSI2_TX1_P
7	12XX_4_SOP0_TDO	67	
8	12XX_4_SOP1_SYNCOUT	68	
9	12XX_4_SOP2_PMICCLKOUT	69	
10		70	
11	12XX_4_WARM_RST	71	12XX_4_CSI2_CLK_N
12	12XX_4_NRST	72	12XX_4_CSI2_CLK_P
13		73	
14	12XX_4_GPIO_2	74	
15	12XX_4_GPIO_1	75	12XX_4_CSI2_TX2_N
16	12XX_4_GPIO_0	76	12XX_4_CSI2_TX2_P
17		77	
18	12XX_4_BSS_LOGGER	78	
19	12XX_4_MSS_LOGGER	79	12XX_4_CSI2_TX3_N
20	12XX_4_UART_TX	80	12XX_4_CSI2_TX3_P
21	12XX_4_UART_RX	81	
22		82	
23	12XX_4_SPI_CLK1	83	12XX_4_LVDS_FRCLK_N
24	12XX_4_SPI_MOSI1	84	12XX_4_LVDS_FRCLK_P
25	12XX_4_SPI_CS1	85	
26		86	
27	12XX_4_SPI_HOST_INTR1	87	12XX_4_LVDS_VALID_N
28	12XX_4_SPI_MISO1	88	12XX_4_LVDS_VALID_P
29		89	
30	12XX_3_TDI	90	
31	12XX_3_TDO	91	
32	12XX_3_TMS	92	12XX_3_CSI2_TX0_N
33	12XX_3_TCK	93	12XX_3_CSI2_TX0_P
34		94	
35	12XX_3_WARM_RST	95	12XX_3_CSI2_TX1_N
36	12XX_3_NRST	96	12XX_3_CSI2_TX1_P
37	12XX_3_SOP0_TDO	97	
38	12XX_3_SOP1_SYNCOUT	98	
39	12XX_3_SOP2_PMICCLKOUT	99	
40		100	
41	12XX_3_BSS_LOGGER	101	12XX_3_CSI2_CLK_N
42	12XX_3_MSS_LOGGER	102	12XX_3_CSI2_CLK_P
43	12XX_3_UART_TX	103	
44	12XX_3_UART_RX	104	12XX_3_CSI2_TX2_N
45		105	12XX_3_CSI2_TX2_P
46		106	
47		107	
48		108	12XX_3_CSI2_TX3_N
49		109	12XX_3_CSI2_TX3_P
50		110	
51	12XX_3_SPI_CLK1	111	
52	12XX_3_SPI_MOSI1	112	12XX_3_LVDS_FRCLK_N
53	12XX_3_SPI_CS1	113	12XX_3_LVDS_FRCLK_P
54	12XX_3_SPI_HOST_INTR1	114	
55	12XX_3_SPI_MISO1	115	
56		116	12XX_3_LVDS_VALID_N
57	TMPSNS_ALERT	117	12XX_3_LVDS_VALID_P
58	12XX_3_GPIO_2	118	
59	12XX_3_GPIO_1	119	SYSTEM_PGOOD
60	12XX_3_GPIO_0	120	CONN_MONITOR_2
P1		P3	
P2		P4	
MH1		MH2	

SYSTEM_5V0
C192 10V 47µF
C193 10V 47µF

PMIC_BUCKEN R145 0 PMIC_BUCKEN_CONN
PMIC_NRST R146 0 PMIC_NRST_CONN

Safety Error Signals

SYSTEM_3V3
R150 10.0k

NERROR_OUT — NERROR_OUT

Note: ERROR_OUT signals are open-drain and active-low. Any one XWR device can pull the NERROR_OUT signal low in this configuration.

R154	0	12XX_1_NERROR_OUT	12XX_1_NERROR_OUT
R156	0	12XX_2_NERROR_OUT	12XX_2_NERROR_OUT
R158	0	12XX_3_NERROR_OUT	12XX_3_NERROR_OUT
R160	0	12XX_4_NERROR_OUT	12XX_4_NERROR_OUT

12XX and PMIC I2C Signals

12XX_1_SCL	12XX_1_SCL	R98	DNP	0	PMIC1_SCL
12XX_1_SDA	12XX_1_SDA	R99	DNP	0	PMIC1_SDA
12XX_2_SCL	12XX_2_SCL	R100	DNP	0	PMIC1_SCL
12XX_2_SDA	12XX_2_SDA	R101	DNP	0	PMIC1_SDA
12XX_3_SCL	12XX_3_SCL	R102	DNP	0	PMIC1_SCL
12XX_3_SDA	12XX_3_SDA	R103	DNP	0	PMIC1_SDA
12XX_4_SCL	12XX_4_SCL	R104	DNP	0	PMIC1_SCL
12XX_4_SDA	12XX_4_SDA	R105	DNP	0	PMIC1_SDA

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: HOST_CONNECTOR	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 9 of 19
Drawn By: a0271760		File: PROC054C_HOST_CONNECTOR.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

XWR1243 Radar SoC - Interfaces

References

???????

ClassName: XWR_20GHZ_LO

FMCW_SYNCIN1
FMCW_CLKOUT
FMCW_SYNCOUT

DIG_SYNCIN
DIG_SYNCOUT
TP1_1

OSC_CLKOUT
XTAL_CLKP
XTAL_CLKM

PMIC_CLKOUT
MCU_CLKOUT
TP2_1

NRST
WARM_RST
NERROR_IN
NERROR_OUT

UART_RX
UART_TX

TCK
TMS
TDO
TDI
TP3_1

SPI_HOST_INTR1
SPI_CLK1
SPI_CS1
SPI_MISO1
SPI_MOSI1

GPIO_0
GPIO_1
GPIO_2

SCL
SDA
BSS_LOGGER
MSS_LOGGER

CSI2_CLK_P
CSI2_CLK_N
CSI2_TX0_P
CSI2_TX0_N
CSI2_TX1_P
CSI2_TX1_N
CSI2_TX2_P
CSI2_TX2_N
CSI2_TX3_P
CSI2_TX3_N
LVDS_FRCLK_P
LVDS_FRCLK_N
LVDS_VALID_P
LVDS_VALID_N

AR_1V0_RF2

ClassName: 12XX_SYNC

DIG_SYNCIN
DIG_SYNCOUT
R1_1 33.2
DIG_SYNCOUT_RS

ClassName: 12XX_CLOCK

OSC_CLKOUT
XTAL_CLKP
XTAL_CLKM
R2_1 33.2
OSC_CLKOUT_RS

PMIC_CLKOUT
MCU_CLKOUT
R4_1 33.2
R5_1 33.2
PMIC_CLKOUT_RS
MCU_CLKOUT_RS

ClassName: 12XX_GENERAL

NRST
WARM_RST
NERROR_IN
NERROR_OUT
R9_1 0
NERROR_OUT_RS

NOTE: UART_RX and UART_TX directions are with respect to XWR12XX

UART_RX
UART_TX
R11_1 33.2
UART_TX_RS

ClassName: 12XX_GENERAL

SCL
SDA
BSS_LOGGER
MSS_LOGGER
R13_1 33.2
R14_1 33.2
R15_1 33.2
SDA_RS
BSS_LOGGER_RS
MSS_LOGGER_RS

ClassName: 12XX_ANTENNA

NOTE: 12XX_X
FMCW_SYNCIN2 unused.
Shorted to GND per datasheet

NOTE: 12XX_X
FMCW_CLKOUT/SYNCOUT unused terminated to 50-ohms per datasheet requirements.

GND

NOTE: 12XX antenna routed as GCPW transmission lines to etched antenna.

12XX_RX1
12XX_RX2
12XX_RX3
12XX_RX4
12XX_TX1
12XX_TX2
12XX_TX3

FMCW_SYNCIN1
FMCW_CLKOUT
FMCW_SYNCOUT

12XX Interfaces

U1_1A

G13	RESERVED	
M2	RX1	12XX_RX1
K2	RX2	12XX_RX2
H2	RX3	12XX_RX3
F2	RX4	12XX_RX4
B4	TX1	12XX_TX1
B6	TX2	12XX_TX2
B8	TX3	12XX_TX3
B1	FM_CW_SYNCIN1	FMCW_SYNCIN1
D15	FM_CW_SYNCIN2	
B15	FM_CW_CLKOUT	FMCW_CLKOUT
D1	FM_CW_SYNCOUT	FMCW_SYNCOUT
N10	SYNC_IN	
P11	SYNC_OUT	DIG_SYNCOUT_RS
A14	OSC_CLKOUT	OSC_CLKOUT_RS
E14	CLKP	XTAL_CLKP
F14	CLKM	XTAL_CLKM
P13	PMIC_CLK_OUT	PMIC_CLKOUT_RS
N9	MCU_CLK_OUT	MCU_CLKOUT_RS
C14	VSENSE	GPADC6
C13	ANAMUX	GPADC5
P1	ANALOGTEST1	GPADC1
P2	ANALOGTEST2	GPADC2
P3	ANALOGTEST3	GPADC3
R2	ANALOGTEST4	GPADC4
P12	RESET	NRST
N12	WARM_RESET	WARM_RST
F7	NERROR_IN	NERROR_IN
N8	NERROR_OUT	NERROR_OUT_RS
N5	RS232_RX	UART_RX
N6	RS232_TX	UART_TX_RS
P4	RESERVED	SCL
R3	RESERVED	SDA
R4	RESERVED	BSS_LOGGER_RS
R5	RESERVED	MSS_LOGGER_RS

XA1243FPBIGABLQ1

ClassName: 12XX_POWER_ANA

A13	VOUT_14SYNTH	AR_1V4_SYNTH
A10	VOUT_14APLL1	AR_1V4_APLL
B10	VBGAP	AR_VBGAP
A2	VOUT_PA	AR_VOUT_PA
B2	VOUT_PA	

R188_1 0 AR_1V0_RF2

G15	CSI2_TX0_P	CSI2_TXP[0]
G14	CSI2_TX0_N	CSI2_TXM[0]
H15	CSI2_TX1_P	CSI2_TXP[1]
H14	CSI2_TX1_N	CSI2_TXM[1]
J15	CSI2_CLK_P	CSI2_CLKP
J14	CSI2_CLK_N	CSI2_CLKM
K15	CSI2_TX2_P	CSI2_TXP[2]
K14	CSI2_TX2_N	CSI2_TXM[2]
L15	CSI2_TX3_P	CSI2_TXP[3]
L14	CSI2_TX3_N	CSI2_TXM[3]
M15	LVDS_FRCLK_P	HS_DEBUG1_P
M14	LVDS_FRCLK_N	HS_DEBUG1_M
N15	LVDS_VALID_P	HS_DEBUG2_P
N14	LVDS_VALID_N	HS_DEBUG2_M

P8	QSPI_CS_RS	R6_1 0	QSPI_CS
R10	QSPI_CLK_RS	R7_1 0	QSPI_CLK
R11	QSPI_D0		
P9	QSPI_D1		
R12	QSPI_D2		
P10	QSPI_D3		

M13	TCK		
L13	TMS		
J13	TDO_RS	R8_1 33.2	TDO
H13	TDI		

P6	SPI_HOST_INTR1_RS	R10_1 33.2	SPI_HOST_INTR1
R9	SPI_CLK1		
R7	SPI_CS1		
P5	SPI_MISO1_RS	R12_1 33.2	SPI_MISO1
R8	SPI_MOSI1		

N4	GPIO[0]	GPIO_0
N7	GPIO[1]	GPIO_1
M13	GPIO[2]	GPIO_2

R16_1 10.0k
R17_1 10.0k
R18_1 10.0k

GND

ClassName: 12XX_QSPI

QSPI_FLASH_3V3
R3_1 47.5k

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: 12XX_JTAG

ClassName: 12XX_GENERAL

ClassName: 12XX_GENERAL

XWR LDO and Bandgap Output Capacitors

AR_1V4_SYNTH
C1_1 16V 1uF
AR_VBGAP
C2_1 16V 0.22µF

Place output capacitors as close to power pins as possible - minimum mounting inductance.

GND

AR_1V4_APLL
C3_1 16V 1uF
AR_VOUT_PA
C4_1 16V 0.22µF
C5_1 10V 10uF

GND

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AR_1V0_RF2 optionally shorted to AR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AR_VOUT_PA to AR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3
R27_1 10.0k
R28_1 10.0k

QSPI_D0	R30_1 0	QSPI_D0_RS	
QSPI_D1	R31_1 0	QSPI_D1_RS	
QSPI_D2	R32_1 0	QSPI_D2_RS	
QSPI_D3	R33_1 0	QSPI_D3_RS	

U2_1

8	VCC	QSPI_FLASH_3V3
1	CS	QSPI_CS
6	SCLK	QSPI_CLK
5	SI/SIO0	
2	SO/SIO1	
3	WP/SIO2	
7	HOLD/SIO3	
EP	GND	9 4

MX25V1635FZNQ

NOR Flash 16Mb (2M x 8) 80MHz CLK

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

GND

ClassName: SYSTEM_3V3

SYSTEM_3V3
R29_1 0
QSPI_FLASH_3V3

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_1 10V 10uF
C7_1 16V 1uF
C8_1 50V 0.1uF

GND

Debug Test Header (For Development Purposes)

GPADC1	R21_1	0	GPADC1_CONN
GPADC2	R22_1	0	GPADC2_CONN
GPADC3	R23_1	0	GPADC3_CONN
GPADC4	R24_1	0	GPADC4_CONN
GPADC5	R25_1	0	GPADC5_CONN
GPADC6	R26_1	0	GPADC6_CONN

J1_1
DNP
TSM-106-01-L-DV

GND

ClassName: 12XX_DEBUG

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 6/27/2019
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 12XX_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 19
Drawn By: a0271760		File: PROC054C_12XX_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

TEXAS INSTRUMENTS
http://www.ti.com

XWR1243 Radar SoC - Interfaces

References

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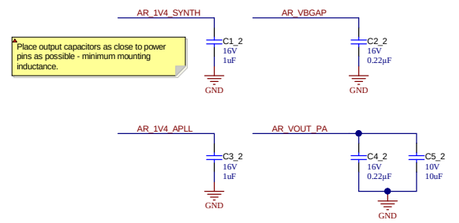
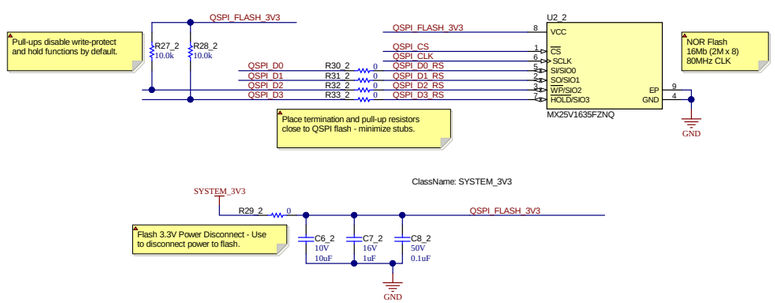
XWR LDO and Bandgap Output Capacitors

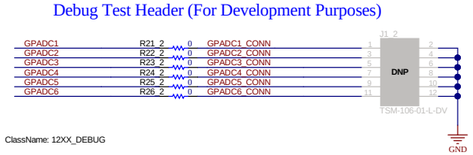


12XX Interfaces

NOR QSPI FLASH (For Development Purposes)



Debug Test Header (For Development Purposes)



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 6/27/2019
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 12XX_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 19
Drawn By: a0271760		File: PROC054C_12XX_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

XWR1243 Radar SoC - Interfaces

References

???????

ClassName: XWR_20GHZ_LO

FMCW_SYNCIN1 — FMCW_SYNCIN1
FMCW_CLKOUT — FMCW_CLKOUT
FMCW_SYNCOUT — FMCW_SYNCOUT

DIG_SYNCIN — DIG_SYNCIN
DIG_SYNCOUT — DIG_SYNCOUT — TP1_3

OSC_CLKOUT — OSC_CLKOUT
XTAL_CLKP — XTAL_CLKP
XTAL_CLKM — XTAL_CLKM

PMIC_CLKOUT — PMIC_CLKOUT
MCU_CLKOUT — MCU_CLKOUT — TP2_3

NRST — NRST
WARM_RST — WARM_RST
NERROR_IN — NERROR_IN
NERROR_OUT — NERROR_OUT

UART_RX — UART_RX
UART_TX — UART_TX

TCK — TCK
TMS — TMS
TDO — TDO
TDI — TDI — TP3_3

SPI_HOST_INTR1 — SPI_HOST_INTR1
SPI_CLK1 — SPI_CLK1
SPI_CS1 — SPI_CS1
SPI_MISO1 — SPI_MISO1
SPI_MOSI1 — SPI_MOSI1

GPIO_0 — GPIO_0
GPIO_1 — GPIO_1
GPIO_2 — GPIO_2

SCL — SCL
SDA — SDA
BSS_LOGGER — BSS_LOGGER
MSS_LOGGER — MSS_LOGGER

CSI2_CLK_P — CSI2_CLK_P
CSI2_CLK_N — CSI2_CLK_N
CSI2_TX0_P — CSI2_TX0_P
CSI2_TX0_N — CSI2_TX0_N
CSI2_TX1_P — CSI2_TX1_P
CSI2_TX1_N — CSI2_TX1_N
CSI2_TX2_P — CSI2_TX2_P
CSI2_TX2_N — CSI2_TX2_N
CSI2_TX3_P — CSI2_TX3_P
CSI2_TX3_N — CSI2_TX3_N
LVDS_FRCLK_P — LVDS_FRCLK_P
LVDS_FRCLK_N — LVDS_FRCLK_N
LVDS_VALID_P — LVDS_VALID_P
LVDS_VALID_N — LVDS_VALID_N

AR_1V0_RF2 — AR_1V0_RF2

12XX Interfaces

NOTE: 12XX antenna routed as GCPW transmission lines to etched antenna.

ClassName: 12XX_ANTENNA

NOTE: 12XX_X FMCW_SYNCIN2 unused. Shorted to GND per datasheet

NOTE: 12XX_X FMCW_CLKOUT/SYNCOUT unused terminated to 50-ohms per datasheet requirements.

GND

12XX_RX1 — M2 — RX1
12XX_RX2 — K2 — RX2
12XX_RX3 — H2 — RX3
12XX_RX4 — F2 — RX4
12XX_TX1 — B4 — TX1
12XX_TX2 — B6 — TX2
12XX_TX3 — B8 — TX3

FMCW_SYNCIN1 — B1 — FM_CW_SYNCIN1
D15 — FM_CW_SYNCIN2
FMCW_CLKOUT — B15 — FM_CW_CLKOUT
FMCW_SYNCOUT — D1 — FM_CW_SYNCOUT

ClassName: 12XX_SYNC

DIG_SYNCIN — N10 — SYNC_IN
DIG_SYNCOUT — R1_3 — 33.2 — DIG_SYNCOUT_RS — P11 — SYNC_OUT

ClassName: 12XX_CLOCK

OSC_CLKOUT — R2_3 — 33.2 — OSC_CLKOUT_RS — A14 — OSC_CLKOUT
XTAL_CLKP — E14 — CLKP
XTAL_CLKM — F14 — CLKM

PMIC_CLKOUT — R4_3 — 33.2 — PMIC_CLKOUT_RS — P13 — PMIC_CLK_OUT
MCU_CLKOUT — R5_3 — 33.2 — MCU_CLKOUT_RS — N9 — MCU_CLK_OUT

ClassName: 12XX_GENERAL

GPADC6 — C14 — VSENSE
GPADC5 — C13 — AVAMUX
GPADC1 — P1 — ANALOGTEST1
GPADC2 — P2 — ANALOGTEST2
GPADC3 — P3 — ANALOGTEST3
GPADC4 — R2 — ANALOGTEST4

NRST — P12 — RESET
WARM_RST — N12 — WARM_RESET
NERROR_IN — F7 — NERROR_IN
NERROR_OUT — R9_3 — 0 — NERROR_OUT_RS — N8 — NERROR_OUT

NOTE: UART_RX and UART_TX directions are with respect to XWR12XX

UART_RX — N5 — RS232_RX
UART_TX — R11_3 — 33.2 — UART_TX_RS — N6 — RS232_TX

ClassName: 12XX_GENERAL

SCL — P4 — RESERVED
SDA — R13_3 — 33.2 — SDA_RS — R3 — RESERVED
BSS_LOGGER — R14_3 — 33.2 — BSS_LOGGER_RS — R4 — RESERVED
MSS_LOGGER — R15_3 — 33.2 — MSS_LOGGER_RS — R5 — RESERVED

U1_3A — G13 — RESERVED

XA1243FPBIGABLQ1

ClassName: 12XX_POWER_ANA

VOUT_14SYNTH — A13 — AR_1V4_SYNTH
VOUT_14APLL1 — A10 — AR_1V4_APLL
VBGAP — B10 — AR_VBGAP
VOUT_PA — A2 — AR_VOUT_PA
VOUT_PA — B2 — AR_VOUT_PA
R188_3 — 0 — AR_1V0_RF2

Place R188 as close as possible to VOUT_PA/RF2 pins

Note: AR_1V0_RF2 optionally shorted to AR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.

R188 installed - shorts AR_VOUT_PA to AR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation

CSI2_TXP[0] — G15 — CSI2_TX0_P
CSI2_TXM[0] — G14 — CSI2_TX0_N
CSI2_TXP[1] — H15 — CSI2_TX1_P
CSI2_TXM[1] — H14 — CSI2_TX1_N
CSI2_CLKP — J15 — CSI2_CLK_P
CSI2_CLKM — J14 — CSI2_CLK_N
CSI2_TXP[2] — K15 — CSI2_TX2_P
CSI2_TXM[2] — K14 — CSI2_TX2_N
CSI2_TXP[3] — L15 — CSI2_TX3_P
CSI2_TXM[3] — L14 — CSI2_TX3_N
HS_DEBUG1_P — M15 — LVDS_FRCLK_P
HS_DEBUG1_M — M14 — LVDS_FRCLK_N
HS_DEBUG2_P — N15 — LVDS_VALID_P
HS_DEBUG2_M — N14 — LVDS_VALID_N

QSPI_CS_RS — P8 — QSPI_CS — R6_3 — 0 — QSPI_CS
QSPI_CLK_RS — R10 — QSPI_CLK — R7_3 — 0 — QSPI_CLK
QSPI[0] — R11 — QSPI_D0
QSPI[1] — P9 — QSPI_D1
QSPI[2] — R12 — QSPI_D2
QSPI[3] — P10 — QSPI_D3

QSPI_FLASH_3V3
R3_3 — 47.5k

Place termination and pull-up resistors close to QSPI controller - minimize stubs.

ClassName: 12XX_QSPI

TCK — M13 — TCK
TMS — L13 — TMS
TDO_RS — J13 — TDO_RS — R8_3 — 33.2 — TDO
TDI — H13 — TDI

ClassName: 12XX_JTAG

SPI_HOST_INTR1_1 — P6 — SPI_HOST_INTR1_RS — R10_3 — 33.2 — SPI_HOST_INTR1
SPI_CLK_1 — R9 — SPI_CLK1
SPI_CS_1 — R7 — SPI_CS1
MISO_1 — P5 — SPI_MISO1_RS — R12_3 — 33.2 — SPI_MISO1
MOSI_1 — R8 — SPI_MOSI1

ClassName: 12XX_GENERAL

GPIO[0] — N4 — GPIO_0
GPIO[1] — N7 — GPIO_1
GPIO[2] — M13 — GPIO_2

R16_3 10.0k — R17_3 10.0k — R18_3 10.0k — GND

ClassName: 12XX_GENERAL

XWR LDO and Bandgap Output Capacitors

AR_1V4_SYNTH — C1_3 16V 1uF — GND
AR_VBGAP — C2_3 16V 0.22µF — GND

Place output capacitors as close to power pins as possible - minimum mounting inductance.

AR_1V4_APLL — C3_3 16V 1uF — GND
AR_VOUT_PA — C4_3 16V 0.22µF — C5_3 10V 10uF — GND

NOR QSPI FLASH (For Development Purposes)

Pull-ups disable write-protect and hold functions by default.

QSPI_FLASH_3V3 — R27_3 10.0k — R28_3 10.0k

QSPI_D0 — R30_3 — 0 — QSPI_D0_RS
QSPI_D1 — R31_3 — 0 — QSPI_D1_RS
QSPI_D2 — R32_3 — 0 — QSPI_D2_RS
QSPI_D3 — R33_3 — 0 — QSPI_D3_RS

Place termination and pull-up resistors close to QSPI flash - minimize stubs.

QSPI_FLASH_3V3 — U2_3 — 8 — VCC
QSPI_CS — 1 — CS
QSPI_CLK — 6 — SCLK
5 — SI/SIO0
2 — SO/SIO1
3 — WP/SIO2
7 — HOLD/SIO3
EP — 9
GND — 4

MX25V1635FZNQ

NOR Flash 16Mb (2M x 8) 80MHz CLK

GND

ClassName: SYSTEM_3V3

SYSTEM_3V3 — R29_3 — 0 — QSPI_FLASH_3V3

Flash 3.3V Power Disconnect - Use to disconnect power to flash.

C6_3 10V 10uF — C7_3 16V 1uF — C8_3 50V 0.1uF — GND

Debug Test Header (For Development Purposes)

GPADC1 — R21_3 — 0 — GPADC1_CONN
GPADC2 — R22_3 — 0 — GPADC2_CONN
GPADC3 — R23_3 — 0 — GPADC3_CONN
GPADC4 — R24_3 — 0 — GPADC4_CONN
GPADC5 — R25_3 — 0 — GPADC5_CONN
GPADC6 — R26_3 — 0 — GPADC6_CONN

J1_3 — DNP — TSM-106-01-L-DV — GND

ClassName: 12XX_DEBUG

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 6/27/2019
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 12XX_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 19
Drawn By: a0271760		File: PROC054C_12XX_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

Texas Instruments — http://www.ti.com

XWR1243 Radar SoC - Interfaces

References

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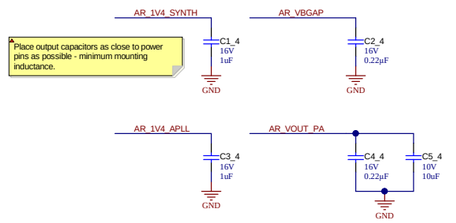
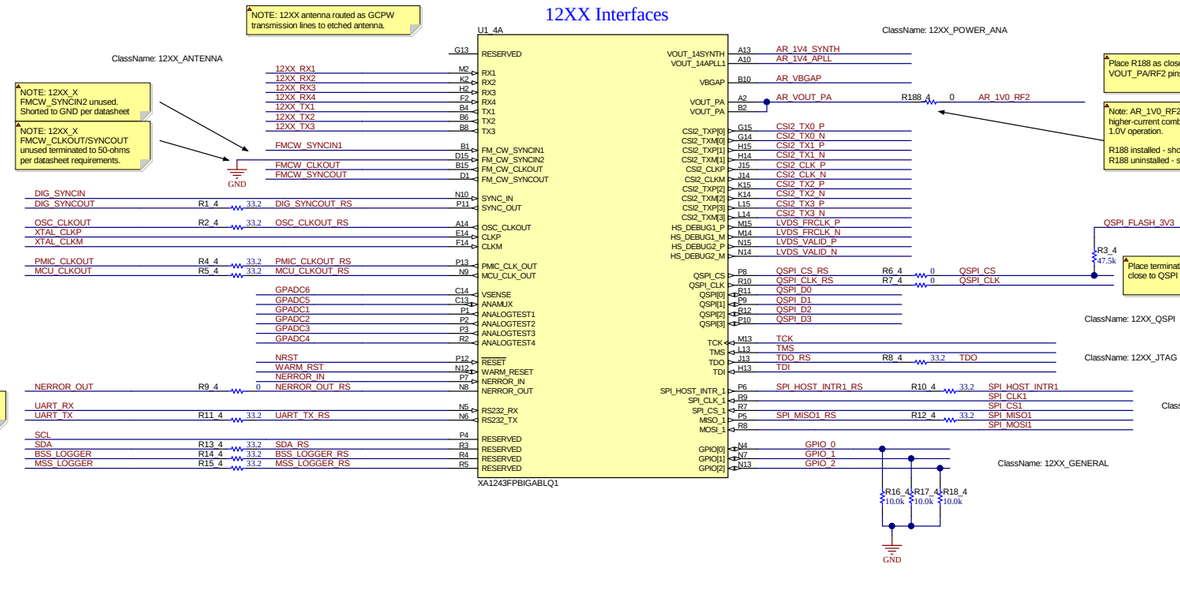
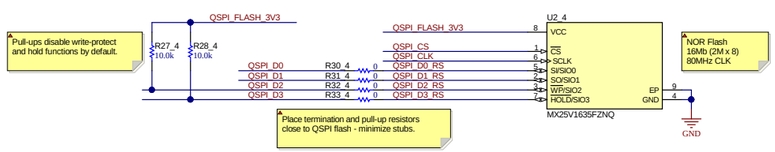
XWR LDO and Bandgap Output Capacitors



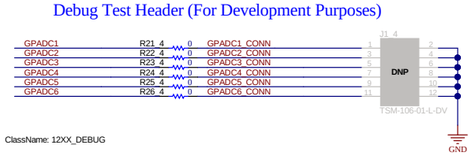
12XX Interfaces



NOR QSPI FLASH (For Development Purposes)



Debug Test Header (For Development Purposes)



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 6/27/2019
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 12XX_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 19
Drawn By: a0271760		File: PROC054C_12XX_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

References

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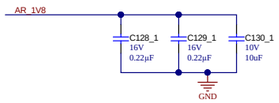
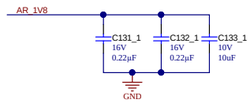
XWR1243 Radar SoC - Power

XWR Power - BGA Decoupling

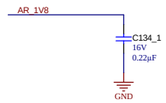
BB SUPPLY



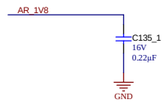
VCOLDO SUPPLY

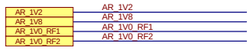


DIFF IO SUPPLY

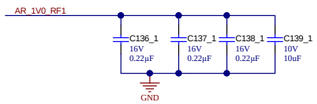


1V8_VIO SUPPLY

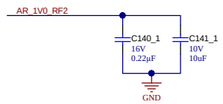




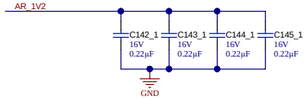
RF1 SUPPLY



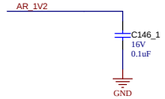
RF2 SUPPLY



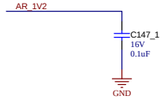
DIG CORE SUPPLY



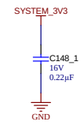
SRAM SUPPLY



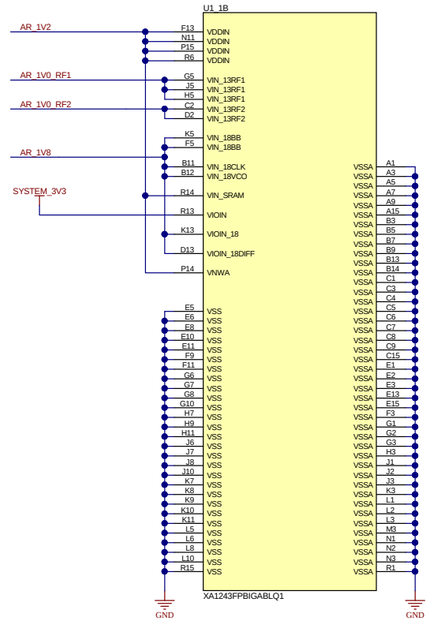
VNWA SUPPLY



3V3_IO SUPPLY



XWR Power



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: DECOUPLING_CAPS_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 11 of 19
Drawn By: a0271760		File: PROC054C_12XX_DECOUPLING_CAPS_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

References

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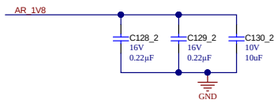
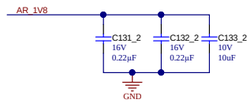
XWR1243 Radar SoC - Power

XWR Power - BGA Decoupling

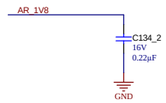
BB SUPPLY



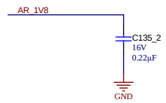
VCOLDO SUPPLY

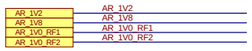


DIFF IO SUPPLY

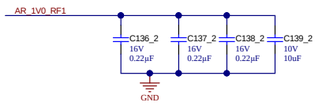


1V8_VIO SUPPLY

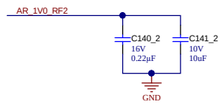




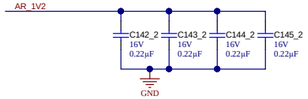
RF1 SUPPLY



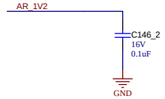
RF2 SUPPLY



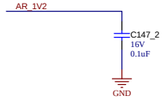
DIG CORE SUPPLY



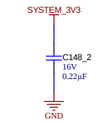
SRAM SUPPLY



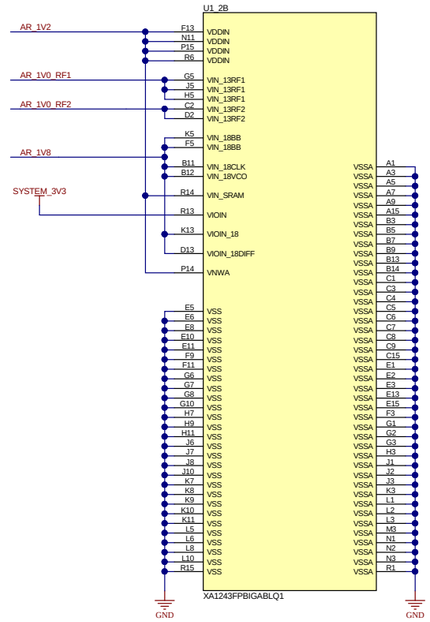
VNWA SUPPLY



3V3_IO SUPPLY



XWR Power



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: DECOUPLING_CAPS_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 11 of 19
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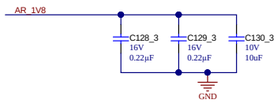
References

???????

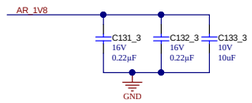
XWR1243 Radar SoC - Power

XWR Power - BGA Decoupling

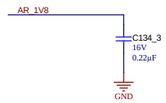
BB SUPPLY



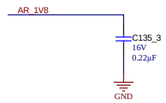
VCOLDO SUPPLY

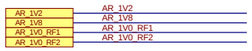


DIFF IO SUPPLY

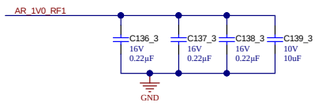


1V8_VIO SUPPLY

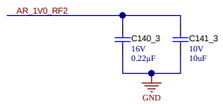




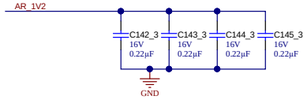
RF1 SUPPLY



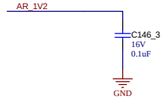
RF2 SUPPLY



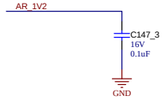
DIG CORE SUPPLY



SRAM SUPPLY

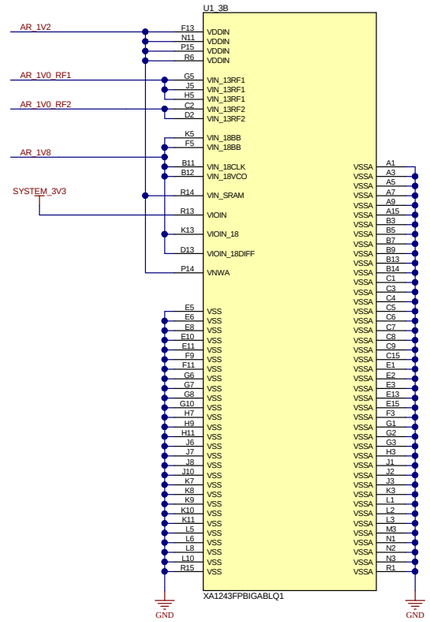


VNWA SUPPLY



3V3_IO SUPPLY

XWR Power



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
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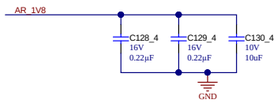
References

???????

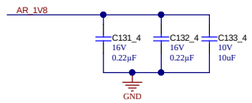
XWR1243 Radar SoC - Power

XWR Power - BGA Decoupling

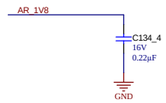
BB SUPPLY



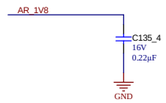
VCOLDO SUPPLY

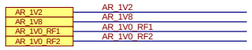


DIFF IO SUPPLY

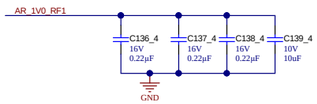


1V8_VIO SUPPLY

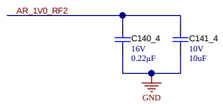




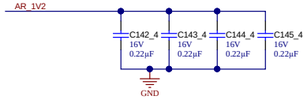
RF1 SUPPLY



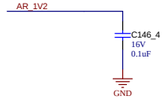
RF2 SUPPLY



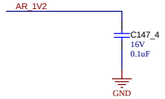
DIG CORE SUPPLY



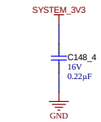
SRAM SUPPLY



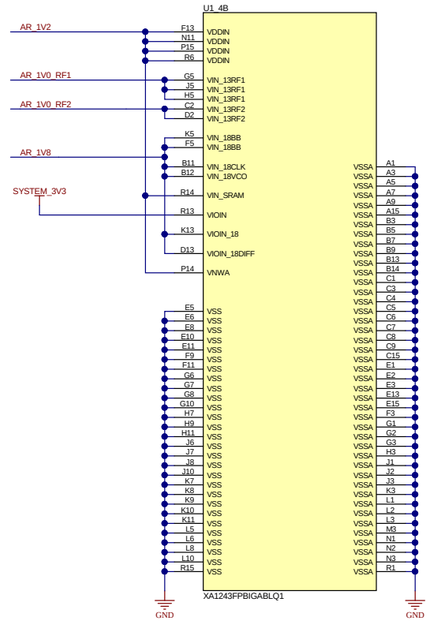
VNWA SUPPLY



3V3_IO SUPPLY



XWR Power



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
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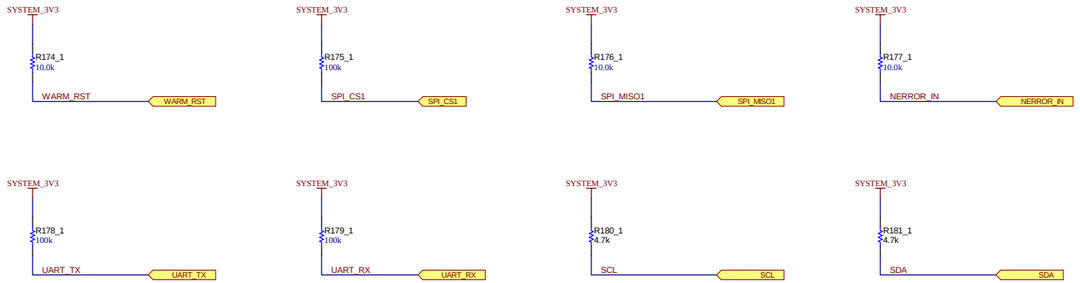
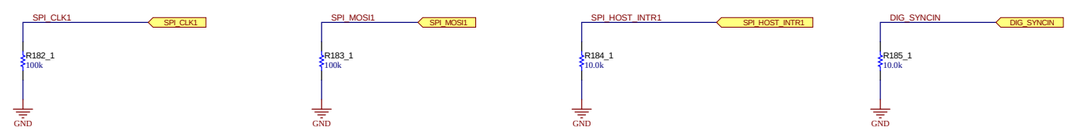
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 11 of 19
Drawn By: a0271760		File: PROC054C_12XX_DECOUPLING_CAPS_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



PULL DOWN OPTIONS

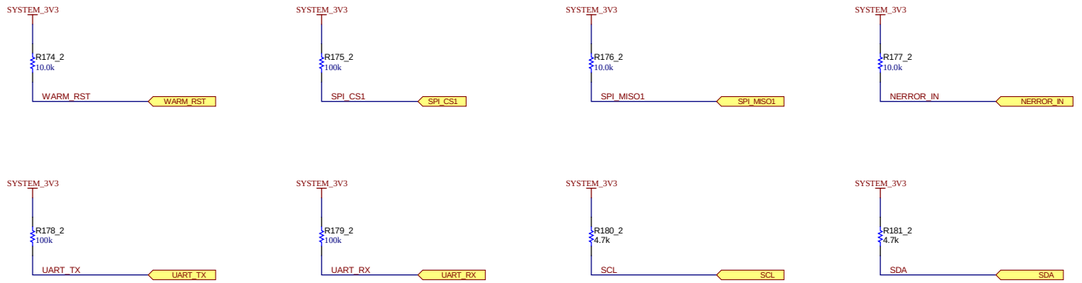


Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: PULL_UP_DOWN_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 12 of 19
Drawn By: a0271760		File: PROC054C_PULL_UP_DOWN_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

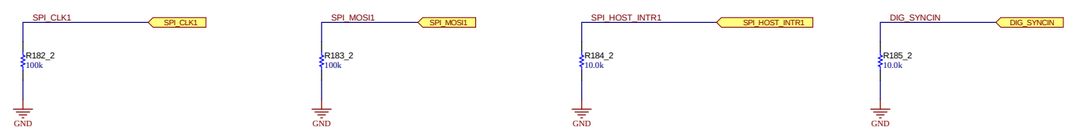
TEXAS INSTRUMENTS
http://www.ti.com

XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



PULL DOWN OPTIONS



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: PULL_UP_DOWN_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 12 of 19
Drawn By: a0271760		File: PROC054C_PULL_UP_DOWN_1.SchDoc	Size: C
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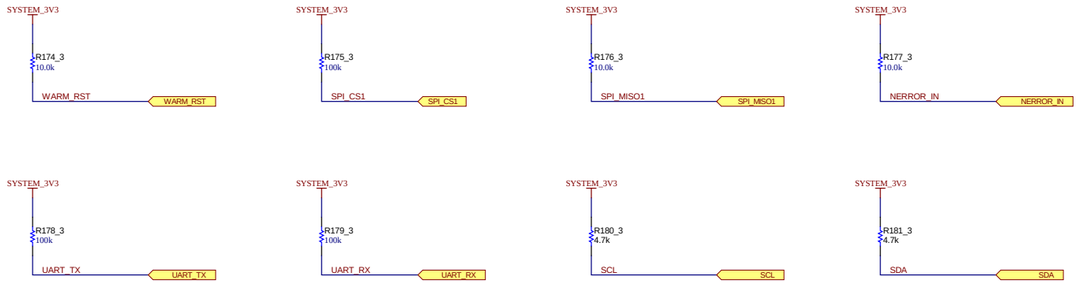
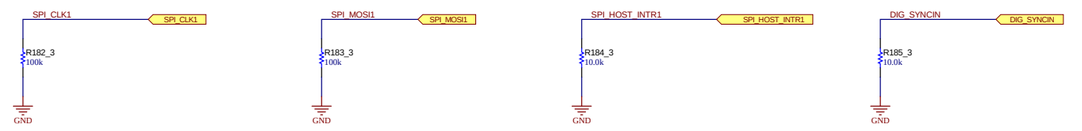
http://www.ti.com

XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



PULL DOWN OPTIONS



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: PULL_UP_DOWN_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 12 of 19
Drawn By: a0271760		File: PROC054C_PULL_UP_DOWN_1.SchDoc	Size: C
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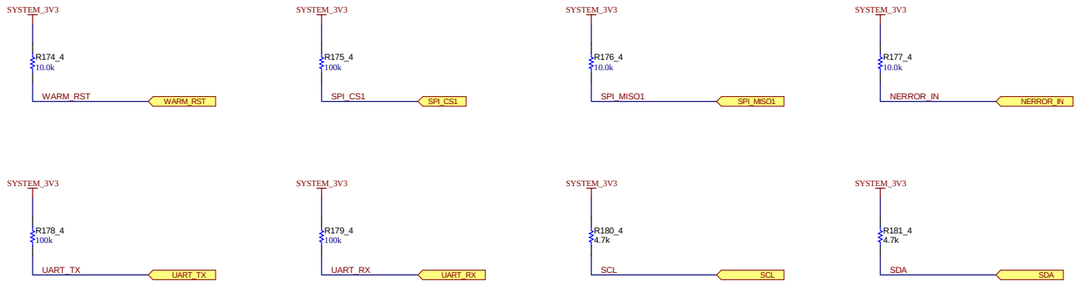
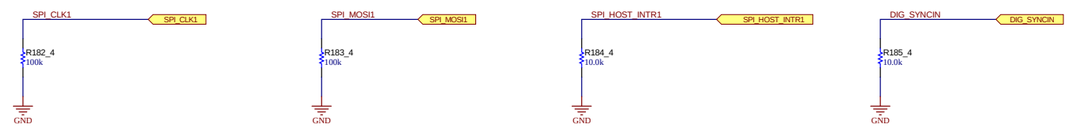
XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS



PULL DOWN OPTIONS



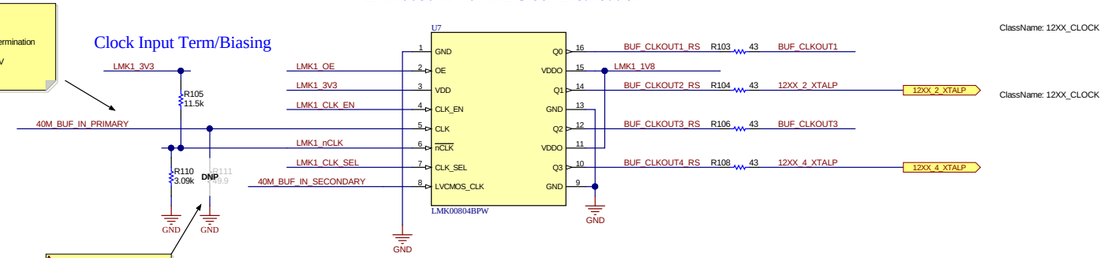
Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: PULL_UP_DOWN_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 12 of 19
Drawn By: a0271760		File: PROC054C_PULL_UP_DOWN_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

Cascade RF 40 MHz Clock Generation and Distribution

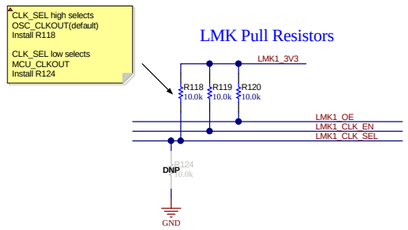
References

LMK00804BEVM User's Guide

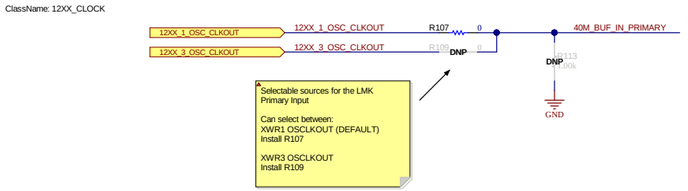
LMK00804B 40MHz Clock Distribution



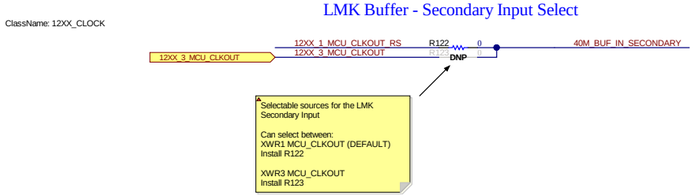
LMK Pull Resistors



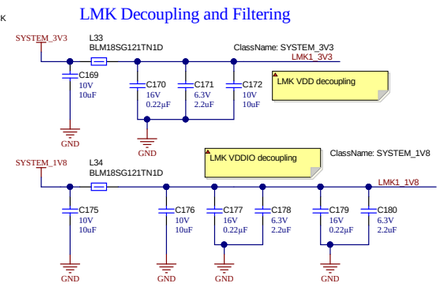
LMK Buffer - Primary Input Select



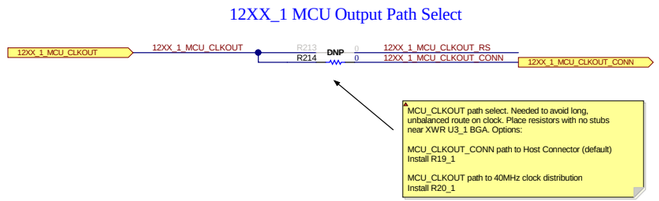
LMK Buffer - Secondary Input Select



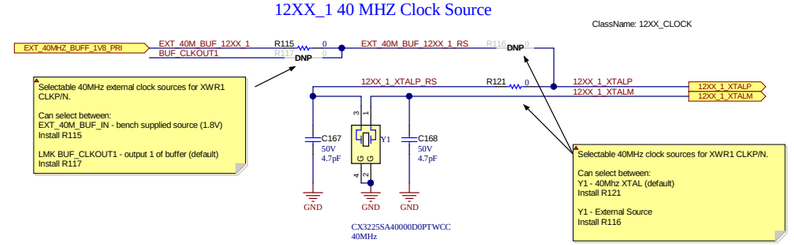
LMK Decoupling and Filtering



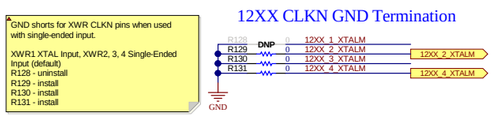
12XX_1 MCU Output Path Select



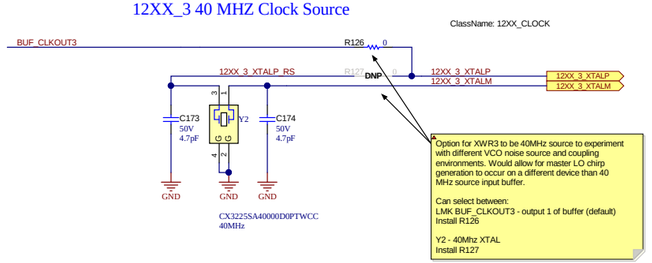
12XX_1 40 MHZ Clock Source



12XX CLKN GND Termination



12XX_3 40 MHZ Clock Source



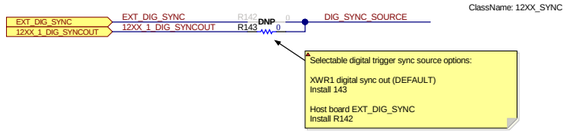
Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: 40MHZ_CLOCK_1	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 13 of 19
Drawn By: a0271760		File: PROC054C_40MHZ_CLOCK_1.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

Cascade RF Digital Sync Trigger and 20GHz LO Distribution

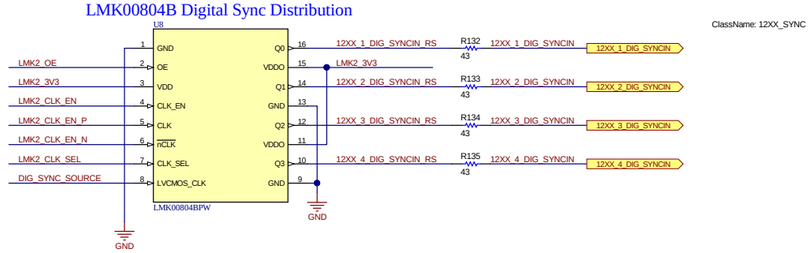
References

LMK00804BEVM User's Guide

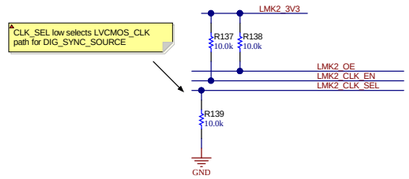
Digital Sync Source Select



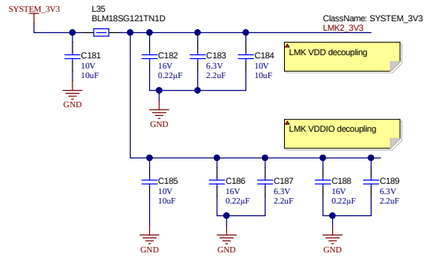
LMK00804B Digital Sync Distribution



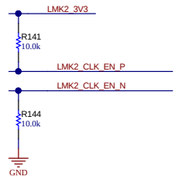
LMK Pull Resistors



LMK Decoupling and Filtering

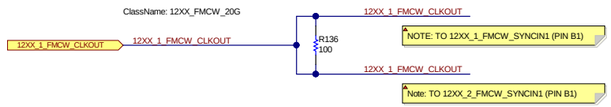


LMK Unused Input

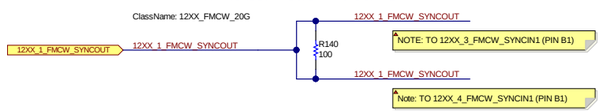


FMCW 20GHz LO SYNC

Wilkenson Power Divider #1



Wilkenson Power Divider #2



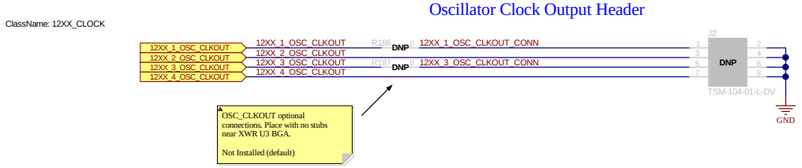
Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: FMCW_SYNC	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 14 of 19
Drawn By: a0271760		File: PROC054C_FMCW_SYNC.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

References

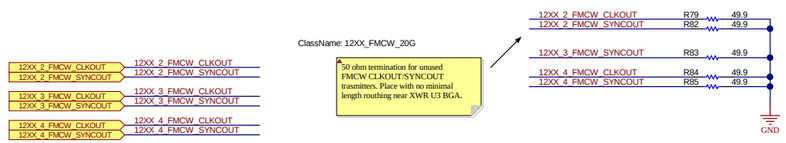
NONE

Test Headers, Connectors and Terminations

Oscillator Clock Output Header



Unused 20GHz LO Output Termination



20GHz LO Test Output

Orderable: NOT ORDERABLE	Designed for: Public Release — Mod. Date: 11/28/2018
TID #: N/A	Project Title: PROC054
Number: PROC054 — Rev: C	Sheet Title: SMA_SMP_CONNECTORS
SVN Rev: Not in version control	Assembly Variant: 001 — Sheet: 15 of 19
Drawn By: a0271760	File: PROC054C_SMA_SMP_CONNECTORS.SchDoc — Size: C
Engineer: a0271760	Contact: http://www.ti.com/mmwave

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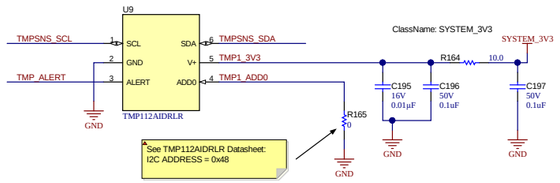
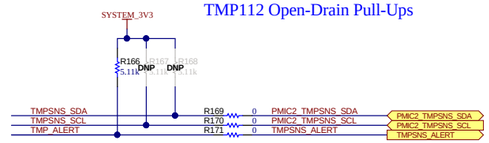
System Temperature Sensors

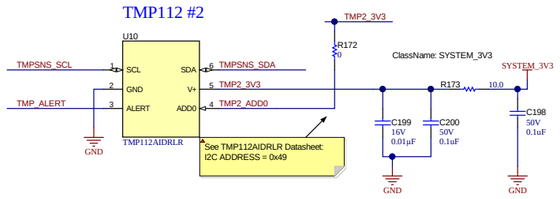
TMP112 #1



TMP112 Open-Drain Pull-Ups



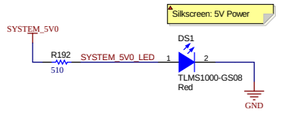
TMP112 #2

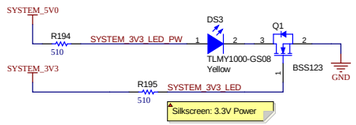


Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: ON_BRD_TEMP_SENSOR	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 16 of 19
Drawn By: a0271760		File: PROC054C_ON_BRD_TEMP_SENSOR.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

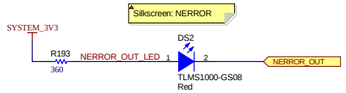
Cascade Radar RF Board Indicator LED

POWER LEDS

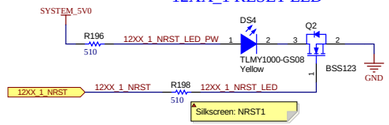




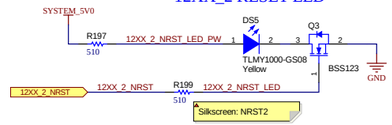
ERROR LEDS



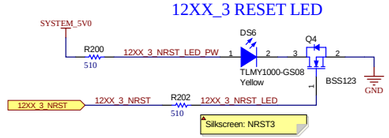
12XX_1 RESET LED



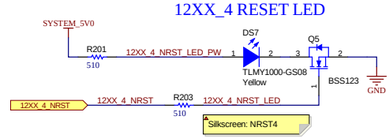
12XX_2 RESET LED



12XX_3 RESET LED



12XX_4 RESET LED



Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: SYSTEM_LED	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 17 of 19
Drawn By: a0271760		File: PROC054C_SYSTEM_LED.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	http://www.ti.com

Cascade Radar RF Board - Hardware, Mounting Holes and Logos

DNP FID1 DNP FID2 DNP FID3 DNP FID4 DNP FID5 DNP FID6

PCB Number: PROC054
PCB Rev: C

PCB LOGO
Texas Instruments

CE Mark

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

PCB LOGO
ESD Susceptible

CAUTION HOT SURFACE

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: Hardware	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 18 of 19
Drawn By: a0271760		File: PROC054C_EVM_Hardware.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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Cascade Radar RF Board - Revision History

Revision History

Rev	Date	Released By	Notes
1	2018/07/09	Randy Rosales <rosales.r@ti.com>	Initial release for layout cleanup and internal review.
2	2018/07/17	Randy Rosales <rosales.r@ti.com>	Updating based on 2018/07/09 comments. Combined PMIC_BUCK_EN and PMIC_NRST Combined PMIC1_PGOOD and PMIC2_PGOOD into single SYSTEM_PGOOD Updating NRST generation scheme from LP87524P PMIC Created separate 12XX_X reset generation paths Combined GPIO2 and PGOOD into PGOOD net Removing leftover resistor selection options from the previous LDO and PMIC power paths. Removing first level LC filtering options from the previous LDO and PMIC power paths. Removed: L3, L6, L19, L22 Removed: C21, C29, C78, C86 Removed: C21, C29, C78, C86 This also removed a few power net segments which will now be fed directly from PMIC output Combined 12XX_1_1V8_FILT and 12XX_4_1V8_FILT into 12XX_14_1V8_FILT Combined 12XX_2_1V8_FILT and 12XX_3_1V8_FILT into 12XX_23_1V8_FILT Changing XWR LC filter to use TDK NLCV32T-R10M-EFRD identified by power team analysis PMIC1_12XX_14_1V8 now directly feeds into SYSTEM_1V8 supply - there was no reason to run this through XWR 1.8V LC filter. Added SYSTEM_5V0 to 3.3V resistor divider for LP87524 PMIC pull-up resistors Updated U2 to the Macronix MX25V1635FZNQ - aligning with other XWR EVM kits Removed R125 - Optional resistor remaining from previously removed option for alternative XTAL input Changed NERROR_OUT LED bias to SYSTEM_3V3 Updated coversheet block diagram Updated power distribution block diagram
2	2018/07/17	Randy Rosales <rosales.r@ti.com>	Added variant information for do not populate stuffing options.
3	2018/07/18	Randy Rosales <rosales.r@ti.com>	Removed 50 ohm terminations to ground at the J2 OSCCLK_OUT test header Removed test headers on PMIC output rails Added zero-ohm resistor between PMIC GPIO3 and PGOOD Replaced all note, class and netname instances of AWR with XWR for industrial/automotive alignment of schematics Replaced all series termination on LMK00804B output with 43 ohm resistors per LMK00804B datasheet Replaced XWR reset generation circuit with discrete AND gate Required for achieving clean reset of XWR devices across all device margins Netname error on XWR SPI interface - MISO netname change R112 and EXT_40MHZ_CLK_1V8 removed - this was an alternative clock path that is no longer supported Eliminated RF1/2 channel naming error in PROC054_System_Power.SchDoc and PROC054_System_Top.SchDoc
4	2018/07/21	Randy Rosales <rosales.r@ti.com>	Changed R54 to pull-up resistor. LP87524P GPIO2 and GPIO3 both configured as open-drain output.
5	2018/07/21	Randy Rosales <rosales.r@ti.com>	Added 10kohm pull-up to LP87524P GPIO3 - required after change separating out GPIO3 and PGOOD nets Aligned PMIC1 and PMIC2 RF1 and RF2 LC filter components with 1.2V and 1.8V filter Previous RF1 and RF2 LC values were still not merged from removal of LDO option separation of RF1 and RF2 supplies
6	2018/07/28	Randy Rosales <rosales.r@ti.com>	Changing all layout critical resistors and capacitors to small-outline version in Altium Vault library Required to allow Tessolve to implement original decoupling and series resistor layout near the 12XX BGA Will allow for more compact routing throughout the design as well Changed R136, R140 FMCW LO power divider resistor to RF resistor CH02016-100RJFT Changed U3 and U4 PMIC to reference proper P-version in Altium vault. Adding zero-ohm resistors to 12XX_1/2/3/4 I2C interfaces, optionally shorting those interfaces to the PMIC1_I2C Changed NERROR_OUT LED to sourced from shorted NERROR_OUT Originally being fed 12XX_1_ERROR_OUT
7	2018/08/08	Randy Rosales <rosales.r@ti.com>	Added R188 which shorts AR_VOUT_PA to AR_1V0_RF2 supply nets. Recommended for supporting increased current into the RF2 supplies in 1.0V mode supporting simultaneous 3 TX operation
8	2018/08/09	Randy Rosales <rosales.r@ti.com>	Added burn danger logo Added ESD danger logo Consolidated FMCW 20G LO, digital sync and clock net classes. Created the following net classes: 12XX_FMCW_20G 12XX_CLOCK 12XX_SYNC Removed extraneous MCU_CLKOUT_CONN path from XWR2, XWR3 and XWR4 Consolidated XWR1 MCU_CLKOUT path output options on PROC054_40MHZ_CLK1 schematic sheet Renamed schematic PROC054_40MHZ_FMCW_SYNC to PROC054_FMCW_SYNC Aligned antennas with 12XX prefix naming convention Added all nets on 40MHZ_CLOCK_1 schematic sheet to netclass12XX_CLOCK
9	2018/08/10	Randy Rosales <rosales.r@ti.com>	Added additional nets to the 12XX_SYNC net class Added additional nets to the 12XX_FMCW_20G net class Replaced J3 with correct Rosenberger 19S101 part from TI Altium Vault.
10	2018/08/16	Randy Rosales <rosales.r@ti.com>	Added additional R19 and R20 0-ohm resistors to create optional feedback path for bench supply connector P3

Orderable: NOT ORDERABLE		Designed for: Public Release	Mod. Date: 11/28/2018
TID #: N/A		Project Title: PROC054	
Number: PROC054	Rev: C	Sheet Title: Revision History	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 19 of 19
Drawn By: a0271760		File: PROC054C_Revision_History.SchDoc	Size: C
Engineer: a0271760		Contact: http://www.ti.com/mmwave	

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