COTS Controversy:
Test-in or Build-in Quality?

Beyond Quality – Assuring the Reliability of Plastic Encapsulated Integrated Circuits

Uprating and upscreening commercial components to extended temperatures are dangerous practices that can adversely affect reliability and maintainability. Instead, look closely at the IC manufacturer's fabrication, assembly and qualification process, policies and procedures.

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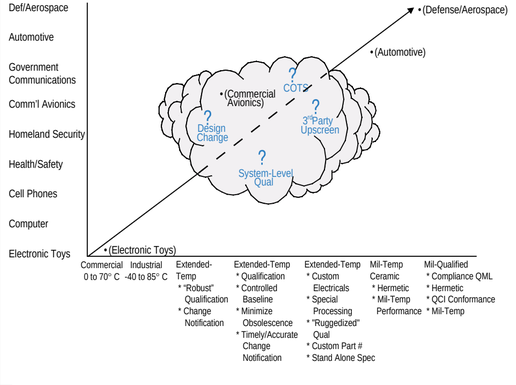

Figure 1

Multiple factors cloud COTS components selection. Unfortunately, defense and aerospace applications are well out of the mainstream markets targeted by most IC manufacturers.

For more than forty years the Department of Defense was the leader in publishing guidance for component reliability and maintainability. But as a part of Defense Acquisition Reform, the responsibility has now shifted to the defense original equipment manufacturers (OEMs) where most programs are governed by performance-based specifications. Military and aerospace OEMs using commercial off-the-shelf (COTS) components must now establish their own standards for qualification and reliability.

Commercial semiconductor products are not designed for military and aerospace applications. Instead, they're designed for use in a wide range of applications and environments that are often at odds with defense applications (Figure 1). With military and aerospace platforms, some applications are very benign while other applications require careful selection of the proper device type to ensure system reliability. Each environment has very different requirements that must be addressed to determine what type of integrated circuit can be used in that environment.

Specifications such as ISO9000 and AS9000 focus on the quality systems used to manufacture integrated circuits. Other specifications such as AEC Q100 and JEDEC standards rely on device level qualification and testing to ensure delivered product meets the needs of the OEM. While a good start, such practices are not in and of themselves adequate to ensure long-term reliability in harsh environments.

Even when the semiconductor manufacturer performs additional qualification and screening for operation at extended temperatures, it only provides a means to facilitate—not replace—OEM qualification of COTS devices. Instead, defense system designs must examine the IC manufacturer's fabrication, assembly and qualification procedures for integrated circuits to ensure reliable operation over extended temperatures.

IC Obstacles

Military and commercial avionics OEMs currently purchase 0.5% to 1.0% of the total number of commercial integrated circuits sold. With so many commercial applications driving OEM IC designs, as much as 30 or 40 percent of COTS devices destined for military use require uprating or upscreening, depending on the OEM and the application. For the purposes of this discussion, uprating is defined as use beyond the environment and application for which the part was designed. Upscreening, on the other hand, is defined as performing additional testing and/or lot acceptance to use product beyond data sheet conditions. Other applications, such as ground-based communication systems, are more benign and COTS components may be suitable for use without additional qualification or screening.

Uprating and upscreening are problematic at best. Very few, if any, manufacturers will support this effort, and few upscreening test facilities have the ability to test complex parts. The actual process of upscreening has the potential to degrade component reliability. For example, there is the possibility of yield loss and damage due to electrical overstress and electrostatic discharge. Mechanical damage can degrade moisture performance, and burn-in can cause lead finish degradation.

As part of uprating and upscreening, OEMs typically perform some type of qualification testing at the device and system level to ensure safe and reliable operation in their specific application. Integrated circuit (IC) suppliers, on the other hand, perform qualification testing and monitors based upon generic industry standards. Existing industry standards for plastic encapsulated microcircuit qualification and reliability monitors are based upon historical data, experiments and field experience with the use of these devices in commercial and industrial applications.

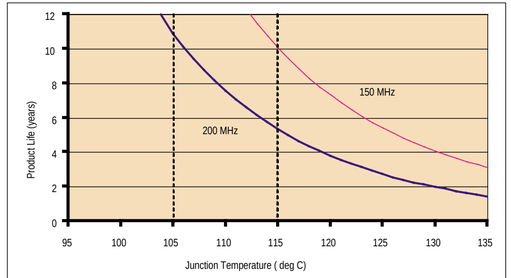

Figure 2

Electromigration: Life versus Junction Temperature. Maintaining the proper junction temperature prolongs device life; reducing clock speed is beneficial to both.

The applicability of these standards in determining the suitability for use and safety performance in military and aerospace applications has not been established. The value of process monitors in assessing relative quality and reliability of semiconductor devices is quite limited. Since these monitors are performed on a periodic basis on random samples of devices, they cannot be considered acceptance tests on any specific group of components.

To further compound the problem, device and process changes that do not affect commercial applications could impact the performance or suitability of devices for military or other high-reliability environments. Changes to die design, wafer fabrication processes, assembly processes and package components such as mold compounds may not be considered as affecting the form, fit and function of COTS devices and may not be disclosed by the IC manufacturer. Therefore, IC manufacturer quality and reliability data, if available, only reflects a one-time snapshot of the existing process baseline. It is an aggregate estimate of product performance within published data sheet limits based upon history.

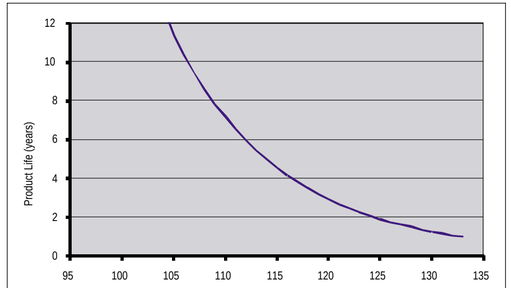

Figure 3

TQFP Packaged Product Gold Wire Bond Life versus Junction Temperature. As Tj increases, the bond degrades and device reliability decreases exponentially.

COTS Standard Qualification and Screening

Testing and screening semiconductor products is performed in accordance with the manufacturer's data sheet for that device. Components are processed per "best commercial practices" to the manufacturer's internal baseline flow. Processing and screening is typically documented in the manufacturer's Quality Manual. Almost all semiconductor manufacturers are certified to ISO9001.

To ensure a device exhibits the best quality and reliability possible when using that technology over an extend temperature range or in harsh environments, additional evaluation is needed:

- Reliability and electromigration checks at maximum recommended operating conditions in the target package
- Electrical characterization over temperature
- Confirmation of package performance over extended temperatures (for example, some mold compounds are not suitable for extended temperature)

The term "Qualification Pedigree" is used in the aerospace industry to define the qualification and characterization performed by a manufacturer. Reliability monitors are usually performed on a regular basis and include EFR (extrinsic failure rate) and IFR (intrinsic failure rate) life test, temperature cycle and Biased Humidity or Highly Accelerated Stress Testing (HAST). Test methods should be based upon accepted JEDEC and EIA standards. In the event a monitor discloses a device quality or reliability issue, the manufacturer decides what corrective action is required and whether to issue customer notification.

This product evaluation and qualification augments the product qualification and

TI Enhanced Plastic Product Family

In response to customer needs, Texas Instruments has released the Enhanced Plastic (EP) product family to facilitate, not replace, OEM qualification of COTS devices through baseline control and enhanced qualification pedigree.

Enhanced Plastic (EP) devices are TI catalog products comprehending devices from multiple families including Digital Signal Processors (DSP), Analog and Mixed-Signal, Digital Logic, ASIC, Microcontrollers and Programmable Logic. Enhanced Plastic (EP) devices offer several advantages over standard COTS products:

- Stand-alone data sheets
- A controlled baseline—one assembly/test site and one wafer fabrication site
- Enhanced product change notification (PCN) via electronic distribution
- Die revisions
- Assembly process changes
- Material changes such as mold compound and lead finish
- Electrical performance
- Manufacturing location
- Extended temperature up to and including -55°C to +125°C
- Qualification pedigree to assure reliable operation over specified temperature range
- Assurance from TI that the device will perform to data sheet electrical specifications in environments that require extended temperatures
- Standard Nickel-Palladium-Gold or Tin-Lead lead finish

TI EP package qualification comprehends performance at extended temperatures with package element concerns such as glass transition temperature and thermal expansion coefficients taken into account. Electrical testing is warranted to meet the data sheet over the specified temperature range. Device characterization and statistical process controls are used to ensure performance over the specified temperature range. Assembly, test and qualification changes require approval of the TI Technical Review Board (TRB).

For EP devices, TI will provide change notification via the TI electronic parts change notification (PCN) system if a change has the potential to affect form, fit, function or reliability. In other words, changes to the baseline will be communicated prior to implementation. Distributors will be independently notified to facilitate notification of their customers.

In the event a proposed change does affect form, fit, function or reliability, TI will take steps to minimize the impact on the customer. This may include continuing production of the established baseline after commercial production has changed, establishing a wafer bank of the current die revision and/or offering a lifetime buy on the configuration in question.

TI's new products will offer an alternative to upscreening for customers who believe that a plastic packaged part is suitable for their particular application. Although the EP products receive additional testing and process verification over and above their commercial counterparts, they may still not be suitable for all environments. For those applications that require a ceramic/hermetic packaged integrated circuit, TI has an expansive product line to meet their needs. More information on EP products is available on the Texas Instruments website at http://www.ti.com/sc/ep.

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reliability monitors already inherent in a manufacturer's process. These standard qualification and reliability monitors should include:

- Extended temperature die reliability
- Package materials
- Overall qualification and reliability policies and procedures
- Wafer level reliability
- Die level reliability
- Package level reliability

Die Level Design Reliability at Extended Temperatures

IC manufacturers design devices in accordance with a formal set of design rules. These design rules are computer verified at numerous points during die design, layout and photomask generation. A design model is developed for a specific technology node with a device reliability model driven by predetermined reliability goals. These goals are typically set to meet the expectations of the commercial end customers. This model defines a specific set of maximum design conditions required to meet the reliability goals.

A careful evaluation of the technology and the device in question is required to ascertain if a candidate device will be reliable over extended temperatures. Arbitrary derating of such a device could result in extreme degradation of operating life. Figure 2 shows the operating life of a high complexity device versus junction temperature, both at the specified operating speed of 200 MHz and a reduced operating speed of 150 MHz. In some cases, different recommended operating conditions are required at maximum temperature. In other cases, a thermally enhanced package is used for extended temperatures where a standard package will suffice for the commercial part.

Package Materials Design Considerations

With plastic encapsulated integrated circuits, a critical consideration when contemplating extended temperature operation is the physical properties of the package itself. Multiple factors dictate the type of encapsulant used. These include the flow properties during the mold process, cure characteristics, thermomechanical stress of the die, high temperature performance and moisture performance. Since a single encapsulant cannot meet all requirements, designers must consider the trade-offs. In some cases, the designer will select a mold compound for optimal performance and consider only the commercial or industrial temperature ranges.

Encapsulants consist of multiple components including resins, fillers, flame-retardants and mold release agents. Of particular interest with respect to device reliability, are the flame-retardants. Bromated epoxies will release bromine when heated. Bromine has the effect of accelerating intermetallic formation between the gold bond wires and the aluminum die bond pads (Kirkendall voiding or "purple plague").

When a device is in use the actual temperature of the mold compound is higher than ambient due to internal heating of the die. Therefore the junction temperature of the device must be taken into consideration when evaluating bond life. Candidate devices must be evaluated for Au/Al bond intermetallic life based upon the die junction temperature at maximum recommended operating conditions. Failure to consider these factors can have a drastic effect on product life. Figure 3 depicts intermetallic related product life of gold wire bonds in a 144-pin thin-quad-flat-pack (TQFP) versus junction temperature.

Control Point	Test	Sample Point	Sample size/Frequency	Control Method
Metal	Visual	Post etch	Each lot	Lot accept
	Thickness	Post deposition	Each run	SPC
	SEM step coverage	Post sinter	1 wafer/deposition system and/or prod family/week	Monitor
Field oxide	Phosphorus level	Post metal etch or post emitter diffusion	1 wafer/week	Monitor
	C-V test	Finished wafer	Each lot	Monitor
Interlevel Oxide (ILO)	Integrity	Post via etch	1 wafer/reactor/week or 1 wafer/ILO structure/week	Monitor
	Thickness	Post deposition	1 pilot/reactor/run	SPC
	Visual	Post etch	Each lot	Lot accept
	Wt % phosphorus (doped ILO/MLO)	Post deposition	3 pilots/reactor/week	Monitor
Gate oxide	C-V test	Post oxidation	1 pilot/furnace/week	Monitor
Glassivation	Visual	Post etch	Each lot	Lot accept
	Thickness	Post deposition	Each run	SPC
	Refractive index	Post deposition	Each run	Monitor
	Integrity	Post etch	1 wafer/reactor/week or 1wafer/deposition type/week	Monitor

Table 1 *Precondition performed.

Typical Wafer Level Reliability Monitor Program. A wafer level reliability monitor program put in place by the manufacturer is crucial to ensuring long-term silicon reliability and reduction of lot-to-lot variations.

Standard Qualification and Reliability Monitors

Qualification and reliability monitoring is usually performed at several levels. In general, any new process or device technology is extensively qualified as a stand-alone entity. Variations of existing processes or technologies receive a less extensive qualification. For example, the release of a new family of digital signal processors using a new wafer fabrication process would receive a different level of qualification than an existing product die revision. A new package technology qualification would differ from the release of a qualified die into an existing package.

After initial qualification, various quality and reliability monitors are performed. In the wafer fabrication facilities, wafer level reliability monitors are performed to ensure that the wafer fab processes are in control and producing die to the wafer fabrication baseline. In the assembly sites, package-related testing is performed to ensure that the assembly process is in control and producing reliable devices. Periodic extrinsic failure rate (EFR) and intrinsic failure rate (IFR) life test monitors are performed. Monitors for leading edge technologies are more extensive than those performed for mature technologies.

Wafer Level Reliability Monitors

Most wafer fabrication facilities have established controlled specifications to define wafer level reliability controls procedures and testing. In general, these procedures address metallization, protective overcoat, multilevel/interlevel dielectrics and gate/storage dielectrics parameters. The specifics vary depending on process technology, such as bipolar or MOS. Table 1 is a typical wafer level reliability monitor program for a TI wafer fab.

Description	Condition	Sample Size	Referenced Method	
Bias Life Test	125°C/1000 hour or equivalent	116/0	JESD22-A108	*
Biased Humiduty or HAST	85°C/85%/1000 hours or 130°C/85%/96 hours	77/0	JESD22-A101 JESD22-A110	*
Autoclave	121°C @ 2 atmospheres absolute for 96 hours	77/0	JESD22-A102	*
Temperature Cycle	-65°C to +150°C non-biased for 1000 cycles	77/0	JESD22-A104	*
Solder Heat	260°C for 10 seconds	22/0	JESD22-A106	
Resistance to Solvents	Ink symbol only	12/0	JESD22-A107	
Solderability	Condition A (steam age for 8 hours)	22/0	ANSI/J-STD-002-92	
Flammability	Method A/Method B	5/0	UL-1964	
Bond Strength		76/0	ASTM F-459	
Die Shear		5/0	MIL-STD-883 Method 2019	
High Temp Storage	150°C/1000 hours	45/0	JESD22-A103-A	*
Moisture Sensitivity	Surface Mount Only	12/0	J-STD-020-A	

Table 2 * Precondition performed.

Typical New Package Qualification. Semiconductor package qualifications are driven by industry standards and commercial customer requirements.

Die Level Reliability Monitors

Periodic extrinsic failure rate and intrinsic failure rate life test monitors should be performed for each technology from each wafer fab. This typically consists of steady state life test for 1,000 hours at 125°C or equivalent. End point electrical testing is performed to the data sheet conditions but typically only at 25°C. Extensive testing is performed for a new technology. For periodic monitors of high-volume products, sample sizes range upward to thousands of devices each quarter per technology—inclusive of all wafer fabs. For high-complexity devices, the sample sizes may range upward of several hundred devices.

Conditions found during life test (that is, constant high temperature, low or no ambient humidity, and continuous device operation) do not address humidity-induced failure mechanisms or temperature cycling-induced failure mechanisms, which are found in non-benign environments. These are addressed by the HAST or 85C/85% RH, autoclave and temperature cycling tests. For moisture sensitive (per JESD A112A) plastic surface mount devices, preconditioning per JESD A113A is typically performed before the moisture and temperature cycling tests. Therefore, life test data must be supplemented with other environmental test data in determining how a plastic device will function in a given environment. Actual reliability in field conditions is also affected by board assembly techniques and conditions encountered during extended dormant storage.

Package Level Reliability Monitors

Package related monitors are typically performed by each assembly facility as dictated by the complexity of the technology and major end customer requirements. End point electrical testing is usually performed to the datasheet at 25°C. Table 2 is a typical new package qualification performed to JEDEC standards.

After qualification, periodic monitors are required to ensure the assembly process is under control. Typically Biased Humidity (or HAST), Autoclave (or unbiased HAST), Temperature Cycling and Bake tests are performed as monitors. Monitor sample sizes are derived based upon total volume of production and the maturity of the package family. Sample sizes and actual testing performed are subject to change. ■■

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