

Application Report

Using AFE77xx in a Digital Pre-Distortion System



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ABSTRACT

To combat the linear power limitation of the PA (power amplifiers) while reducing the total cost of the radio, radio manufacturers use lower cost PAs with certain linearity and power delivery while utilizing digital pre-distortion (DPD) to linearize the PA. Instead of having separate feedback path for the observation of the PA, the AFE77xx family of devices have built-in RF sampling analog-to-digital converters within the high channel count transceiver device to facilitate the DPD implementation. The AFE77xx family of devices have four zero-IF transmitter chains, four zero-IF receiver chains, and two dedicated RF sampling ADC based feedback path for DPD feedback purpose. This device with such high level of integration saves the overall system cost, especially in systems where DPD is required. This application report highlights the implementation of DPD with the AFE77xx, the signal chains of the transmitter and feedback receivers, and various key considerations for the system engineers to consider during DPD system planning.

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1 Terminologies

- PA: Power amplifier
- TXQMC: Transmitter quadrature modulator correction. This is used to correct for modulation images and local oscillator feedthrough.
- DPD: A technique where a digitally pre-distorted signal is applied to the power amplifier to compensate for the non-linearity of the power amplifier.
- TX: Transmitter Chain. There are four available transmitters in AFE77xx.
- FB: Feedback Observation Chain for Digital Pre-distortion. There are two available observation chain in the AFE77xx.
- DL: Downlink or traffic transmitter time duration
- RX: Traffic receiver chain. There are four available receivers in AFE77xx.
- UL: Uplink or traffic receiver time duration
- LO: Local oscillator. This is used for direct upconversion or downconversion mixing.
- NCO: Numerically controlled oscillator. This is used in the feedback path to downconvert RF signals to baseband.
- LO Feedthrough: Leakage power at local oscillator frequency due to DC offsets in the mixing circuits. This can be calibrated to a reduced level through TXQMC.
- Image: Unwanted image centered at the opposite side of the signal centered at local oscillator frequency. This is due to imperfect quadrature mixing of the mixing circuit. This can be calibrated to a reduced level through TXQMC.
- Nyquist image: This is the aliases image due to Nyquist sampling.
- MIMO: Multiple-input-multiple-output transceivers
- JESD204: High speed serial link defined by JEDEC Standard Committee
- SERDES: High speed serializer and deserializer

2 Introduction to DPD

In a typical telecom basestation and various derivatives such as small cell and distributed antenna systems, the total power delivery of the power amplifier (PA) and power efficiency are now key specifications for current fourth generation (4G) system and transitional systems for the upcoming 5th generation (5G). As demands for mobile data increases, the telecom equipment has to have smaller form factors while potentially supporting multiple-input-multiple-output antenna arrays (MIMO). The smaller physical size and higher density of the radio equipment are the driving forces for the higher power efficiency.

Although the number of antenna per radio equipment are going up, the cost of the equipment must be held flat in order for the radio manufacturers to be competitive in the growing landscape. In an ideal situation, the PA should be linear to deliver power that is proportional to the gain (k) of the PA and the input power (V_{in}), as shown in [Figure 2-1](#). However, the PAs have non-ideal linearity performance that can be characterized by the typical 1 dB compression point and third order intercept points (as shown in [Figure 2-2](#)). Engineers must consider these non-linear behavior in the design to understand the trade-off in the linear performance of the PA and the maximum output power limitation.

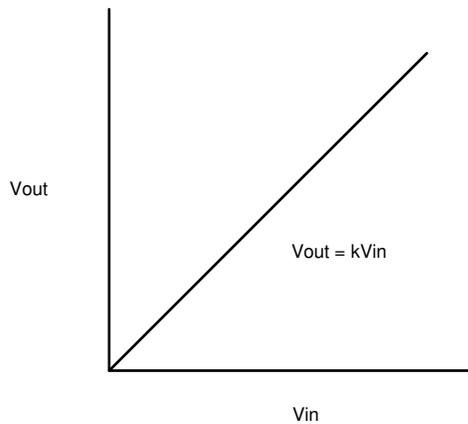


Figure 2-1. Ideal Power Amplifier Behavior with Linear Gain Model

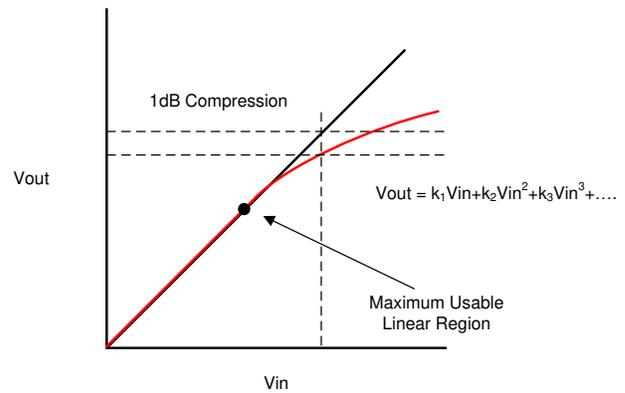


Figure 2-2. Actual Power Amplifier Behavior with Non-Linear Gain Coefficient Model

To combat the linear power limitation while reducing the total cost of radio, radio manufacturers have to be creative and use lower cost PAs with lower linear power delivery limit. Engineers apply innovative techniques to these types of PAs to drive the PAs into non-linear or even close to saturation region in order to provide higher transmit power delivery. The technique is done with digital processing, and is known as digital pre-distortion, or DPD. As shown in [Figure 2-1](#), the goal of the DPD is to characterize the non-linear behavior of the PA, and inject the signal with inverse of the non-linear function into the PA to linearize the total output. When comparing between [Figure 2-2](#) and [Figure 2-3](#), the available usable region of the PA can be increased after DPD linearization, and this translates to higher available output power of the radio system.

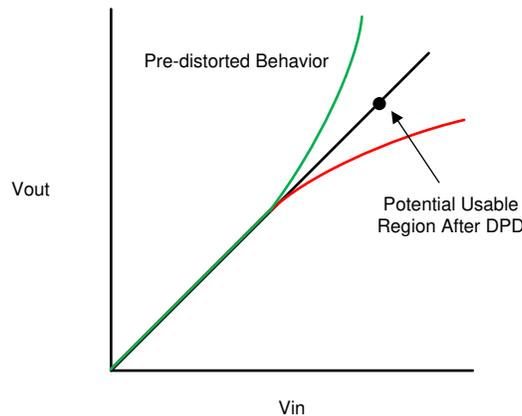


Figure 2-3. Total Power Amplifier Behavior with Predistorted Input

Various digital processing optimization and algorithm architecture have been studied and implemented in both the academia and industry, with the goal of increasing PA power delivery and efficiency. To implement the DPD, a radio must have a feedback path for transmit observation. To aid the system designers completing their radio transceiver system with DPD, TI's AFE77xx family of transceivers includes a high performance feedback observation path for the implementation.

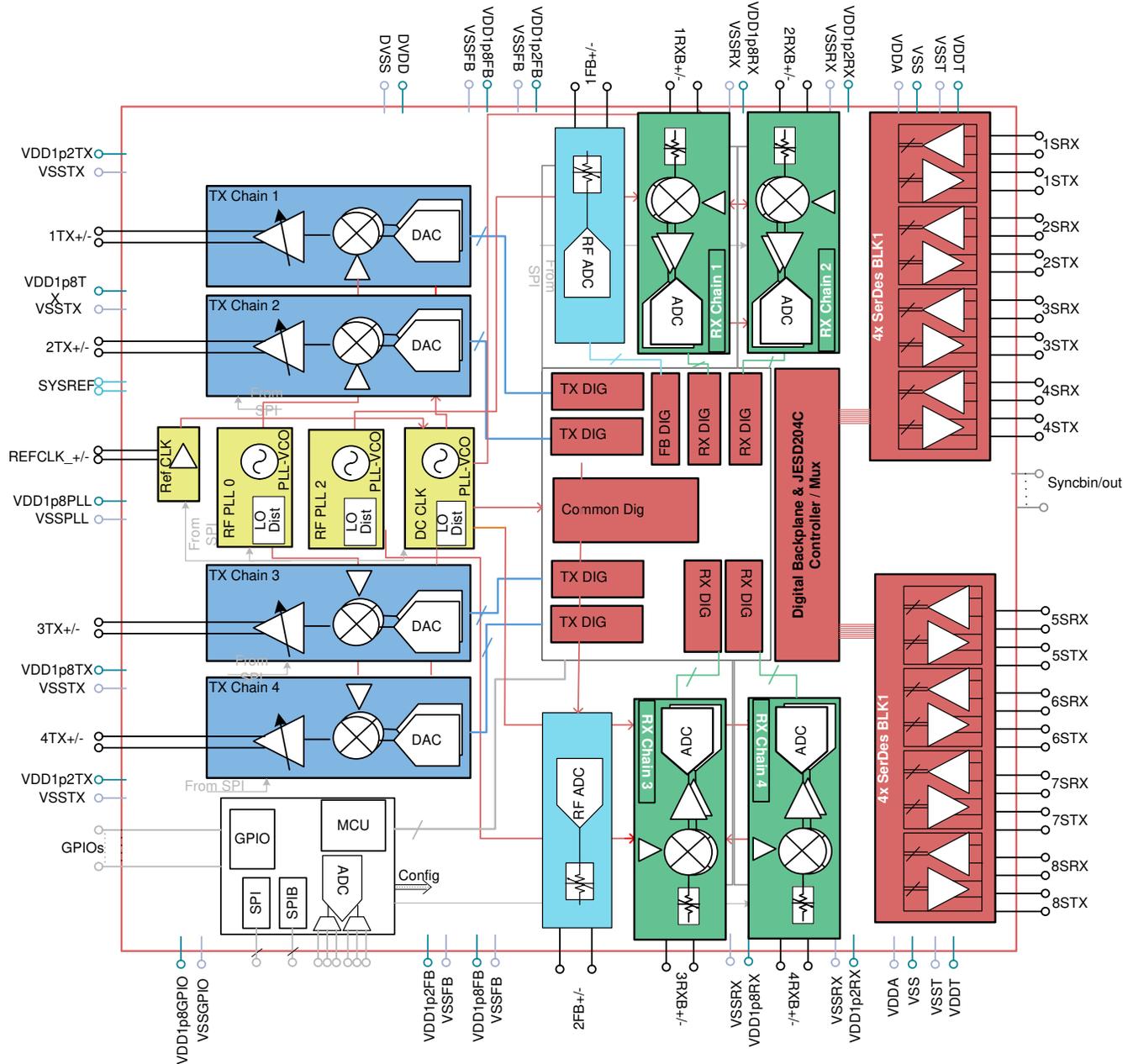


Figure 2-4. AFE77xx Family of Transceivers Block Diagram

3 Basics Building Blocks for DPD

3.1 Basic DPD System Building Blocks

In terms of the building blocks of the DPD system, the system consists of a negative feedback and also a forward correction path, as shown in Figure 3-1. The forward path can be simplified with a basic digital upconversion block with DAC, modulator, and the PA. The negative feedback path consists of an observation path that observe the PA output with demodulator, ADC, and digital downconversion block. The observed data during DPD operation is fed into the DPD processing loop in a negative feedback fashion to pre-distort the forward path. The pre-distorted power curve should be inversely proportional to the linearity curve of the PA in order to linearize the total PA output.

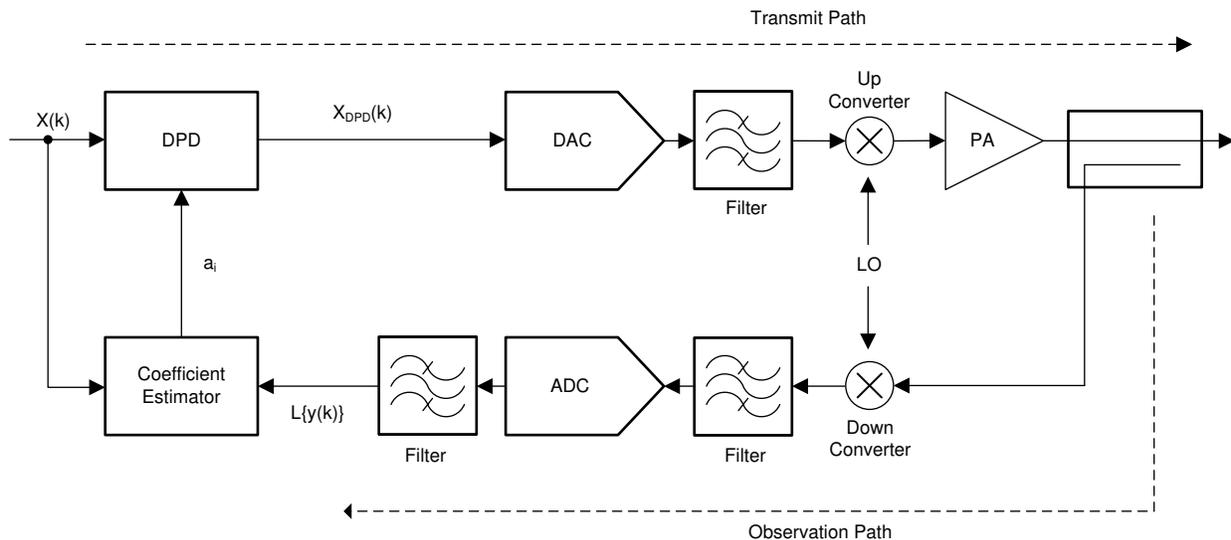


Figure 3-1. Basic DPD Building Blocks

3.2 Loop Analysis for DPD

In terms of mathematical negative feedback analysis, the forward path of the DPD has an incoming complex signal $X(k)$, and the signal goes through DPD correction to be pre-distorted based on the PA behavior. The pre-distorted signal is $X_{DPD}(k)$, and goes through the DAC, modulator, and then to the PA chain. The observation path is formed by a coupler from the PA output, and the observed path is down-converted and sampled by the ADC to feed into the coefficient estimator. The coefficient estimator basically measures the error between the $L\{y(k)\}$ and the forward path $X(k)$. Note that there are proper delay blocks to ensure that the input from $L\{y(k)\}$ and $X(k)$ are compared correctly at the right timing. The error signal is then used to update the values in the DPD coefficient. Moreover, the signal $X(k)$ is typically a known training signal with high auto-correlation profile for the DPD channel estimation phase. This estimation phase of the DPD loop may run periodically.

4 Implementation of DPD System with AFE77xx

The AFE77xx family consists of the necessary building blocks for any DPD system. Figure 4-1 shows the entire AFE77xx transmitter chain to be used as the forward path building block for the DPD and the entire AFE77xx feedback receiver chain to be used as the observation feedback path for the DPD. This diagram should help the system designer in terms of understanding the data paths of their DPD system utilizing the AFE77xx signal chain.

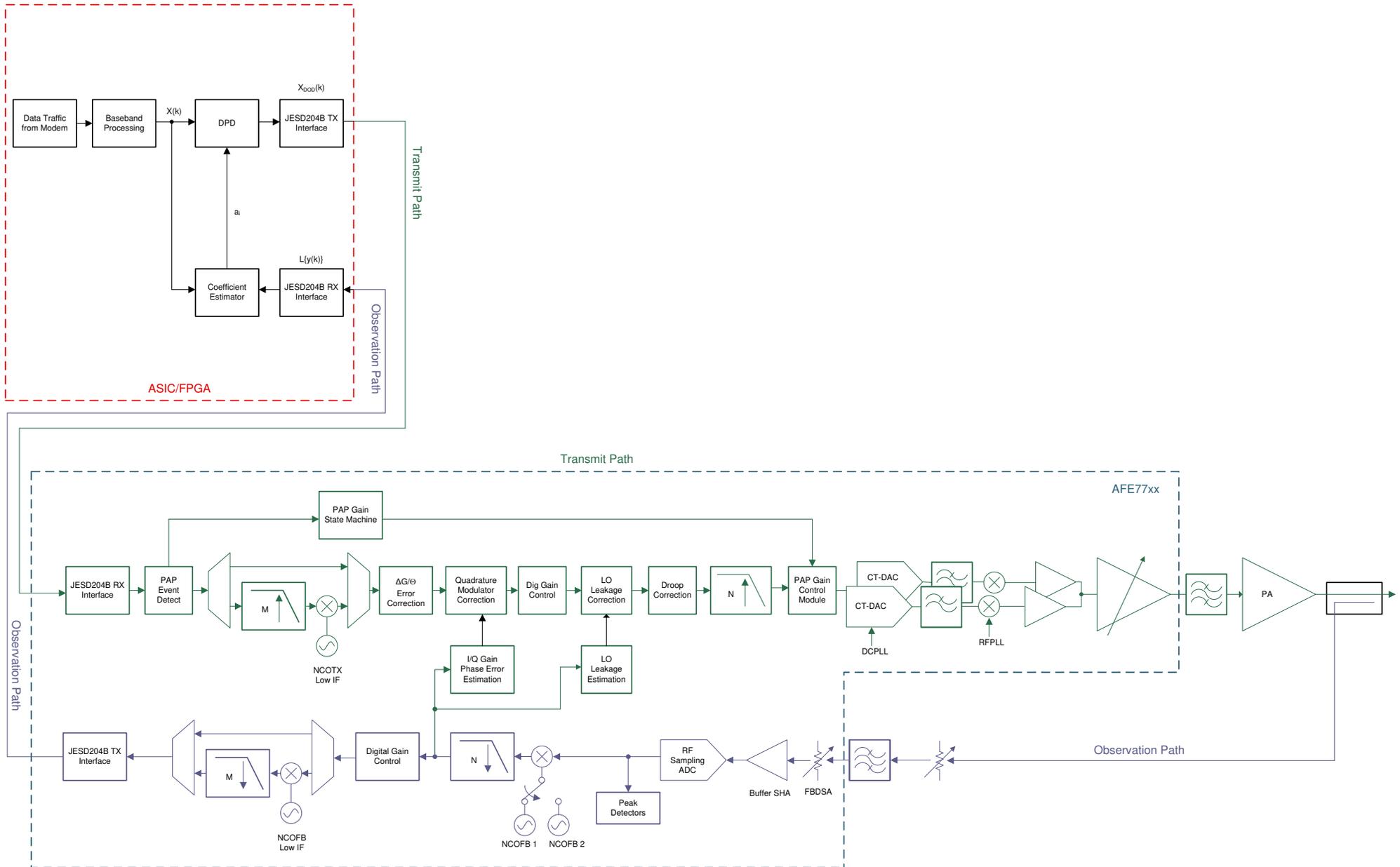


Figure 4-1. Total DPD Solutions Utilizing TI AFE77xx TX/FB Building Blocks

4.1 AFE77xx Transmitter Path Overview

The AFE7799 integrates four transmitter chains based on 0-IF architecture and its block diagram is shown in Figure 4-2. The analog portion of the transmitter chain includes two 14-bit, 3.4-Gsps IQ DACs, followed by a programmable reconstruction and DAC image rejection filter, an IQ modulator driving a wideband RF amplifier with 39-dB range gain control. The digital section of the transmitter chain includes several blocks that allow to interpolate and filter the signal from the supported input rates to the DAC clock rate and compensate for some impairments of the analog section (like LO leakage, IQ mismatch, DSA steps error).

The two IQ DACs can be configured to work in two different sampling rate modes: 48x (2949.12 Msps) and 54x (3317.76 Msps).

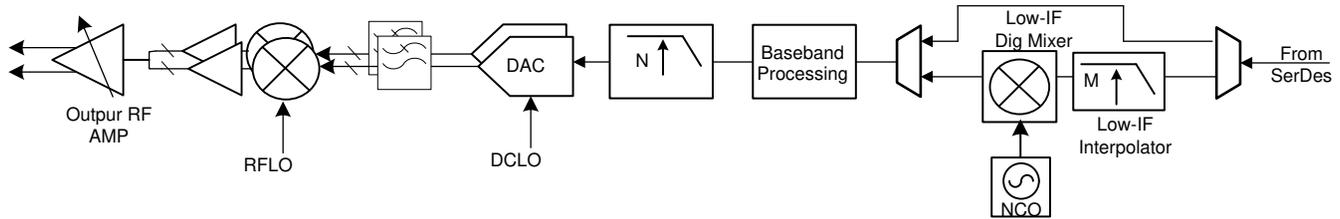


Figure 4-2. TX Chain Block Diagram

The digital section of the AFE7799 transmitter chain is shown in Figure 4-2. The input to the TX chain is a complex signal from the JESD block. The first function is the PA protection block, which can be used to monitor the input signal to check when input power manifests behaviors that could damage the power amplifier.

After the PA protection block, there is the low IF interpolation stage, followed by a low IF mixer with NCO. These blocks provide an increased sample rate so that the input signal can be offset in frequency for a low IF mode of operation. When a frequency shift is not used, these blocks can be bypassed.

The next block is the baseband processing functions. This includes gain control and compensation for analog components. The final digital block is the 2nd Interpolation stage, with the output of the signal going to the I/Q DACs.

The IQ mismatch compensation block is controlled by startup and real time tracking algorithms. It provides baseband frequency dependent sideband suppression and LO feed through compensation. The AFE7799 supports a mode where the host can control via a GPIO pin when the QMC coefficients are updated. When the mode is configured through the SPI, the estimator keeps calculating the correction parameters, but the QMC block coefficients are updated with the most recent ones only when the allocated pin (TXQMCEN) is set high. See Section 8 for details.

4.2 AFE77xx Feedback Observation Receiver Path Overview

The AFE7799 includes two feedback (FB) chains based on direct RF sampling architecture. Figure 4-3 shows the FB chain block diagram. The FB chain is normally used as an observation path of the power amplifier (PA) output for providing input to the external DPD engine. The direct sampling architecture offers an inherently wideband receiver chain and it simplifies the calibration of the TX chains impairments. The feedback path is composed of an analog, RF chain and a digital block.

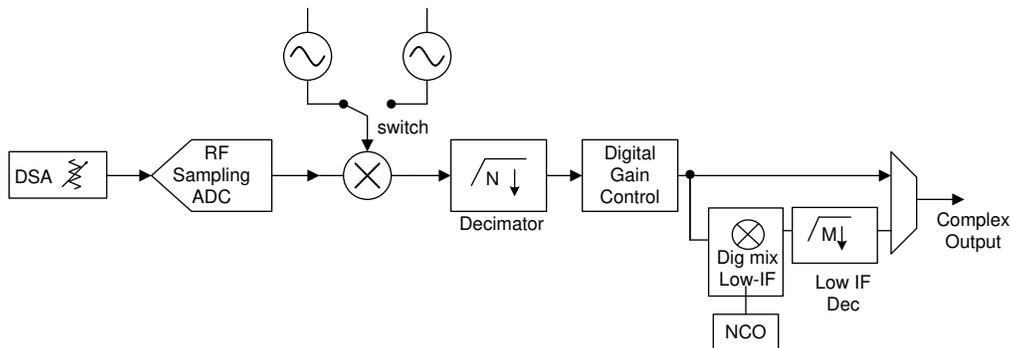


Figure 4-3. Feedback Path Block Diagram

The FB path analog block includes an input DSA and a RF sampling ADC.

The input DSA has a total of 16 dB of attenuation range with a resolution of 1 dB. The DSA attenuation is set via SPI.

The 14-bit RF ADC can be configured to work in two different sampling rate modes: 48x (2949.12 Msps) and 54x (3317.76 Msps).

The digital section of the AFE7799 feedback chain is shown in [Figure 4-3](#). The input to the FB digital section is a real RF signal from the FB ADC. The first function is a mixer to convert to a complex baseband signal. The mixer has two switchable NCOs, so for a dual band application, the NCO phase can be maintained when the other NCO is being used. Following the mixer is a decimation stage. The output of the decimation stage is used by the AFE7799 for the IQ mismatch correction engine, in parallel to the main signal path which goes to a digital gain block. That is followed by a low IF mixer with NCO, and then finally a second decimation state. These blocks are used to match the TX signal when it is offset in frequency for a low IF mode of operation. When a frequency shift is not used, these blocks can be bypassed. The advantage of using RF sampling ADC and digital downconversion stage for FB path is that the analog artifacts such as image and LO feedthrough are minimum by design and have little impact to the DPD estimation phase.

5 High Level Implementation of DPD System in AFE77xx

The general concept of a DPD is similar to any type of equalization control loop. The loop fundamentally have the following stages:

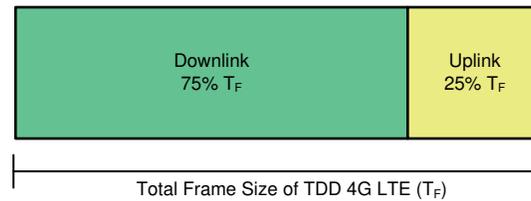
1. Generating a known training sequence for the loop. This training sequence must have very good auto-correlation characteristic. The transmitter forward path generates the training sequence, and the training sequence in this path has additive noise (inherent in any type of transmitter system) and also non-linearity added by the PA. The FB receiver receives this training sequence, along with FB receiver noise and non-linearity. The system compares the generated training sequence with the received training sequence with auto-correlation. The two need to have good auto-correlation in order for the training sequence to be detected properly.
2. The estimation phase involves auto-correlating the generated training sequence and received training sequence. The additional information besides the training sequence is the non-linearity factors of both the transmitter and FB receiver path, and overall noise. Assuming the process is random (white noise), the noise should have minimum impact to the estimation and auto-correlation process.
3. The loop applies the pre-distorted signal based on estimated non-linearity to the forward path. This pre-distorted signal then goes through the distorted signal chain and PA to achieve linearization.

The study of the DPD itself is beyond the scope of this application note. There are many industrial and academic studies that have more depth than this paper. To narrow down the scope of discussion, the following example of DPD application in typical time division duplex (TDD) system helps the readers focus on the utilities of the AFE77xx and the DPD application. A TDD system is a dynamic environment with transmit and receive channels are at the same or similar offset (TXLO, RXLO, and FB NCO at the same frequency), while the timing of the transmit and receive are staggered at some time offset (TX downlink [DL] at one time slot, and RX uplink [UL] at another time slot with some pre-defined duty cycle). This scenario of DPD application covers the planning of the DPD training sequence, timing of the estimation phase, and other various loops that may go on top of the DPD processing.

5.1 Overview of Time Domain Duplex Systems

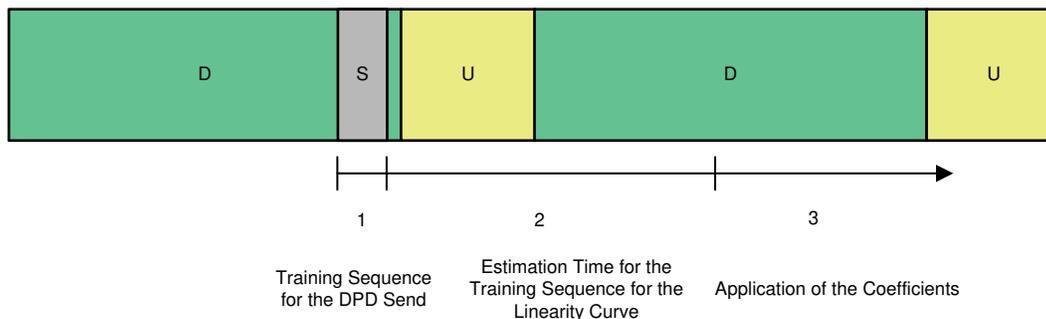
In a TDD condition (as shown in [Figure 5-1](#)), the DL is slotted for traffic transmitter active mode. During this time frame, the FB receiver can also be enabled for DPD loop estimation phase. The traffic receivers may not need to be active during this slot. Besides the DL time, the rest of the time is UL phase. In this phase, the traffic transmitters and the FB receiver may not need to be active. ¹

¹ In a typical 4G LTE TDD system, the typical DL time is about 75% of the total frame time, while the typical UL time is about 25% of the total frame time. This is driven mostly by the amount of data traffic flow is from the content provider to the mobile device. In the upcoming 5G system where mobile to mobile sharing traffic may increase, the DL to UL ratio may be closer to 50%.


Figure 5-1. Typical TDD Downlink/Uplink Ratio for 4G LTE

5.2 Training Sequence Generation

In typical communication protocol such as the 4G LTE TDD system, a time slot called the Special Slot can be utilized to send out the DPD training sequence. As shown in [Figure 5-2](#), the DL chain can use this time slot to transmit the training sequence needed for the DPD. The FB ADC can then capture the training sequence to perform the coefficient estimates. Finally, the DPD loop can apply the coefficients to achieve linearization.


Figure 5-2. Typical Estimation and Correction Phase for DPD Using Special Slot Setup

The same Special Slot can be used for other purposes in the radio system such as forward power observation, reflective power observation, and various other estimation needed in the DL chain. Similar to DPD, these other observation process can be done periodically.

5.3 Special TDD Features in AFE77xx

In AFE77xx integrated transceiver, external GPIOs are provided to switch the transmitter, feedback, and receiver between standby and active modes during TDD. The purposes for the TDD switching is two folds:

1. To activate only the necessary blocks in the perspective time slot, and place the unnecessary blocks into standby mode to reduce overall device power consumption. For instance, during DL time slot, the traffic receivers in the AFE77xx can be in standby mode. On the other hand, during UL time slot, the traffic transmitters and also the FB receivers can be in standby mode. TI designs the wake-up and standby times of the respective blocks to be within 2 μ s, less than the typical guard band for TDD conditions.
2. In the JESD204B/C serial link where both the traffic receivers and FB receivers have active SERDES transmitter lanes (STX1 to STX8), the STX lanes may be shared amongst the time slot to reduce the overall usage of high speed SERDES ports. This may reduce overall system cost by reducing the number of SERDES lane required.

[Table 5-1](#) shows the external GPIOs used in TDD mode on AFE77xx. There are five total GPIOs used to switch between downlink and uplink TDD modes: TXEN1, TXEN2, RXEN1, RXEN2, and 1FBEN.

Table 5-1. Device Status in TDD Mode

TDD MODE	TXEN1/TXEN2	RXEN1/RXEN2	1FBEN	TRANSMITTER MODE	RECEIVER MODE	FEEDBACK MODE
Downlink	1	0	1	Active	Standby	Active
Uplink	0	1	0	Standby	Active	Standby

The control of the TDD GPIOs is not mutually exclusive so it is possible for uplink and downlink modes to be in standby or active at the same time. For instance, in some special applications where the overall traffic is low

(that is during night time in remote areas, some channels in the radio can to be placed in power consumption saving mode).

Regarding potential savings of the overall high speed SERDES port count, the FB and RX ADCs can time share the SERDES lanes to minimize SERDES resource usage in the FPGA and AFE77xx. The information on the SERDES lanes can be dynamically switched between Feedback and Receiver ADCs depending on the state of RXEN1/RXEN2 and 1FBEN GPIOs. This is summarized in [Table 5-2](#).

Table 5-2. RX/FB State vs. GPIO

RXEN1/RXEN2	1FBEN	RX CHAINS	FB CHAIN	SERDES LANES TO
1	0	On	Off	RX
0	1	Off	On	FB
1	1	On/Off	On/Off	RX/FB ²
0	0	Off	Off	

6 Latency of the TX/FB

Digital pre-distortion estimation and calibration require known latency from the transmitter chain to the feedback observation chain. By design, the JESD204B/C standards supported by the AFE77xx have deterministic latency in both the transmitter and feedback path. To be exact, upon every start-up of the AFE77xx, the transmitter and feedback data path has precise delay. The startup process includes the powering-up of the device, reset of the device, programming of the device, and also the JESD204B/C handshaking processes.

Additionally, the AFE77xx has the following features to aid the DPD implementation:

6.1 Delay Block in the TX Chain

A programmable delay of the incoming signal is available in the TX chain of the AFE77xx. The programmable delay is split into coarse and fine delay. The coarse delay is within the interpolation chain, and has a resolution of $T_{in}/2$, where $T_{in} = 1/F_{in}$, or interface sampling rate. The coarse delay can be programmed in the range of 0 to 4 $T_{in}/2$ via 3-bit SPI register.

The fine delay block is at the output of the interpolation filter. It can be configured in integer multiples of the DAC clock period up to 31 clocks via a dedicated 5-bit SPI register. The delay is applied simultaneously to both I and Q path (complex) and is possible to program different delays for each TX chain.

6.2 TXLO and FBNCO Frequency Offset

While the DPD is running, the frequency offset between the TXLO and FBNCO must be maintained to prevent phase accumulation error and latency error. The FB ADC digital mixer and NCO can have synchronized frequency offset with respect to the TX modulator and TXLO under the following conditions:

1. FB ADC has two independent NCOs to match two different TXLO frequency for dual band case or to sample two different bands.
2. If the reference clock to the AFE77xx (reference clock for the DC-PLL and RF-PLL) are multiples of 61.44 MHz (that is $F_{ref} = N * 61.44$ MHz), then the FB ADC NCO can have exact raster frequency of 1 kHz. If the RF-PLL for the TXLO can have fractional mode in 1 kHz raster, then the frequency offset between the TX and FB can be zero.

7 Feedback Anti-Aliasing Filtering

As the feedback path of the AFE77xx is based on RF sampling architecture, any spectral power that are Nyquist multiple of the in-band signal aliases into the in-band signal. Therefore, to facilitate DPD algorithm and also the AFE77xx internal TXQMC algorithm, the feedback path must have anti-aliasing filtering.

[Figure 7-1](#) shows the simplified portion of the TX and FB block. As highlighted in the introduction, the TX portion consisted of direct upconversion circuits with the typical baseband DAC and analog modulators, while the FB portion is the RF sampling ADC circuits. The nodes highlighted here are the baseband DAC output for the in-phase signal (I) and quadrature signal (Q), the modulator output of baseband to RF, and the sampled data of the RF sampling ADC.

² (1,1) case as (1,0) or (0,1) based on a programmable SPI configuration

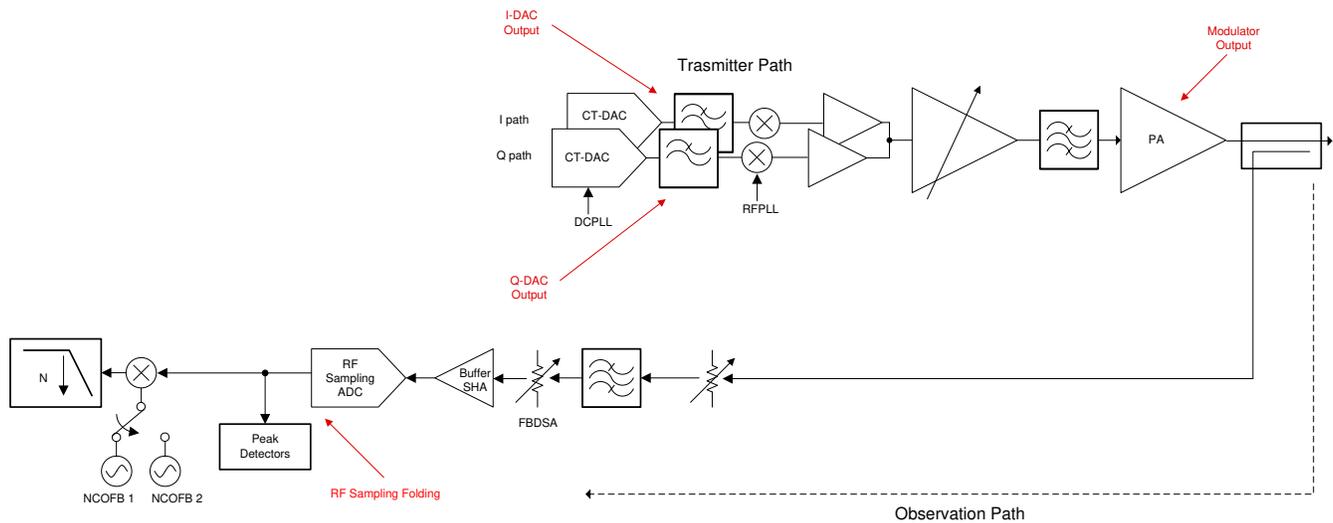


Figure 7-1. DAC Output, Modulator Output, and RF Sampling ADC Input Stages for Analysis of Image Filter Requirements

The DAC output on either the I or the Q path can be analyzed as shown in the frequency spectrum in Figure 7-2. The baseband signal to be upconverted is shown in dark green. Since the DAC is also a sampler, there are Nyquist images located at multiples of the Nyquist frequency (that is $F_{S_DAC}/2$ frequency). Although there is baseband output filtering, the filtering is not the ideal brickwall filtering and there is some remnant power. The dark red is the image of the baseband signal with symmetrical amplitude and phase information as the baseband. The light red is the folded image with flipped amplitude and phase information (180° out of phase).

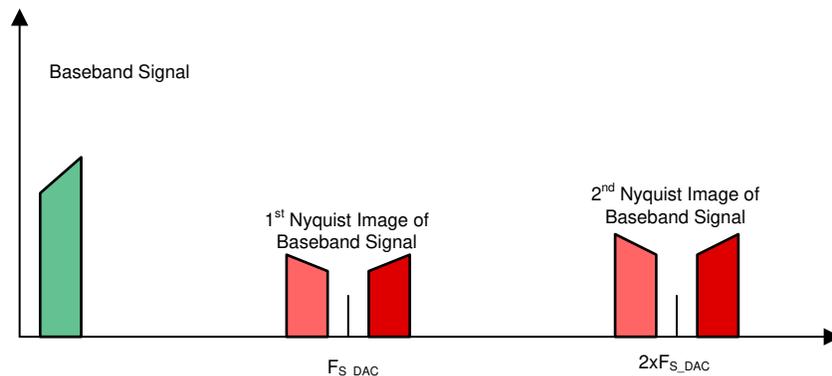


Figure 7-2. DAC Output Spectrum

The I and Q signal then goes through upconversion through the modulator path. Through LO mixing, the final RF spectrum is shown in Figure 7-3. The dark green is the modulated waveform, while the light green is the image artifact due to the imperfect quadrature mixing of the analog component. There is also some slight LO feedthrough due to the DC offsets in the mixing process. Both the image artifact and LO feedthrough can be corrected by the TXQMC algorithm.

If the bandwidth of focus is near the signal of interest at the LO frequency, Figure 7-3 shows two additional area that impact feedback performance.

1. Straight mixing of the 1st Nyquist image and TXLO: This is in reference to the first Nyquist image of the baseband signal centered at F_{S_DAC} as shown in Figure 7-2. Basically, the first Nyquist image of the DAC output is directly modulated to RF with LO mixing. Therefore, the 1st Nyquist image is now located at center of $F_{S_DAC} + F_{LO}$.
2. Image due to mixing of 2nd Nyquist image and TXLO: This is in reference to the second Nyquist image of the baseband signal centered at $2xF_{S_DAC}$ as shown in Figure 7-2. With the LO mixing, there is a primary modulated signal locate at $2xF_{S_DAC} + F_{LO}$ (this is not shown for simplicity), and there is an image located at $2xF_{S_DAC} - F_{LO}$ due to the imperfect quadrature mixing.

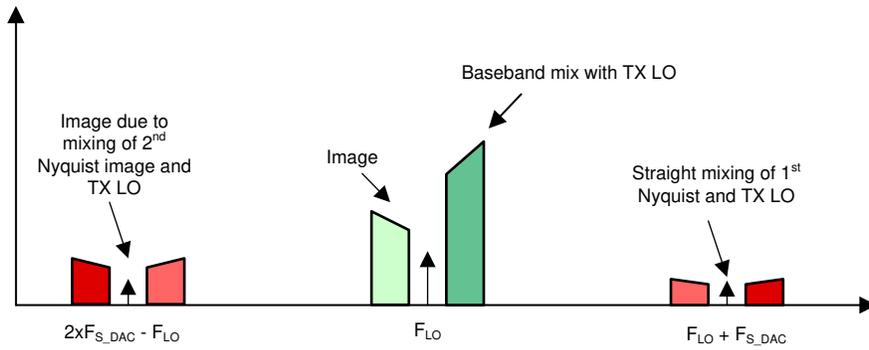


Figure 7-3. Modulator Output Spectrum

The impact of these images (or images of an image) is highlighted in Figure 7-4. First, since the FB ADC sampling rate at F_{S_ADC} is typically set at the same rate as baseband DAC sampling rate at F_{S_DAC} , these images are folded within the Nyquist bandwidth of the FB ADC. Moreover, since the FB NCO is set to be the same as the TXLO, these images fold in-band within the decimation bandwidth of the FB ADC path. All the folding of the images (or images of an image) on top of the actual baseband signal creates problems during the estimation phase of both DPD and TXQMC algorithms. Therefore, TI recommends sufficient bandpass filtering around the in-band signal for best DPD and TXQMC performance.

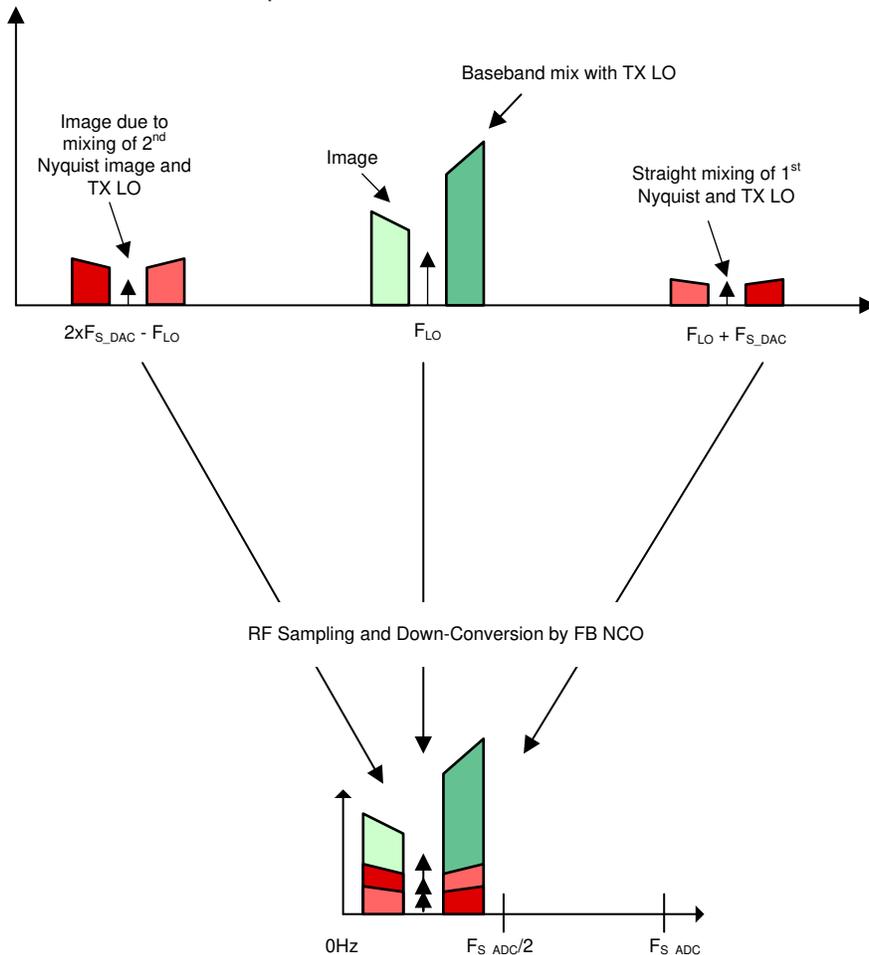


Figure 7-4. Folding of the Images Due to TXLO Image and RF Sampling

1. A low pass filter is generally not suitable within the feedback path.
2. $F_{S_DAC} - F_{LO}$ spur and $3x F_{S_DAC} - F_{LO}$ generally appear at low frequency or at very high frequency for 1.8 GHz, 2.4 GHz, or 3.5 GHz band of signals.

3. As F_{LO} approaches to 4.5 GHz, $3xF_{S_DAC}-F_{LO}$ and F_{LO} appear nearby. Additional adjustment such as sample rate F_{S_DAC} or F_{S_ADC} adjustment may be necessary.

8 TX Quadrature Modulator Correction (QMC) Interaction

The DPD estimation and adaptation may also occur in parallel to the TX QMC and LO leakage convergence. The system engineer should allow a dedicated time window during the initial convergence of QMC and LO leakage correction, which typically takes about 50 ms. In this dedicated time window, the DPD adaptation can be kept frozen. Similarly, TI recommends that during initial DPD convergence, the TX QMC and LO leakage estimation to be frozen. Once the initial DPD convergence is completed, the TX QMC and LO leakage correction can be updated at a much faster rate. This is also known as autonomous TXQMC phase and typically takes about 10 ms to complete.

The DPD loop time is highly dependent on the basis of DPD algorithm estimation. Assuming the time needed for DPD adaptation is in the order of 100 ms to achieve good linearity performance, the time window of TX-FB connection for TX QMC and LO leakage can be aligned with the DPD adaptation time window as shown in Figure 8-1. This can avoid allocating dedicated time window for QMC and LO leakage tracking calibration.

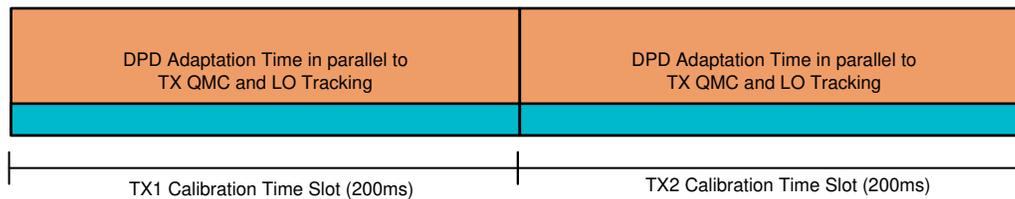


Figure 8-1. TXQMC Runtime in Parallel with DPD

The AFE77xx also supports the mode where the DPD adaptation and QMC/LO tracking are done in separate dedicated time windows. This may be more suitable for systems where multiple calibrations are required (that is DPD adaptation, output power observation, reflective power observation, and so forth) to be done periodically for a particular TX path to track time and temperature variations. Assuming that a time window of 200 ms is periodically allocated for all calibrations required of a particular TX chain, system engineers can keep a dedicated time window of 30 ms by maintaining the TX-FB pair connection in a time window of 200 ms to enable the QMC and LO leakage to track time and temperature variations. However, to maintain the uniform calibration scenario between the TXQMC initial convergence phase and the tracking phase, TI recommends to keep the TX-FB pair connection dedicated to QMC and LO leakage tracking for a period of at least 50 ms in a time window of 200 ms as shown in Figure 8-2.³

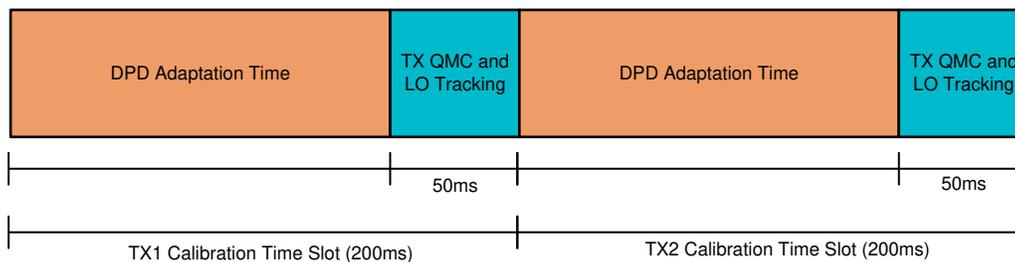


Figure 8-2. Dedicated TXQMC Time Slot and Dedicated DPD Adaptation Time Slot

During the TX QMC and LO leakage tracking, the correction coefficients are periodically updated. The design of coefficient update is glitch free. However, if required by application, the AFE7xx also supports a mode in which the QMC and LO leakage algorithm continues to estimate the coefficients in the background, but updates the coefficients only if an additional GPIO is enabled as shown in Figure 8-3. This mode of updating the data path coefficients based on the additional GPIO is termed as "Host-Triggered Update Mode". In the Host-Triggered Update Mode, once the additional GPIO is triggered, the TX QMC and LO leakage coefficients for the four TX channels updated after 200 μ s.

³ During the initial time of TX QMC tracking, the algorithm tracks from the uncorrected quadrature mismatch and LO leakage levels. The initial QMC tracking time is about 50 ms. The autonomous estimate and coefficient update after the initial QMC tracking is in the order of 10 ms.

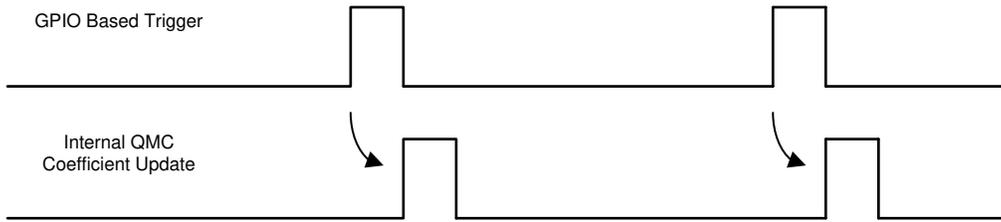


Figure 8-3. Internal TXQMC Coefficient Update Utilizing External GPIO Based Trigger

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2019) to Revision B (August 2021) Page

- Updated the numbering format for tables, figures and cross-references throughout the document..... 1
-

Changes from Revision * (April 2019) to Revision A (July 2019) Page

- Edited the abstract..... 1
 - Edited [Section 2](#) 3
 - Edited [Section 4.1](#) 8
 - Edited [Section 4.2](#) 8
 - Edited [Section 5](#) 9
 - Edited [Section 5.3](#) 10
-

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