Application Brief

Ultra-Low-Noise JFET Preamplifier Design for High Impedance Sensors

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Introduction

Sensors with a high source impedance can be purely resistive, capacitive, inductive or a combination of the three. High source impedance sensors that produce small signals on the order of a few thousandths of a volt often require amplfication from a low noise and high input impedance pre-amplifier. Amplifiers with bipolar junction transistor (BJT) input stages are popular for the low voltage noise characteristics. BJT devices typically have higher current noise compared to the complementary metal-oxide semiconductor (CMOS)-input and junction field-effect transistor (JFET)-input counterparts. When paired with high source impedance sensors, the current noise from BJT input stages translates into an increase of additional voltage noise. Using a complementary metal-oxide semiconductor (CMOS) device is a good choice for a high input impedance; however, the noise performance is worse than that of a bipolar input. The discrete junction field-effect transistor (JFET) has better 1/f noise performance than the CMOS device and also has high input impedance. More details are found in the *Trade-offs Between CMOS, JFET, and Bipolar Input Stage Technology* application report. This application brief discusses how to interface high source impedance sensors with high current noise BJT instrumentation amplifiers using discrete matched JFETs. Two preamplifier topologies are compared in this application brief with analysis of trade-offs and how to decide when to use one topology over the other.

Preamplifer Topologies

Figure 1 shows a preamplifier topology using the INA849. The INA849 is biased with a single supply of 12V. The OPA145 outputs a mid-supply DC voltage of 6V and drives the reference pin R_{ef} and the input common mode voltage of the INA849. The INA849 has a BJT input stage with ultra low voltage noise. BJT input stages are popular choices for the low voltage noise characteristics. When paired with high source impedance sensors the current noise from BJT input stages translates into an additional voltage noise.

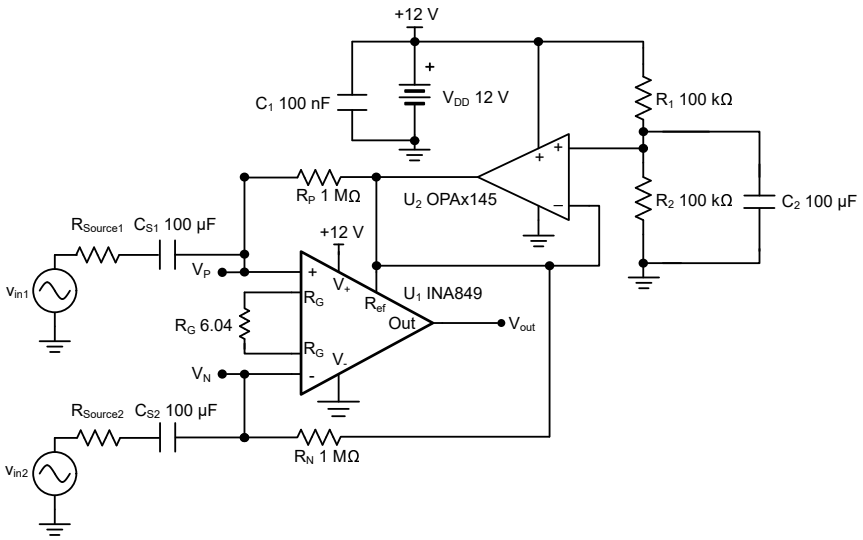

Figure 1. INA Preamplifier

A discrete JFET such as TI's JFE2140, when followed by a bipolar instrumentation amplifier such as the INA849, offers a way to achieve high input impedance and low noise with flexible biasing, see Figure 2. The JFETs Q_{1A} and Q_{1B} are each configured in a source follower configuration and replace the front end of the INA849. The INA849 is configured in a gain of 60dB. Source impedances $R_{source1}$ and $R_{source2}$ are now connected to the high input impedance and low current noise discrete JFET front end. The discrete JFET and INA preamplifier circuit offers the low input current noise of the JFETs and the low voltage noise of the INA.

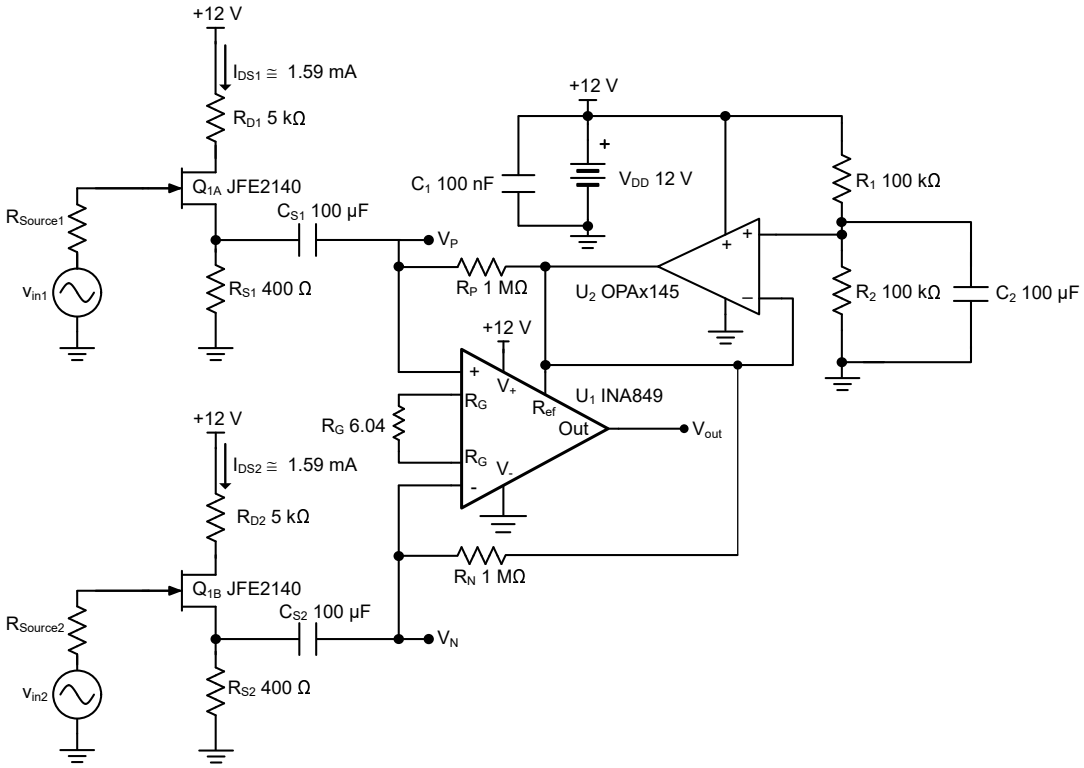

Figure 2. Discrete JFET and INA Preamplifier

Noise

Figure 3 shows noise performance comparisons between the two preamplifier topologies shown in Figure 1 and Figure 2 with various source impedances R_{source}. With low source impedance sensors the INA849 outperforms the JFET design. As R_{source} increases the preamplifier shown in Figure 2 outperforms the INA849 alone.

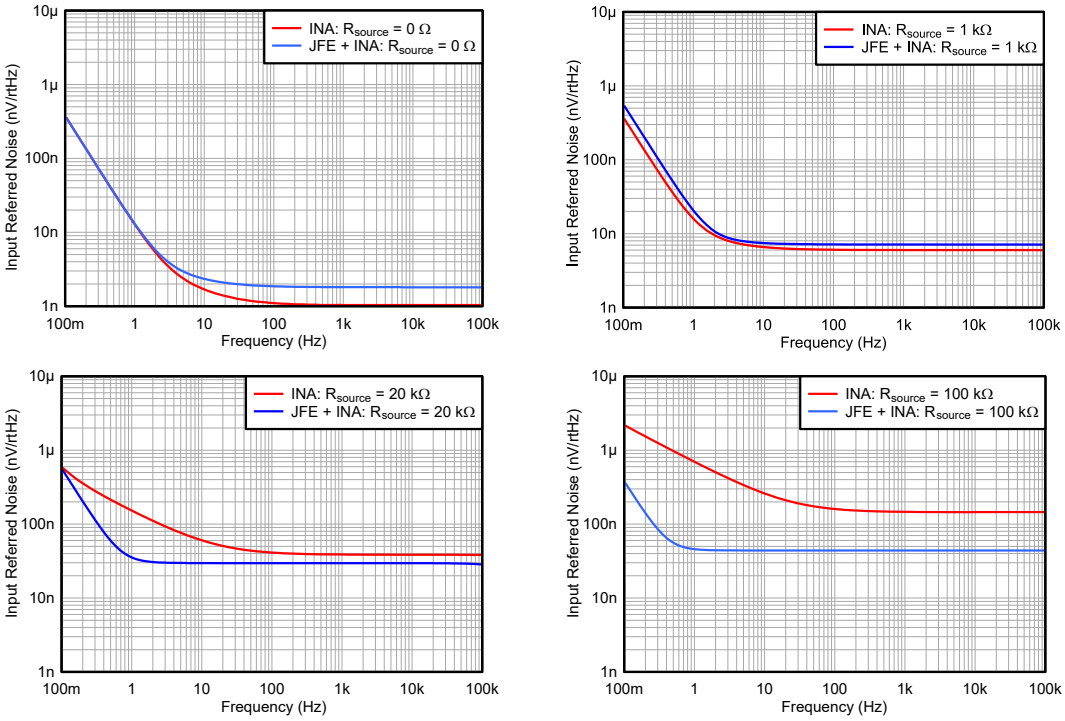

Figure 3. Preamplifier Noise Comparison with Various Source Impedances

Table 1 shows the total circuit current consumption and noise tradeoffs between the two preamplifier topologies. The total current consumption from the design shown in Figure 1 is 6.71mA. The total current consumption of the JFET front end design shown in Figure 2 is 9.88mA. This represents a 47.2% increase in total current consumption. The addition of the discrete JFETs improves the noise performance by reducing the input referred broadband noise by -64.4% when using a source impedance of R_{source} = 100kΩ. Figure 3 shows the improvement in the $\frac{1}{f}$ noise when using the JFET + INA849 topology paired with high source impedances.

Table 1. Preamplifier Topology Comparison

Preamplifier Topology	Total Iq (mA)	Percent Increase in Iq	Total Voltage Noise $\left(\frac{nV}{\sqrt{Hz}}\right)$ Input Referred f = 1kHz	Percent Decrease in Voltage Noise R_{source} = 100kΩ
INA849	6.71	-	162.07	-
JFET + INA849	9.88	47.2%	57.63	-64.4%

When deciding to use one of the two topologies shown in Figure 1 and Figure 2 a simple calculation is used. In general if $R_{source} > \frac{4kT}{(i_n)^2}$ the use of the JFET input devices results in lower noise. Additional detail can be found in the application note Impact of Current Noise in CMOS and JFET Amplifiers. The INA849 has a typical current noise specification of $i_n = 1.1 \frac{pA}{\sqrt{Hz}}$.

$$R_{source} > \frac{4 \times 1.38 \times 10^{-23} \times (273.15^{\circ} + 25)}{\left(1.1 \times 10^{-12}\right)^2} \quad (1)$$

$$R_{source} > 13.6\ k\Omega \quad (2)$$

When R_{source} = 13.6kΩ, Table 2 shows that $e_{nR} = e_{ni\_INA}$ = 21.16 (nV/√Hz). Following this guidance there is a $\sqrt{2}$ improvement in noise when using the discrete JFET and INA preamplifier from Figure 2.

Table 2. Source Impedance and Calculated Noise Comparison

R_{source}(Ω)	e_{nR} (nV/√Hz)	e_{ni_INA}(nV/√Hz)	INA Calculated Total Input Referred Noise $e_{n\_Total\_INA}$(nV/√Hz)	JFET + INA Calculated Total Input Referred Noise $e_{n\_Total\_JFET\_INA}$(nV/√Hz)
100	1.81	0.16	2.08	2.56
500	4.06	0.78	4.25	4.44
1000	5.74	1.56	6.03	6.01
1,360	6.69	2.12	7.09	6.93
5,000	12.83	7.78	15.04	12.95
10,000	18.14	15.56	23.92	18.23
13,600	21.16	21.16	29.94	21.23
50,000	40.57	77.78	87.73	40.61

The values in Table 2 are calculated using Equation 3 through Equation 6 where the values shown in Table 3 are used.

Table 3. Table of Values

Value	Description
$k_B = 1.38 \times 10^{-23}\ JK^{-1}$	Boltzmann Constant
$T = 298.15\ K$	Temperature in Kelvin
$e_{n\_JFET} = 1.5 \frac{nV}{\sqrt{Hz}}$	Broadband Voltage Noise of JFE2140 Biased at 1.59mA, f = 1kHz
$e_{n\_INA} = 1 \frac{nV}{\sqrt{Hz}}$	Broadband Voltage Noise of INA849 G = 60dB, f = 1kHz
$i_n = 1.1 \frac{pA}{\sqrt{Hz}}$	Broadband Current Noise of INA849 G = 60dB, f = 1kHz

The preamplifier topologies have balanced inputs. For this reason a $\sqrt{2}$ factor is used in Equation 3 and Equation 4.

$$e_{nR} = \sqrt{2}\sqrt{4k_B T R_{Source}} \quad (3)$$

$$e_{ni\_INA} = \sqrt{2} R_{Source} i_n \quad (4)$$

$$e_{n\_Total\_INA} = \sqrt{{e_{nR}}^2 + {e_{ni\_INA}}^2 + {e_{n\_INA}}^2} \quad (5)$$

$$e_{n\_Total\_JFET\_INA} = \sqrt{{e_{nR}}^2 + {e_{n\_INA}}^2 + {e_{n\_JFET}}^2} \quad (6)$$

Design Considerations

Discrete JFETs offer bias flexibility by adjusting the drain to source voltage V_{DS} and gate to source voltage V_{GS}. A few key JFET biasing considerations can be made when designing the preamplifier topology shown in Figure 2. Figure 4 shows the drain to source current I_{DS} vs V_{DS}. Bias the JFETs with sufficient V_{DS} to operate in the saturation region.

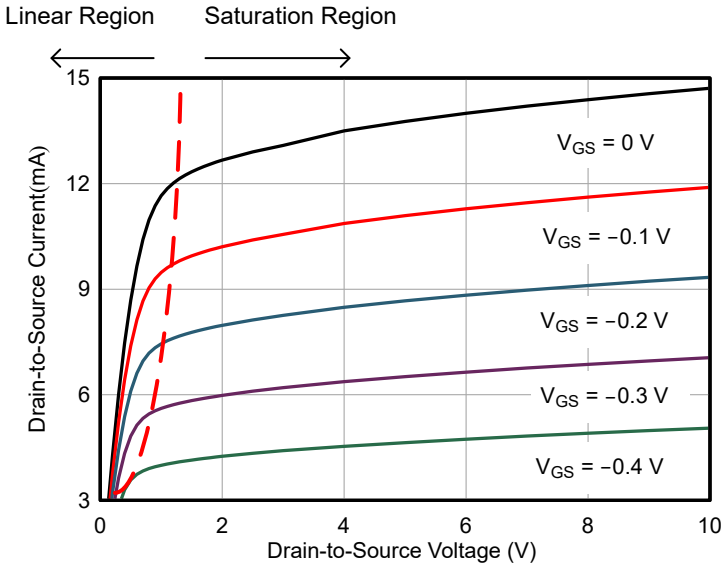

Figure 4. I_D vs V_{DS}

Figure 5 shows I_G vs V_{DS}. Bias V_{DS} such that the gate current is lower than the INA849 bias current.

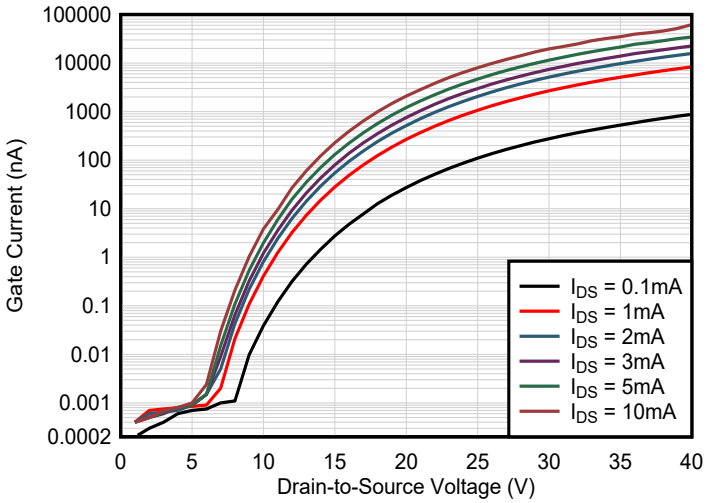

Figure 5. I_G vs V_{DS}

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