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FREQUENCY-TO-VOLTAGE CONVERSION

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Precision frequency-to-voltage converters (FVC)s can be made using voltage-to-frequency converters (VFCs). Burr-Brown offers a complete line of precision free-running VFCs.

VFC110 High frequency, low jitter VFC
4MHz max full-scale, ±0.02% typ linearity at 2MHz

VFC121 Precision single-supply VFC (+4.5V to +36V)
1.5MHz max full-scale, 0.03% max nonlinearity at 100kHz

VFC320 Precision VFC
1MHz max full-scale, 0.005% max nonlinearity at 10kHz

This bulletin describes three techniques for making a precision FVC using a VFC. The standard technique has high precision, but high ripple or slow settling. Adding an output filter can improve the settling-time, ripple trade-off, but adds error. A third new technique can eliminate ripple from the FVC output and improve settling time by more than 1000/1 as compared to the conventional FVC. Moreover, the DC precision is unaffected.

FVC APPLICATIONS

A rapidly-growing application for frequency-to-voltage converters is high-voltage analog signal isolation. High-voltage analog isolation amplifiers (ISO Amps), such as the Burr-Brown ISO121, are available for isolating signals up to 8000V. Higher voltage isolation of tens-of-thousands or even millions of volts as in utility-power-transmission line monitoring, nuclear event monitoring, and protection from lightning strikes calls for other techniques. You can get virtually unlimited isolation by using a voltage-to-frequency converter (VFC) to digitize an analog signal and transmit it over a fiber-optic data link to a FVC where the signal is reconstructed.

Many times VFCs are favored for analog-to-digital conversion because of their integrating input characteristic and high resolution (modern Sigma-delta analog-to-digital converters are really a variation of a VFC with digital filtering and encoding). An analog signal digitized by a VFC can be transmitted to a remote receiver serially over a single twisted pair wire cable or isolated with a single optical isolator. At the other end, the digital signal can be both

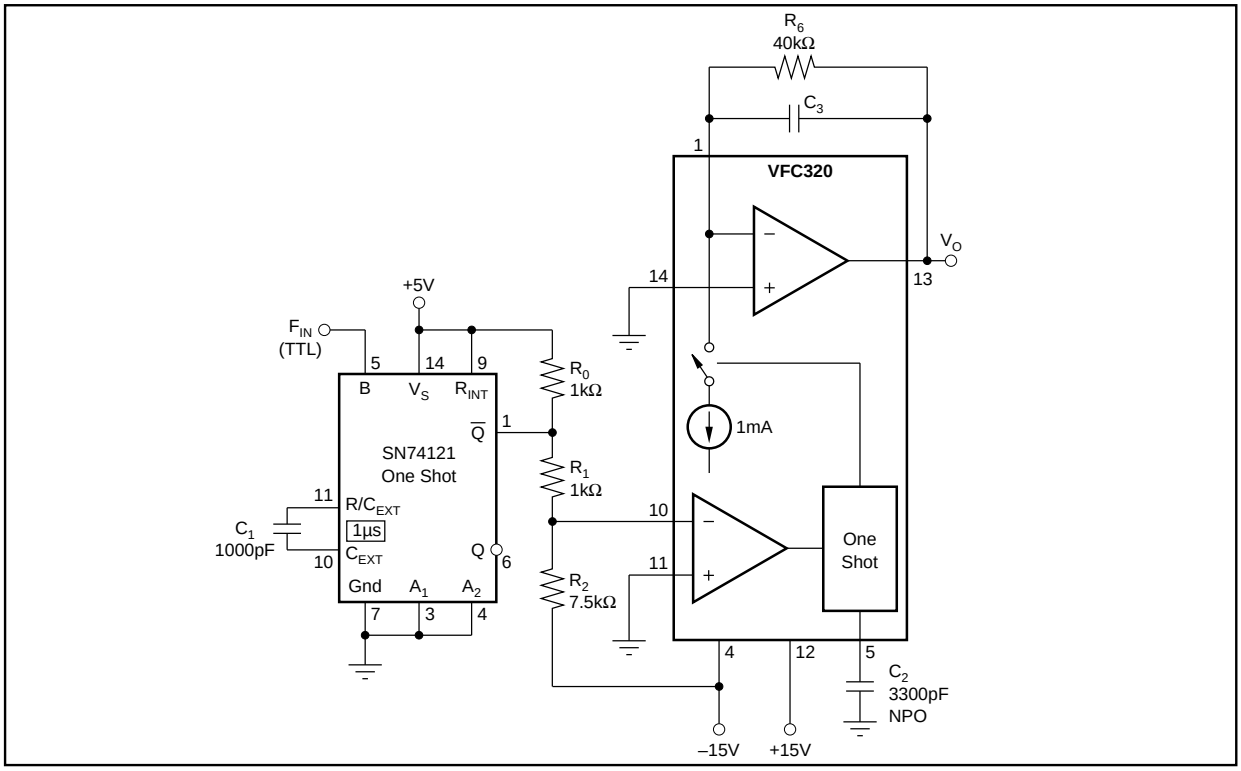

FIGURE 1. A Conventional Frequency-to-Voltage Converter. This FVC can be made by connecting a Burr-Brown VFC320 voltage-to-frequency converter in the FVC Mode. Select C_3 for ripple/settling-time trade off.

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digitally processed and reconstructed to analog. An analog signal is often required, as in medical applications, for bedside monitoring on a CRT or LCD display. The fast-settling, ripple-free characteristics of the FVC described here makes it ideal for this application too.

THE CONVENTIONAL FVC

In an conventional FVC, a one-shot-controlled current reference is averaged. A serious problem with the conventional FVC results from a trade-off between ripple and settling time. Improved resolution from the FVC demands low ripple, but decreasing the ripple increases settling time.

An example of a conventional FVC circuit is shown in Figure 1. It uses a Burr-Brown VFC320 voltage to frequency converter connected in the FVC mode. The SN74121 one shot along with input resistors, R_1, R_2, and pull-up resistor R_0 convert a TTL-logic-level input into a 1µs negative-going pulse to trip the ground-referenced comparator in the VFC320. When tripped, the comparator triggers a precision one shot in the VFC320. When triggered, a 1mA current reference in the VFC320 is switched to the input of an averaging transimpedance amplifier for the period of the one shot.

The transimpedance amplifier can be thought of as an integrator consisting of an op amp in the VFC320 with an external integrating capacitor, C_3. A current proportional to the integrator output voltage is summed in through feedback resistor, R_6. Both the periodic 1mA current pulse and the current through R_6 are integrated in C_3. The average voltage at the output of the integrator is proportional to the input frequency, the precision one-shot period, the current reference, and the external feedback resistor, R_6.

The duration of the one-shot period is determined by the external one-shot capacitor, C_2. In this example, the one-shot pulse-width is set at 25µs for a full-scale FVC input range of 10kHz. It has been empirically determined that best VFC or FVC linearity is obtained when the one shot pulse width is approximately 25% of the full-scale input period.

The integrator output ramps up during the one-shot period, integrating the sum of the 1mA current source and the current through the feedback resistor. Then, the one-shot output ramps down during the balance of the input frequency period, integrating only the current through the feedback resistor. The peak-to-peak value of this ramp appears at the FVC output as ripple.

The value of the integrator capacitor affects the FVC output ripple, but does not affect the average DC output voltage. Increasing the value of the integrator capacitor decreases the voltage ripple, and increases the time for the integrator output to settle for a change in input frequency. Settling time follows a single pole response. The following relationships apply for the conventional FVC:

$$V_O = F_{IN} \bullet T_{OS} \bullet I_R \bullet R_6$$

(same for conventional and fast-settling FVC)

$$\text{RIPPLE} \approx T_{OS} \bullet I_R / C_3$$

$$t_S = R_6 \bullet C_3 \bullet \ln\left(\frac{100\%}{P\%}\right)$$

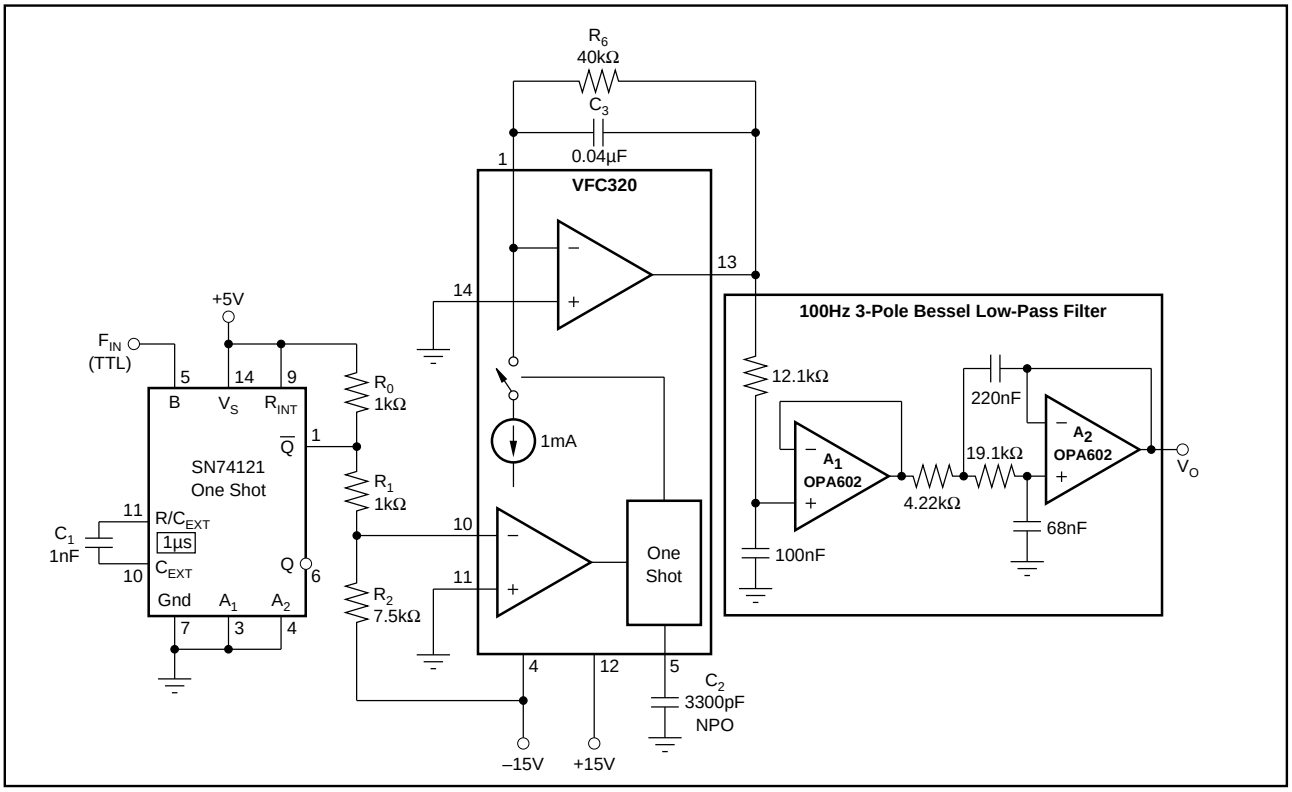

FIGURE 2. A Conventional Frequency-to-Voltage Converter. This converter with a 3-pole low-pass Bessel filter added to the output has less than 1mV ripple at 1.2kHz and can settle to 0.01% in 18ms.

Where:

V_O = Average output voltage [V]

F_{IN} = Input frequency [Hz]
(10kHz full-scale in this example)

I_R = Current reference [A]
(1mA for the VFC320)

T_{OS} = One-shot period [s]
(25µs in this example)

t_S = time for the output to settle to desired tolerance [s]

R_6 = Integrator feedback resistor [Ω]
(40kΩ for 10V full scale output with 10kHz input)

RIPPLE = Variation in V_O [Vp-p]

C_3 = Value of integrator capacitor [F]

P = Desired precision of the output signal
[% of full-scale]

CONVENTIONAL FVC PERFORMANCE

The conventional FVC has excellent DC performance, but poor dynamic performance. For example, consider an FVC with 10V full-scale output for 10kHz input. Using the VFC320 voltage-to-frequency converter with I_R = 1mA and T_{OS} = 25µs, R_6 must be 40kΩ. In the conventional FVC, for 0.01% resolution (1mV ripple), C_3 must be set to 25µF and settling time is an astoundingly long 9.2s.

FILTERING THE CONVENTIONAL FVC

In practice, the settling-time/ripple trade-off of the conventional FVC can be improved substantially by filtering the FVC output with a higher-order low-pass filter as shown in Figure 2. In this approach, a conventional FVC is designed with relatively high output ripple to give fast settling time. Then a high-order low-pass filter is added in series with the FVC output to reduce the ripple.

In the Figure 2 example, a value of 40kΩ was used for R_6 to set a 10V full-scale output for a 10kHz input. A value of 0.04µF is used for C_3 giving approximately 625mV max ripple. This is an arbitrary but adequate value to give excellent linearity and a 10V full-scale output. Higher ripple would reduce the linear output range of the FVC because, at full-scale output, the FVC must swing 10V plus approximately one half the ripple voltage.

There are many output filter possibilities for a filtered FVC. Because of its excellent pulse response a Bessel filter gives the fastest settling of any standard filter type. The tables below show examples of FVC performance for Bessel filters of order 2 through 5. The 3-pole Bessel filter gives a good settling-time complexity trade-off. Figure 2 shows the conventional FVC with a 3-pole Sallen-Key Bessel filter. With the filter f_{-3dB} frequency set to 100Hz, ripple at 1.2kHz is below 1mV and settling time to 0.01% is 18ms. Notice that ripple increases dramatically below 1.2kHz when higher-order filters are used.

The Sallen-Key filter architecture, used for the low-pass filter, was selected for low gain error. You can't include the filter in the feedback loop because the excessive phase-shift would cause instability. Since the filter must be added outside the integrator feedback loop, DC errors such as gain offset and offset drift add to the transfer function of the FVC.

FILTERED FVC PERFORMANCE WITH BESSEL FILTER

FILTER ORDER	f-3dB (Hz)	SETTLING (0.01%) (ms)	RIPPLE (at 1.2kHz) (mV)	RIPPLE (at 400Hz) (mV)
2	35	38	1	8
3	100	18	1	25
4	155	17	1	59
5	205	17	1	134

In the unity-gain Sallen-Key architecture, the op amps are connected as voltage-followers so gain error is negligible. You still must use low-drift precision op amps to reduce offset and offset drift errors.

Other active filters can be designed with easy-to-use DOS-compatible programs available free of charge from Burr-Brown—request the FilterPro™ filter design software. These programs make it easy to design a wide variety of practical Sallen-Key, Multiple Feedback (MFB), and State-Variable active filters up to tenth order. State-Variable active filters use the UAF42 monolithic Universal Active Filter which contains on-chip precision capacitors so that external capacitors are not required.

The filtered FVC gives a good improvement in settling time. However, even with the complexity of a 3-pole filter, its performance pales in comparison to the fast-settling FVC. Filtering, with a 3-pole filter, can give 18ms settling to 0.01% with less than 1mV ripple at 1.2kHz, but ripple increases at lower frequencies. For comparison, the new fast-settling FVC, using the same R_6, C_3 values, settles to 0.01% in 7.4ms with less than 1mV ripple at any frequency.

THE NEW FAST-SETTLING FVC

Instead of using a filter in series with the output, the fast-settling FVC uses a sample/hold amplifier inside the integrator feedback loop of the conventional FVC. One way to think of the fast-settling FVC is as a conventional FVC with an adaptive N-pole filter in its feedback. The order, N, of the adaptive filter approaches a very high value so that all integrator output ripple is removed regardless of input frequency. By comparison, the output ripple of the filtered FVC increases with decreasing frequency. Also, delay of the adaptive filter is low so that it can be included in the feedback loop to the integrator without adversely affecting stability. This is not possible with a conventional filter. With the filter included in the feedback loop, DC filter errors (sample/hold errors) such as gain, offset, and offset drift are divided-down by the loop gain of the integrator amplifier to negligible levels.

The fast-settling FVC is shown in Figure 3. For comparison to the filtered FVC, the same values are used for R_6 and C_3. In theory, a smaller value could be used for C_3 in the fast-settling FVC for better settling time. Ripple at the output is eliminated by using a sample/hold to sample the VFC320

integrator output. The only constraint on ripple voltage is that it must be within the linear output-swing range of integrator amplifier. Gain can be added in the sample/hold circuit to reduce the peak amplitude needed from the integrator output. In the filtered approach, added gain would also gain-up the ripple.

In the fast-settling FVC, the sample/hold acquires a feedback signal from the integrator output ramp in approximately 1µs so that the ripple of the ramp is translated to a higher frequency and substantially eliminated by a simple single-pole high-frequency filter, R_5, C_5. The delay through the high-frequency filter is low enough so that it can also be included in the feedback loop.

Since the sample/hold is in the feedback loop of the integrator, trigger timing is unimportant. The feedback loop automatically adjusts the relative level of the integrator output signal for proper alignment with the trigger pulse.

The sample/hold circuit in Figure 3 is controlled by the SN74121 one-shot through a SN7406 open-collector inverter connected as a level shifter. Pull-down resistor R_8 is added at the output of the integrator amplifier to boost output drive to the sample/hold capacitor, C_4.

Design of the sample/hold is greatly simplified because DC accuracy is unimportant. The complete sample/hold circuit consists of a common DMOS FET, Q_1, hold capacitor, C_4, and FET-input op amp, A_1. High frequency sampling glitches are also filtered out by the R_5, C_5 output filter. Since the glitch filter is also in the integrator feedback loop, associated DC errors are eliminated, and low DC output impedance is maintained.

Sample/hold gain is set to 2.0V/V by R_3 and R_4. The sample/hold gain attenuates (by two) the maximum output excursion necessary from the VFC320 integrator output, allowing both a comfortable +10V full-scale output from the FVC and a large ripple signal at the integrator output.

Gain in the feedback loop of the integrator also increases slew rate and bandwidth. With a high slew-rate op amp used for A_1, FVC slew rate is limited by the integrator op amp. Adding a gain of two in the feedback loop doubles the FVC slew rate. The actual sample/hold gain is not critical. Because it is in the feedback loop, gain errors in the sample/hold circuit do not affect the gain of the FVC or degrade its accuracy.

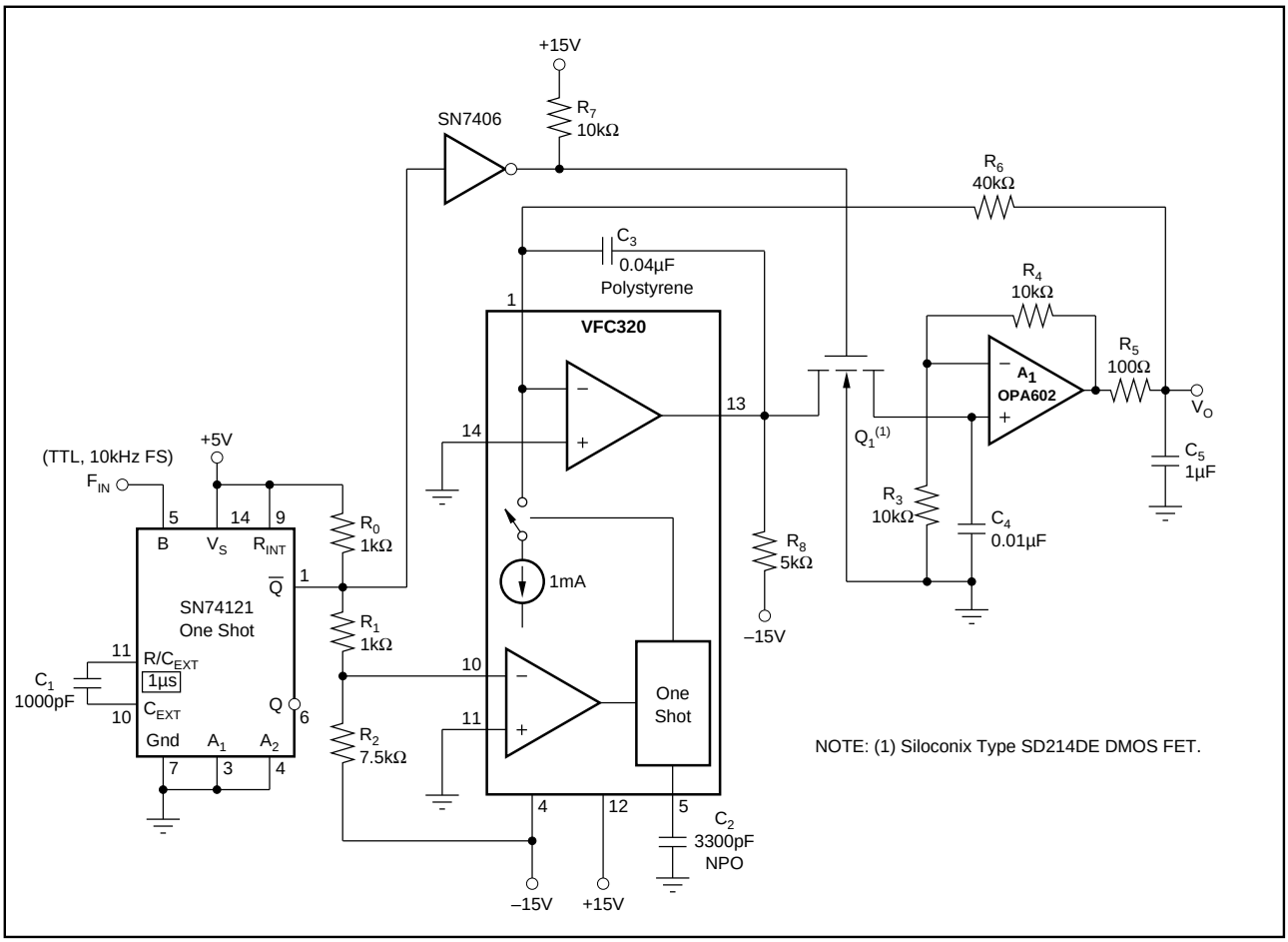

FIGURE 3. Fast-Settling Frequency-to-Voltage Converter. This converter is formed by adding a sample/hold in the feedback loop of the conventional FVC. It can settle to 0.01% in 7.4ms without ripple. Because the sample/hold is in the feedback loop, FVC precision is unaffected.

FAST-SETTLING FVC PERFORMANCE

The fast-settling FVC has the same DC transfer function as the simple FVC, but with neglegable ripple at the output. Measured DC performance of the Figure 3 FVC circuit gave nonlinearity better than 10ppm (better than 16 bits).

The scope photo in Figure 4 shows the excellent small signal ±1V (actually +6V to +8V) output step response for the FVC with a 6kHz to 8kHz input frequency change. If phase margin were low, this signal would exhibit overshoot and ringing.

Settling time of the fast-settling time FVC approximates that predicted by a single-pole system boosted by the gain in the feedback loop:

$$T_S = \ln\left(\frac{100\%}{P\%}\right) \cdot R_6 \cdot C_3/GAIN$$

Where:

GAIN = Gain of sample/hold circuit in feedback loop of integrator [V/V]

With $R_6 = 40k\Omega$, $C_3 = 0.04\mu F$, and GAIN = 2.0V/V as shown in Figure 3, 7.4ms settling to 0.01% is predicted. The scope photo in Figure 5 shows good agreement between theoretical and measured settling time for a large signal +1.2V to +10V output step due to a 1.2kHz to 10kHz input frequency change. The scope photo shows the residual error signal superimposed on the theoretical output signal. Each graticule division is approximately 0.01%.

The circuit used to measure settling time is shown in Figure 5A. A +1.2V to +10V square wave is applied to the input of both a VFC and to a precision difference amplifier. This square-wave input is the theoretical output signal—shown as one of the two traces on the scope photo Figure 5. The VFC converts the input voltage square wave into a modulated TTL-level 1.2kHz to 10kHz frequency signal. The frequency signal feeds directly into the FVC under test. The output of the FVC, ideally a delayed reproduction of the input square wave, feeds into the inverting input of the difference amplifier. The difference amplifier subtracts the FVC output from the VFC input. The output of the difference amplifier, (FVC output)-(VFC input) is the residual error signal—shown as the second trace on scope photo Figure 5. For this method to work, the VFC must have small dynamic error compared to the FVC. The VFC used in these measurements was the Burr-Brown VFC320.

Scope photo Figure 7 is a picture of a sine-wave modulated 1kHz to 9kHz TTL-level (0V to 5V) FVC input signal superimposed on the 1V to 9V FVC output. This photo was taken by driving a 1V to 9V sine-wave signal into the Figure 5A test circuit and looking at the FVC input and output. At the lower 1kHz frequency input, the steps between frequency input pulses can be seen on the sine-wave output showing excellent settling between pulses.

DISCUSSING STABILITY OF THE FAST-SETTLING FVC

Stability in sampled systems depends on sampling frequency. Since the sample/hold in the feedback loop of the fast-settling FVC is controlled by the input frequency, there is a minimum input frequency required to assure loop

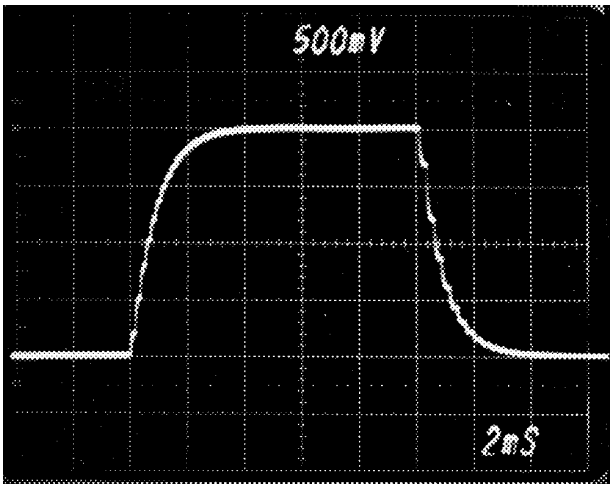

FIGURE 4. Small-Signal Step Response of the Fast-Settling FVC Shows Excellent Stability.

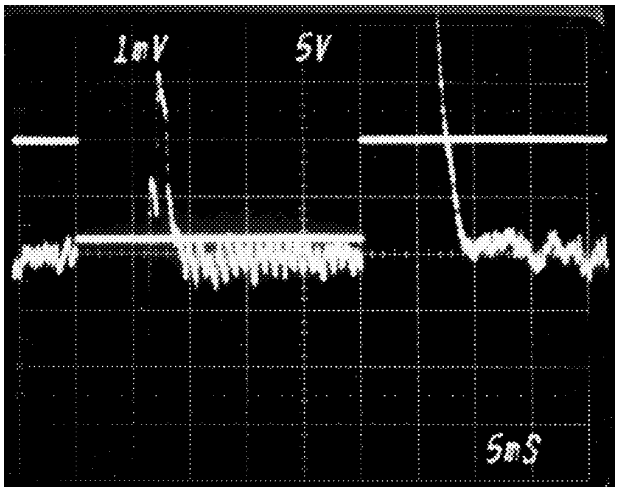

FIGURE 5. Settling Residue of the Fast-Settling FVC Confirms 0.01% Settling is Approximately 7.4ms.

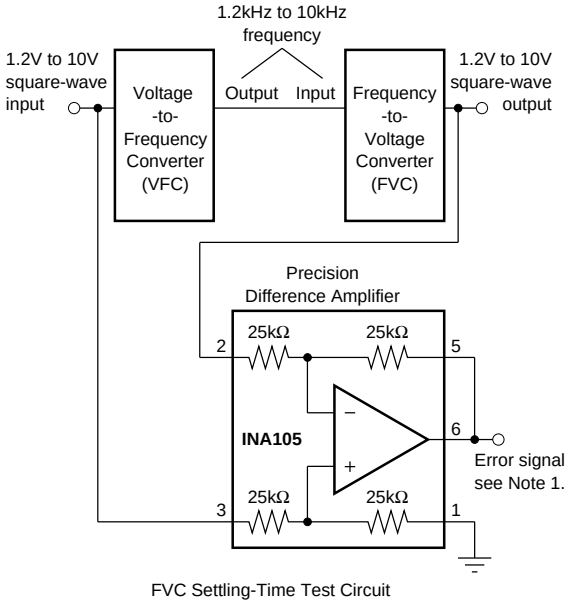

FIGURE 5A. FVC Settling-Time Measurement Circuit Used for Figure 5.

stability. As input frequency decreases, delay through the sample/hold increases thereby decreasing phase margin of the integrator loop. The feedback loop block diagram shown in Figure 6 gives a fairly accurate stability-criteria analysis. Phase margin of the loop is as follows:

$$MARGIN = 180° - 90° - delay_1 - delay_2 - delay_3$$

Where:

MARGIN = phase margin of the loop

90° = phase delay of the R_6, C_3 dominant pole

$delay_1$ = delay of sample-hold switch, Q_1, and hold capacitor, C_4

$$delay_1 = Tan^{-1}(f_{UG} \cdot 2 \cdot \pi \cdot R_{Q1} \cdot C_4)$$

$delay_2$ = delay due to R_5, C_5 output filter

$$delay_2 = Tan^{-1}(f_{UG} \cdot 2 \cdot \pi \cdot R_5 \cdot C_5)$$

$delay_3$ = delay due to sample period

$$delay_3 = \frac{360 \cdot f_{UG}}{2 \cdot f_{IN}}$$

f_{UG} = unity-gain frequency of the overall integrator loop

$$f_{UG} = GAIN/(2 \cdot \pi \cdot R_6 \cdot C_3)$$

GAIN = gain of the sample/hold circuit in the feedback loop

Solving for f_{IN},

(See Equation Below)

Where, in addition to previous definitions:

R_{Q1} = On-resistance of sample/hold switch-transistor, Q_1 [Ω]

Substituting the values from Figure 3, and using 25Ω for R_{Q1}, gives the following results:

MARGIN (°)	F_{IN} (Hz)
60	1200
45	780
30	600
0	400

For best pulse response and settling time the minimum input frequency should be 1.2kHz for the Figure 3 circuit example. At input frequencies below 400Hz, the loop will be unstable and the output will oscillate or lock-up.

$$f_{IN} = \frac{-90° \cdot Gain}{\pi \cdot C_3 \cdot R_6 \left(Margin - 90° + \tan^{-1}\left(\frac{Gain \cdot R_5 \cdot C_5}{R_6 \cdot C_3} \right) + \tan^{-1}\left(\frac{Gain \cdot R_{Q1} \cdot C_4}{R_6 \cdot C_3} \right) \right)}$$

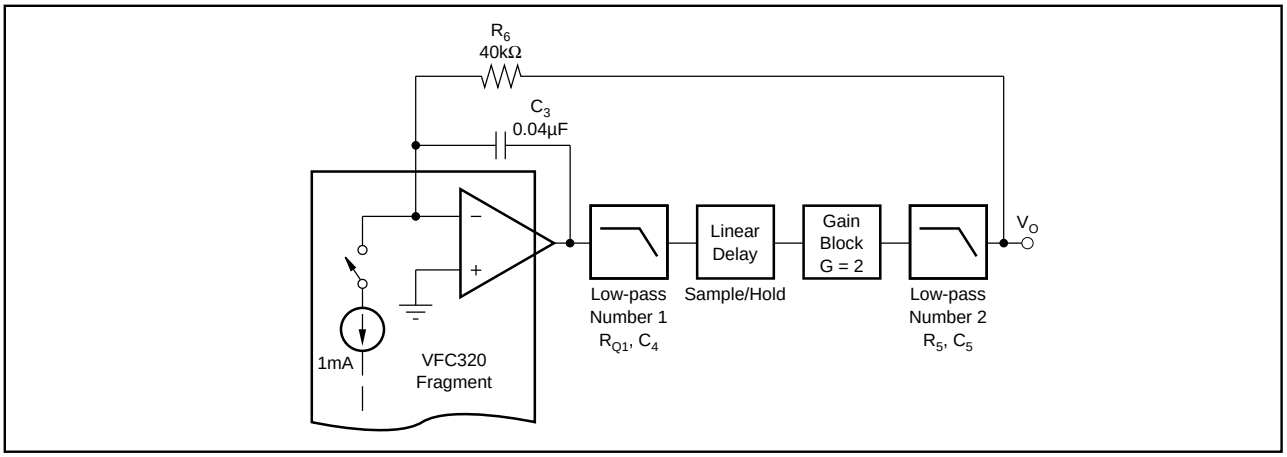

FIGURE 6. This Integrator Feedback-Loop Block Diagram can be Used for Stability Analysis of the Fast-Settling FVC.

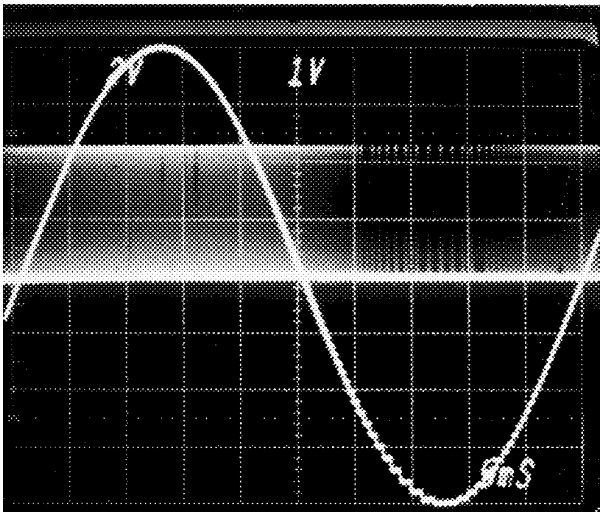

FIGURE 7. Dual-Trace Scope Photo Showing Frequency-to-Voltage Converter 1V to 9V Output for a 1kHz to 9kHz TTL-Level Frequency Input.

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