Application Report
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Logic in Live-Insertion Applications With a Focus on GTLP

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ABSTRACT

Live-insertion capability is an essential part of today's high-speed data systems because those systems are expected to run continuously without being powered down. This application report delves into the cause and prevention of live-insertion and nanosecond-discontinuity effects, using both simulation and actual test measurements from a specially built GTLP EVM. Hypothetical cases for precharge circuitry are also simulated for comparison of the impact of live-insertion events on different logic families. GTLP test results and simulation of the new VME technology show their robustness in dealing with live-insertion events.

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Introduction

High-speed data systems continue to drive faster data rates and are expected to support an extremely wide variety of system features, while the levels of reliability they are expected to meet also continue to increase. One of the most common strategies for keeping a system running continuously is live insertion (also known as hot plugging or hot swapping). Live insertion continues to be more prevalent within state-of-the-art systems, however, establishing a high reliability rating for such a system is not easy.

Live-insertion systems require additional care during design to ensure that signal-integrity levels remain acceptable throughout an operating system. In addition to signal-integrity concerns, hot-plugged devices can have adverse effects on other devices, which are caused by quickly changing voltage levels and damaging current flow. Protective circuitry, components, and specialized software control can reduce the risks associated with line-insertion operations.

Bus-type architectures, such as asynchronous transfer mode (ATM), which typically use logic families such as FutureBus+ (FB+) or Gunning Transceiver Logic Plus (GTLP), provide the main structure for data-communication (datacom) and telephone-communication (telecom) applications. A specially designed GTLP 20-slot backplane evaluation module (EVM) has been developed to demonstrate signal integrity during live insertion and to identify and analyze possible dangers to devices. The EVM represents a realistic system and is intended to emulate real-world issues and solutions in a typical live-insertion, parallel-bus system.

Electrical Protection Definitions

The following definitions are specifically defined by Texas Instruments and may or may not agree with other semiconductor vendor definitions.

Level 0 Isolation

A device with level 0 isolation is incapable of being inserted safely into a backplane without first powering down the host power supply. The device does not have circuitry designed for protection against instantaneous current flow or sudden changes in voltage, and does not have the capability to enter the high-impedance state during a hot-swap event. Damage to the device and other components on the board are almost certain if the daughter card device and the system are not powered down before insertion or removal. Also, system glitches and loss of data-signal integrity will occur.

Level 1 Isolation (Partial Power Down)

A device with level 1 isolation prevents damage to itself by limiting the current transfer between an energized bus and the device input and output when powered down (when the power supply, $V_{CC,}$ is forced to 0 V). This static-current limitation allows insertion or removal of a board into a backplane without interrupting the host system power. However, the host system must suspend signaling during daughter-card insertion or removal. For full device protection during extraction or insertion of daughter cards, the output-enable pin should be utilized in standard logic devices other than GTLP and FB devices, so that the outputs remain in the high-impedance state and damage to the device does not occur. I_{off} circuitry is required for this level of isolation.

Level 2 Isolation (Hot Insertion)

A device that supports hot insertion (level 2 isolation) prevents driver conflict during card insertion or removal. In addition to the level 1 isolation capabilities, the device remains in the high-impedance state from a power-supply voltage of 0 V to a specified voltage (typically 1.5 V for GTLP, 2.2 V for FB, and 2.1 V for ABT devices). In the case of GTLP and FB, above this specified voltage the output of the device either pulls the bus low, if enabled, or assumes the voltage on the bus, if disabled. For standard ABT devices, above V_{CC} = 2.1 V the output state of the device is low or high (depending on the input voltage), if enabled, or assumes the voltage on the bus, if disabled. Data along the active bus might be corrupted during insertion or removal in accordance to level 2 isolation compliance. I_{off} circuitry is required, as well as power-up 3-state (PU3S) circuitry.

Level 3 Isolation (Live Insertion)

A device suitable for live insertion allows insertion or removal of a card without limitations, restrictions, or requirements of other circuitry on system power and signaling. Data is not corrupted under any circumstances during the insertion or extraction event. To avoid bus contention (described later in this application report) for standard logic devices during insertion or extraction, the user must use pullup or pulldown resistors on the output-enable pin to ensure the output remains in the high-impedance state. To precharge the outputs, a BIAS V_{CC} pin typically is used to place a bias voltage somewhere between the logic-high and logic-low voltages on the bus. I_{off}, PU3S, and precharged I/Os typically are required to meet these requirements, all of which are defined and specified in TI data sheets.

Live-Insertion Device Features

As mentioned previously, the three necessary circuits that support level 3 isolation are I_{off}, PU3S, and precharged outputs. All three features need to be active during live insertion to prevent data from producing glitches. All three circuits are featured in GTLP devices and are explained in the following paragraphs.

I_{off}

I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down. This condition can occur when subsections of a system are powered down (partial power down) to reduce energy consumption. All TI standard logic devices with the I_{off} specification allow only 100 μA of maximum current. Any current in excess of this amount (for example, a forward-biased p-n junction) is not considered normal leakage current.

TI GTLP devices do not need extra current-limiting circuitry on the bus I/O port (typically the B port) pins during partial power down. To understand why this is the case, consider a typical CMOS input and totem-pole output structure (see Figure 1). Inherent in all CMOS designs are the parasitic diodes in all n-channel and p-channel MOSFETs, which must be properly biased to prevent unwanted current paths.

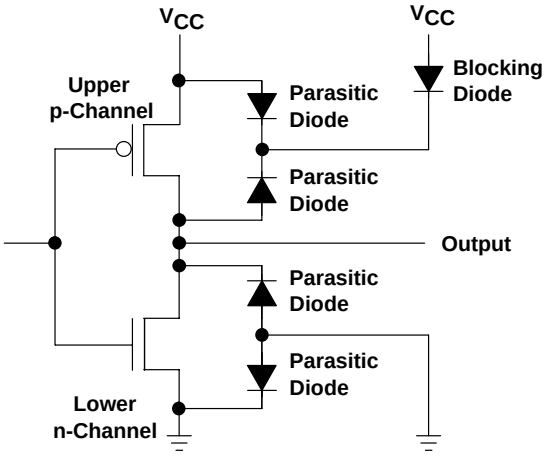

Figure 1. Typical CMOS Totem-Pole Output With I_{off}

The common cathode connection for the parasitic diodes on the p-channel MOS transistor is called the back gate and is typically tied to the highest potential on the IC (V_{CC} in TI logic devices). For p-channel transistors, which are directly connected to external pins, the back gate is blocked with a diode to prevent excess currents flowing from the external pin to V_{CC} when the output voltage is greater than V_{CC} by at least 0.7 V. This blocking diode is a subcircuit of the complete I_{off} feature in several logic families, such as ABT and LVC. Conversely, the n-channel back gate is usually shorted to the lowest potential (ground for most TI logic devices). The n-channel, however, does not pose a problem because the parasitic diode is already positioned to block current when the device is powered down and the output is biased high.

If the blocking diode previously described were missing, the device is powered down and a voltage greater than a diode drop (approximately 0.7 V) is applied to the I/O, the back-gate parasitic diode on the upper p-channel transistor directly connected to the I/O would forward bias. This condition could cause excessive current flow from an output pin, for example, and load down the output line. An even more catastrophic event–damage to the device–can occur. A blocking diode is required for this type of structure and application. TI logic devices with CMOS output structures also incorporate other specialized circuitry to eliminate any current paths.

Next, consider a typical CMOS input structure with bus-hold circuitry, which is essentially a weak latch that holds the previous state of the input inverter (see Figure 2). The blocking diode is required in the upper p-channel transistor, which is connected to the external input pin. Furthermore, this only applies to input circuits with bus hold because non-bus-hold devices do not have p-channel drains or sources directly attached to the input pin.

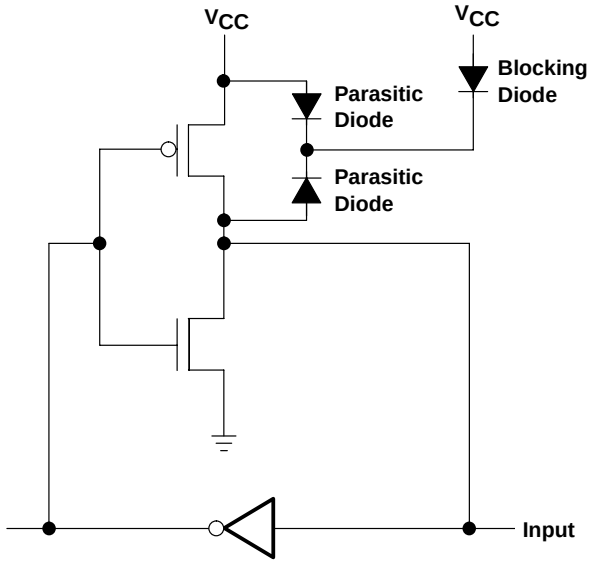

Figure 2. Typical CMOS Input With Bus Hold and I_{off}

As previously stated, TI GTLP devices have no precautionary blocking diodes or current-limiting circuitry on the bus pins. I_{off} blocking diodes are needed only when CMOS p-channel transistors are attached directly to an I/O at the drain and V_{CC} at the source, and vice versa. No such condition exists on a GTLP I/O. Because the upper output transistor is not present and the precharge circuitry does not have any direct p-n junctions to V_{CC}, the output does not have current in excess of leakage current. The same can be said about the differential pair of the GTLP input structure. Figure 3 shows the embedded circuitry of the I/O structures.

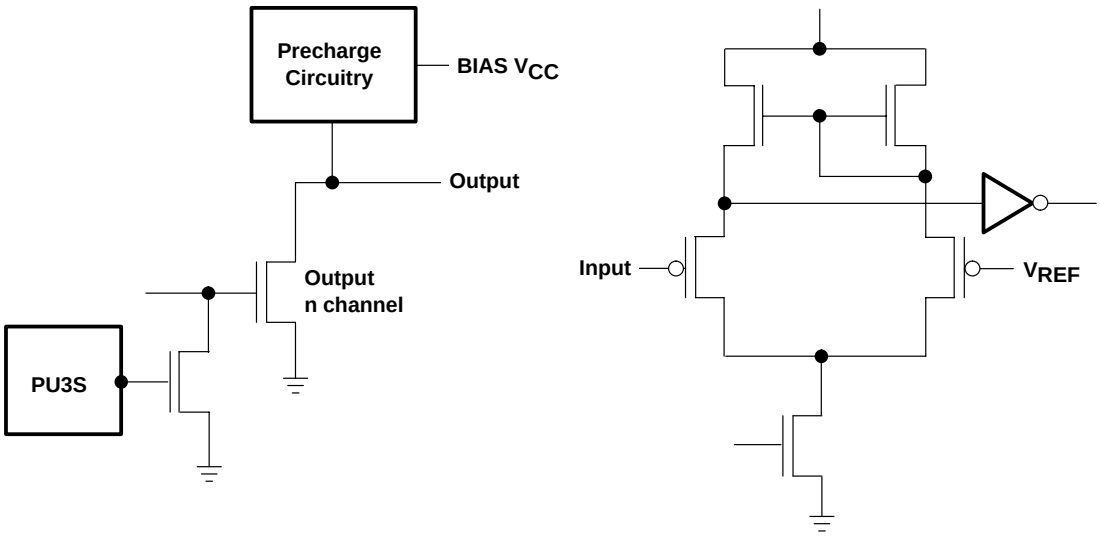

Figure 3. TI GTLP Output and Input Structures

Because any given GTLP I/O never experiences a voltage greater than the termination voltage (V_{TT} = 1.5 V) during normal operation (except during switching transients, which last only a few nanoseconds), I_{off} is specified from 0 V to 1.5 V at the I/O. If I_{off} is required for a TTL-compatible I/O, the highest potential on the bus is near 4.5 V, if the supply voltage is 5 V. In this case, I_{off} would be specified from 0 V to 4.5 V, assuming there is no ESD clamp diode to V_{CC} on the input, output, or I/O.

PU3S

For level 2 isolation, both I_{off} and PU3S circuits are necessary. While I_{off} is tested in a steady-state dc environment, PU3S is checked dynamically by ramping the power supply from 0 V to its maximum recommended value, then back to 0 V. The power-up or power-down ramp rate also affects the internal circuitry, but is recommended not to have a ramp rate faster than 20 μs/V for GTLP devices and slower than that (~200 μs/V) for older logic technologies. Since typical power supplies power up within a few milliseconds (due in part to the enormous capacitance distributed throughout the PCB), the PU3S circuit should function properly in all applications.

PU3S circuitry disables the device outputs at a V_{CC} range of 0 V to 1.5 V for GTLP devices. At a certain guard-banded voltage above 1.5-V V_{CC}, the device asserts a voltage at the output, as indicated by its respective bit input voltage. This is true only if the output-enable pin is floating or a voltage is applied to it, so that it enables the outputs during normal operation of the device. In an application, if a customer requires the output to be in the high-impedance state while the device is being powered up or powered down, the output-enable pin must be set so that it disables the output. For example, a device with an active-low output-enable pin places the output in the high-impedance state when it is biased high. In this case, in order for the device output to remain disabled while the device is powering up or powering down, the output-enable pin can be tied to V_{CC} through a weak pullup resistor (≈10 kΩ).

A voltage-versus-time plot demonstrates how PU3S operates (see Figure 4). As the device is being powered up, until it reaches the minimum V_{CC} (typically 1.5 V), the device output GTLP B port remains in the high-impedance state. That is, the device output is in its third state (3-state) and the output transistor is disabled or turned off, thereby allowing the I/O voltage to be pulled to V_{TT} (see Figure 4). When the PU3S circuitry senses that V_{CC} is slightly above 1.5 V, the device resumes normal functionality and the output is enabled. As shown in Figure 4, the output assumes a low state when enabled. The falling edge of the power supply shows similar results. Just before V_{CC} reaches 1.5 V, the output is disabled.

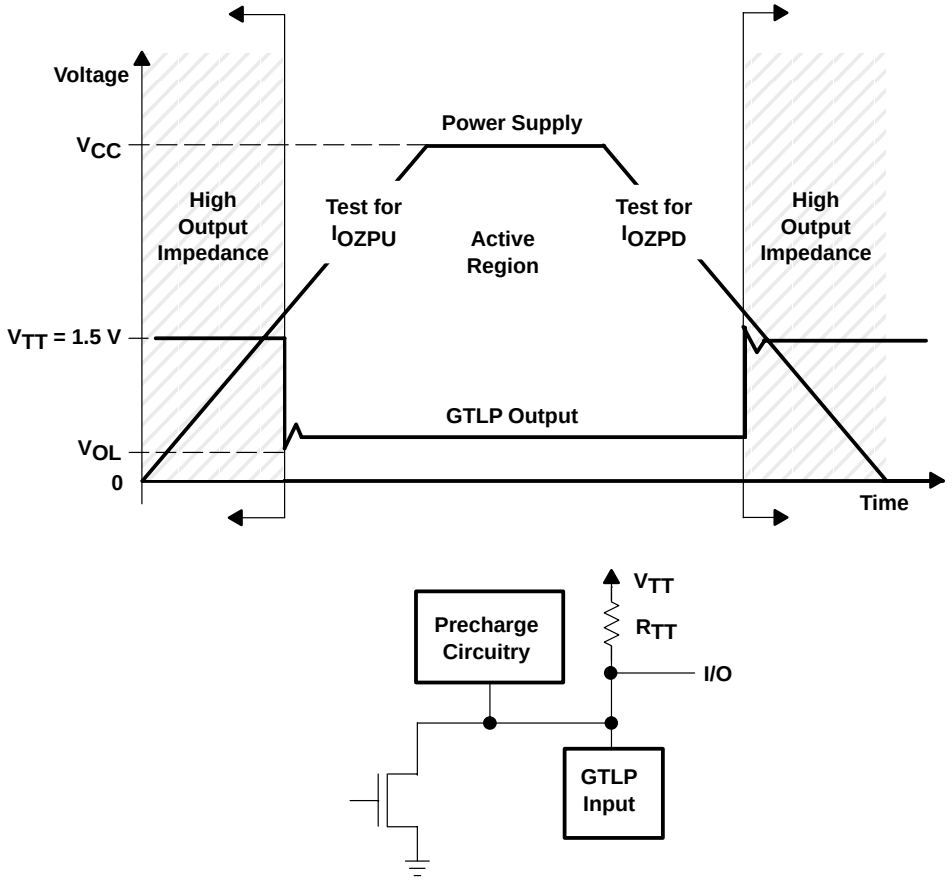

Figure 4. TI GTLP I/O Test for I_{OZPU} and I_{OZPD}

In all GTLP data sheets, TI specifies a maximum output current of 100 μA during power up (I_{OZPU}) and power down (I_{OZPD}), while the output should be in the high-impedance state. If these specifications are included in a TI data sheet, PU3S is assured and explicitly calls out these tests in the live-insertion specifications. Any current in excess of 100 μA during any high-impedance test is not considered normal (or acceptable) leakage current.

Precharged I/Os

Level 3 isolation requires that during an insertion or extraction event, data must not be corrupted to the point where the signal transition actually traverses through the threshold region of an input device and switches the logic state of its output. Some factors that can minimize corruption of data during live insertion are:

- Output transistors placed in the high-impedance state
- Logic state of the output and bus before insertion
- Low I/O capacitance
- Precharge voltage of the output

I_{off}, I_{OZPU}, and I_{OZPD} disable the outputs, as required by live insertion. Bus contention, which is the result of two output buffers placed inadvertently in opposing states, would result if the device outputs were not disabled during live insertion, forcing large current surges from the supply and upper output transistor of one device, through the bus, to the lower output transistor of another device, and eventually to ground. This situation occurs in totem-pole output devices and can result in false data transfer. Additionally, damage to the devices is possible.

Because GTLP devices do not have an upper output transistor and the bus topology relies on an external termination resistor to serve as a passive pullup mechanism, the bus contention condition previously described is not possible. However, if a GTLP output is enabled low inadvertently, the bus is forced to a low level and unexpected data results, without damage to the GTLP I/O. Therefore, the I_{off}, I_{OZPU}, and I_{OZPD} features are still required in GTLP technology, even though the normally destructive bus contention is not an issue.

TI GTLP and other technology data sheets specify the important parameter of maximum capacitance of the device input (C_i), output (C_o), and/or I/O (C_{io}). These parameters can be found in the electrical characteristics table, which describes dc test parameters, conditions, and allowable limits. Why is maximum capacitance a concern in live insertion? The answer lies in the effect of abruptly applying a voltage to a capacitor.

Take, for example, an energized bus at a high logic state. Before a card is inserted into the backplane, the card output voltage could be close to, or at, ground. Each signal pin that is being attached to the bus has an inherent capacitance due to the input and output IC structure, the IC package, the stub, and the connector itself. The total capacitance can be 12 pF to 20 pF. The electrical property of a capacitor is to resist a change in voltage. Therefore, when the connector pin makes contact, the card capacitance tries to force the bus signal as close to ground as it can and then increase asymptotically towards the original voltage. The degree to which the voltage can be forced low is dependent on the card and backplane parasitics. The larger the supporting parasitics, the bigger the perturbation. Figure 5 shows what can happen when a high-parasitic capacitance is associated with the plug-in card. When the voltage spike crosses the input threshold voltage of a receiver, the data is corrupted. Insertion or removal of a card does not present a concern when a bus is biased at a logic low level because any perturbation will, at most, force the bus voltage very close to 0 V.

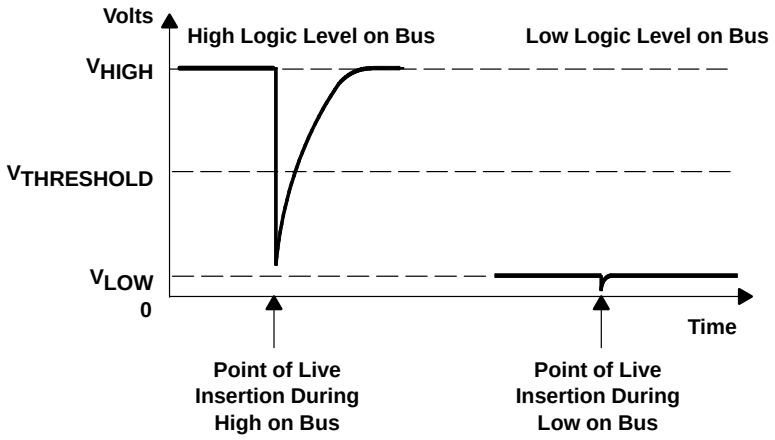

Figure 5. Possible Data Corruption Scenarios During Live Insertion

A way of limiting the glitch from crossing the threshold voltage is to reduce C_{io} to weaken the strength of this effective capacitor. TI GTLP devices incorporate optimally reduced C_o, C_i, and C_{io} characteristics for this purpose. Ideally, it would be better to eliminate the capacitance altogether, but that is not possible due to the fact that the larger the output transistor, which is needed for high drive capability and the more effective the ESD protection, the result is a larger pin capacitance. Another helpful manner in which the glitching effect can be reduced is to precharge the output pin of the device to a voltage centered between the low-level and high-level output voltages before the connector pin is attached to the active bus. Figure 6 shows that by setting the precharge voltage equal to the GTLP input threshold voltage (1 V), this perturbation can be reduced. Any glitch produced on the bus no longer crosses the input threshold region of the receiver, regardless of the state the bus is in when the glitch is generated. However, in the low state, the bus voltage is forced high and approaches the precharge voltage level but never actually crosses the threshold, eliminating any chance of propagating a false data bit throughout the system.

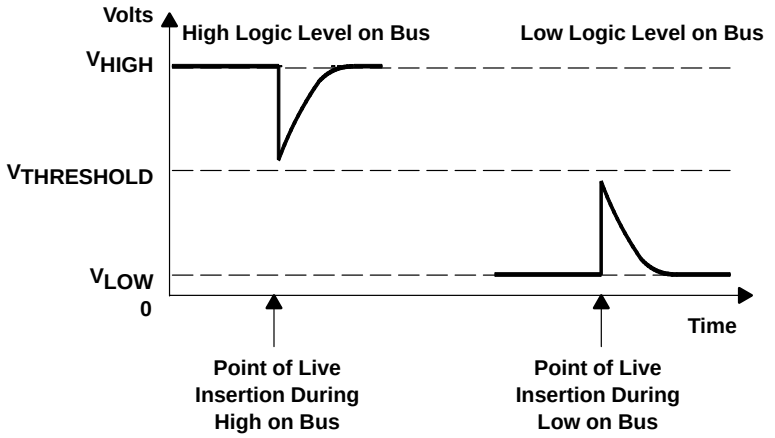

Figure 6. Precharge BIAS V_{CC} Functionality

It should be obvious that live insertion is not only a feature that is appropriate for applications where cards are inserted to or extracted from a running system, but also is required for maintaining noncorrupt data signaling. TI offers only a few technologies with full live-insertion capabilities and many more with lower levels of isolation (see Table 1). The devices listed in Table 1 are generalizations; therefore, each device data sheet must be examined for isolation-level compliance.

Table 1. Generalized Isolation Levels for TI Technologies

ISOLATION LEVEL	TECHNOLOGY
Level 0	AC, ACT, AHC, AHCT, ALB, ALS, ALVC, AS, F, (CD)FCT, HC, HCT, HSTL, LS, PCA, PCF, S, SSTL, SSTV, TTL
Level 1 (partial power down)	AVC, LV, LVC, (CY)FCT, GTL, LS, ALS, AUC
Level 2 (hot insertion)	ABT†, ALVT, BCT, LVT, LVCZ
Level 3 (live insertion)	ABTE†, FB, VME‡, GTLP

† TI ABTE and some ABT devices do not specify I_{OZPU} and I_{OZPD}.
‡ VMEH22501 available in the second quarter of 2002

True live-insertion capabilities are specified only in two technologies, GTLP and the new VMEH22501. These technologies are specifically designed to operate in backplane environments, i.e., distributed loads, where live insertion is practiced extensively.

Standard GTLP System Operation

A fully operational system helps to further understand the impacts of hot-swap transients. Figure 7 shows the network topology of a typical 20-slot ATM data bus for GTLP technology. The bus is fully loaded, having all cards populated, and is terminated with 33-Ω pullup resistors to 1.5 V at each end of the network. The network is driven by the SN74GTLPH1655 from slot 1, and the receivers (all SN74GTL1655 devices) are monitored in slots 2 and 20 at a clock frequency of 23 MHz and a data signaling rate of 23 Mbps.

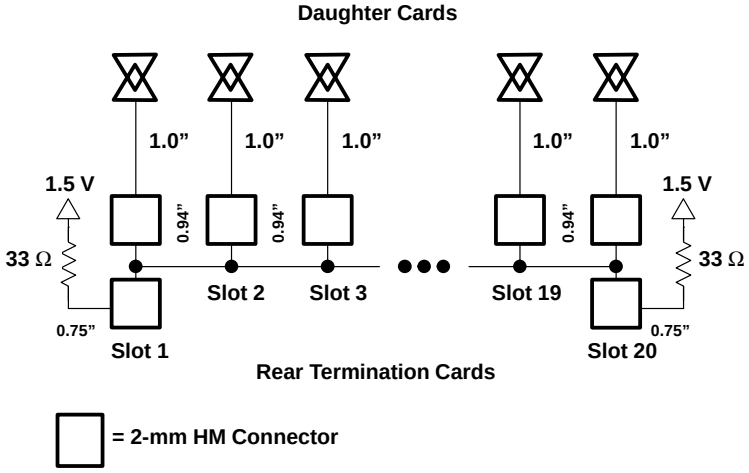

Figure 7. 20-Slot GTLP Network Topology

Figure 8 shows the physical testing results of the GTLP system previously described. The testing was performed with the Tektronix TDS 784C 1-GHz oscilloscope and Tektronix P6245 TDS500/600 (<1 pF, 1 MΩ, >1.5 GHz, 10X) probes. In this fully loaded case, the 33-Ω pullup resistor optimally terminates the backplane because it matches the approximately 33-Ω loaded trace impedance. For heavily loaded conditions such as this, the SN74GTLPH1655 is capable of operating with a minimum of 22-Ω pullup resistors (equivalent to 11-Ω effective dc resistance). If the termination resistance is not optimized to match the backplane characteristic impedance, the maximum frequency achievable and optimal signal integrity is compromised.

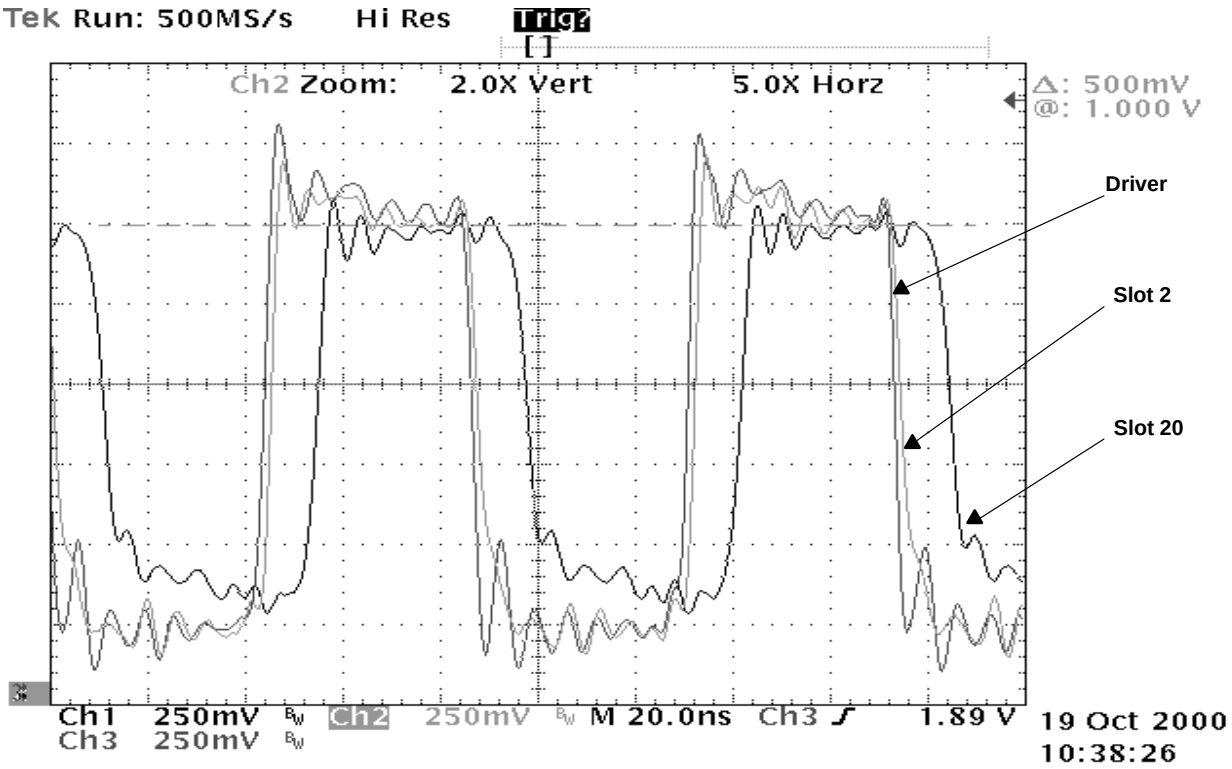

Figure 8. Measured GTLP System

In actual system designs, waveforms are not as noisy as shown in Figure 8. Waveforms in Figure 8 were obtained from the SMB connectors, which are routed about 2 in. from the backplane connectors on the daughter cards for ease of probing backplane signals for the oscilloscope. The longer these stubs are, the noisier the system is. Normally, the backplane signal is not taken past the GTLP device B-port I/O pin but, for ease of measurement, it was routed to the edge of the card. Also, in this configuration, LVTTL clock noise is picked up through nonideal routing on the driver cards, causing added noise in the GTLP system. Another important aspect of the GTLP system described is that it simultaneously switches all outputs, thus inducing added noise to ground. Even under these nonideal, worst-case conditions, GTLP performance has sufficient noise margins.

Live-Insertion Measurements on a GTLP System

Live-insertion events become more troublesome in a lightly loaded system topology and are even more significant when data is transmitted along an actively transitioning bus. Figure 9, which shows the lightly loaded case of Figure 7, represents the partially loaded ATM bus topology using GTLP technology undergoing live insertion. Partially loaded networks tend to present the worst-case impact of live insertion (and its accompanying side effect called nanosecond discontinuity, which is discussed later), as a result of minimized total system capacitance and an inability to effectively absorb the newly transferred energy. This is especially true when daughter cards and their associated capacitance are absent in the vicinity of the hot-swapped card.

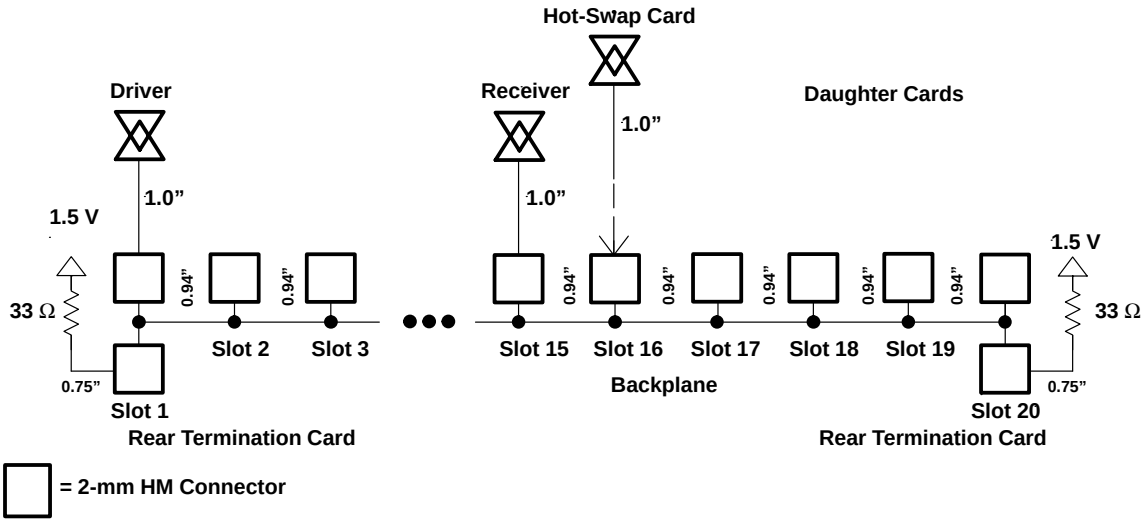

Figure 9. Lightly Loaded Hot-Swap GTLP System Topology

Laboratory measurements have shown the worst-case condition to be when data is high. The waveforms in Figure 10 show a lightly loaded, active-high bus when a card is inserted with no precharge capability. The monitored signals shown are the driver, the inserted card, and an adjacent receiver card.

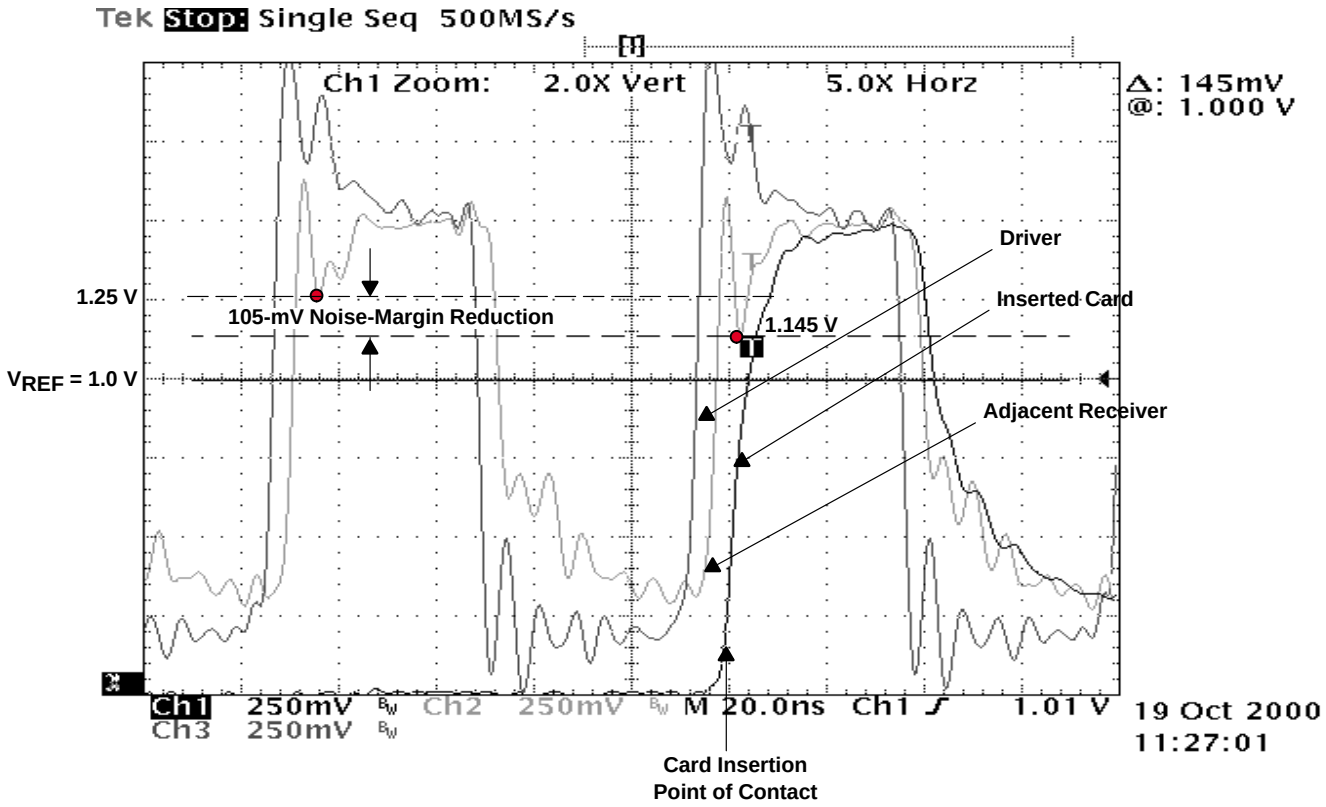

Figure 10. Live Insertion Without Precharge

Before the card was inserted into the backplane, the worst-case high-level voltage on the neighboring receiver card was 1.25 V. However, due to the live insertion event while the data was high, the high level degraded to 1.145 V, which could be unacceptable to some designers. Figure 11 shows waveforms under the same conditions with precharge present. In this case, the precharge level is approximately 1.2 V. The SN74GTL1655 is specified with an output voltage between 1 V and 1.2 V when precharge dominates the output driver. The insertion perturbation is not detected on the adjacent receiver card due to precharging of the output before insertion.

To make a valid comparison of the precharging benefits shown in Figures 10 and 11, the insertion events should be performed at the same moment in time, i.e., on the undershoot voltage just after the low-to-high transition. However, after hundreds of attempts to catch the insertion at the proper moment in time, it was decided to use the closest insertion events.

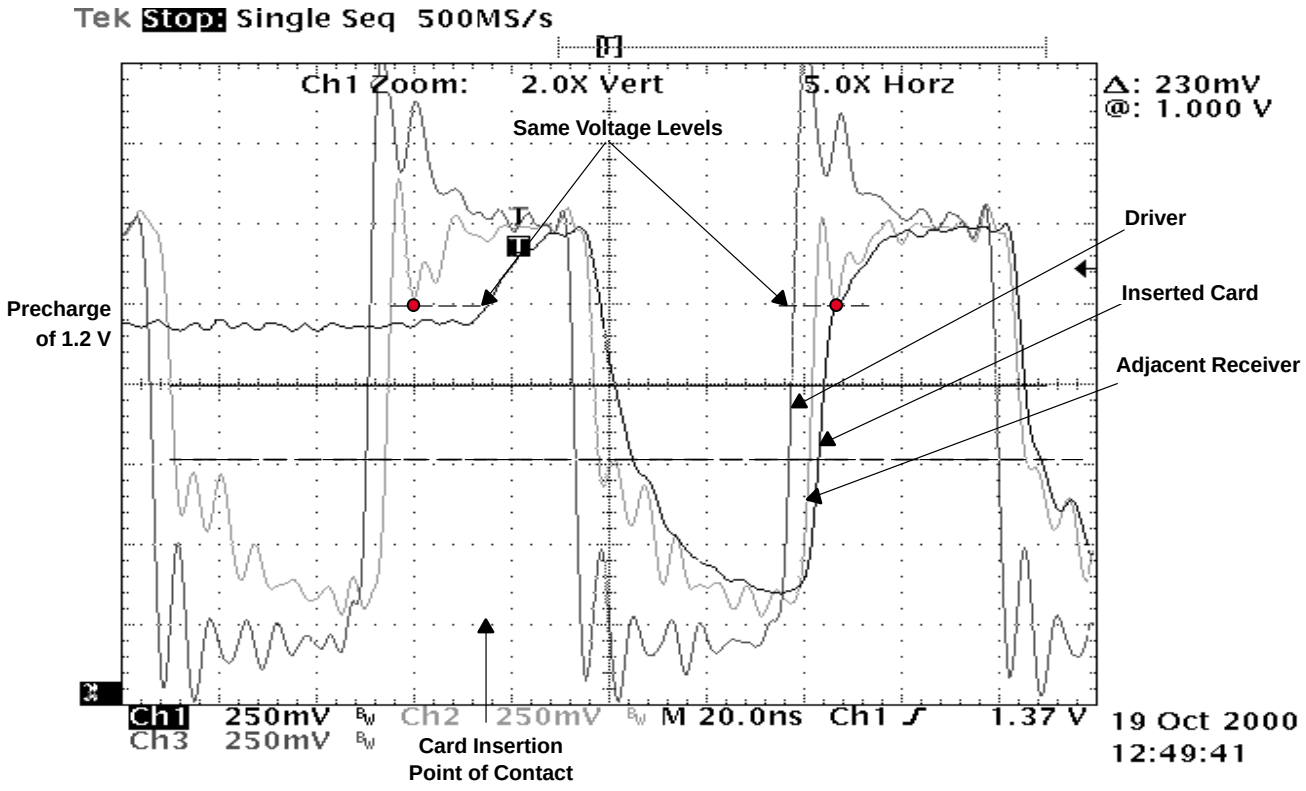

Figure 11. Live Insertion With Precharge

The waveforms shown in Figures 10 and 11 were obtained using a specially designed 20-slot, 19-in. EVM showcasing TI GTLP products. The system topology used in precharge or nonprecharge measurements is identical for all measurements and simulations (see Figure 9).

For TI GTLP precharge circuitry to function properly, a voltage with the same value as the V_{CC} supply must be applied to the BIAS V_{CC} pin prior to insertion on the activated bus and prior to V_{CC} being applied to the device. If V_{CC} is applied before the card is inserted, the precharge circuitry is disabled and removes any output bias voltage. Once V_{CC} is raised to its specified normal lower operating voltage range, the precharge is removed from the output. The recommended sequence to power up a TI GTLP device is ground (GND) and BIAS V_{CC}, then data, and then V_{CC}. This can be accomplished by using connector-pin sequencing on the card, with the GND and BIAS VCC being the longest, data I/O shorter, and V_{CC} being the shortest.

Live-Insertion/Nanosecond-Discontinuity Evaluation

Nanosecond discontinuities are short duration periods of no electrical conduction as a result of the relative motion (movements on the order of atomic distances) between the conductive structures at the connector contact interface. The discontinuities can occur during both engagement and disengagement operations during periods of low-normal-force contact. Typically, connector reliability is based on the ability of the connector to provide and maintain a mechanical connection once fully mated. When a connector is evaluated for hot-swap requirements, the first electrical contact occurs at a point well before the mechanical design can provide sufficient normal force to ensure continuous contact between the mating contacts. During this period of time, nanosecond discontinuities occur. On an atomic scale, surfaces of the contacts look like mountain ranges coming together. As the contacts grind against one another, electrical shorts and opens occur until sufficient normal force brings a sufficient number of the mountains together to establish a low, reliable, and stable contact resistance. After full normal force is applied, there are no more electrical opens during the remainder of the sliding operation between pin and receptacle. Figure 12 provides a visualization of the live-insertion nanosecond discontinuity.

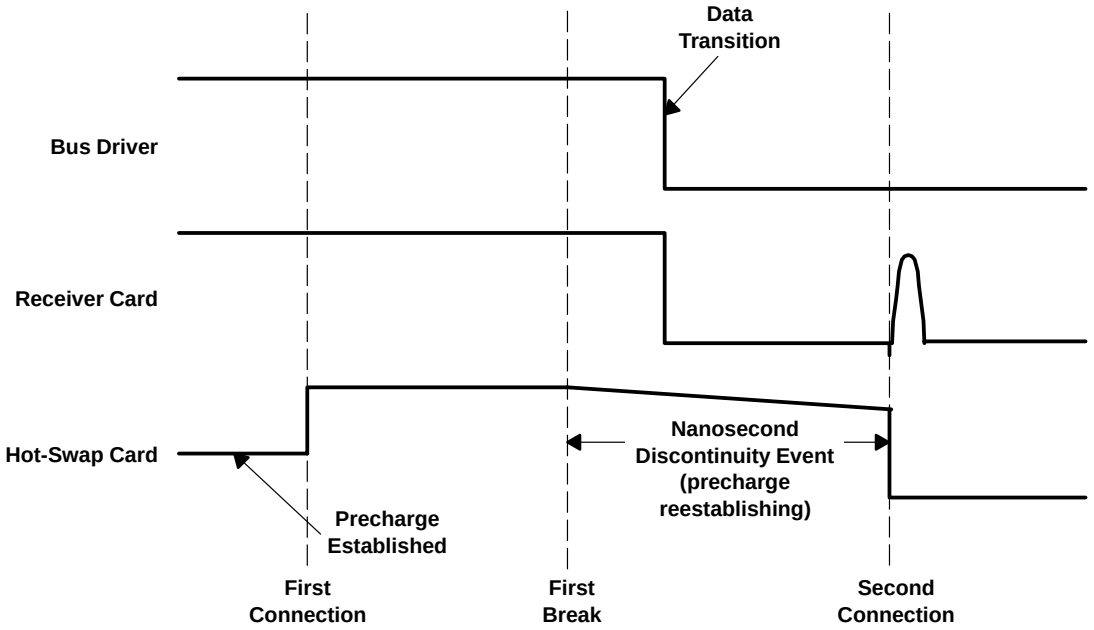

Figure 12. System Effects During Live-Insertion Nanosecond Discontinuity

When connectors mate, nanosecond discontinuities present a possible problem only after initial contact has been made and until sufficient normal force is achieved. Once the inserted card is charged to bus potentials, additional (nanosecond) disconnects and reconnects can become a significant issue. The discontinuities can cause backplane bus voltages of one logic level to be connected electrically with a daughter card charged to the opposite logic level. The connection of these two different potentials results in an instantaneous energy transfer between the two structures. Significant energy transfer can adversely affect voltage levels of signals expected to run flawlessly during a live-insertion event. These types of disturbances can occur over many waveform cycles, possibly causing multiple data glitches across many data and control lines. To alleviate the effects of nanosecond discontinuities, Tyco Electronics provides Quiet Mate™ connectors that slowly transfer the energy.

Figure 13 shows a nanosecond-discontinuity event captured using the EVM configured as shown in Figure 9. Figure 13 shows that connection was lost just as the bus was transitioning from a low to a high state and reconnected in another cycle when the data was high. Because precharge is not present between the breaks, the I/O voltage remains at the first-break connection voltage. The worst-case glitch that was captured forced an output voltage to 1.185 V. This represents about 160 mV of noise-margin degradation and is very close to the GTLP input threshold nominally set at 1 V ±50 mV. More significant glitches occurring at the right times further degrade signal integrity.

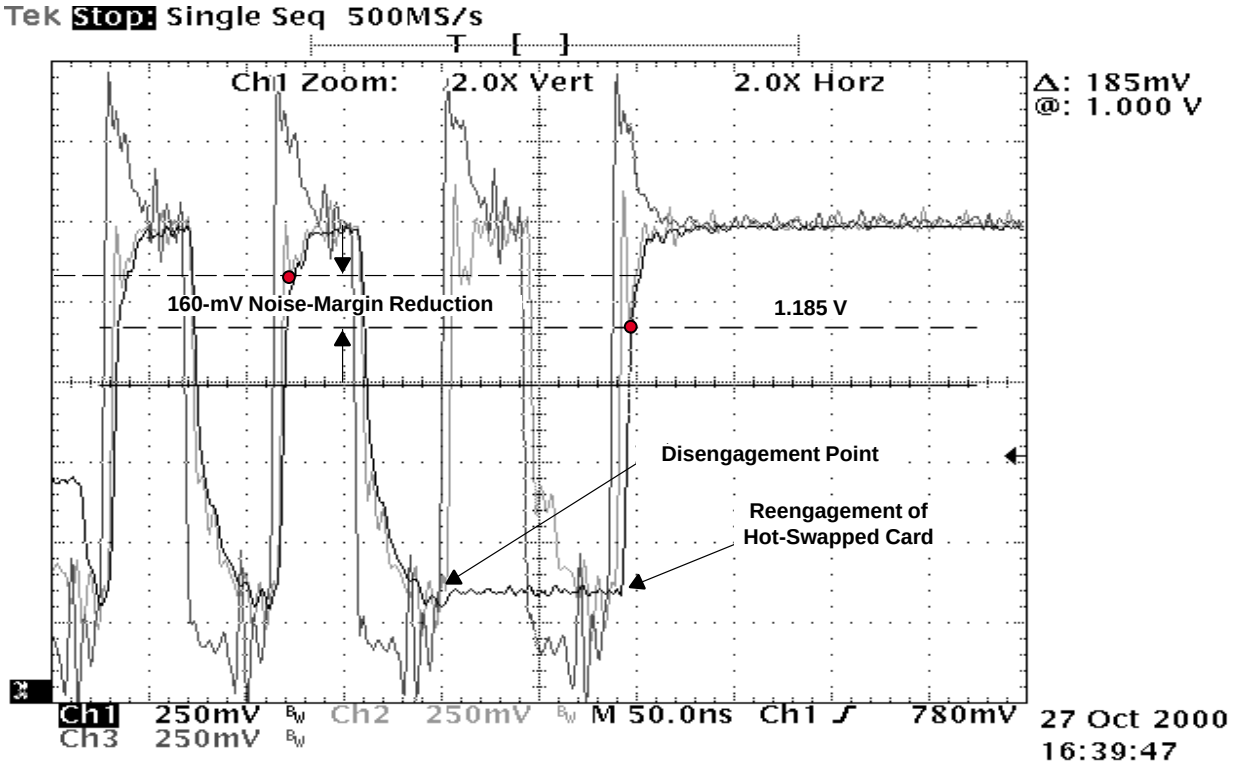

Figure 13. Effect of Measured Nanosecond Discontinuity

If precharge were present, the voltage after the first break point would try to slowly increase toward the specified precharge level. However, because the response rate is very slow compared to nanosecond discontinuities, the precharge voltage may not necessarily help after the initial I/O mating.

Simulations Using Various TI Technologies

Simulation offers the flexibility to change system topologies and replace driver models from one technology to another. Another added benefit to simulation is that output drivers can be precharged to any voltage desired, regardless of whether the actual device has this capability. With HSPICE simulation, designers can get an insight into actual system performance before the board manufacturing process. The 20-slot GTLP system topology in Figure 7 was modified (in simulation only) to have a Thevenin-equivalent termination scheme, which is most commonly used with push-pull totem-pole output drivers. In this case, the end terminations were replaced with 86 Ω to 3.3 V and 120 Ω to ground as shown in Figure 14. Also, the model for the GTLP driver was replaced with the HSPICE model for the ABT, ABTE, LVT, and the new VME logic families. These technologies were chosen because of their widespread use in driving backplane environments. Each technology family was analyzed for performance on the backplane.

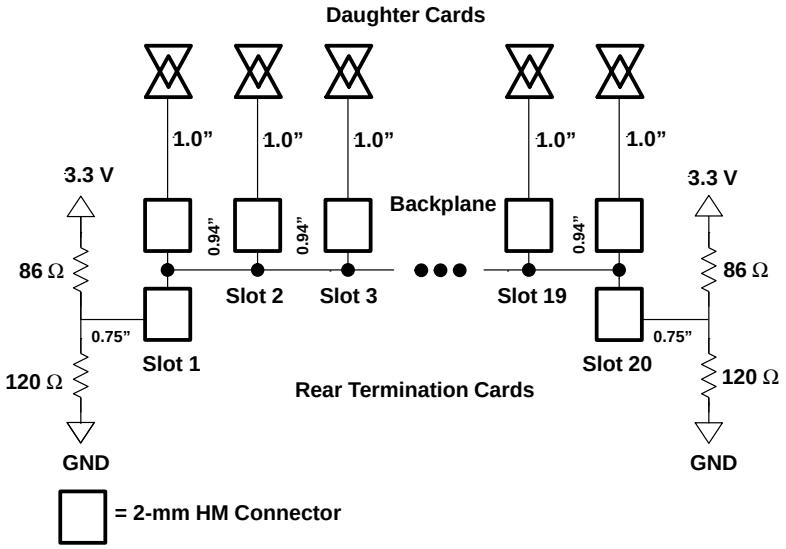

Figure 14. Thevenin-Terminated ATM Network Topology

The performance of the SN74ABT244, SN74LVT244A, and the new SN74VMEH22501 (available second quarter 2002) devices in a fully loaded system (shown in Figure 14) is shown in Figure 15. The switching transitions have been staggered in time for ease of distinction, and only the waveforms at the nearest and farthest receiver input are shown (slots 2 and 20 in Figure 14). Any device from its respective family of devices is expected to perform similarly. Also, the older technologies, in general, have faster transition times (rise and fall times) as they change from one state to another, while the new VME device changes monotonically across the threshold region. Although not shown, the ABTE family of devices behaves similar to the ABT technology.

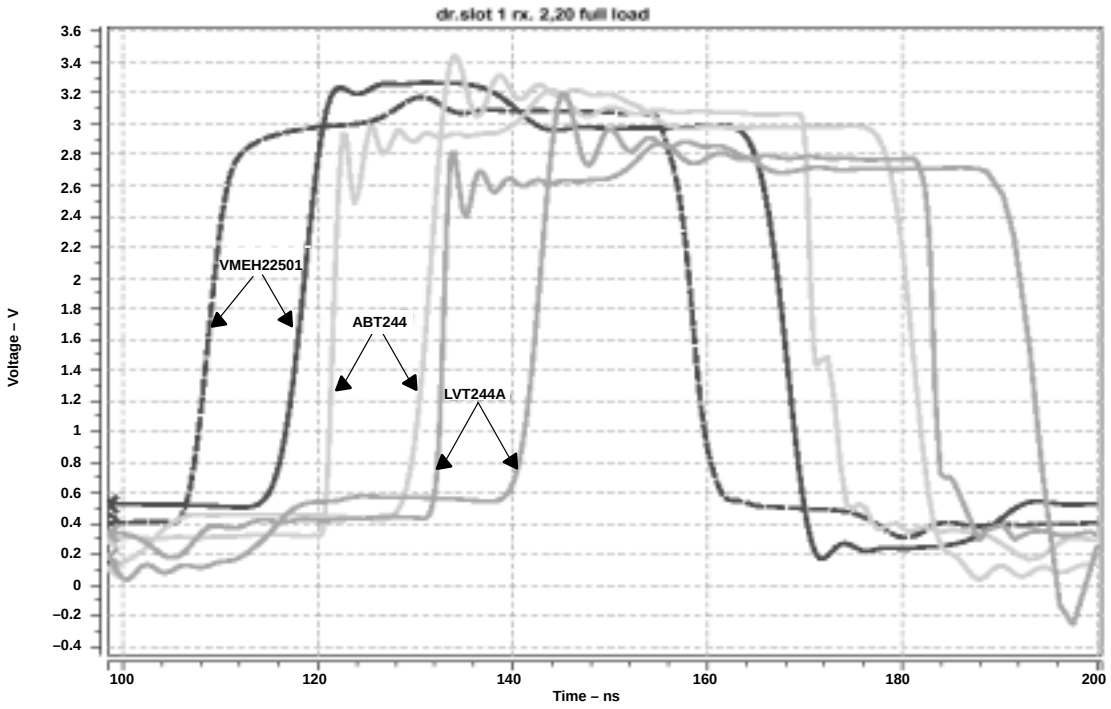

Figure 15. Simulated Results for Fully Loaded ATM Topology With Different Technologies

The ABT and LVT family of devices have an LVTTL input threshold, which means that the input voltage should be greater than 2 V and lower than 0.8 V for good logic-high and logic-low levels, respectively, and should transition between these voltages in a monotonically increasing or decreasing manner. Both ABT and LVT devices show a slight inflection point on the falling edge in slot 2. In all three cases, slot 2 is the first-switching waveform. The VME technology, which has an input threshold set at $0.5 \times V_{CC} \pm 50$ mV, shows better performance in both slot positions.

Figures 16 through 23 show simulation waveforms for the live-insertion event using different TI logic technologies. To increase the effect of the live-insertion event, the system topology is modified to a lightly loaded case, such as the one shown in Figure 9. However, since the ABT, ABTE, LVT, and VME devices have push-pull outputs, the termination was also modified to that of Figure 14.

Figure 16 shows the simulated behavior of the ABT technology during a live-insertion event, with no precharge present. The driver is in slot 1, the hot-swapped card is in slot 16, and an adjacent receiver card is in slot 15. It is important to note that ABT and LVT device families have no capability to precharge a driver output, while the ABTE and VME technologies have this feature incorporated in the device with the BIAS V_{CC} pin.

Simulations provide the capability to precharge an output prior to insertion. The ABT and LVT family of devices do not have this functionality, but Figure 17 shows what would happen if this feature were included. A small reduction in the perturbation on the adjacent receiver card occurred in every case simulated.

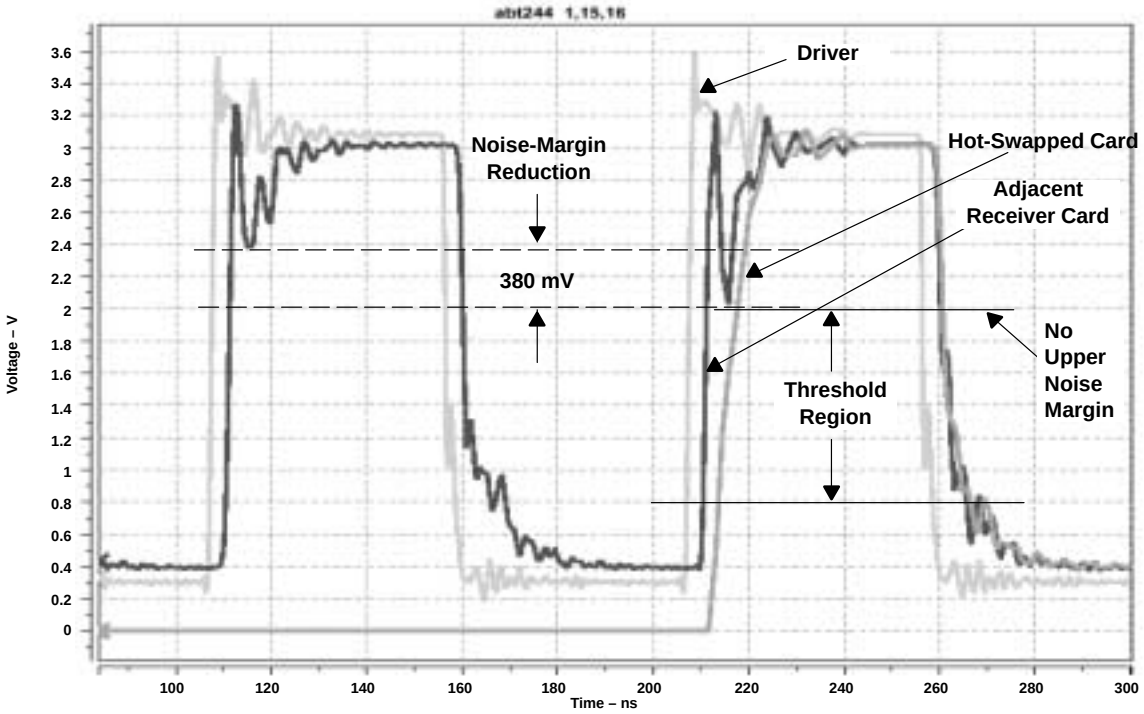

Figure 16. Simulated ABT Device in Live-Insertion Event

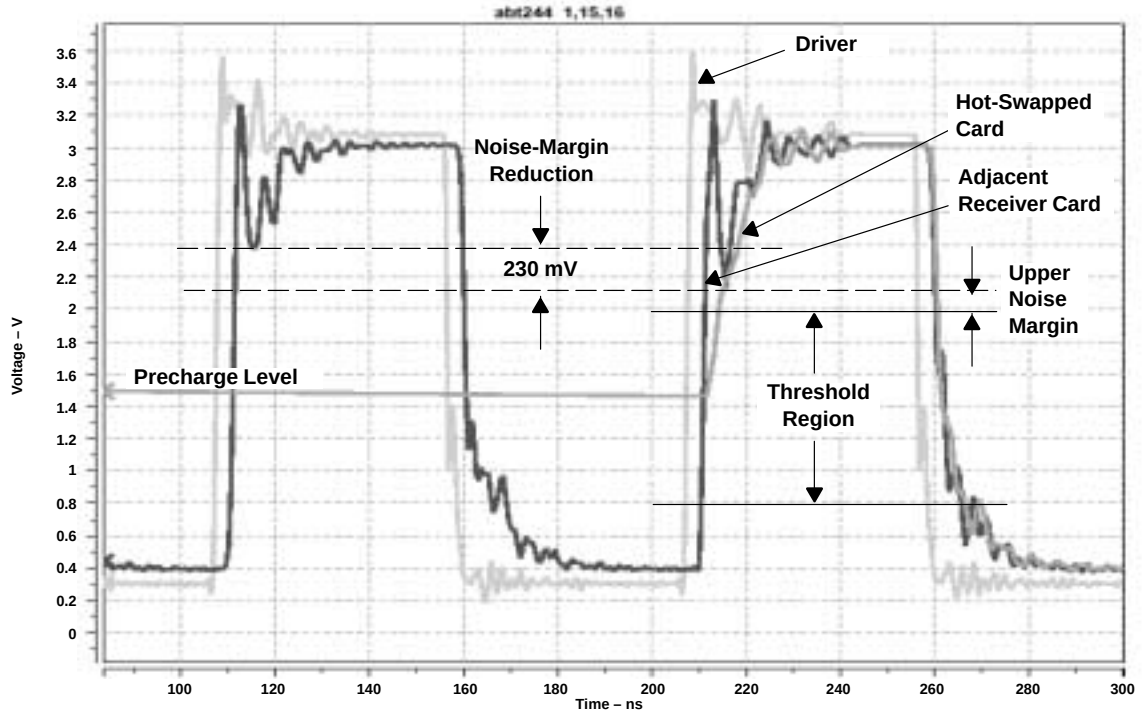

Figure 17. Simulated ABT Device in Live-Insertion Event With Precharge

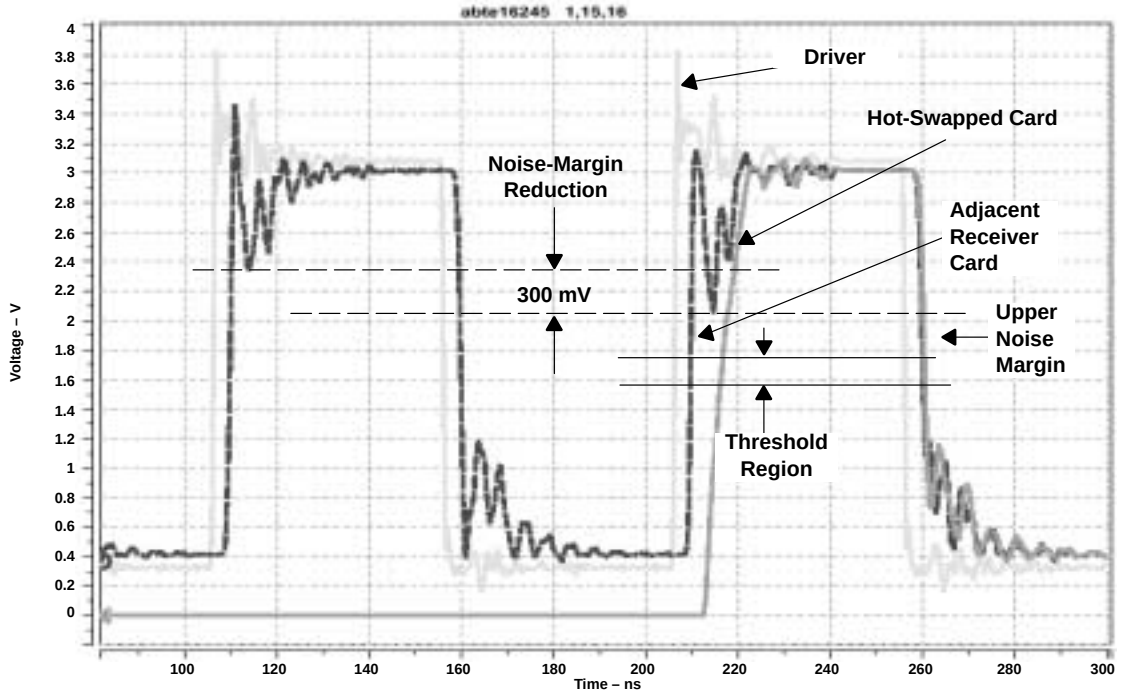

Figure 18. Simulated ABTE Device in Live-Insertion Event

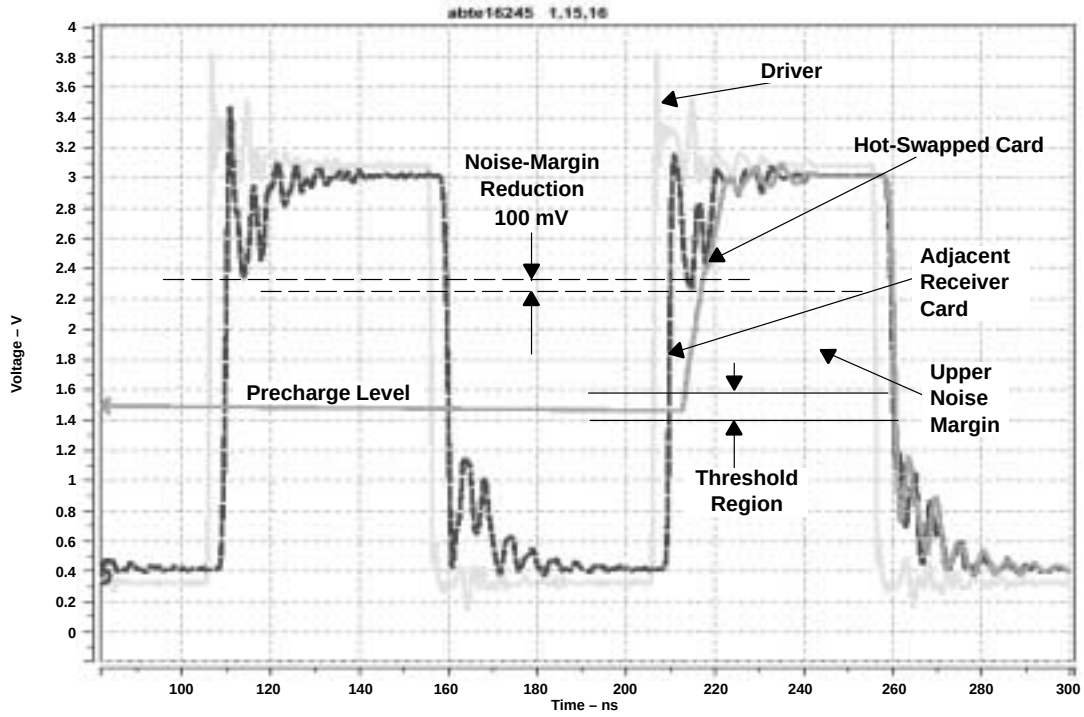

Figure 19. Simulated ABTE Device in Live-Insertion Event With Precharge

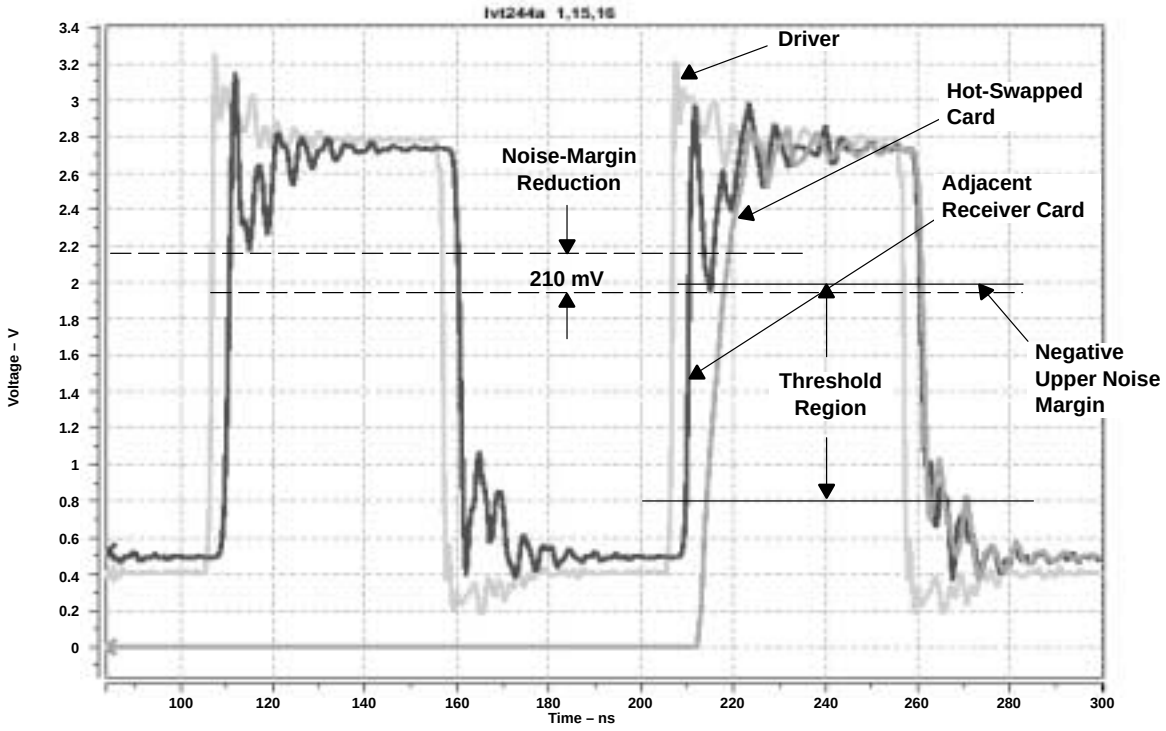

Figure 20. Simulated LVT Device in Live-Insertion Event

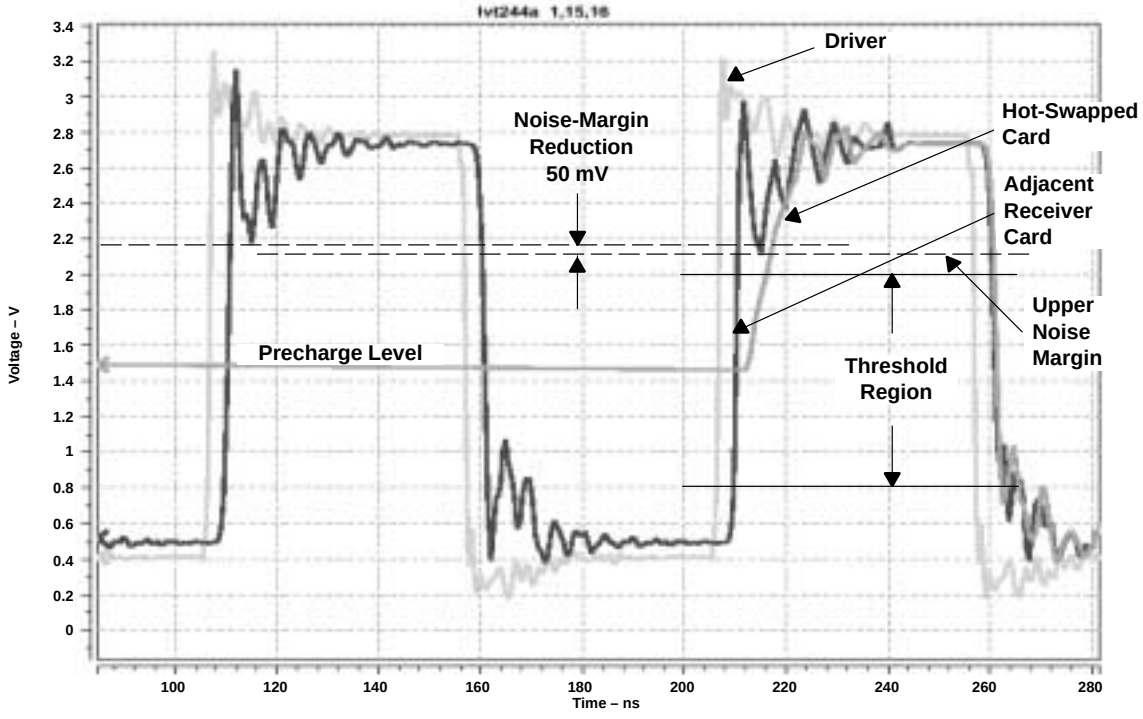

Figure 21. Simulated LVT Device in Live-Insertion Event With Precharge

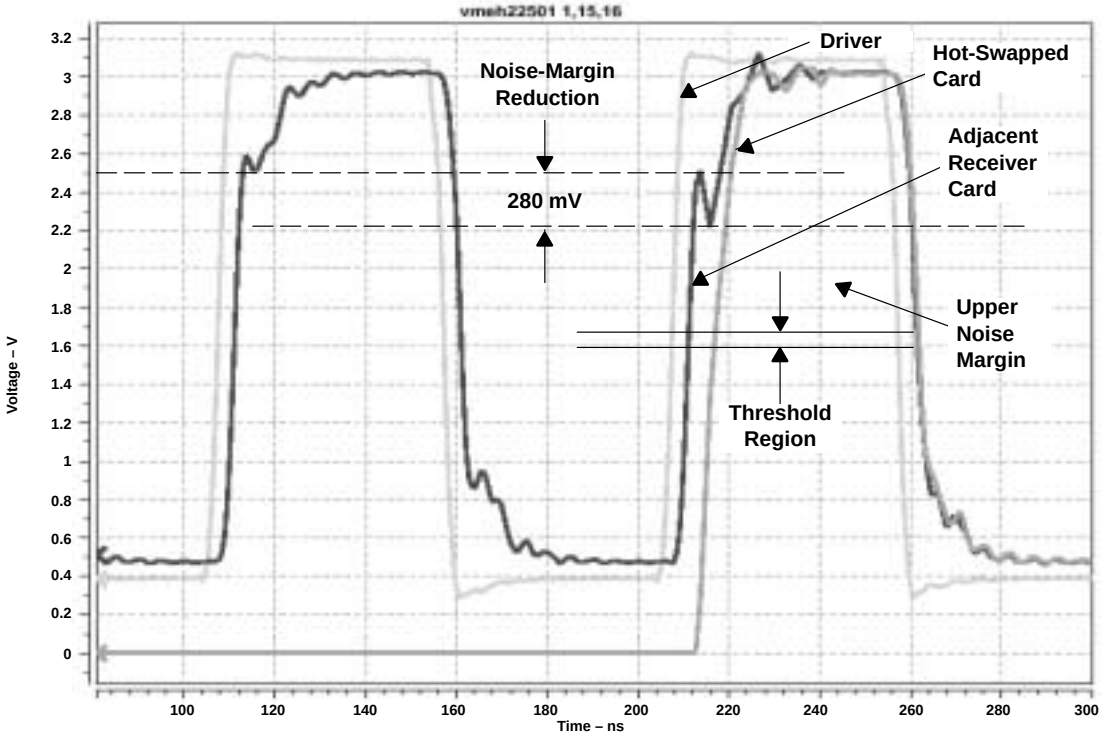

Figure 22. Simulated VME Device in Live-Insertion Event

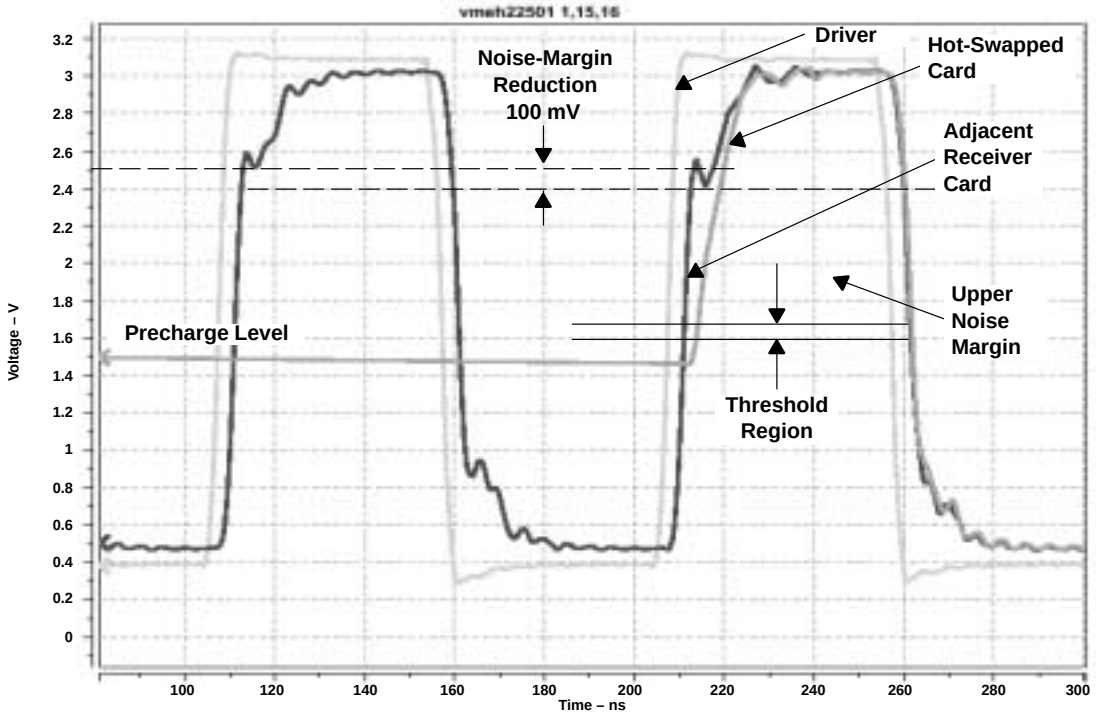

Figure 23. Simulated VME Device in Live-Insertion Event With Precharge

Simulations have shown that for older technologies with LVTTL input thresholds, precharge would have been useful had it been incorporated in the device. In all simulations, precharge offered a better noise-margin performance. By using devices with precharge circuitry and narrower input thresholds, better noise-margin performance is assured.

The newer VME technology has better slew-rate control while the output switches logic states and, therefore, provides some improvement. Coupled with the small ±50-mV threshold region, precharging an output on a VME device during live insertion may offer a significant performance enhancement (see Table 2). The noise margins remain above 520 mV with or without precharge.

Table 2 summarizes simulation values (except GTLP). Upper noise margins are measured from the worst-case high level (first undershoot after the logic state transitions from low to high) to the maximum input threshold of the device. Similar results can be shown for lower noise margins, but the upper noise margins tend to give worse results. For a system in which data is clocked and a decrease in frequency is acceptable, the data is clocked after all transients from switching from one state to another have dissipated. Therefore, in clocking systems, noise margins tend to be larger than those in Table 2 because of the timing of data recognition. When data is being transmitted in the transparent mode, data must at all times stay above the maximum input threshold and below the minimum input threshold to ensure correct data transmission.

Table 2. Simulation Summary

FAMILY	TEST CONDITION	INPUT THRESHOLD TYPE	NORMAL DYNAMIC $V_{OH(min)}$ (V)	DYNAMIC $V_{OH(min)}$ DUE TO LIVE-INSERTION EVENT (V)	NOISE-MARGIN REDUCTION (mV)	UPPER NOISE MARGIN (mV)
ABT	No precharge	LVTTL (0.8 V to 2 V)	2.38	2.0	380	0
	Precharge†		2.39	2.16	230	160
ABTE	No precharge	ETL (1.5 V ±100 mV)	2.35	2.05	300	500
	Precharge		2.32	2.24	80	690
LVT	No precharge	LVTTL (0.8 V to 2 V)	2.16	1.95	210	–50
	Precharge†		2.15	2.1	50	100
VME	No precharge	Pseudo-ETL ($0.5 \times V_{CC}$ ±50 mV)	2.5	2.22	280	520
	Precharge		2.5	2.4	100	700
GTLP‡	No precharge	GTLP (1 V ±50 mV)	1.25	1.145	105	95
	Precharge		1.25	1.25	0	200

† Actual device technology does not have this capability. Simulation results shown are strictly for comparison purposes.
‡ Actual EVM measurements. Simulations of nanosecond discontinuities, where events can be precisely placed in time to cause worst-case conditions, have shown that upper noise margins become negative.

Results in Table 2 highlight the need for precharge using BIAS V_{CC} on devices that either do not have optimized I/Os for backplane environments (such as ABT and LVT) or have small noise margins (such as GTLP). Also, only upper-noise-margin values are presented because simulation and laboratory measurements show this to be the worst-case situation.

The designer must determine what noise-margin level is required for a system. For example, if 500 mV of upper noise margin is not sufficient, while 690 mV provides greater confidence, precharge should be used in live-insertion applications of the ABTE device.

Conclusion

Live insertion and its accompanying side effect, the nanosecond discontinuity, are present concerns and will continue to be of concern for the board-level designer. Several factors associated with a live-insertion event need to be considered. Items such as software controllability of the driver, outputs placed in the high-impedance state, the state of the bus and output prior to insertion, connector-pin resistivity, and I/O capacitance must be carefully analyzed and optimized. Simulation tools aid in proving these systems prior to manufacturing.

Simulations have shown that live insertion can result in erroneous data values (especially evident in lightly loaded system topologies). Test data has also captured live-insertion glitches, but has been unable to capture the worst-case magnitudes of these events due to the evasiveness of such phenomena. Correlation between test and measurement data provides confidence in the simulations, and has reassured that the worst-case phenomena simulated are very possible in real systems.

GTLP technology is susceptible to these glitches because it is implemented in bus configurations intended to be hot plugged and provides relatively small high and low noise margins. Precautionary measures should be taken using precharge circuitry to reduce the effects of live insertion.

For similar technologies, such as ABT, ABTE, LVT, and VME, live-insertion events continue to cause significant noise-margin reduction and must be analyzed and designed carefully to ensure that live-insertion scenarios do not adversely affect the integrity of the driven and monitored signals. However, newer ABTE and VME technologies, with reduced input thresholds and increased noise margins, further improve device toleration of live-insertion events and might help reduce the types of hot-swap protection necessary to design a successful live-insertion system.

Glossary

ABT — Advanced BiCMOS Technology

ABTE — Advanced BiCMOS Technology for Enhanced Transceiver Logic (ETL)

GTL — Gunning Transceiver Logic. Operates at signal levels of V_{TT} = 1.2 V, V_{REF} = 0.8 V and V_{OL} = 0.4 V. GTL+ is a derivative of GTL that operates at higher-noise-margin signal levels of V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{OL} = 0.55 V and moves V_{REF} from the normal ground-bounce area.

GTLP — Gunning Transceiver Logic Plus. Normally associated with slower-edge-rate devices optimized for distributed loads that allow higher-frequency operation in heavily loaded backplane applications.

Nanosecond discontinuity — Very fast connect and disconnect phenomena that occur between two conductive bodies when they are under insufficient normal force (the force perpendicular to the interface that keeps the interface under pressure) and in motion relative to one another. This condition occurs at the initial moments of connection and the final moments of a disconnect in any electrical connector.

I_{off} — Maximum leakage current into or out of the input or output transistors when forcing the input or output to 4.5 V and V_{CC} = 0 V

I_{OZPD} — Current that flows into or out of the output stage when the device is being powered down from the high-impedance state

I_{OZPU} — Current that flows into or out of the output stage when the device is being powered up from the high-impedance state

LVT — Low-Voltage Technology TI ABT products specifically designed for 3.3-V operation

PU3S — Power-up 3-state. TIs internal integrated circuitry designed to keep the output structure from turning on while the device is being powered up or powered down.

R_{TT} — Bus-line termination resistance. R_{TT} should be equal to Z for incident-wave switching and optimum signal integrity.

Z — Bus-line loaded impedance. A modification of the natural impedance as a result of capacitive loading and other system characteristics.

Z_O — Bus-line natural impedance. It is determined by physical specific line construction and dimensions.

Acknowledgements

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