

Application Brief

Protecting 12-V MSDI Devices in a 24-V System



Ishraq Khandaker

The [TIC12400-Q1](#) and [TIC10024-Q1](#) devices are 24-input Multiple Switch Detection Interface (MSDI) devices designed to detect the external mechanical switch status in a 12-V automotive system by acting as a low-power consumption interface between the switches and the low-voltage microcontroller. Although these devices cannot be directly implemented in a 24-V system, users can implement an input protection circuit and enable operation in 24-V systems.

Input Protection Circuit

The maximum recommended voltage for the voltages at INx pins is 35 V. While these devices have the capability to operate under recommended conditions in a 24-V system, the ratings of the devices will be violated for the following conditions:

- Jump start condition (48 V)
- ISO 7637-2 battery transients (–600 V to 330 V)
- ISO 16750-2 load dump up to 202-V (unsuppressed, 65-V suppressed)

Figure 1 shows the proposed input protection circuit to protect the MSDI from the previously-listed conditions. Note that the protection circuit varies between the battery-connected switches and the ground-connected ones.

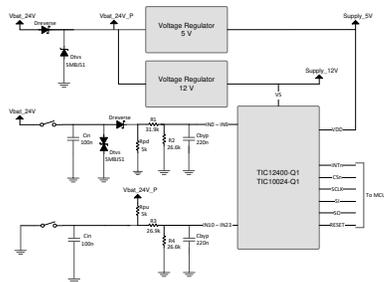


Figure 1. Proposed Input Protection Circuit

Selecting a TVS Diode

The transient voltage suppression (TVS) diode selected should be based on the stand-off voltage (V_r) to ensure proper operation of the system during jump-start condition. A TVS with 51-V stand-off voltage is a

good option to avoid any conduction at 48 V. Also, a 48-V stand-off may not be sufficient for the suppressed load dump, as discussed later in this section.

It is important to ensure that the selected TVS diode is able to shunt the necessary amount of current from the pulses without being damaged. Among the ISO 7637-2 transient pulses, Pulse 2a will require the TVS diode to shunt the most current, up to 56 A based on the peak pulse voltage (112 V) and input impedance (2 Ω). The other pulses have lower voltage peak or higher input impedance. Therefore, if the protection circuit can withstand ISO 7637-2 Pulse 2a, it will be able to withstand other pulses.

Most TVS diode data sheets specify the parameters based on the 10/1000- μ s waveform, which differs from the ones specified in the ISO 7637-2. The relevant peak pulse current and clamping voltage for the ISO 7637-2 can be estimated using the peak pulse power rating curve and electrical characteristics table from the TVS data sheet along with:

$$I_{pp} \text{ for } T \mu\text{s pulse} = \frac{(P_{pp} @ T \mu\text{s})}{(P_{pp} @ 1000 \mu\text{s})} \times \left(I_{pp} @ \frac{10}{1000} \mu\text{s} \right) \quad (1)$$

$$I_p = (V_{in} - V_{c \max}) / R_i \quad (2)$$

$$V_c = (I_p / I_{pp}) (V_{c \max} - V_{br \max}) + V_{br \max} \quad (3)$$

where

- I_p = actual test pulse current
- I_{pp} = max peak pulse current from EC table
- V_c = clamping voltage at I_p
- $V_{c \max}$ = max specified clamping voltage, reached at I_{pp}
- $V_{(br)\max}$ = upper limit of breakdown voltage from EC table
- P_{pp} = peak pulse power from data sheet curve
- R_i = input impedance for ISO 7637-2 pulses

Following the previous equations with the configuration in Figure 2, Pulse 2a (50 μ s) will generate a pulse current (I_p) of 14.8 A and the TVS will clamp to 74.7 V (V_c). Given these calculations and the equations explained in the *Resistor Divider and Low Pass Filter* section, the SMBJ diode will be sufficient to protect the MSDI from the worst ISO 7637-2 pulse. Note that a bidirectional TVS diode is recommended to clamp the voltage across C_{in} when the circuit is exposed to the negative pulses. If the system design does not include C_{in} , a unidirectional TVS diode shall be sufficient and placed at the cathode of the reverse protection diode. Furthermore, if ground-connected switches are pulled up to the protected side of the battery, protection diodes are not necessary at those INx pins.

The SMBJ51 TVS diode is also sufficient to protect the device against the suppressed load dump pulse, which is clamped to 65 V in the alternator. It is critical that the system side TVS, in this case, has higher breakdown and clamping voltages to allow the alternator TVS to shunt all of the current from the load dump. The system side TVS will not see enough current to break down and hence, the resistor dividers will only see 65 V. For the unsuppressed load dump, a TVS with a higher peak pulse current rating, such as the Littelfuse SLD series, must be used instead of the SMBJ51.

Selecting a Reverse Polarity Protection Diode

In the case where bidirectional TVS diodes are used, a Schottky diode rated higher than the maximum clamping voltage will be sufficient as long as the TVS is connected at the anode of the Schottky diode. If unidirectional TVS are used, the Schottky diode must be placed before the TVS and its reverse voltage must be rated above the 220 V produced by Pulse 3a.

Resistor Divider and Low Pass Filter

In addition to the diode protection, a resistor divider must be used at the INx pins to accommodate for the MSDI comparator thresholds and user logic thresholds for a given 24-V application.

Consider that the logic at the INx pins should be LOW when the voltage at the pin is ≤ 4 V and HIGH when the voltage is ≥ 5 V. The resistor divider must ensure that a 5-V input is divided down to the appropriate comparator threshold value to output HIGH. In this case the 2-V setting for the THRES_COMP register is the best option; see the *Electrical Characteristics* section of the [TIC12400 data sheet](#) for details. The resistor divider must then divide the input voltage by 2.2 to meet the comparator thresholds. These

resistors are also dependent on the value of C_{byp} and the desired low pass filter (LPF) based on application needs.

Lab Test and Results

The proposed input protection circuit, along with the TIC12400-Q1 EVM, was tested for the double battery condition and ISO 7637-2 Pulse 2a as the following images show.

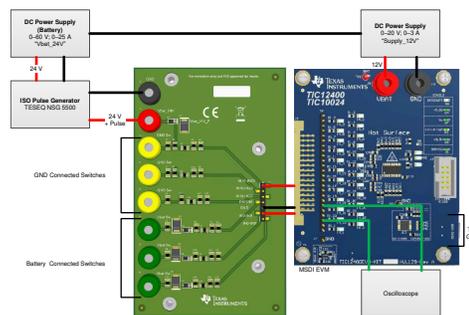


Figure 2. Test Setup



Figure 3. Double Battery Condition, Switches Connected

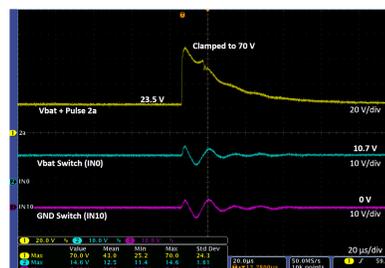


Figure 4. Pulse 2a Applied, Switches Connected

As Figure 3 and Figure 4 illustrate, the expected logic and voltages per the proposed circuit are obtained when the switches are closed, without violating recommended operating conditions. The parasitic inductances of the wires and capacitances of the board may cause some LC oscillations, but this ripple does not impact the INx pin logic when tested with the EVM GUI.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated