Application Report
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Using the AGC, DRC and Beep Generator Function in TLV320AIC3204/54/3100/10/11/20/36 Devices

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ABSTRACT

The new AIC devices have the built-in feature of AGC, DRC, and the Beep Generator. Using these features requires initializing a group of control registers inside the TLV320AIC3204/3254/3100/3110/3111/3120/36 devices. This application report is intended to help the user how to handle these features and what are the applications of these features.

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1 AGC

1.1 Introduction

The AGC feature is included for ADC recording. In TLV320AIC3100/3110/3111/3120, this feature is only present for the microphone input, but in devices like TLV320AIC3204/3254/36, this feature is included in the stereo ADC's and is applicable only for Microphone input. This feature helps the users to improve analog recording performance.

Automatic Gain control (AGC) is an algorithm that is used to maintain nominally constant output voltage at the output of Programmable gain Amplifier (PGA) that feeds the ADC. This smart feature is used when the amplitude of the input signal is varying dynamically and frequently, AGC can adjust the gain of PGA so that the output is held at a constant level (called Target level). Without AGC, the gain of PGA would have been manually changed for the frequently changing the input signal. An example application for AGC use is when a person speaking on phone is moving closer or far away from microphone so the input is either weak or loud. Use of AGC over fixed gain PGA thus helps in adjusting the signal at fixed level to meet the real-world conditions. AGC module uses low pass filtered version of input to calculate the absolute average of the signal and it operates at ADC sampling frequency rate.

Using the AGC feature built in TI devices requires loading up of proper registers either by I2C™ or SPI interface. This application note is intended to provide a detailed explanation and example-setup for using AGC in TI devices like TLV320AIC3204/3254, TLV320AIC3100/3110/3111/3120 and TLV320AIC36.

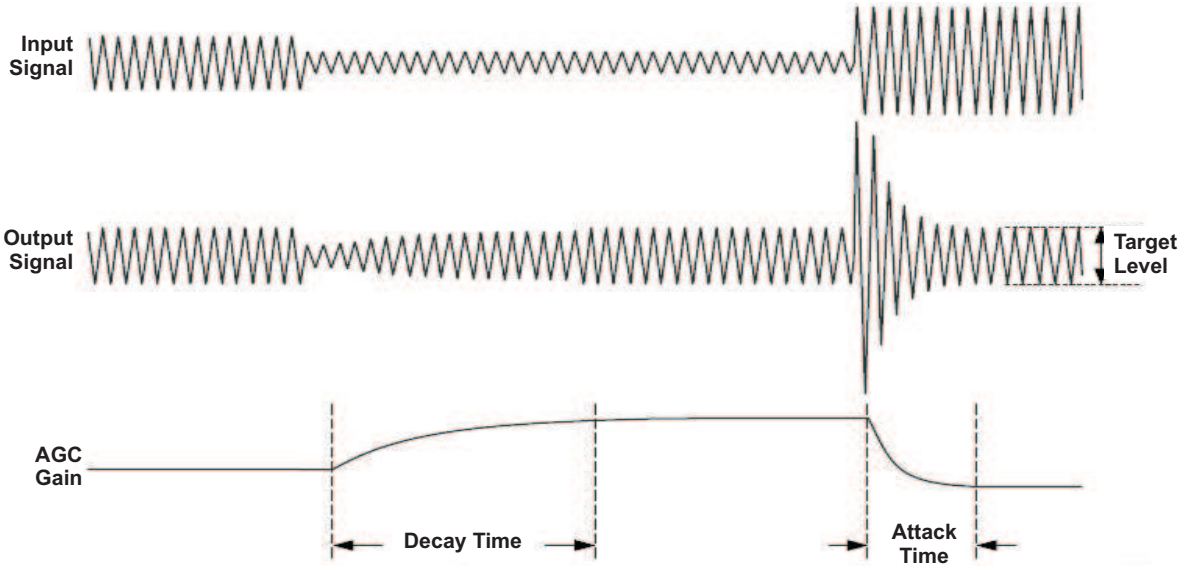

Figure 1. AGC Function

1.2 AGC Parameters

The AGC algorithm has different parameters which can be used depending upon the requirements of the user. The parameters and their description are given in Table 1.

Table 1. AGC Parameters Description

AGC PARAMETERS	DESCRIPTION
Target Level	This represents the nominal output level that the AGC attempts to hold the ADC output signal. It is expressed relative to full scale range of the ADC range (in db) so it is recommended that the target level be set with enough margin to avoid clipping of loud signals.
Attack Time	This determines how quickly the AGC circuitry decreases the PGA gain when the input signal exceeds the target level. It is expressed in fractions of ADC sampling rates.
Decay time	This determines how quickly the AGC circuitry increases the PGA gain when the input signal falls below the target level. It is expressed in fractions of ADC sampling rates.
Noise Threshold	A threshold used to differentiate noise from very weak signals so that the PGA does not amplify the noise also. So is the signal is below this reference, it is considered as noise and the output of ADC is 0 db.
Maximum PGA gain	Allows the user to restrict the maximum gain of PGA. Can be used in very noisy environments when noise is greater than the set noise threshold so as not to amplify the noise too much.
Hysteresis	Hysteresis around the noise threshold avoids fluctuation of ADC output between target and no signal when the signal is around noise threshold. So the signal around noise threshold, it has to rise above the hysteresis to be amplified to target level. Reverse if a signal is around noise threshold, it has to fall below hysteresis to be considered as noise and set to 0db.
Noise Debounce time	If the signal level falls below noise threshold level, it has to stay there for a time greater than Noise debounce time, only then the ADC output is set to 0 to avoid false noise artifact effects.
Signal Debounce time	If the signal level goes above the noise threshold level, it has to stay there for at least Signal debounce time to allow PGA to switch to target level to prevent false switching.

For example, if the noise threshold selected is low, the larger noise may be picked up and amplified with a large gain. If the noise threshold selected is set thigh, the weaker signal may be considered by the AGC as noise and fail to be amplified. Similarly, if the maximum gain applicable variable is kept too high, then any noise which is above the noise threshold may increae and create a noisy output; but if it is kept low, normal speech signals may not be gained up enough to reach the target gain level at the output.

The selection of the AGC variables depends on the practical application and environment. Some variables become more important under certain conditions. For example, if the input signal is often hovering around the noise threshold, hysteresis and debounce time become critical.

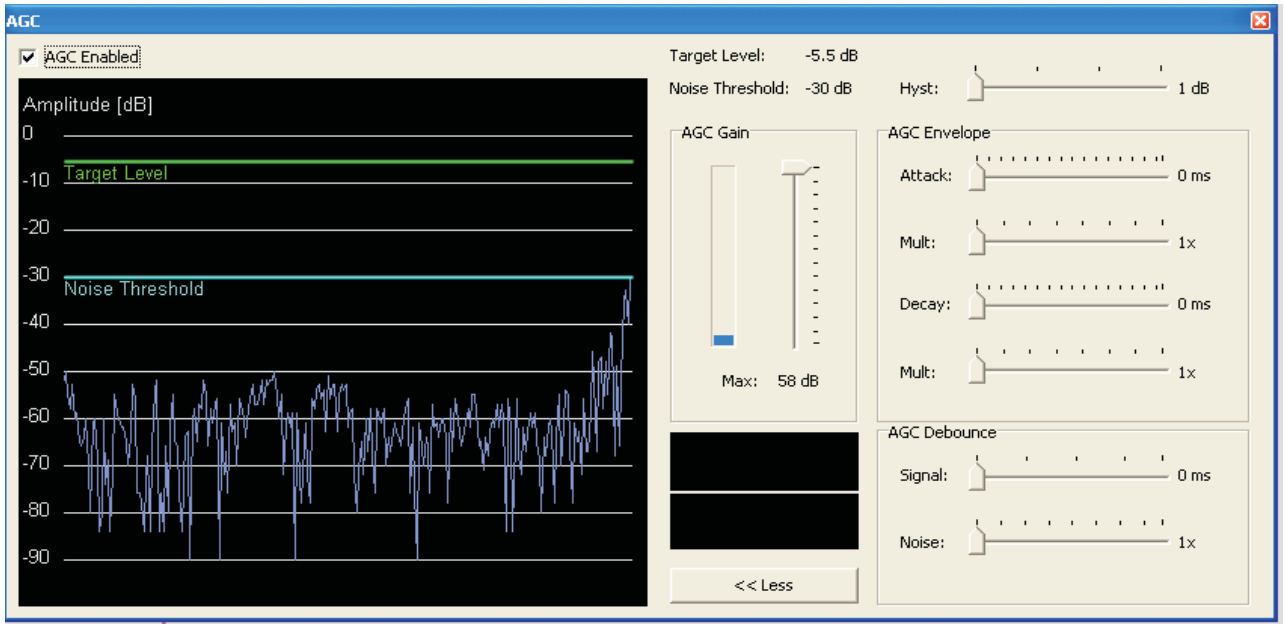

Figure 2. A Snapshot From Control Software Showing GUI Settings for AGC Parameters

1.3 Control Registers and Status

The AGC parameters mentioned in Table 2 should be written with proper values at different locations in memory of AIC devices. Table 2 shows which parameters are present at what locations for devices like TLV320AIC3204/3254/36. Table 3 for devices like TLV320AIC3100/3110/3111/3120.

Table 2. TLV320AIC3204/3254/36 AGC Parameter Settings(1)

AGC Variable	Control Register Left ADC	Control Register Right ADC	Bit
AGC enable	Page0, Register86	Page0, Register94	D(7)
Target Level(dB)	Page0, Register86	Page0, Register94	D(6:4)
Hysteresis(dB)	Page0, Register87	Page0, Register95	D(7:6)
Attack Time(2)	Page0, Register89	Page0, Register97	D(7:0)
Decay time(2)	Page0, Register90	Page0, Register98	D(7:0)
Noise Threshold(dB)	Page0, Register87	Page0, Register95	D(5:1)
MaxPGA applicable(dB)	Page0, Register88	Page0, Register96	D(6:0)
Noise Debounce time(2)	Page0, Register91	Page0, Register99	D(4:0)
Signal Debounce time(2)	Page0, Register92	Page0, Register100	D(3:0)
Gain Applied by AGC(dB)(3)	Page0, Register93	Page0, Register101	D(7:0)
AGC noise threshold flag(3)	Page0, Register45(sticky flag)(4) Page0,Register47(non-sticky-flag)	Page0, Register45(sticky flag)(4) Page0,Register47(non-sticky-flag)	D(6:5)
AGC saturation flag(3)	Page0, Register36	Page0, Register36	D(5),D(1)
ADC saturation flag(3)	Page0, Register42(sticky flag)(4) Page0,Register43(non-sticky-flag)	Page0, Register42(sticky flag)(4) Page0,Register43(non-sticky-flag)	D(3:2)

(1) For the range of values that can be applied to these parameters, see data sheet of the device under test.
(2) These times are as a function of ADC sampling clock periods.
(3) These parameters are just read-only.
(4) Sticky flag bits. These are read-only bits. They are automatically cleared once they are read and are set only if the source trigger occurs again.

Status Variables

1. **Gain applied by AGC** can be read by Register93 and Register101.
2. **AGC noise threshold Flag** is a read-only flag indicating that the input signal has levels lower than the Noise Threshold, and thus is detected as noise (or silence). In such a condition the AGC applies a gain of 0 dB.
3. **AGC saturation flag** is a read-only flag indicating that the ADC output signal has not reached its Target Level. However, the AGC is unable to increase the gain further because the required gain is higher than the Maximum Allowed PGA gain. Such a situation can happen when the input signal has very low energy and the Noise Threshold is also set very low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.
4. **ADC Saturation flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC Target Level is kept very high and the energy in the input signal increases faster than the Attack Time.

Table 3. TLV320AIC3100/3110/3111/3120 AGC Parameter Settings(1)(2)

AGC Variable	Control Register Left ADC	Bit
AGC enable	Page0, Register86	D(7)
Target Level(dB)	Page0, Register86	D(6:4)
Hysteresis(dB)	Page0, Register87	D(7:6)
Attack Time(3)	Page0, Register89	D(7:0)
Decay time(3)	Page0, Register90	D(7:0)
Noise Threshold(dB)	Page0, Register87	D(5:1)

(1) For the range of values that can be applied to these parameters, see data sheet of the device under test
(2) For explanation to sticky flag and other flags, see above this table.
(3) These times are as a function of ADC sampling clock periods.

Table 3. TLV320AIC3100/3110/3111/3120 AGC Parameter Settings[1][2] (continued)

AGC Variable	Control Register Left ADC	Bit
MaxPGA applicable(dB)	Page0, Register88	D(6:0)
Noise Debounce time[3]	Page0, Register91	D(4:0)
Signal Debounce time[3]	Page0, Register92	D(3:0)
Gain Applied by AGC(dB)[4]	Page0, Register93	D(7:0)
AGC noise threshold flag[4]	Page0, Register45(sticky flag)[5]	D(6)
AGC saturation flag[4]	Page0, Register36	D(5)
ADC saturation flag[4]	Page0, Register39(sticky flag)[5]	D(3)

(4) These parameters are just read-only.

(5) Sticky flag bits. These are read-only bits. They are automatically cleared once they are read and are set only if the source trigger occurs again

1.4 Example

Note that for writing to the corresponding register of that variable, just use the syntax w AIC_address Register_address Data where AIC_address is the address of the device under use in Hex, Register_address and Data in Hex.

1. When the noise is very low as compared to the signal, the following values can be used in the application.

   (a) Target gain = –5.5 dB
   (b) Attack time = 20 ms and decay time = 500 ms
   (c) Noise threshold = –90 dB
   (d) Maximum gain applicable = 50 dB
   (e) Hysteresis disabled.
   (f) Debounce time from normal to silence = 0 ms
   (g) Debounce time from silence to normal = 0 ms

   Note that with Example 1 settings, the background noise may become considerable when noise is beyond the noise threshold because the maximum gain applicable is higher (+50 dB) and thus big noise may get gained up with high gain.

2. When noise is relatively large, the following values may be used in the application

   (a) Target gain = –10 dB
   (b) Attack time = 20 ms and decay time = 500 ms
   (c) Noise threshold = –90 dB
   (d) Maximum gain applicable= 40 dB
   (e) Hysteresis = 2 dB
   (f) Debounce time from normal to silence = 2 ms
   (g) Debounce time from silence to normal = 0 ms.

   Note that the Example 2 settings, even though the noise is above the noise threshold, will not be as much gain as in Example 1 as the Maximum gain applicable has been reduced.

Script for the above example assuming TLV320AIC3111 device is in use assuming Fs=44.1kHz with:

```
w 30 00 00  #go to page 0
 w 0 56 A0  3#Enable AGC, set Target gain = –10 dB
w 30 57 7E  #set hysteresis = 2 dB, Noise threshold = –90 dB
w 30 58 50  #set Maximum gain = 40 dB
w 30 59 08  #set attack time = 20 ms
w 30 5A 32  #Decay time = 500 ms
w 30 5B 00  #Noise debounce time = 0 ms
w 30 5C 06  #signal debounce time = 2 ms
```

ADC gain and powering up is not taken into account here, That part of code must be added.

2 DRC

2.1 Introduction

Dynamic Range compression (DRC) is included at the DAC side of TI codec devices that monitors the output of DAC and adjusts the gain of DAC so as to avoid clipping of loud signals. So when the output of DAC is low, DRC increases the applied gain so as to make the signal sound loud. Contrary to this, if a peaking signal is detected it autonomously reduces the applied gain to avoid the hard clipping. This results in sounds more pleasing to the ear as well as sounding louder during nominal periods. DRC typically works on the filtered version of the input signal. As the low frequency signals contain no audio information, but they have significant amount of energy content. So the input of DAC is fed to a high pass filter and then the output of this high pass filter is fed to a low pass filter. The output of low pass filter is used in the energy estimation of the signal and the output of high pass filter is fed to one of the processing blocks of DAC. These filters are implemented as first order IIR filters given by:

For TLV320AIC3204/3254/36

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}}$$

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}}$$

For TLV320AIC3100/3110/3111/3120

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}}$$

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}}$$

The co-efficient No, N1, D1 are user programmable. These are 16 bits(2 Registers wide) for TLV320AIC3100/3110/3111/3120 and 24 bits(3 Registers wide) for TLV320AIC3204/3254.

Table 4. DRC HPF and LPF Coefficients for TLV320AIC3204/3254/36

Coefficient	Location
HPF N0	C71 Page46, Register 52 to 54
HPF N1	C72 Page46, Register 56 to 58
HPF D1	C73 Page46, Register 60 to 62
LPF N0	C74 Page46, Register 64 to 66
LPF N1	C75 Page46, Register 68 to 70
LPF N2	C76 Page46, Register 72 to 74

Table 5. DRC HPF and LPF Coefficients for TLV320AIC3100/3110/3111/3120

Coefficient	Location
HPF N0	C71 Page9, Register 14 and 15
HPF N1	C72 Page9, Register 16 and 17
HPF D1	C73 Page9, Register 18 and 19
LPF N0	C74 Page9, Register 20 and 21
LPF N1	C75 Page9, Register 22 and 23
LPF N2	C76 Page9, Register 24 and 25

2.2 DRC Parameters

The DRC algorithm has different parameters which can be used depending upon the requirements of the user. The parameters and their description are given in Table 6.

Table 6. DRC Parameters Description

Variable	Description
PGA gain	Depending upon the threshold set, DAC input is gained up this amount if input is less than threshold.
Threshold	DRC threshold represents the level of the DAC playback signal at which the gain compression becomes active. Keeping the DRC threshold value too high may not leave enough time for the DRC block to detect peaking signals, and can cause excessive distortion at the outputs. Keeping the DRC threshold value too low can limit the perceived loudness of the output signal.
Hysteresis	It is a programmable window around the programmed DRC threshold that must be exceeded for the disabled DRC to become enabled, or the enabled DRC to become disabled. DRC hysteresis feature prevents the rapid activation and de-activation of gain compression in the DRC in cases when the output of the DAC digital volume control rapidly fluctuates in a narrow region around the programmed DRC threshold.
Hold time	When the input signal to the DAC falls below the threshold, it has to stay below it for atleast the hold time to enable gaining it up. This parameter helps in minimizing audible artifact effects.
Attack rate	When the output of the DAC digital volume control exceeds the programmed DRC threshold, the gain applied in the DAC digital volume control is progressively reduced to avoid the signal from saturating the channel. This process of reducing the applied gain is called attack. To avoid audible artifacts, the gain is reduced slowly with a rate equaling the attack rate.
Decay rate	When the DRC detects a reduction in output signal swing beyond the programmed DRC threshold, the DRC enters a decay state, where the applied gain in the digital-volume control is gradually increased to programmed values. To avoid audible artifacts, the gain is slowly increased with a rate equal to the decay rate.

Selection of the values for each of these parameters strictly depends upon application and environmental conditions.

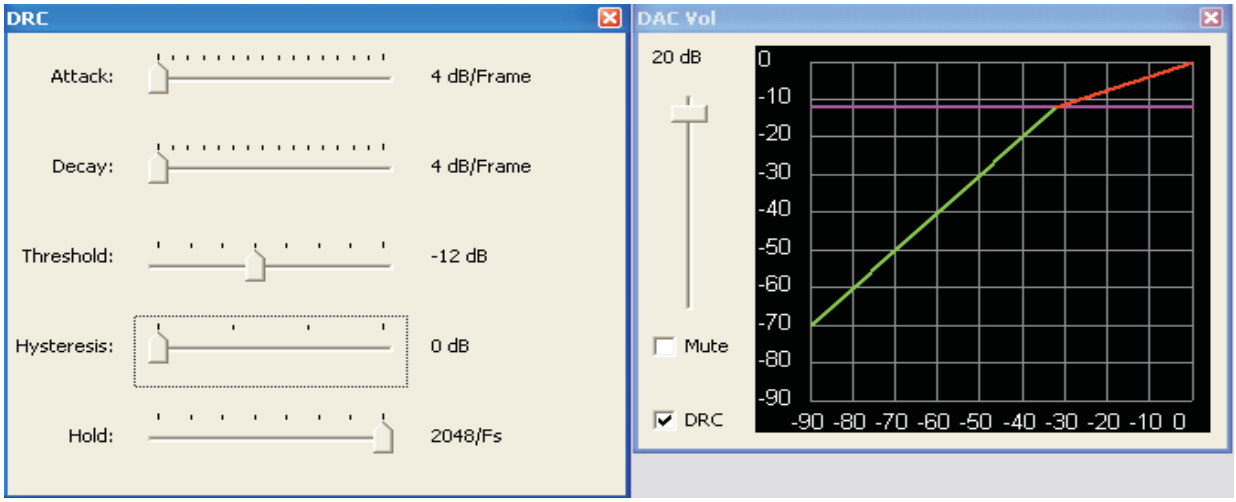

Figure 3. A Snapshot From Control Software Showing GUI Settings for DRC Parameters

2.3 Control Registers and Status

The DRC parameters mentioned in Table 6 should be written with proper values at different locations in memory of AIC devices. Table 7 shows which parameters are present at what locations for devices like TLV320AIC3204/3254/36/3100/3110/3111/3120.

Table 7. TLV320AIC3204/3254/36/3100/3110/3111/3120 DRC Parameter Settings[(1)]

DRC Variable	Control Register Left DAC	Control Register Right DAC	Bit
DRC enable	Page0, Register 68	Page0, Register 68	D(6:5)
Threshold(dB)	Page0, Register 68	Page0, Register 68	D(4:2)
Attack time[(2)]	Page0, Register 70	Page0, Register 70	D(7:4)
Decay time[(2)]	Page0, Register 70	Page0, Register 70	D(3:0)
Hold time(ms)	Page0, Register 69	Page0, Register 69	D(6:3)
Hysteresis(dB)	Page0, Register 68	Page0, Register 68	D(1:0)
DAC gain(dB)	Page0, Register 65	Page0, Register 66	D(7:0)
DRC signal threshold flag[(3)]	Page0, Register44(sticky) Page0, Register46(non-sticky)	Page0, Register44(sticky) Page0, Register46(non-sticky)	D(3:2)

(1) For the range of values that can be applied to these parameters, see data sheet of the device under test.
(2) These times are as a function of ADC sampling clock periods.
(3) For Sticky flags, see the AGC section.

Status Variable
DRC signal threshold flag is set when the Signal exceeds the threshold, so DRC compression becomes active. This flag has both the sticky and non-sticky version.

2.4 Example

Note that for writing to the corresponding register of that variable, just use the syntax w AIC_address Register_address Data where AIC_address is the address of the device under use in Hex, Register_address and Data in Hex.

PGA gain = 12 dB
Threshold = –24 dB
Hysteresis = 3 dB
Hold time = 0 ms

Attack rate = 2.4414e–4 dB per 1/DAC_fS
Decay rate = 3.9062e–3 dB per 1/DAC_fS

Script for the above example considering Fs=44.1kHz with:

```
w 30 00 00  #go to page 0
w 30 41 18  #make gain of Left DAC=12 dB
w 30 42 18  #make gain of right DAC=12 dB
w 30 44 7F  #Enable DRC for both DAC channels, set threshold=24dB, Hysteresis= 3dB
w 30 45 00  #Make DRC hold=0 ms
w 30 46 E2  #Make DRC attack and Decay as required
```

Data routing to DAC, powering up the DAC channel and setting up the High-pass and Low-pass filter coefficients are not taken into account and should be written in similar manner after looking at the register concerned from the data sheet.

3 Beep Generator

3.1 Introduction

A special function has also been included in the processing block PRB_P25 for generating a digital sine-wave signal that is sent to the DAC. This is intended for generating key-click sounds for user feedback. The sine wave generator is flexible, and is completely register programmable via 9 registers of 8 bits each to provide many different sounds.

3.2 Beep Generator Parameters

Table 8. Beep Generator Parameters Description

Variable	Description
Volume	Left and Right Beep channels have independent volume control register bits.
Duration	Bursts of sine and cosine can be generated of duration based on 3 registers which are based on DAC clock periods.
Frequency	Any frequency till fs/2 can be generated by writing appropriate value to registers.

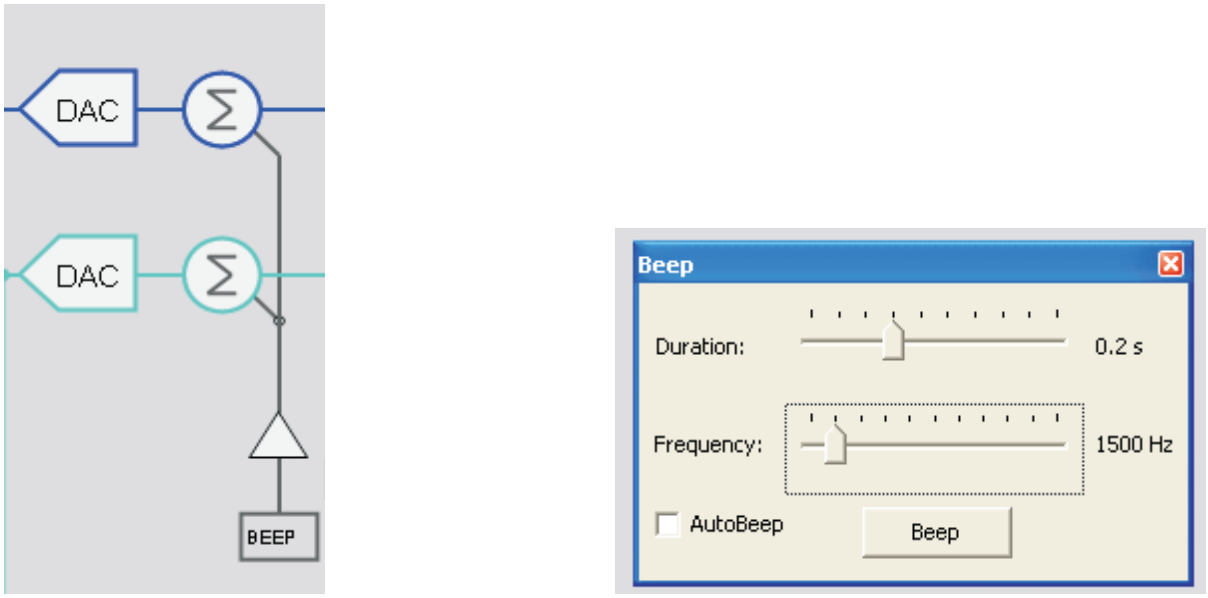

Figure 4. A Snapshot From Control Software Showing GUI Settings for Beep Generator Parameters

3.3 Register Settings

Programming page 0 / register 71 through page 0 / register 79 (8 bits each) completely controls the functionality of this generator and allows for differentiating sounds. Variable and its corresponding register locations can be seen in Table 9.

Table 9. TLV320AIC3204/3254/36/3100/3110/3111/3120 Beep Generator Parameter Settings[1]

Variable	Left DAC Control Register	Right DAC Control Register	Bits
Beep Enable	Page0, Register71	Page0, Register71	D7
Volume control	Page0, Register71	Page0, Register72	D(5:0), D(7:6)
Duration(sample length)	Page0, Register73,74,75	Page0, Register73,74,75	24 bits from 3 registers
Frequency(Sin(x) and Cos(x))[2]	Page0, Register76,77,78,79	Page0, Register76,77,78,79	D(7:0)

(1) For the range of values that can be applied to these parameters, see data sheet of the device under test.

(2) Programmed Value for these registers is Beep Sin(x)(7:0), where
Sin(x) = sin(2 x π x Fin/Fs), and Cos(x) = cos(2 x π x Fin/Fs) where Fin is desired beep frequency and Fs is DAC sample rate.

We have Sin(x) and Cos(x) registers to set because the Sine wave tone generated is calculated from Sin and cosine terms from the formula
Sin{(n+1)x} = 2 Sin(nx)Cos(x) - Sin(n-1)x
Where x=2 x π x Fin/Fs Fin = Desired tone frequency, Fs = Sampling frequency

Now for setting up frequency and beep length, following equations should be used and fed to the registers:
Sine = dec2hex(round(sin(2 x π x Fin/Fs) x 2^{15}))
Cosine =dec2hex(round(cos(2 x π x Fin/Fs) x 2^{15}))
For the above two equations, Fin(desired tone frequency) and Fs is the sampling frequency are known, so Sine and Cosine Coefficients can be calculated and written to registers76,77,78,79.
Beep Length =dec2hex(floor(Fs x Cycle/Fin))
Here cycle=number of cycles that are needed for a required time. So, once the duration of beep is known, one can say N x T = Time where N=number of cycles and T=1/Fin. So in this way N can be calculated as T(Beep time period) and Time(Beep Duration) are known. Now these cycles should be wholly related to sampling period. So, from the above equation beep length can be calculated and written in the registers 73,74,75.

3.4 Example

	LEFT BEEP CONTROL	RIGHT BEEP CONTROL	BEEP LENGTH			SINE		CONSINE	
			MSB	MID	LSB	MSB	LSB	MSB	LSB
REGISTER	71	72	73	74	75	76	77	78	79

So for 2kHz tone beep for 2 seconds,
Fs=44.1Khz, Fin=2kHz. So using N x T=time, putting T = 1/2000 and time = 2 provides N = 4000.
Now using Beep Length=dec2hex(floor(48 x 4000/2)) = dec2hex(96000) = 0x17700.
So Beep Length = 0x017700 is written in 3 registers 73,74,75.

Now Sine and Cosine coefficients are calculated from equations
Sine=dec2hex(round(Sin(2 x π x Fin/Fs) x 2^{15})), putting values we get
Sine =d ec2hex(round(9211))
Sine = 0x23FB, so Register 76 and 77 are written 0x23 and 0xFB respectively.

Similarly calculating Cosine coefficient
Cosine = 0x7AD7, so registers 78 and 79 are written 0x7A and 0xD7 respectively .

Script for setting up the previous example assuming Fs=48kHz with:

```
w 30 00 00  #go to page 0
w 30 49 01  #Writing Beep length to registers 73,74,75 and 30 being the Codec address.
w 30 4A 77  #73=49 in hex and so on.
w 30 4B 00  #Now writing Sine and cosine coefficients MSB first then LSB in
w 30 4C 23
w 30 4D FB  #76,77,78,79
w 30 4E 7A
w 30 4F D7
#now that all coefficient settings are done, we can move on to control the volume of left and right
channel beep and turn on beep. Assuming Volume of left and right beep= –2dB
w 30 48 04  # Making gain of right –2dB and making right and left channel independent
w 30 47 84  #Making gain of left channel -2dB and turning on the beep.
```

DAC settings are not taken in account here.

4 References

1. Ultra low power Stereo Audio codec TLV320AIC3204 data sheet (SLOS602A).
2. Ultra low power Stereo Audio codec with embedded mini-DSP TLV320AIC3254 data sheet (SLAS549A).
3. Low-Power Audio Codec with Audio Processing and Mono Class-D Amplifier data sheet TLV320AIC3100 (SLAS667).
4. Low-Power Audio Codec with Audio Processing and Stereo Class-D Speaker Amplifier TLV320AIC3110 data sheet (SLAS647).
5. Low-Power Audio Codec with Embedded mini-DSP and Stereo Class-D Speaker Amplifier TLV320AIC3111 data sheet (SLAS644B).
6. Low-Power Mono Audio Codec with Embedded mini-DSP and Mono Class-D Speaker Amplifier TLV320AIC3120 data sheet (SLAS653).
7. Low Power Stereo Audio Codec with Embedded mini-DSP TLV320AIC36 data sheet (SBAS387).

Appendix A Sample Code

Here is a sample code for the user for the entire Codec setup for the registers for ADC, DRC and Beep Generator assuming device under use is TLV320AIC3111, Sampling frequency=44.1kHz and the following parameters:

AGC

Target gain = –10 dB
Attack time = 20 ms and decay time = 500 ms
Noise threshold = –90 dB
Maximum gain applicable= 40 dB
Hysteresis = 2 dB
Debounce time from normal to silence = 2 ms
Debounce time from silence to normal = 0 ms.

DRC

PGA gain = 12 dB
Threshold = –24 dB
Hysteresis = 3 dB
Hold time = 0 ms
Attack rate = 2.4414e–4 dB per 1/DAC_fS
Decay rate = 3.9062e–3 dB per 1/DAC_fS

Beep Generator

Tone frequency=2kHz
Beep length=2sec

```
# Start of the
code
w 30 00 00      #select page0
w 30 01 01      #software reset
w 30 04 07      #Set PLL_CLKIN=BLCK and CODEC_CLKIN=PLL_CLK
w 30 05 91      #PLL powered up, set PLL variable P=R=1
w 30 06 20      #Set PLL variable J=32
w 30 07 00      # Set PLL variable D(msb)=0
w 30 08 00      # D(lsb)=0
w 30 1B 01      # Mode=I2S, Word length=16, BCLK, WCLK are inputs to codec.
w 30 0B 84      #NDAC powered up and set to 4
w 30 0C 84      #MDAC powered up and set to 4
w 30 0D 00      #DOSR=128, DOSR(9:8)=0
w 30 0E 80      #DOSR(7:0)=128
w 30 12 84      #NADC powered up and set to 4
w 30 13 84      #MADC powered up and set to 4
w 30 14 80      #AOSR=128
w 30 3C 19      #DAC PRB set to PRB_P19
w 30 3D 04      # ADC PRB set to PRB_R4
w 30 3F D6      #Set the DAC datapath
w 30 00 01      #page 1 is selected
w 30 21 46      # De-pop, Driver power-on time=600ms, Step time=4ms
w 30 1F C6      #Power on HP drivers
w 30 23 88      #DAC_L routed to HPL, DAC_R routed to HPR
w 30 28 0E      #HPL driver unmuted and gain set to 1dB
```

```
w 30 29 0E      # HPR driver unmuted and gain set to 1dB
w 30 24 00      #Analog Volume control gain set to 0dB for HPL
w 30 25 00      # Analog Volume control gain set to 0dB for HPR
w 30 2E 0B      #MICBIAS=AVDD
w 30 30 40      #MIC with Rin=10k
w 30 31 40      #CM with Rin=10k
w 30 40 0C      #DAC unmated
w 30 51 80      #Power ADC channel
w 30 52 00      #Unmute ADC channel
#AGC settings
w 30 00 00      #go to page 0
w 30 56 A0      #Enable AGC, set Target gain= -10dB
w 30 57 7E      #set hysteresis=2dB, Noise threshold=-90dB
w 30 58 50      #set Maximum gain=40dB
w 30 59 08      #set attack time=20ms
w 30 5A 32      #Decay time=500ms
w 30 5B 00      #Noise debounce time=0ms
w 30 5C 06      #signal debounce time=2ms
#DRC settings
w 30 00 00      # go to page 0
w 30 41 18      #make gain of Left DAC=12 dB
w 30 42 18      #make gain of right DAC=12 dB
w 30 44 7F      #Enable DRC for both DAC channels, set threshold=24dB, Hysteresis= 3dB
w 30 45 00      #Make DRC hold=0 ms
w 30 46 E2      #Make DRC attack and Decay as required
#Beep Generator settings
w 30 00 00      # go to page 0
w 30 49 01      #Writing Beep length to registers 73,74,75 and 30 being the Codec address.
w 30 4A 77      #73=49 in hex and so on.
w 30 4B 00
w 30 4C 23      #Now writing Sine and cosine coefficients MSB first then LSB in register
w 30 4D FB      #76,77,78,79
w 30 4E 7A
w 30 4F D7
#now that all coefficient settings are done, we can move on to control the volume of left and right
channel beep and turn on beep. Lets assume Volume of left and right beep= -2dB
w 30 48 04      # Making gain of right –2dB and making right and left channel independent
w 30 47 84      #Making gain of left channel –2dB and turning on the beep.

##End of Code##
```

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