Technical White Paper

PCI Express® Generation 4 Compliance Test Report With TMUXHS4412

ABSTRACT

This technical paper describes how to set up and configure the HSDC092 evaluation board to test PCI Express® (PCIe®) Generation 4 CBB and AIC compliance test. A test report is presented and discussed.

Table of Contents

1 Introduction 1
2 Test Setup and Procedure 2
2.1 Test Board Configuration 2
2.2 Test Setup 3
2.3 Test Procedure 4
3 Test Report 5
4 Summary 7

List of Figures

Figure 2-1. HSDC092 Evaluation Module 2
Figure 2-2. PCI Express® 4.0 TX CBB, AIC Test Setup 3
Figure 3-1. Test Report of Presets - 1 5
Figure 3-2. ISI Test Report 6
Figure 3-3. Test Report of ISI Eye Diagram Test 6
Figure 3-4. ISI Eye Diagram 7

List of Tables

Table 2-1. PCI Express® 4.0 Compliance Test Configuration 3

Trademarks

1 Introduction

The TMUXHS4412 is an analog differential passive MUX or DEMUX that works for many high-speed differential interfaces for data rates up to 20 Gbps including PCI Express® 4.0.

This document presents a test report of PCI Express® 4.0 CBB, AIC compliance test with the TMUXHS4412 by using TI's HSDC092 EVM.

2 Test Setup and Procedure

A PCI Express® 4.0 CBB, AIC compliance test is required for any device to be listed on the PCI-SIG Integrators List. This section presents the test setup and test procedure of PCI Express® 4.0 CBB, AIC compliance test. The configuration of the HSDC092 evaluation board featuring the TMUXHS4412 is also discussed.

2.1 Test Board Configuration

The HSDC092 evaluation module is used for the PCI Express® 4.0 compliance test. U1, U2, U3, and U4 are replaced with the TMUXHS4412. It features two MUXes and two DEMUXes that can extend the transmission distance of a PCIe® Gen 4 8 × bus. The EVM can be directly plugged into a PCIe® slot on a server or PC motherboard using the PCIe® Edge connector on the board and paired with a PCIe® add-in card using one of the two PCIe® connectors on the EVM.

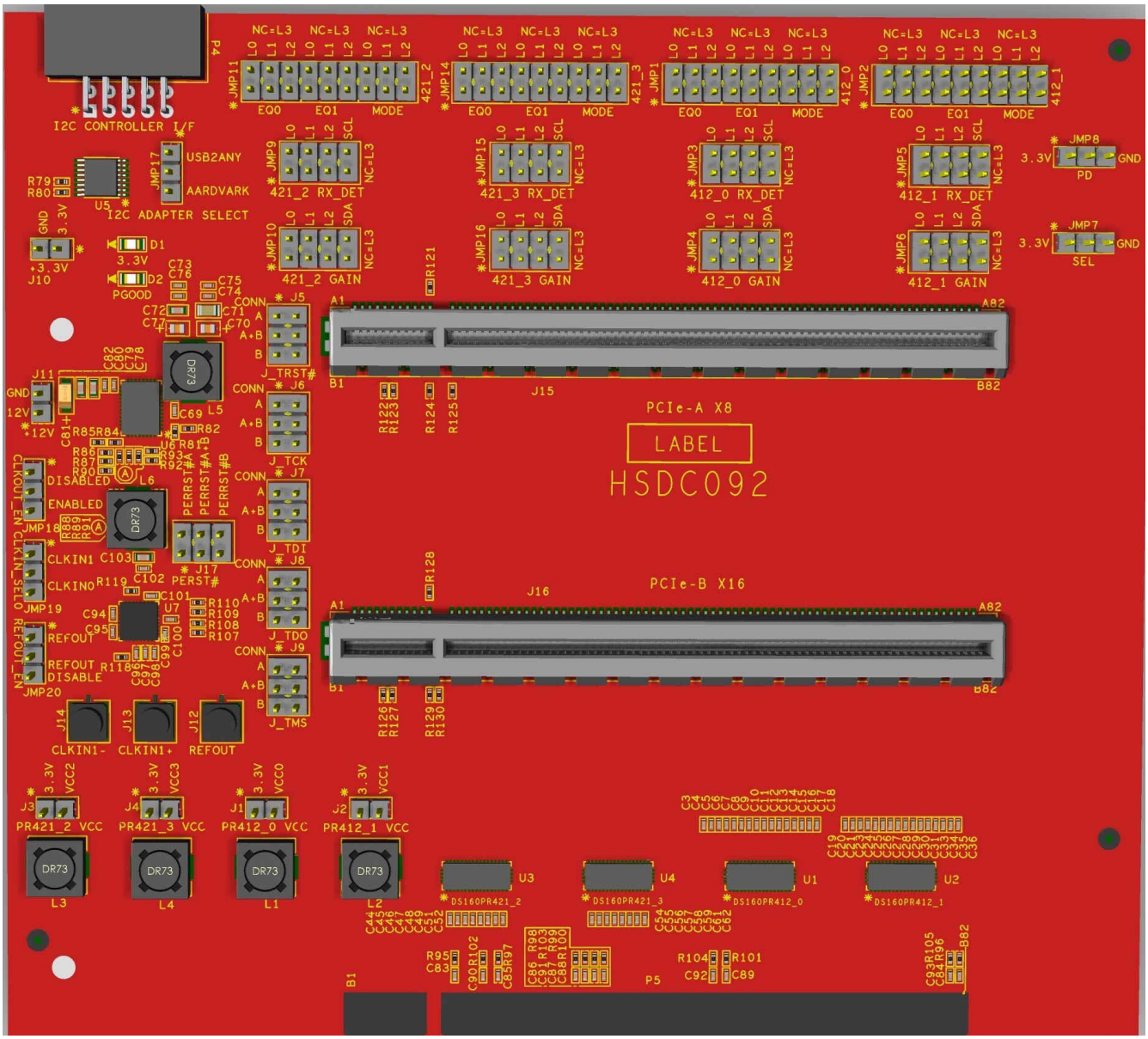


Figure 2-1. HSDC092 Evaluation Module

Table 2-1 lists the board configuration for PCI Express® 4.0 CBB, AIC compliance test.

Table 2-1. PCI Express® 4.0 Compliance Test Configuration

SHNT#	Header	SHNT Across Pins
1	JMP7	1–2 or 2–3
2	JMP8	2–3
3	JMP1	float
4	JMP2	float
5	JMP3	float
6	JMP4	float
7	JMP5	float
8	JMP6	float
9	JMP9	float
10	JMP10	float
11	JMP11	float
12	JMP14	float

2.2 Test Setup

Figure 2-2 is the setup for PCI Express® TX CBB, AIC compliance test. The required hardware includes:

1. HSDC092 evaluation board
2. PCI-SIG CBB4 board
3. CPI-SIG ISI board
4. TekTronic DPO77002SX scope

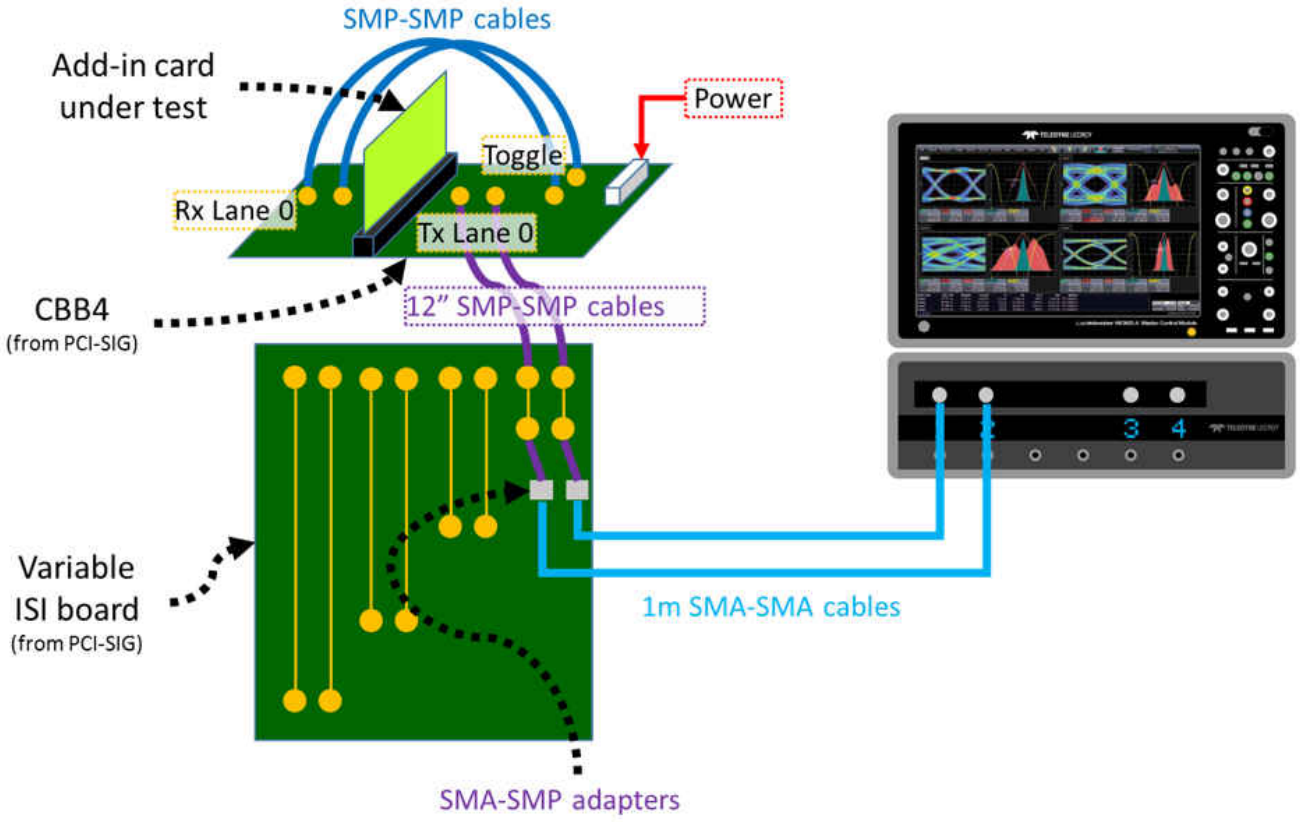


Figure 2-2. PCI Express® 4.0 TX CBB, AIC Test Setup

2.3 Test Procedure

The following steps show the test procedure:

1. Configure the HSDC092 evaluation board as detailed in Table 2-1.
2. Plug the EVM into a PCIe® 16 × server motherboard slot. Ensure the motherboard is powered dwn before installing the EVM or configured for hot-plug operation.
3. Install a compatible PC Ie® endpoint card into one of the PCIe® connectors (J16) on the EVM based on configuration of the SEL pin.
4. Power-up the motherboard.
5. Run PCIe® CBB, AIC compatibility compliance test suite on the scope to check P0–P10 presets.
6. Attach PCIe® SIG compliance board media (ISI board) and the output of this transmission line goes to the Tek scope.
7. Checked Broadcom end point by itself only and ran CBB test.
8. Attached the same end point into J16 and performed CBB test again.

3 Test Report

3.1 Test Summary

TX presets: BRCM, J16 meets the PCI Express® 4.0 requirement.

ISI Eye openings:

1. BRCM meets all preset requirements
2. J16 is able to pass P06, P07, P08, and P09 only. Technically, at least one preset needs to pass to claim compatibility

Figure 3-1 through Figure 3-4 illustrate the test reports for preset and ISI eye opening test.

TekExpress PCI Express

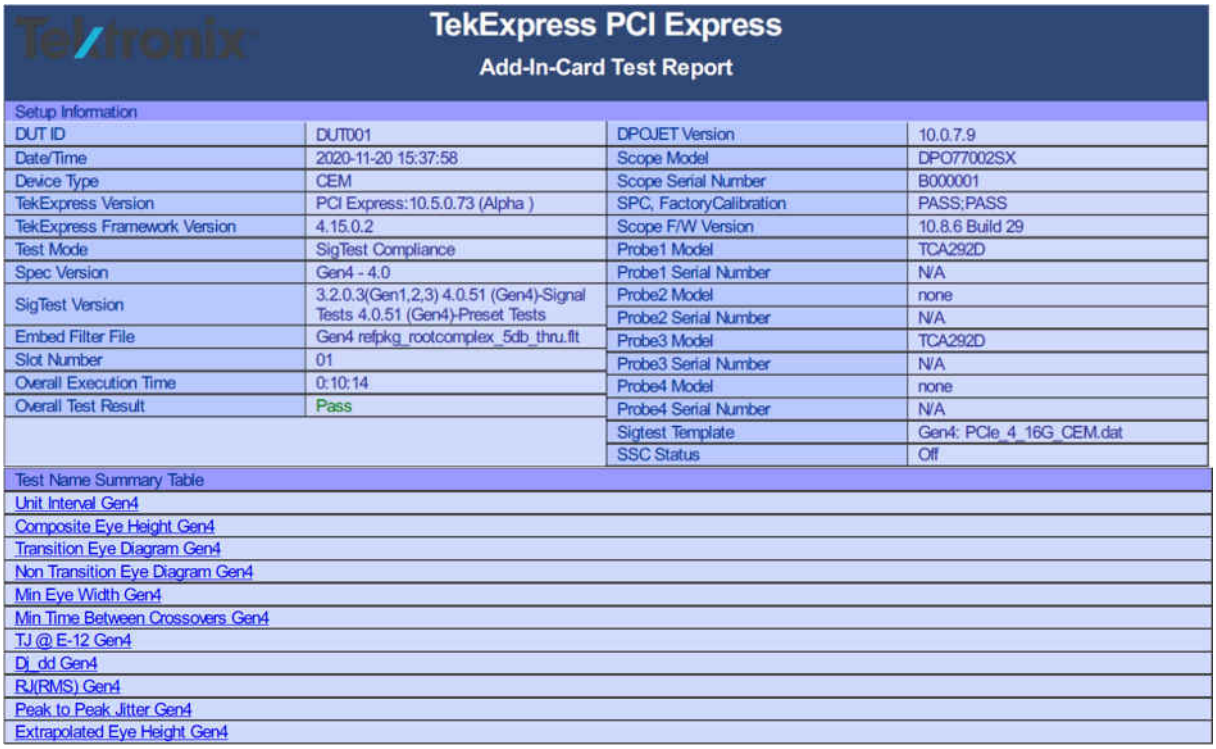
Add-In-Card Test Report

Setup Information			
DUT ID	DUT001	DPOJET Version	10.0.7.9
Date/Time	2020-11-18 16:51:50	Scope Model	DPO77002SX
Device Type	CEM	Scope Serial Number	B000001
TekExpress Version	PCI Express:10.5.0.73 (Alpha)	SPC, FactoryCalibration	PASS;PASS
TekExpress Framework Version	4.15.0.2	Scope F/W Version	10.8.6 Build 29
Test Mode	SigTest Compliance	Probe1 Model	TCA292D
Spec Version	Gen4 - 4.0	Probe1 Serial Number	N/A
SigTest Version	3.2.0.3(Gen1,2,3) 4.0.51 (Gen4)-Signal Tests 4.0.51 (Gen4)-Preset Tests	Probe2 Model	none
		Probe2 Serial Number	N/A
Embed Filter File	Gen4 refpkg_rootcomplex_5db_thru.flt	Probe3 Model	TCA292D
Slot Number	01	Probe3 Serial Number	N/A
Overall Test Result	Pass	Probe4 Model	none
Overall Execution Time	0:08:18	Probe4 Serial Number	N/A
		Sigtest Template	Gen4: PCIe_4_16G_CEM.dat
		SSC Status	Off

PRESET RESULTS

Preset Name	Lane Name	PreShoot	De-Emphasis	Vb	Result
P0 Gen4	Lane0	0.000 dB	-6.085 dB	491.560 mV	Pass
P10 Gen4	Lane0	0.000 dB	-8.676 dB	364.773 mV	Pass
P01 Gen4	Lane0	0.000 dB	-3.540 dB	658.937 mV	Pass
P02 Gen4	Lane0	0.000 dB	-4.677 dB	578.047 mV	Pass
P03 Gen4	Lane0	0.000 dB	-2.522 dB	740.875 mV	Pass
P04 Gen4	Lane0	0.000 dB	0.000 dB	990.426 mV	Pass
P05 Gen4	Lane0	2.082 dB	0.000 dB	779.376 mV	Pass
P06 Gen4	Lane0	2.502 dB	0.000 dB	742.529 mV	Pass
P07 Gen4	Lane0	4.024 dB	-6.620 dB	363.705 mV	Pass
P08 Gen4	Lane0	3.600 dB	-3.619 dB	489.499 mV	Pass
P09 Gen4	Lane0	3.547 dB	0.000 dB	658.358 mV	Pass

Figure 3-1. Test Report of Presets - 1



TekExpress PCI Express

Add-In-Card Test Report

Setup Information			
DUT ID	DUT001	DPOJET Version	10.0.7.9
Date/Time	2020-11-20 15:37:58	Scope Model	DPO77002SX
Device Type	CEM	Scope Serial Number	B000001
TekExpress Version	PCI Express:10.5.0.73 (Alpha)	SPC, FactoryCalibration	PASS;PASS
TekExpress Framework Version	4.15.0.2	Scope F/W Version	10.8.6 Build 29
Test Mode	SigTest Compliance	Probe1 Model	TCA292D
Spec Version	Gen4 - 4.0	Probe1 Serial Number	N/A
SigTest Version	3.2.0.3(Gen1,2,3) 4.0.51 (Gen4)-Signal Tests 4.0.51 (Gen4)-Preset Tests	Probe2 Model	none
		Probe2 Serial Number	N/A
Embed Filter File	Gen4 refpkg_rootcomplex_5db_thru.flt	Probe3 Model	TCA292D
Slot Number	01	Probe3 Serial Number	N/A
Overall Execution Time	0:10:14	Probe4 Model	none
Overall Test Result	Pass	Probe4 Serial Number	N/A
		Sigtest Template	Gen4: PCIe_4_16G_CEM.dat
		SSC Status	Off

Test Name Summary Table
Unit Interval Gen4
Composite Eye Height Gen4
Transition Eye Diagram Gen4
Non Transition Eye Diagram Gen4
Min Eye Width Gen4
Min Time Between Crossovers Gen4
TJ @ E-12 Gen4
Dj_dd Gen4
RJ(RMS) Gen4
Peak to Peak Jitter Gen4
Extrapolated Eye Height Gen4

Figure 3-2. ISI Test Report

Min Eye Width Gen4								
Measurement Details	Lane Name	Data Rate	Equalization	Measured Value	Test Result	Margin	Low Limit	High Limit
Min Eye Width R1	Lane0	16Gbps	P06 Gen4	36.135 ps	Informative	N.A	N.A	N.A
Min Eye Width R2	Lane0	16Gbps	P06 Gen4	36.021 ps	Informative	N.A	N.A	N.A
Min Eye Width R3	Lane0	16Gbps	P06 Gen4	34.518 ps	Informative	N.A	N.A	N.A
Min Eye Width Mean of 3 Acquisition	Lane0	16Gbps	P06 Gen4	35.558 ps	Pass	L:10.808ps	24.75	N.A
Min Eye Width R1	Lane0	16Gbps	P07 Gen4	33.596 ps	Informative	N.A	N.A	N.A
Min Eye Width R2	Lane0	16Gbps	P07 Gen4	33.705 ps	Informative	N.A	N.A	N.A
Min Eye Width R3	Lane0	16Gbps	P07 Gen4	33.760 ps	Informative	N.A	N.A	N.A
Min Eye Width Mean of 3 Acquisition	Lane0	16Gbps	P07 Gen4	33.687 ps	Pass	L:8.937ps	24.75	N.A
Min Eye Width R1	Lane0	16Gbps	P08 Gen4	33.690 ps	Informative	N.A	N.A	N.A
Min Eye Width R2	Lane0	16Gbps	P08 Gen4	34.483 ps	Informative	N.A	N.A	N.A
Min Eye Width R3	Lane0	16Gbps	P08 Gen4	33.799 ps	Informative	N.A	N.A	N.A
Min Eye Width Mean of 3 Acquisition	Lane0	16Gbps	P08 Gen4	33.991 ps	Pass	L:9.241ps	24.75	N.A
Min Eye Width R1	Lane0	16Gbps	P09 Gen4	34.527 ps	Informative	N.A	N.A	N.A
Min Eye Width R2	Lane0	16Gbps	P09 Gen4	34.368 ps	Informative	N.A	N.A	N.A
Min Eye Width R3	Lane0	16Gbps	P09 Gen4	34.682 ps	Informative	N.A	N.A	N.A
Min Eye Width Mean of 3 Acquisition	Lane0	16Gbps	P09 Gen4	34.526 ps	Pass	L:9.776ps	24.75	N.A

Figure 3-3. Test Report of ISI Eye Diagram Test

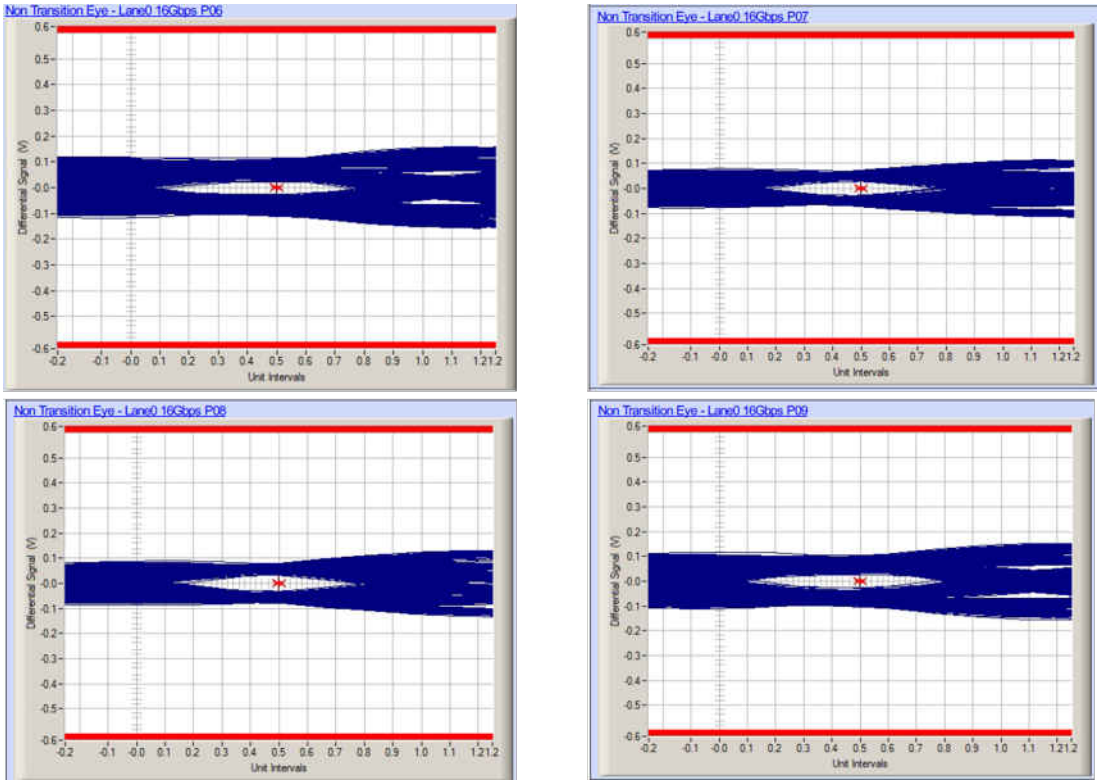


Figure 3-4. ISI Eye Diagram

4 Summary

This technical article described the test setup and procedures of PCI Express® 4.0 CBB, AIC compliance test using the TMUXHS4412 device. The test report is also presented.

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